

Ultra-Broadband Differential Silicon Capacitor Pair UBDC 0402M 2x5.6nF BV30



Rev. 2.01

General description

UBDC Ultra-Broadband Differential silicon Capacitor pair targets Optical communication system such as ROSA/TOSA, SONET and all optoelectronics as well as High speed data system or products.

The UBDC is suitable for DC blocking and AC coupling applications in all broadband optoelectronics and High-speed data system.

The unique technology of integrated passive device in silicon, developed by Murata Integrated Passive Solutions, offers unique performances with low insertion loss, low reflection and phase stability from 287 kHz to 60 GHz+.

These Ultra-Broadband MOS Silicon Differential Capacitors pairs (UBDC) in silicon have been developed in a semiconductor process, in order to combine ultra-deep trench MOS capacitors for high capacitance value of 5.6nF (for kHz–MHz range) and high frequency MIM capacitors for low capacitance value (for GHz range), both in a SMT 0402.

The UBDC capacitor pair provides very high stability of the capacitance over temperature, voltage variation as well as a very high reliability.

UBDC capacitors have an extended operating temperature ranging from -55 to 150°C, with very low capacitance change over temperature (+70ppm/K).

Key features

- Ultra-Broadband performance to 67 GHz
- Resonance free & phase stability
- 100Ω differential characteristic impedance
- Differential insertion loss < 0.9dB up to 60GHz
- Differential return loss > 12dB^(*)
- Ultra-high stability of capacitance value:
 - Temperature 70ppm/K (-55 °C to +150 °C)
 - Voltage < -0.1%/Volts
 - Negligible capacitance loss through ageing
- Low profile: 140μm including bump height
- Break down voltage: 30V
- Low leakage current < 100pA
- High reliability
- High operating temperature (up to 150 °C)
- Compatible with high temperature cycling during manufacturing operations (exceeding 300 °C)
- SAC305 40μm bumps after reflow

Key applications

- ROSA/TOSA
- SONET
- High speed digital logic
- Microwave/millimetre system
- Volume limited applications
- Broadband test equipment

^(*) in 100Ω differential impedance Microstrip.



Functional diagram

The next figure provides implementation set-up diagram.

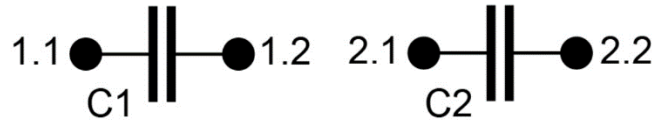


Figure 1 Block Diagram

Electrical performances

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C	Capacitance value	@+25°C	-	5.6	-	nF
ΔC_P	Capacitance tolerance ⁽¹⁾	@+25°C	-15	-	+15	%
T _{OP}	Operating temperature		-55	-	150	°C
T _{STG}	Storage temperature ⁽²⁾		-70	-	165	°C
ΔC_T	Capa. temperature variation	-55 °C to 150 °C	-	70	-	ppm/K
RV _{DC}	Rated voltage ⁽³⁾		-	-	16 ⁽⁴⁾ 13.6 ⁽⁵⁾	V _{DC}
BV	Break down voltage	@+25°C	30	-	-	V
ΔC_{RVDC}	Capacitance voltage variation	From 0 V to RV _{DC} @+25°C	-	-	-0.1	%/V _{DC}
IR	Insulation resistor	@RV _{DC} , +25°C, 120s	-	10	-	GΩ
F _{c-3dB}	Cut-off frequency at 3dB ⁽⁶⁾	@+25°C	-	287	334	kHz
Diff	Diff. characteristic impedance	@+25°C	-	100	-	Ω
IL	Differential insertion loss (100Ω) ⁽⁶⁾ (Microstrip)	@ 20 GHz, @+25°C	-	0.3	-	dB
		@ 40 GHz, @+25°C	-	0.5	-	dB
		@ 60 GHz, @+25°C	-	0.6	-	dB
	Differential return loss (100Ω) (Coplanar)	@ 20 GHz, @+25°C	-	0.6	-	dB
		@ 40 GHz, @+25°C	-	0.75	-	dB
		@ 50 GHz, @+25°C	-	1	-	dB
RL	Differential return loss (100Ω) ⁽⁶⁾ (Microstrip)	Up to 60 GHz, @+25°C	-	14	-	dB
	Differential return loss (100Ω) (Coplanar)	Up to 50 GHz, @+25°C	-	15	-	dB
ESD	HBM stress ⁽⁷⁾	JS-001-2017	2	-	-	kV

Table 1 - Electrical performances

(1): Other tolerance available upon request
 (2): Without packaging
 (3): Lifetime is voltage and temperature dependent, please refer to application note 'Lifetime of 3D capacitors'
 (4): 10 years of intrinsic lifetime prediction at 100°C continuous operation
 (5): 10 years of intrinsic lifetime prediction at 150°C continuous operation
 (6): Simulated based on correlations between simulations and measurement results performed in coplanar mode
 (7): please refer to application note 'ESD Challenge in 3D Murata Integrated Passive technology'



Simulation results of 2x5.6nF UBDC in transmission mode on microstrip transmission line

Module S-parameters

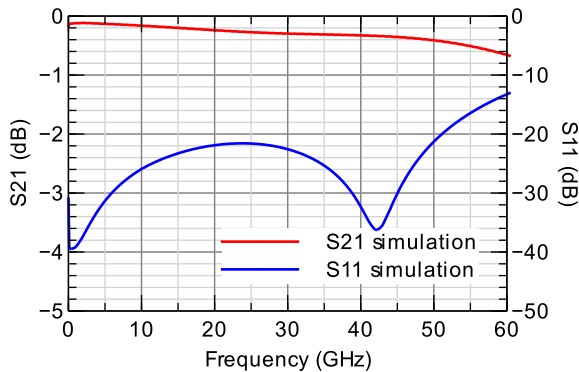


Figure 2 - 2x5.6nF UBDC simulation results (100Ω differential)

Test bench

4-mils (101μm) Rogers RO4350B

Nominal Pad dimensions – pad length = 0.150 mm, pad width and line width = 0.150 mm, pad gap = 0.100 mm
100 Ohm differential – 18μm Cu thickness – full GND plane

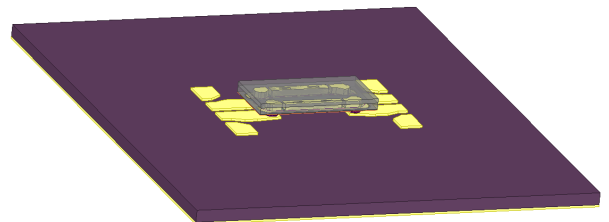


Figure 3 - Microstrip simulation board

Simulation and Measurements results correlation of 2x5.6nF UBDC in transmission mode on coplanar transmission line



Module S-parameters

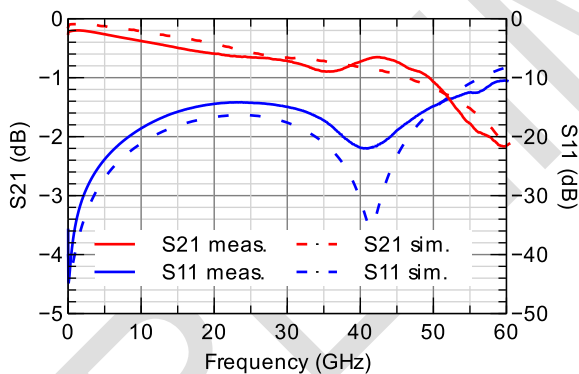
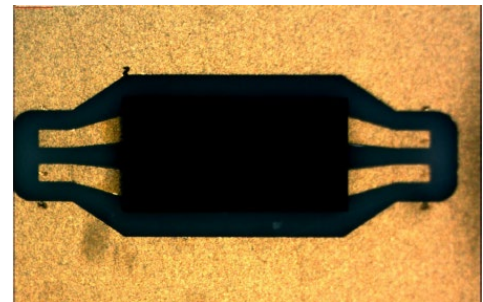


Figure 4 - 2x5.6nF UBDC measurement results (100Ω differential)

Test bench

25-mils (635μm) alumina

1-3μm Au thickness
Measured with GSSG probes and 4-ports VNA



FREE S-Parameters-Based Linear Simulation Models for ADS

<http://www.modelithics.com/mvpmurata.asp>

Figure 5 - 2x5.6nF UBDC soldered on its test board

4x50Ω single ports to 2x100 Ω differential ports transposition (measurement and simulation)

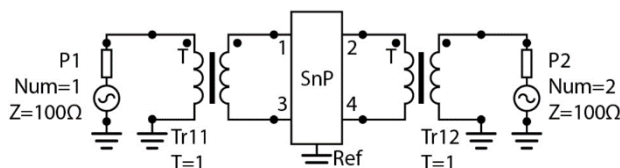


Figure 6 - single-to-differential transposition



Pinning definition

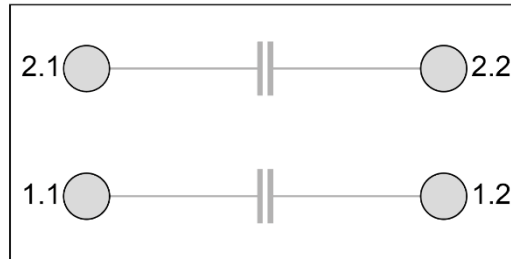


Figure 7 Pinning definition

pin #	Symbol	Coordinates X / Y [µm]
1.1	Signal1	-350.0 / -125.0
1.2	Signal1	350.0 / -125.0
2.1	Signal2	-350.0 / 125.0
2.2	Signal2	350.0 / 125.0

Table 2 - Pinning description. Reference (0,0) located at the centre of the die.

Ordering Information

Murata Integrated Passive Devices delivers products with AQL level II (0.65). Tighter quality levels are available upon request.

Part number	Package		
	Packaging	Finishing	Description
939301721456-F1S	6" film frame carrier ⁽¹⁾	SAC ⁽²⁾	UBDC 0402M – 2x5.6nF – 4 pads – 1mm x 0.5mm x 0.10 mm ⁽⁴⁾
939301721456-T3S	7" T&R with 1Kpieces / reel ⁽³⁾	SAC ⁽²⁾	UBDC 0402M – 2x5.6nF – 4 pads – 1mm x 0.5mm x 0.10 mm ⁽⁴⁾

Table 3 - Packaging and ordering information

- (1) Other film frame carriers are possible on request
- (2) ENIG + SAC305 type 6
- (3) missing capacitors can reach 0.5%
- (4) Refer to Figure9 and Table5

Product Name	Die Name	Description
UBDC721.456	XJA1D456	UBDC 2x5.6nF/0402M/BV30 – 4 pads – 1 x 0.5 x 0.10 mm

Table 4 - Die information



Pad Metallization

The surface mounted UBDC Capacitor is delivered as standard with SAC305 bumping.

Other Metallization, such as ENIG (0.1µm Au / 5µm Ni), Copper, Thick Gold or Aluminum pads are possible on request.

UBDC series is compatible with standard reflow process.

It is recommended to design mirror pads on the PCB.

Silicon dies are not sensitive to humidity, please refer to applications notes 'Assembly Notes' section 'Handling precautions and storage'.

Material regulation

This product is RoHS compliant at the time of publication. For further information about regulation compliancy, please ask your sales representative.

Package outline

The product is delivered as a bare silicon die.

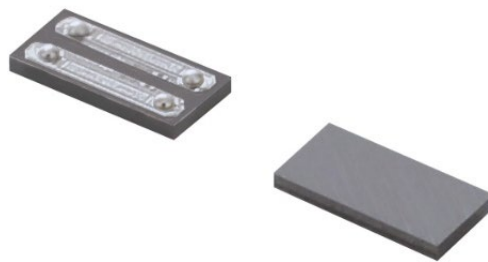


Figure 8 - Micro photography of a 2x5.6 nF Capacitor

L (mm)	W (mm)	T (mm)	c (mm)	P (mm)	e (mm)	t (mm)
1.00 ±0.02	0.50 ±0.02	0.10 ±0.015	0.09	0.70	0.25	0.04 ⁽¹⁾ 0.05 ⁽²⁾

(1) Solder joint height after reflow on board.
(2) Solder bump height before assembly

Table 5 - Dimensions and tolerances

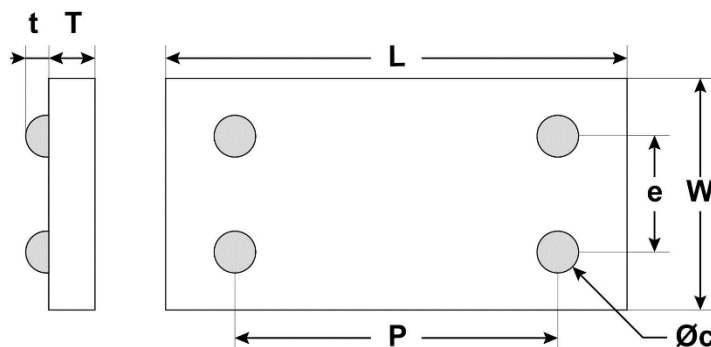


Figure 9 - Package outline Capacitor

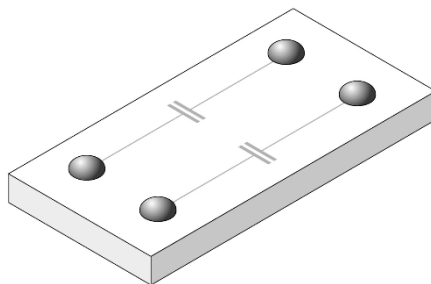


Figure 10 - Package isometric view

PRELIMINARY



Assembly

The attachment techniques recommended by Murata on the customer's substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata capacitors **please download the assembly instructions on <https://www.murata.com/en-us/products/capacitor/siliconcapacitors> and read them carefully.**



Figure 11 Scan this QR Code to access the Murata Silicon Capacitor web page

Packaging format

Please refer to application note 'Products Storage Conditions and Shelf Life'.

Tape and Reel:

Dies are flipped in the tape cavity (bump down) with die ID located near the driving holes of the tape.

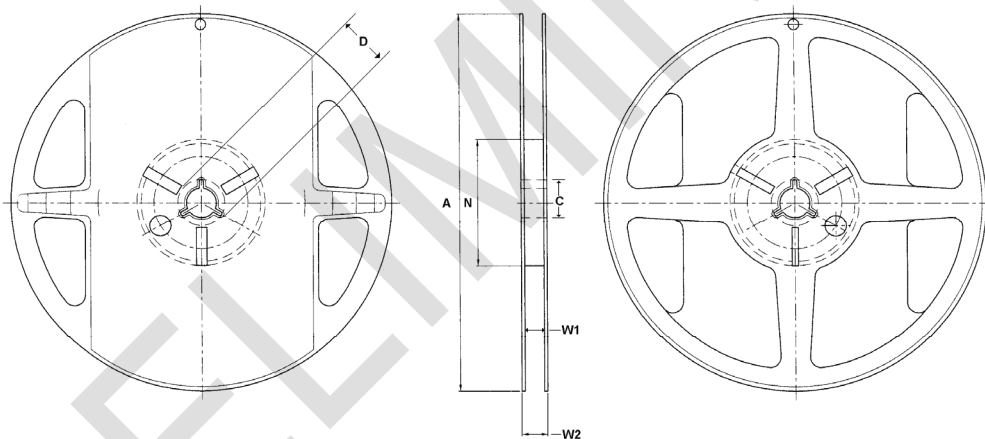


Figure 12 - Reel drawing

Tape Width	Diameter A	C	D	Hub N	W1	W2
8	178 (7 inches)	13.5	20.2	60	9.3	11.5

Table 6 – Reel dimensions (mm)

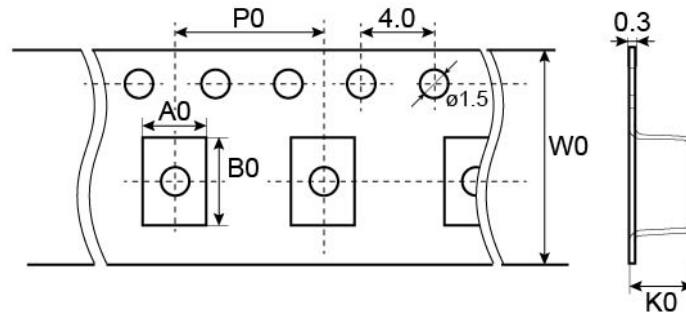


Figure 13 - Tape drawing

Cavity dimensions			Carrier tape width W0	Carrier tape pitch P0	Reel Capacity
Ao	Bo	Ko			
0.59	1.09	0.20	8	4	1000

Table 7 - Tape dimensions (mm)



Film frame carrier:

With UV curable dicing tape (UV performed).

Good dies are identified using the SINF electronic mapping format. No ink is added on wafer to label other dies.

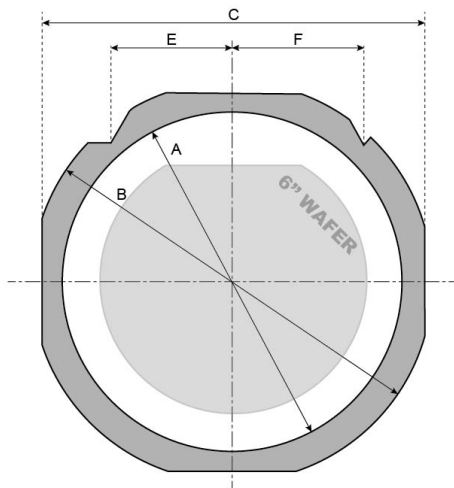


Figure 14 FF070 Frame with a 6" wafer

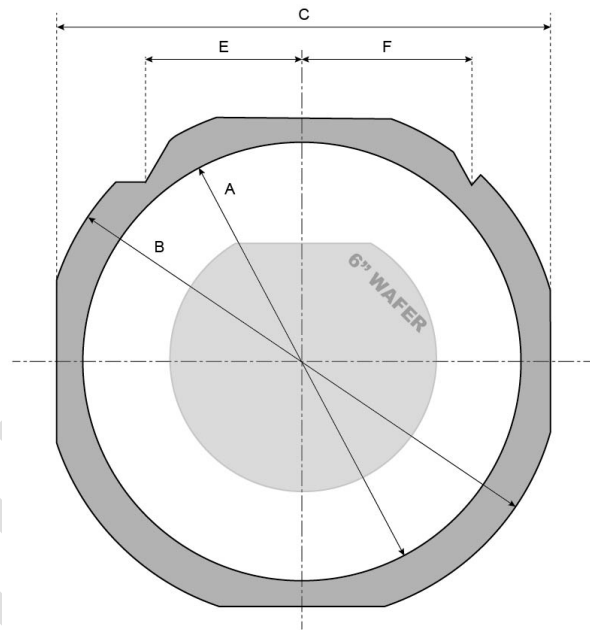


Figure 15 FF108 Frame with a 6" wafer

Frame Reference	Frame Style	Inside diameter A	Outside diameter B	Width C	Thickness	Pin location E	Pin location F
FF070 (1)	DTF-2-6-1	7.638"	8.976"	8.346"	0.048"	2.370"	2.5"
FF108 (1)	DTF-2-8-1	9.842"	11.653"	10.866"	0.048"	2.381"	2.5"

Table 8 - Frame dimensions (inches)

(1) or equivalent



Definitions

Data sheet status

Objective specification: This data sheet contains target or goal specifications for product development.

Preliminary specification: This data sheet contains preliminary data; supplementary data may be published later.

Product specification: This data sheet contains final product specifications.

Limiting values

Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Electrical performances sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

Revision history

Revision	Date	Description	Author
Release 1.00	2017 Sept. 15th	Objective specification	OGA + SBO
Release 2.01	2021 April 26th	Curves with correlation updated Preliminary status	SCA + OGA + LLR + CGU

Disclaimer / Life support applications

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