Wire Bondable Automotive Vertical SiCap WASC 0208 4.7nF BV150

Rev. 2.0

General description

The WAS Capacitor has been qualified according to AECQ-100 up to 68V, Grade 0 (-40°C/+150°C) 2000 cycles TMCL. Qualification report of the BV150 technology according to AECQ100 requirements is available on request.
Target applications are decoupling and filtering of active devices when miniaturization and low ESL are required. This product is a single 4.7nF capacitor in 0.5 x 2mm package size. Other capacitance values and other package size are available as a single die or capacitor array; please feel free to contact us.

The WAS Capacitor is based on PICS Integrated Passive technology.
Standard PCB FR4 can be used.

Assembly: WASC capacitors are directly mounted on the PCB application using die attach and wire bonding.
WASC capacitors have the bottom electrode in Ti (0.1 µm)/Ni (0.3µm)/Au (0.2µm) and top electrode in gold, other top finishing are available on request such as Aluminum.

Key features

- AECQ-100 Qualification
- Full compatible Monolithic ceramic capacitors for replacement
- Ultra-high stability of capacitance value:
  - Temperature 60ppm/K (-55 °C to +150 °C)
  - Voltage <0.02%/Volts
  - Negligible capacitance loss through ageing
- Low profile 0.25mm or 0.1mm, but other thicknesses possible on request
- Small size 0.5 x 2mm
- Break down voltage > 150V
- Low leakage current
- High reliability
- High operating temperature (up to 150 °C)
- Compatible with high temperature cycling during manufacturing operations (exceeding 300 °C)
- Applicable for standard wire bonding assembly (ball and wedge)

Key applications

- Any demanding automotive applications, such as ADAS sensors (Lidars, Radars) as well as all Automotive SiP devices (Mems sensors, TPMS…)
- Supply decoupling / filtering of active device
- High reliability applications
- Devices with battery operations
- High temperature applications
- High volumetric efficiency (i.e. capacitance per unit volume)

Functional diagram

The next figure provides implementation set-up diagram.

Figure 1 Block Diagram

Electrical performances

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C	Capacitance value	@+25°C	-	4.7	-	nF
ΔC_P	Capacitance tolerance (1)	@+25°C	-15	-	+15	%
T_{OP}	Operating temperature		-55	20	150	°C
T_{STG}	Storage temperature (2)		-70	-	165	°C
ΔC_T	Capacitance temperature variation	-55 °C to 150 °C	-	60	-	ppm/K
RV_{DC}	Rated voltage (3)		-		68(4) 61(5)	V_{DC}
BV	Break down voltage	@+25°C	150	-	-	V
ΔC_{RVDC}	Capacitance voltage variation	From 0 V to RV_{DC}, @+25°C	-	-	-0.02	%/V_{DC}
IR	Insulation resistor	@RV_{DC}, +25°C, 120s	-	1	-	GΩ
ESL	Equivalent Serial Inductance	@+25°C, SRF shunt mode	-	10	-	pH
ESR	Equivalent Serial Resistance	@+25°C, shunt mode	-	10	-	mOhm
ESD	HBM stress (6)	JS-001-2017	5	-	-	kV

Table 1 - Electrical performances

(1): other tolerance available upon request
(2): without packaging
(3): Lifetime is voltage and temperature dependent, please refer to application note 'Lifetime of 3D capacitors'
(4): 10 years of intrinsic life time prediction at 100°C continuous operation
(5): 10 years of intrinsic life time prediction at 150°C continuous operation
(6): please refer to application note 'ESD Challenge in 3D Murata Integrated Passive technology'

Pinning definition

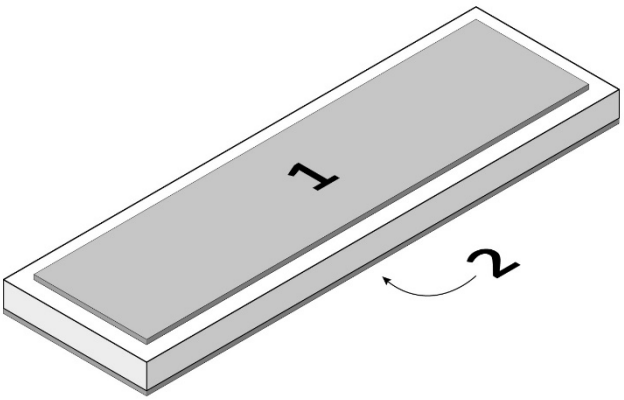

Figure 2 Pinning definition

pin #	Description
1	Top side Electrode finishing: Au
2	Back side Electrode finishing: Ti (0.1 µm)/Ni (0.3µm)/Au (0.2µm)

Table 2 - Pining description.

Ordering Information

Murata Integrated Passive Devices delivers products with AQL level II (0.65).

Part number (16NC)	Die Name	Package		
		Packaging	Finishing	Description
935 247 522 447-F1T	WO0208447	6” FFC	Au(1)	WASC 4.7nF BV150 – 1 bondpad – 0.5 x 2mm x 0.25mm
935 247 522 447-T3T	WO0208447	T&R 1Kunits(2)	Au(1)	WASC 4.7nF BV150 – 1 bondpad – 0.5 x 2mm x 0.25mm
935 248 522 447-F1T	WO0208447	6” FFC	Au(1)	WASC 4.7nF BV150 – 1 bondpad – 0.5 x 2mm x 0.10mm
935 248 522 447-T3T	WO0208447	T&R 1Kunits(2)	Au(1)	WASC 4.7nF BV150 – 1 bondpad – 0.5 x 2mm x 0.10mm

Table 3 - Packaging and ordering information

(1) Au = TiW (0.3µm) / Au (3µm)
(2) missing capacitors can reach 0.5%

Pad Metallization

Standard pad finishings:

TOP: metallization is Au for the top pad and Ti (0.1 µm)/Ni (0.3µm)/Au (0.2µm) for the bottom pad.

Other Metallization, such as Thick Gold or Aluminum pads are possible on request. please ask your sales representative

Material regulation

This product is RoHS compliant at the time of publication. For further information about regulation compliancy, please ask your sales representative.

Package outline

The product is delivered as a bare silicon die, with passivation opening for contacts.

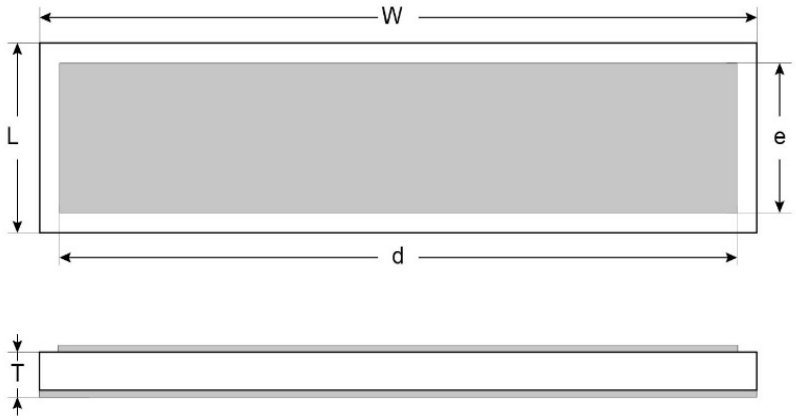

Figure 3 - Package outline drawing

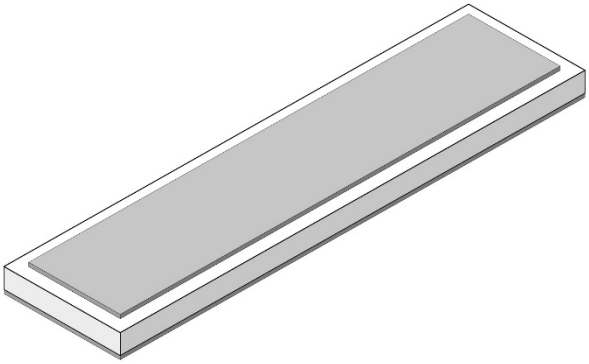

Figure 4 - Package isometric view

L (mm)	W (mm)	T (mm)	d (mm)	e (mm)
0.50 ±0.02	2.00 ±0.02	0.25 or 0.10 ±0.01	1.894	0.394

Table 4 - Dimensions and tolerances

Assembly

The attachment techniques recommended by Murata on the customer's substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata capacitors **please download the assembly instructions on https://www.murata.com/en-us/products/capacitor/siliconcapacitors and read them carefully.**

Figure 5 Scan this QR Code to access the Murata Silicon Capacitor web page

Packaging format

Please refer to application note 'Products Storage Conditions and Shelf Life'.

Tape and Reel:

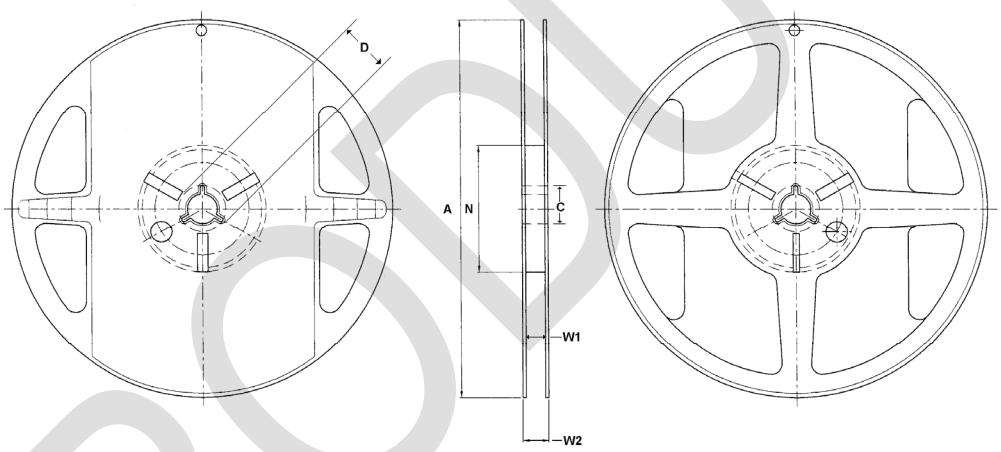

Figure 6 - Reel drawing

Tape Width	Diameter A	C	D	Hub N	W1	W2
8	178 (7 inches)	13.5	20.2	60	9	11.5

Table 5 – Reel dimensions (mm)

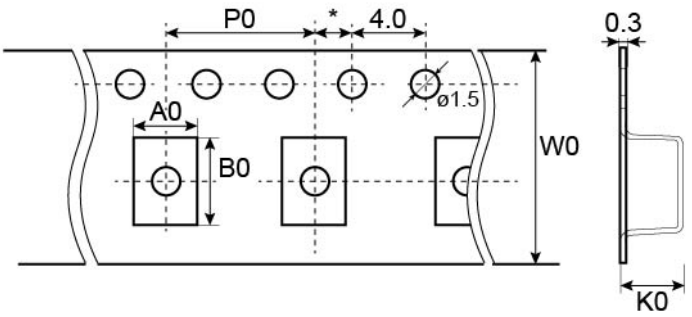

Figure 7 - Tape drawing

Cavity dimensions			Carrier tape width W0	Carrier tape pitch P0
Ao	Bo	Ko		
0.6	2.1	0.2 (for 0.10mm thick.) 0.34 (for 0.25mm thick.)	8 mm	2 mm

Table 6 - Tape dimensions (mm)

Film frame carrier:

With UV curable dicing tape (UV performed)

Good dies are identified using the appropriate e-mapping format. No ink is added on wafer to label other dies.

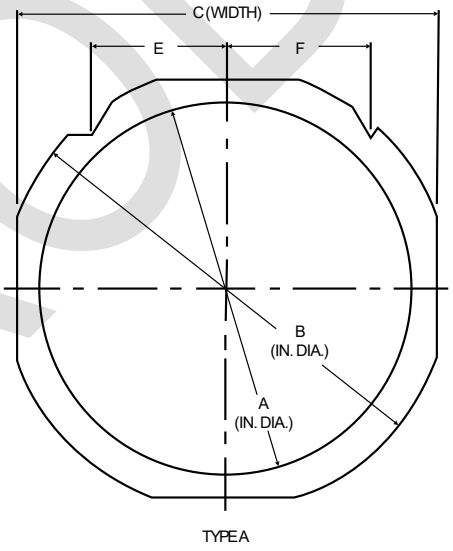

Figure 8 – Film frame drawing

Wafer diameter	Inside diameter A	Outside diameter B	Width C	Thickness	Pin location E	Pin location F	Frame style
6''	7.639"	8.976"	8.346"	0.048''	2.370"	2.5''	DTF-2-6-1

Table 7 - Frame dimensions (inches)

Definitions

Data sheet status

Objective specification: This data sheet contains target or goal specifications for product development.

Preliminary specification: This data sheet contains preliminary data; supplementary data may be published later.

Product specification: This data sheet contains final product specifications.

Limiting values

Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Electrical performances sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

Revision history

Revision	Date	Description	Author
Release 2.0	**2020 July 28th**	**Product Release**	**LLE**

Disclaimer / Life support applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Murata customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Murata for any damages resulting from such improper use or sale.

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