Ultra-Broadband Diff Si Cap Pairs UBDC (2x10nF / 0402M / BV=11V)

Rev. 1.9

General description

Market: UBDC Ultra broadband Differential Silicon Capacitor Pair targets Optical communication system such as ROSA/TOSA, SONET and all optoelectronics as well as High speed data system or products.

The UBDC is suitable for DC blocking and AC coupling applications in all broadband optoelectronics and High-speed data system.

The unique technology of integrated passive device in silicon, developed by Murata Integrated Passive Solutions, offers unique performances with low insertion loss, low reflection and phase stability from 160 kHz to 60 GHz+.

These Ultra-Broadband MOS Silicon Differential Capacitors pairs (UBDC) in silicon have been developed in a semiconductor process, in order to combine ultra-deep trench MOS capacitors for high capacitance value of **min 10 nF** (for kHz–MHz range) and high frequency MIM capacitors for low capacitance value for GHz range), both in a SMT 0402.

The UBDC capacitor pair provides very high stability of the capacitance over temperature, voltage variation as well as a very high reliability.

UBDC capacitors have an extended operating temperature ranging from -55 to 150°C, with very low capacitance change over temperature (+70ppm/K).

Key features

- Ultra-Broadband performance to 67 GHz
- Resonance free & phase stability
- 100Ω differential characteristic impedance
- Differential insertion loss < 0.9dB up to 60GHz
- Differential return loss > 12dB
- Ultra-high stability of capacitance value:
  - Temperature 70ppm/K (-55 °C to +150 °C)
  - Voltage <0.1%/Volts
  - Negligible capacitance loss through ageing
- Low profile: 140µm including bump height
- Break down voltage > 11V
- Low leakage current < 100pA
- High reliability
- High operating temperature (up to 150 °C)
- Compatible with high temperature cycling during manufacturing operations (exceeding 300 °C)
- SAC305 40µm bumps after reflow

Key applications

- ROSA/TOSA
- SONET
- High speed digital logic
- Microwave/millimetre system
- Volume limited applications
- Broadband test equipment

Functional diagram

The next figure provides implementation set-up of the differential capacitor pair (4 connections).

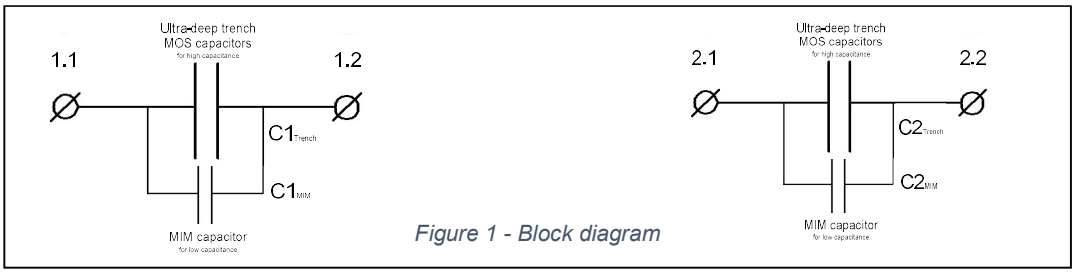


Figure 1 - Block diagram

Electrical performances

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C	Capacitance value	@+25°C	10	11.8	13.6	nF
ΔC_P	Capacitance tolerance (1)	@+25°C	-15	-	+15	%
T_{OP}	Operating temperature		-55	-	150	°C
T_{STG}	Storage temperature (2)		-70	-	165	°C
ΔC_T	Capacitance temperature variation	-55 °C to 150 °C	-	70	-	ppm/K
RV_{DC}	Rated voltage (3)		-	-	3.8(4) 3.4(5)	V_{DC}
BV	Break down voltage	@+25°C	11	-	-	V
ΔC_{RVDC}	Capacitance voltage variation	From 0 V to RV_{DC}, @+25°C	-	-	0.1	$\%/V_{DC}$
IR	Insulation resistor	@RV_{DC}, +25°C, 120s	-	10	-	GΩ
Fc-3dB	Cut-off frequency at 3dB(6)	@+25°C	-	160	184	kHz
Diff	Differential characteristic impedance	@+25°C	-	100	-	Ω
IL	Differential insertion loss (under 100Ω)(6) (Microstrip)	@ 20 GHz, @+25°C	-	0.3	0.4	dB
		@ 40 GHz, @+25°C	-	0.5	0.6	dB
		@ 60 GHz, @+25°C	-	0.6	0.9	dB
RL	Differential return loss (under 100Ω)(6) (Microstrip)	Up to 60 GHz, @+25°C	12	14	-	dB
ESD	HBM stress (7)	JS-001-2017	2	-	-	kV

Table 1 - Electrical performances

(1): Other tolerance available upon request
(2): Without packaging
(3): Lifetime is voltage and temperature dependent, please refer to application note 'Lifetime of 3D capacitors'
(4): 10 years of intrinsic life time prediction at 100°C continuous operation
(5): 10 years of intrinsic life time prediction at 150°C continuous operation
(6): Measured
(7): please refer to application note 'ESD Challenge in 3D Murata Integrated Passive technology'

Module S-parameters of 2x10nF UBDC in transmission mode (microstrip)

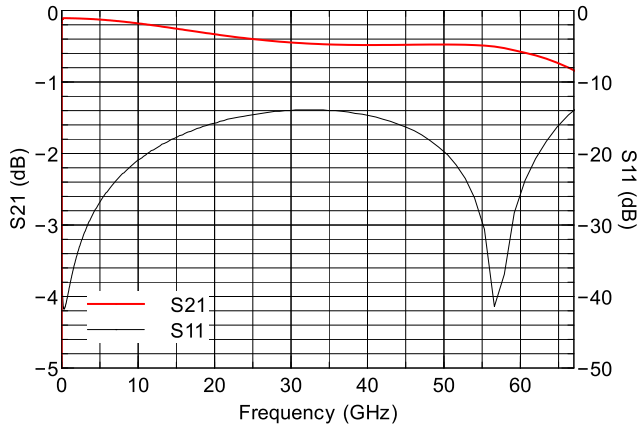


Figure 2 - 2x10nF UBDC simulation results (module of S-parameters)

Schematic of 2x10nF UBDC in transmission mode

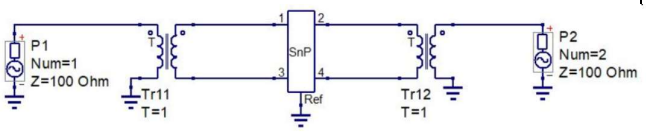
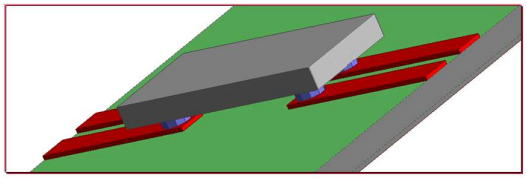


Figure 3 – 2x10nF UBDC measurement schematic

Test bench (microstrip)



4-mils(101µm) Rogers RO4350B.
Nominal Pad dimensions – pad length = 0.150 mm, pad width and line width = 0.150 mm, pad gap = 0.100 mm
100 Ohm differential – 18µm Cu thickness – full GND plane

Figure 4 - test bench picture used for 2x10nF UBDC characterization

Pinning definition

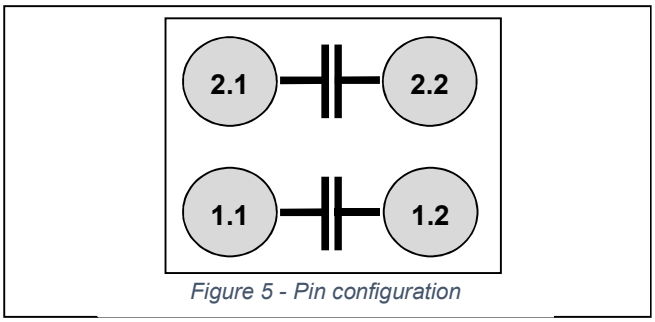


Figure 5 - Pin configuration

pin #	Symbol (optional)	Coordinates X / Y [µm]
1.1	Signal1	-350.0 / -125.0
1.2	Signal1	350.0 / -125.0
2.1	Signal2	-350.0 / 125.0
2.2	Signal2	350.0 / 125.0

Table 2 - Pining description. Reference (0,0) located at the centre of the die.

Ordering Information for UBDC421.510

Regardless of packaging, Murata Integrated Passive Devices delivers products with AQL level II (0.65).

Type number (15NC)	Package		
	Packaging	Finishing	Description
939 301 421 510-F1S	6" film frame carrier(1)	SAC(2)	UBDC402M – 2x10nF – 4 pads – 1mm x 0.5mm x 0.10 mm (4)
939 301 421 510-T3S	7" T&R with 1Kpieces / reel(3)	SAC(2)	UBDC402M – 2x10nF – 4 pads – 1mm x 0.5mm x 0.10 mm (4)

(1) Other film frame carrier are possible on request
(2) ENIG + SAC305 type 6
(3) missing capacitors can reach 0.5%
(4) Refer to Figure7.

Table 3 - Packaging and ordering information

Product Name	Die Name	Description
UBDC421.510	XCA1D510	UBDC 2x10nF/0402M/BV>11V – 4 pads – 1 x 0.5 x 0.10 mm

Table 4 - Die information

Pad Metallization

The UBDC Capacitor is delivered as standard with SAC305 bumping.

Other Metallization, such as ENIG, Copper, Thick Gold or Aluminum pads are possible on request.

Silicon dies are not sensitive to humidity, please refer to applications notes ‘Assembly Notes’ section ‘Handling precautions and storage’.

Material regulation

This product is RoHS compliant at the time of publication. For further information about regulation compliancy, please ask your sales representative.

Package outline

The product is delivered as a barre silicon die, with passivation opening for contacts.

Figure 6 - Micro photography of Capacitor

L (mm)	W (mm)	T (mm)	c (mm)	P (mm)	e (mm)	F (mm)	t (mm)
1.00 ±0.02	0.50 ±0.02	0.10 ±0.01	0.09	0.70	0.25	0.15	0.04(1) 0.05(2)

(1) Solder joint height after reflow on board.
(2) Solder bump height before assembly

Table 5 - Dimensions and tolerances

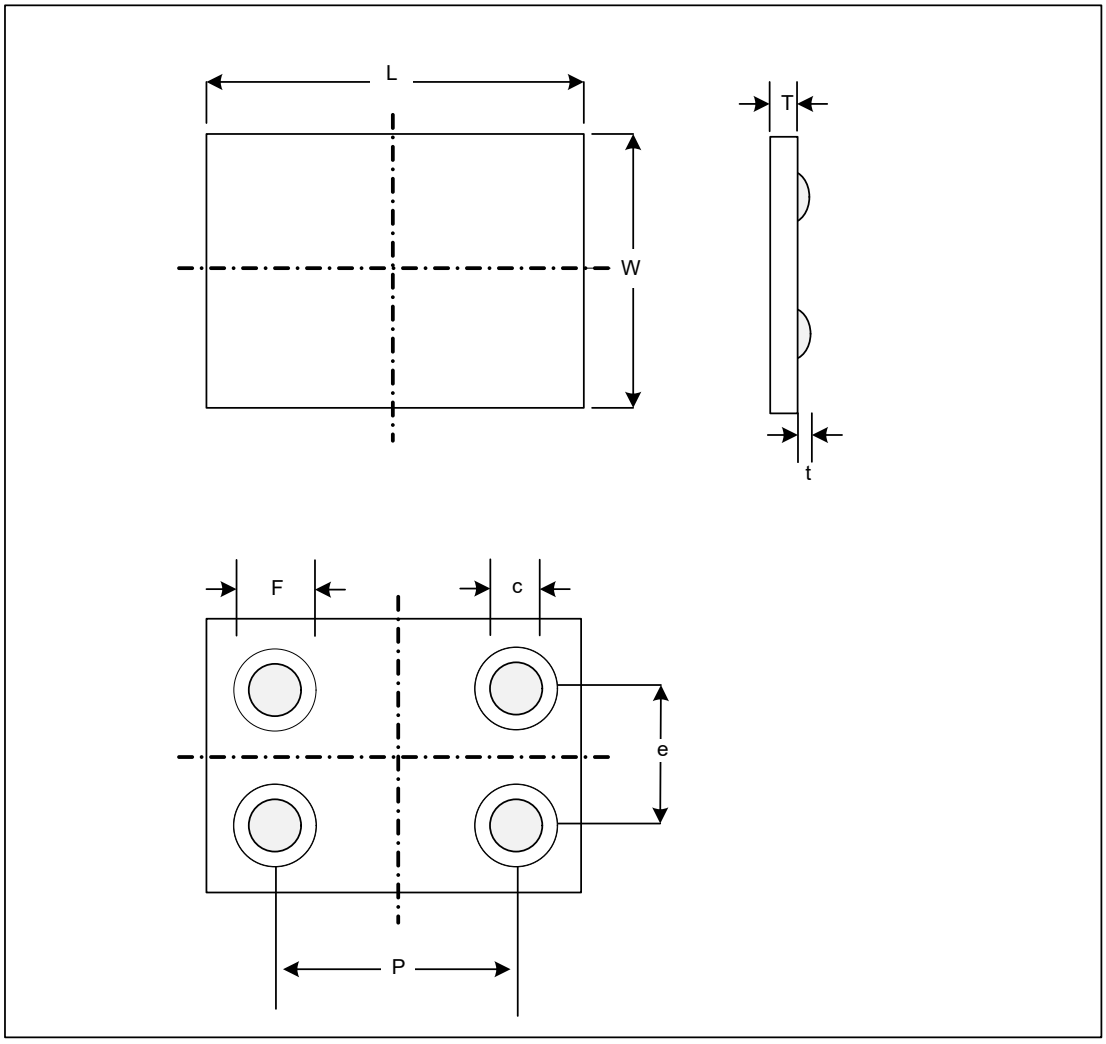


Figure 7 - Package outline Capacitor

Assembly

UBDC series is compatible with standard reflow technology.

It is recommended to design mirror pads on the PCB.

For further information, please see our mounting application note.

The attachment techniques recommended by Murata on the customer's substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata capacitors **please download the assembly instructions on https://www.murata.com/en-us/products/capacitor/siliconcapacitors and read them carefully.**

Figure 8 Scan this QR Code to access the Murata Silicon Capacitor web page

Packaging format

Please refer to application note 'Products Storage Conditions and Shelf Life'.

Tape and Reel: Dies are flipped in the tape cavity (bump down) withdie ID located near the driving holes of the tape.

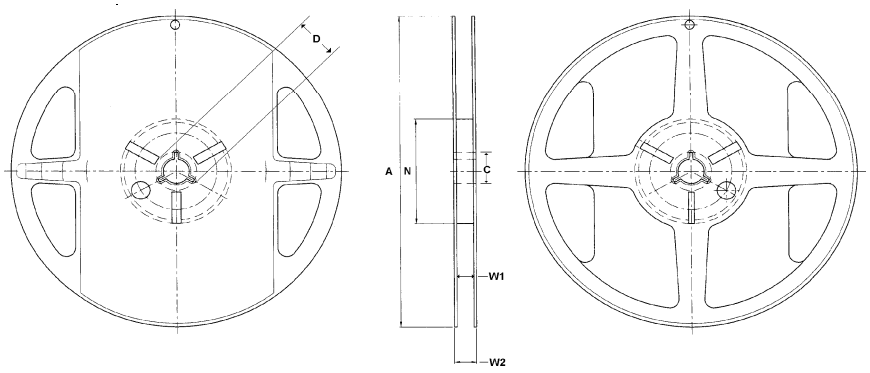


Figure 9 - Reel drawing

Tape Width	Diameter A	C	D	Hub N	W1	W2
8	178 (7 inches)	13.5	20.2	60	9.5	11.5

Table 6 - Reel dimensions (mm)

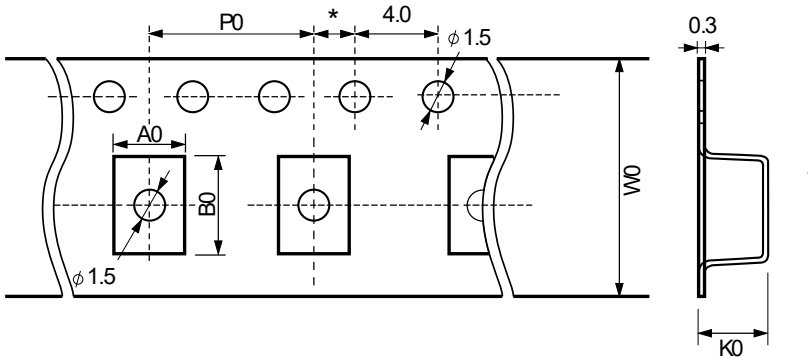


Figure 10 - Tape drawing

Cavity dimensions			Carrier tape width W0	Carrier tape pitch P0
A0	B0	K0		
0.59	1.09	0.20	8	2

Table 7 - Tape dimensions (mm)

(1) Die orientation (flip) within the carrier (Pocket) related to tape and reel orientation

Film frame carrier: FF070 or equivalent

With UV curable dicing tape (UV performed)

Good dies are identified using the SINF electronic mapping format. No ink is added on wafer to label other dies.

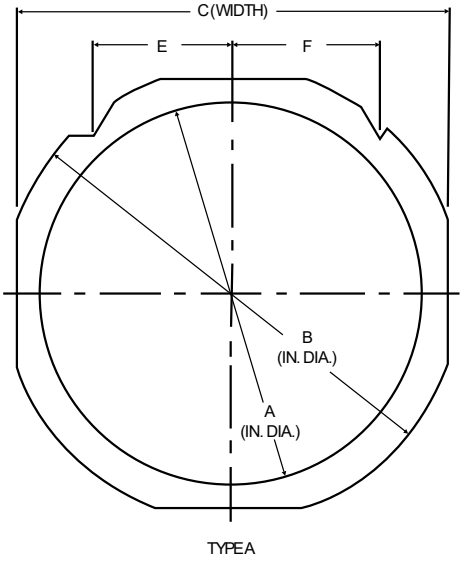


Figure 11 - Film frame drawing

Wafer diameter	Inside diameter A	Outside diameter B	Width C	Thickness	Pin location E	Pin location F	Frame style
6''	7.639"	8.976"	8.346"	0.048''	2.370"	2.5''	DTF-2-6-1

Table 8 - Frame dimensions (inches)

Definitions

Data sheet status

Objective specification: This data sheet contains target or goal specifications for product development.

Preliminary specification: This data sheet contains preliminary data; supplementary data may be published later.

Product specification: This data sheet contains final product specifications.

Limiting values

Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Electrical performances sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

Revision history

Revision	Date	Description	Author.
Release 1.0	**2017 Sept. 15th**	**Objective specification**	**OGA + SBO**
Release 1.9	**2020 April 20th**	**General update**	**OGA**

Disclaimer / Life support applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Murata customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Murata for any damages resulting from such improper use or sale.

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