Ultra Large band Silicon Capacitor ULSC 0402 100nF BV11

Rev. 3.00

General description

ULSC Capacitor targets Optical communication system such as ROSA/TOSA, SONET and all optoelectronics as well as High speed data system or products.
The ULSC is suitable for DC blocking, feedback, coupling and bypassing applications in all broadband optoelectronics and High-speed data system.
The unique technology of integrated passive device in silicon, developed by Murata Integrated Passive Solutions, offers unique performances with low insertion loss, low reflection and phase stability from 16 KHz to 20 GHz. These capacitors in ultra-deep trenches in silicon have been developed in a semiconductor process, in order to integrate trench MOS capacitor providing high capacitance value of 100 nF in a 0402 [1.2x0.7mm] case.
The ULSC capacitor provides very high stability of the capacitance over temperature, voltage variation as well as a very high reliability.
ULSC capacitors have an extended operating temperature ranging from -55 to 150°C, with very low capacitance change over temperature (+70ppm/K).
Assembly: Suitable for surface mounted application on rigid PCB, ceramic substrate, FR4 (laminate) or flex platforms.
Bump finishing: ENIG. Copper pads optional for embedding version and SAC305 type 6 for pre-bumping version, as an optional finishing.

Key features

- Ultra Large band performance to 20 GHz
- Resonance free
- Phase stability
- Insertion low < 0.35dB Typ. up to 20 GHz
- Ultra-high stability of capacitance value:
  - Temperature 70ppm/°C (-55 °C to +150 °C)
  - Voltage <-0.1%/Volts
  - Negligible capacitance loss through ageing
- Low profile: 400µm, 100 µm on request
- Break down voltage : 11V
- Low leakage current < 100pA
- High reliability
- High operating temperature (up to 150 °C)
- Compatible with high temperature cycling during manufacturing operations (exceeding 300 °C)
- Compatible with almost EIA 0402 footprint

Key applications

- ROSA/TOSA
- SONET
- High speed digital logic
- Microwave/millimetre system
- High volumetric efficiency (i.e. capacitance per unit volume)
- Broadband test equipment

Functional diagram

The next figure provides implementation set-up diagram.

Figure 1 Block Diagram

Electrical performances

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C	Capacitance value	@+25°C	-	100	-	nF
ΔC_P	Capacitance tolerance (1)	@+25°C	-15	-	+15	%
T_{OP}	Operating temperature		-55	20	150	°C
T_{STG}	Storage temperature (2)		-70	-	165	°C
ΔC_T	Capacitance temperature variation	-55 °C to 150 °C	-	70	-	ppm/K
RV_{DC}	Rated voltage (3)		-	-	3.8(4) 3.4(5)	V_{DC}
BV	Break down voltage	@+25°C	11	-	-	V
ΔC_{RVDC}	Capacitance voltage variation	From 0 V to RV_{DC}, @+25°C	-	-	-0.1	$\%/V_{DC}$
IR	Insulation resistor	@RV_{DC}, +25°C, 120s	-	10	-	GΩ
ESR	Equivalent Serial Resistance	@+25°C, shunt mode	-	400	-	mΩ
ESL	Equivalent Serial Inductance	@+25°C, SRF shunt mode	-	180	-	pH
Fc-3dB	Cut-off frequency at 3dB	@+25°C	-	16	19	kHz
IL	Insertion loss	@ 20 GHz	-	0.35	-	dB
RL	Return loss	Up to 20 GHz, +25°C	12	-	-	dB
ESD	HBM stress (6)	JS-001-2017	2	-	-	kV

Table 1 - Electrical performances

(1): other tolerance available upon request
(2): without packaging
(3): Lifetime is voltage and temperature dependent, please refer to application note 'Lifetime of 3D capacitors'
(4): 10 years of intrinsic life time prediction at 100°C continuous operation
(5): 10 years of intrinsic life time prediction at 150°C continuous operation
(6): please refer to application note 'ESD Challenge in 3D Murata Integrated Passive technology'

Impedance of 100nF ULSC in Shunt mode

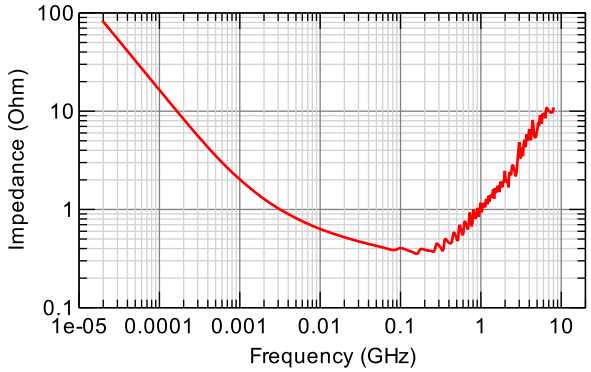


Figure 2 - 100nF ULSC Measured results (module of Z-parameters)

Module S-parameters of 100nF ULSC in transmission mode

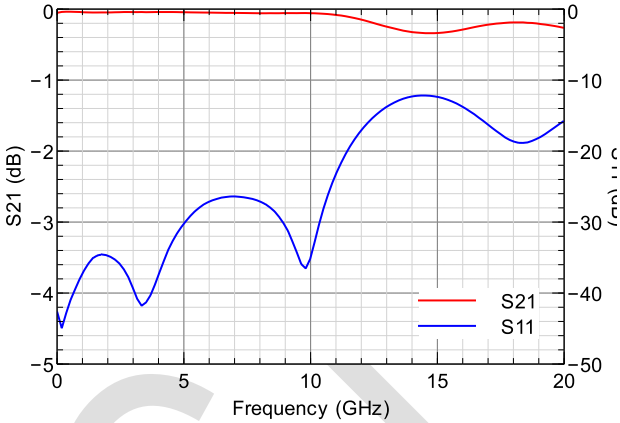
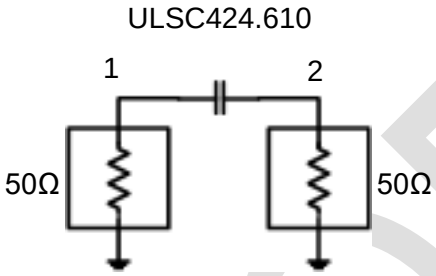


Figure 3 - 100nF ULSC measurement results (module of parameters)

Schematic of 100nF ULSC in transmission mode



Example of 0402 surface mounted

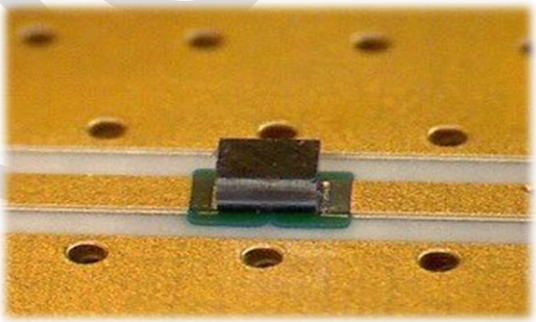


Figure 5 – micro picture of ULSC mounted on board in coplanar mode

10-mil Rogers 4350B.
Microstrip mode – line width = 0.551mm and gap = 0.246 mm.
(nominal 50 ohm characteristic impedance).

Figure 4 - 100nF ULSC measurement schematic

Pinning definition

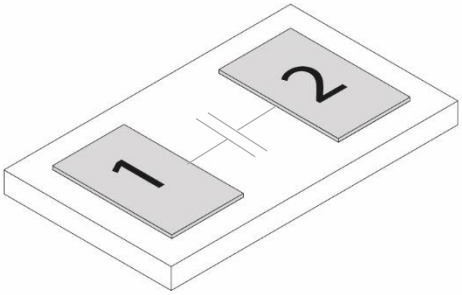


Figure 5 – Pinning definition

pin #	Symbol	Coordinates X / Y
1	Signal	-350.0 / 0.0
2	Signal	350.0 / 0.0

Table 2 - Pining description. Reference (0,0) located at the centre of the die.

Ordering Information

Murata Integrated Passive Devices delivers products with AQL level II (0.65). Tighter quality levels are available upon request.

Part number	Package		
	Packaging	Finishing	Description
935155424610-F1N	6” film frame carrier(1)	ENIG(2)	ULSC 0402 - 100nF – 2 pads – 1.2 x 0.7mm x 0.4mm
935155424610-T3N	T&R 1 000units(3)	ENIG(2)	ULSC 0402 - 100nF – 2 pads – 1.2 x 0.7mm x 0.4mm
935155424610-T4N	T&R 10 000units(3)	ENIG(2)	ULSC 0402 - 100nF – 2 pads – 1.2 x 0.7mm x 0.4mm
935156424610-F1N	6” film frame carrier(1)	ENIG(2)	ULSC 0402 - 100nF – 2 pads – 1.2 x 0.7mm x 0.1mm
935156424610-T3N	T&R 1 000units(3)	ENIG(2)	ULSC 0402 - 100nF – 2 pads – 1.2 x 0.7mm x 0.1mm
935156424610-T4N	T&R 10 000units(3)	ENIG(2)	ULSC 0402 - 100nF – 2 pads – 1.2 x 0.7mm x 0.1mm

Table 3 - Packaging and ordering information

(1) Other film frame carrier are possible on request
(2) ENIG : Min 0.1µm Au / 5µm Ni
(3) missing capacitors can reach 0.5%

Product Name	Die Name	Description
ULSC424.610	UC0402610	ULSC 100nF / 0402 / BV11 – 2 pads – 1.2 x 0.7 x 0.40 mm
ULSC424.610	UC0402610	ULSC 100nF / 0402 / BV11 – 2 pads – 1.2 x 0.7 x 0.10 mm

Table 4 - Die information

Pad Metallization

This surface mounted Silicon Capacitor is delivered as standard with NiAu (ENIG (0.1µm Au / 5µm Ni)).

Other Metallization, such as Copper, Thick Gold or Aluminum pads are possible on request.

Silicon dies are not sensitive to humidity, please refer to applications notes ‘Assembly Notes’ section ‘Handling precautions and storage’.

Material regulation

This product is RoHS compliant at the time of publication. For further information about regulation compliancy, please ask your sales representative.

Package outline

The product is delivered as a bare silicon die.

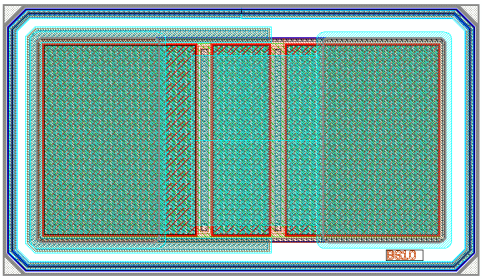


Figure 6 – Layout view

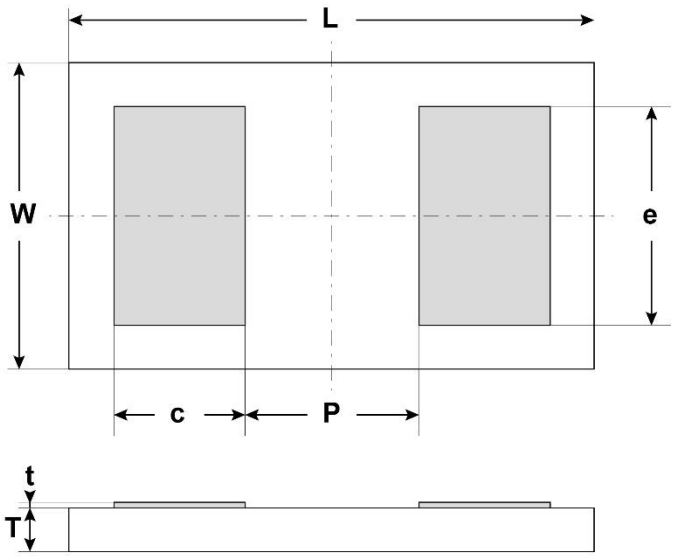


Figure 7: Package outline drawing

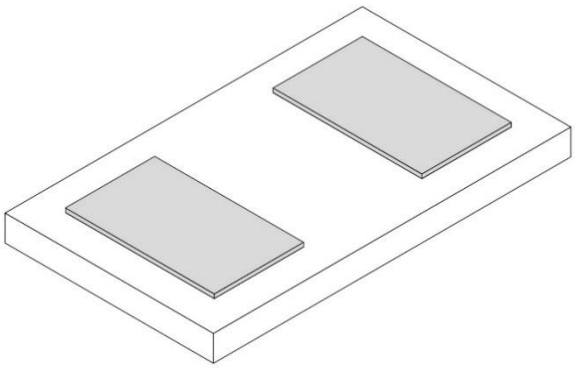


Figure 8: Package isometric view

L (mm)	W (mm)	T (mm)	c (mm)	P (mm)	e (mm)	t (mm)
1.2 ±0.04	0.7 ±0.04	0.40 or 0.10 ±0.01	0.30	0.40	0.50	0.005

Table 5 - Dimensions and tolerances

Assembly

The attachment techniques recommended by Murata on the customer's substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata capacitors **please download the assembly instructions on https://www.murata.com/en-us/products/capacitor/siliconcapacitors and read them carefully.**

Figure 6 Scan this QR Code to access the Murata Silicon Capacitor web page

Packaging format

Please refer to application note 'Products Storage Conditions and Shelf Life'.

Tape and Reel:

Dies are flipped in the tape cavity (bump down) with die ID located near the driving holes of the tape.

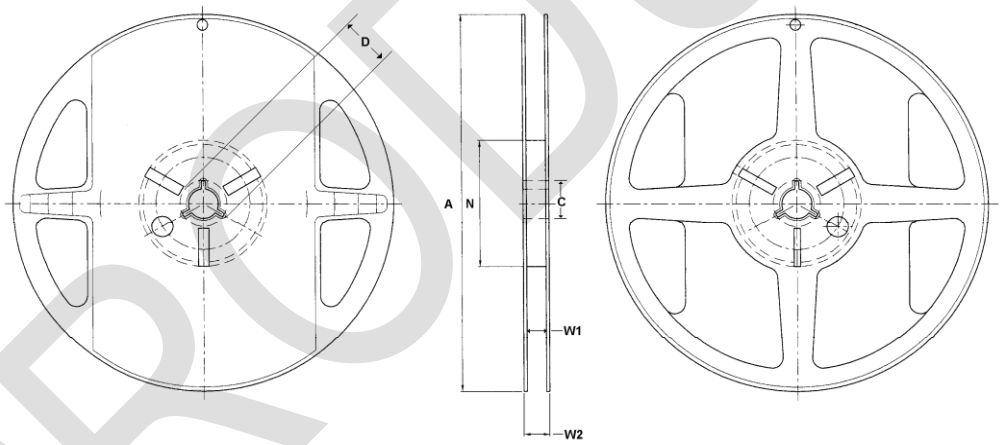


Figure 7 - Reel drawing

Tape Width	Diameter A	C	D	Hub N	W1	W2
8	178 (7 inches)	13.5	20.2	60	9.3	11.5

Table 6 – Reel dimensions (mm)

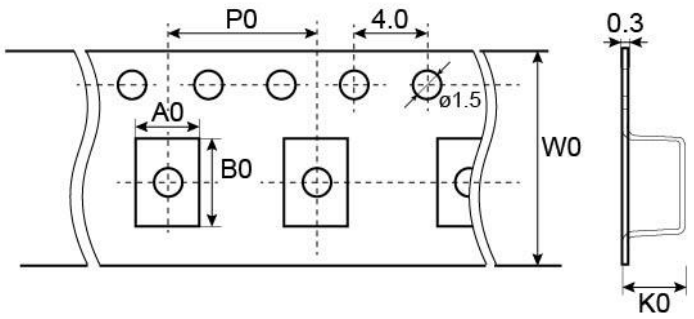


Figure 8 - Tape drawing

Cavity dimensions			Carrier tape width W0	Carrier tape pitch P0	Reel Capacity
Ao	Bo	Ko			
0.92	1.31	0.56	8	4	1 000

Table 7 - Tape dimensions (mm)

Film Frame Carrier:

With UV curable dicing tape (UV performed).

Good dies are identified using the SINF electronic mapping format. No ink is added on wafer to label other dies.

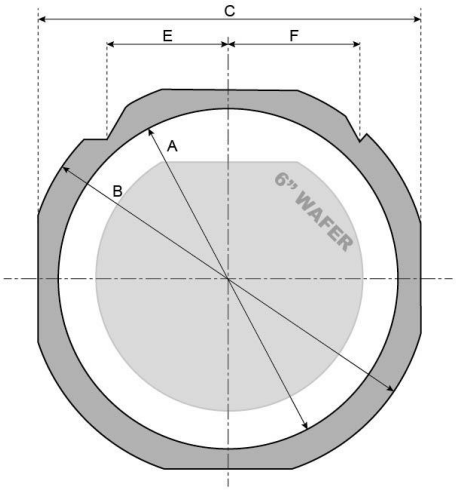


Figure 9 FF070 Frame with a 6" wafer

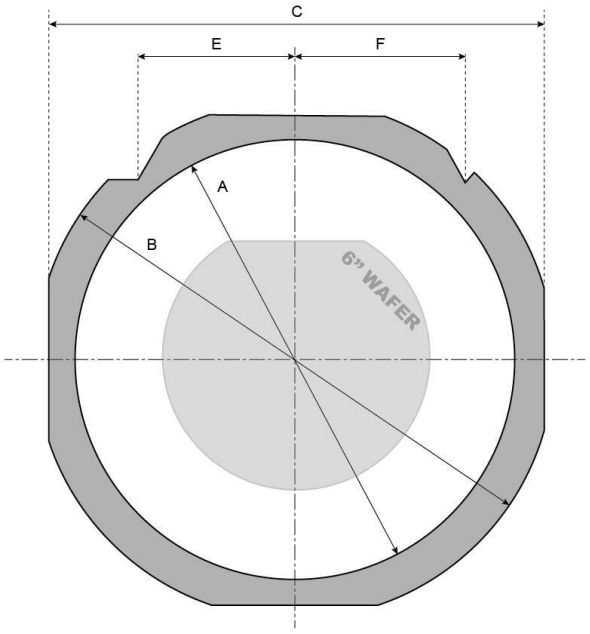


Figure 10 FF108 Frame with a 6" wafer

Frame Reference	Frame Style	Inside diameter A	Outside diameter B	Width C	Thickness	Pin location E	Pin location F
FF070 (1)	DTF-2-6-1	7.638”	8.976”	8.346”	0.048’’	2.370”	2.5’’
FF108 (1)	DTF-2-8-1	9.842”	11.653”	10.866”	0.048”	2.381”	2.5’’

Table 8 - Frame dimensions (inches)

(1) or equivalent

Expander grip ring 6” diameter:

With UV curable dicing tape (UV performed)

Good dies are identified using the SINF electronic mapping format. No ink is added on wafer to label other dies.

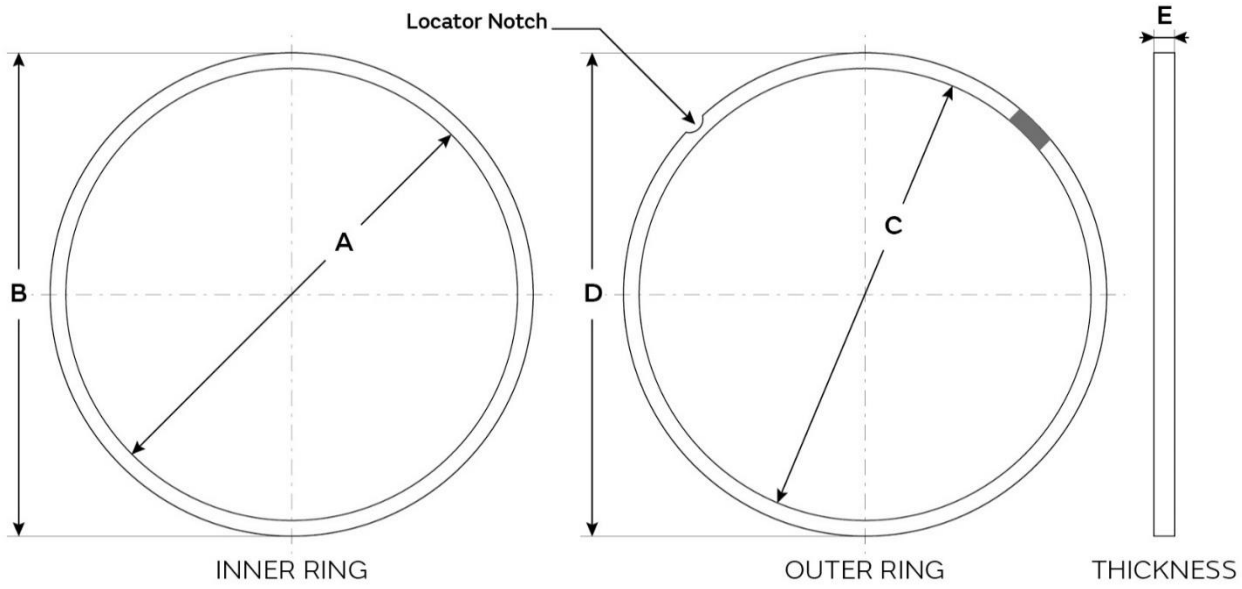


Figure 11 – Grip Ring drawing

Grip Ring Style	A	B	C	D	E	Locator Notch
GRP-2620-6 (1)	7.670”	7.973”	7.975”	8.280”	0.236”	None

Table 9 - Frame dimensions (inches)

(1) or equivalent

Definitions

Data sheet status

Objective specification: This data sheet contains target or goal specifications for product development.

Preliminary specification: This data sheet contains preliminary data; supplementary data may be published later.

Product specification: This data sheet contains final product specifications.

Limiting values

Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Electrical performances sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

Revision history

Revision	Date	Description	Author
Release 1.0	2014 February 18th	Objective specification	LDU
Release 1.1	2014 April 4th	Update	LDU/OGA
Release 1.2	2014 April 17th	Update of die thickness	LDU/OGA
Release 1.3	2014 May 22th	Packing update	OGA
Release 1.4	2014 June 17th	Packing update	OGA
Release 1.5	2017 July 3rd	Murata version	OGA
Release 1.6	2018 April 19th	Transfer FBC 0001	MSI / OGA
Release 3.00	2021 May 21st	Product revision	CGU, LLR, DDE, SCA, DYO, OGA

Disclaimer / Life support applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Murata customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Murata for any damages resulting from such improper use or sale.

www.murata.com

mis@murata.com