Low Profile Silicon Capacitor LPSC 0402 330 pF BV30

Rev.2.0

General description

Murata LPSC 3D Silicon Capacitor targets antenna matching, RF filtering and decoupling of active dies, in applications with height and volume constraints.

This product, based on PICS technology, is a single Low-ESL 330pF +/-5% capacitor in size 0402 offering low profile (100µm thin), with very high stability upon applied voltage, up to 150°C, very low leakage current and high level performances dedicated to industries such as Smart Cards, RFID tags and others where integration as well as excellent antenna matching play a key role.

The 330pF capacitor works efficiently and durably in RFID environments and can withstand 8kV ESD.

Assembly: Dedicated for wirebonding, Flip Chip or bumping either in the modules or directly attached to the inlays. Please refer to our assembly Application note for further recommendations

Pad finishing: Aluminum, other finishing available on request such as nickel/gold electroless, thin copper, lead-free nickel solder coating or thin gold.
Other capacitance values and other package size are available as a single die or capacitor array, on demand.

Market: All demanding market with space constraint such as RFID Tags, Smart Cards, Telecom and other applications where integration needs to be managed for performances

Key features

- **High stability**
  - **Temperature ±0,5%** (-55°C to +150°C)
  - **Voltage <0.1%/Volts**
  - **Negligible capacitance loss through ageing**
- **Small size 0402 (1.2mm x 0.7mm +/-40µm)**
- **Low leakage current <100pA**
- **High reliability**
- **Low ESL caracteristics**
- **Applicable for embedded and wire bonding**
- **Low Profile (100µm)**

Key applications

- **RFID & Smart Cards Applications**
- **HF (13,56MHz) & UHF (800/900MHz)**
- **Decoupling, Antenna matching & filtering of active device**
- **High reliability applications**
- **Devices with battery operations**
- **Volume limited applications**

Functional diagram

The next figure provides implementation set-up diagram.

Figure 1 Block Diagram

Electrical performances

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C	Capacitance value	@+25°C	-	330	-	pF
ΔC_P	Capacitance tolerance (1)	@+25°C	-5	-	+5	%
T_{OP}	Operating temperature		-55	-	+150	°C
T_{STG}	Storage temperature (2)		-70	-	+165	°C
ΔC_T	Capacitance temperature variation	-55°C to +150°C		70		ppm/K
RV_{DC}	Rated voltage (3)		-		16.0 (4) 14.8 (5)	V_{DC}
BV	Breakdown voltage	@+25°C	30	-	-	V_{DC}
ΔC_{RVDC}	DC Capacitance voltage variation	From 0V to RV_{DC}, @22°C	-	-	0.1	$\%/V_{DC}$
IR	Insulation resistance	@ RV_{DC}, +22°C, 120s	10	-	-	GΩ
ESR	Equivalent Series Resistance	@+22°C, shunt mode	-	300 (6)	-	mΩ
ESL	Equivalent Series Inductance	@+22°C, SRF shunt mode	-	500 (6)	-	pH
ESD	HBM stress (7)	JS-001-2017	2	-	-	kV

Table 1 - Electrical performances

(1): other tolerance available upon request
(2): without packaging
(3): Lifetime is voltage and temperature dependent, please refer to application note 'Lifetime of 3D capacitors'
(4): 10 years of intrinsic life time prediction at 100°C continuous operation
(5): 10 years of intrinsic life time prediction at 150°C continuous operation
(6): estimate, theoretical two terminal equivalent (applicable to multi term capacitors)
(7): please refer to application note 'ESD Challenge in 3D Murata Integrated Passive technology'

Pinning definition

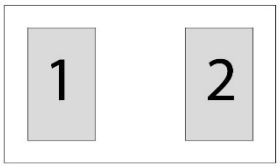

Figure 2 Pinning definition

pin #	Symbol	Coordinates X / Y
1	Signal	- 350 / 0
2	Signal	+350 / 0

Table 2 - Pining description. Reference (0,0) located at the centre of the die.

Ordering Information

Murata Integrated Passive Devices delivers products with AQL level II (0.65). Tighter quality levels are available upon request.

Part number	Package		
	Packaging	Finishing	Description
935121714333-T3N	Tape&Reel 1000 pcs(*)	NiAu(1)	LPSC/0402/330pF/100µm thick/T&R1000/ENIG/BV30 [CJ04023330]
935106049002-F2A	6” wafers on 8” Frame Carrier	Alu(2)	LPSC/0402/330pF(+/-5%)/100µm thick/FF108/3µm Al/BV30 [CJ0402333]
935121714333-F2N	6” wafers on 8” Frame Carrier	NiAu(1)	LPSC/0402/330pF(+/-15%)/100µm thick/FF108/ENIG/BV30 [CJ04023330]
935121714333-F2NJ	6” wafers on 8” Frame Carrier	NiAu(1)	LPSC/0402/330pF(+/-15%)/100µm thick/FF108/ENIG/BV30 [CJ04023330]

Table 3 - Packaging and ordering information

(1) Electroless Nickel – Immersion Gold
(2) AlSiCu
(*) missing capacitors can reach 0.5% (only applicable to T&R)

Product Name	Die Name	Description
935121714333	CJ0402333	LPSC/0402/330pF/BV30

Pad Metallization

The standard pad finishing metallization is NiAu (ENIG).

Other Metallization, such as Aluminum pads are possible on request.

Silicon dies are not sensitive to humidity, please refer to applications notes ‘Assembly Notes’ section ‘Handling precautions and storage’

Material regulation

This product is RoHS compliant at the time of publication. For further information about regulation compliancy, please ask your sales representative.

Package outline

The product is delivered as a bare silicon die, with passivation opening for contacts.

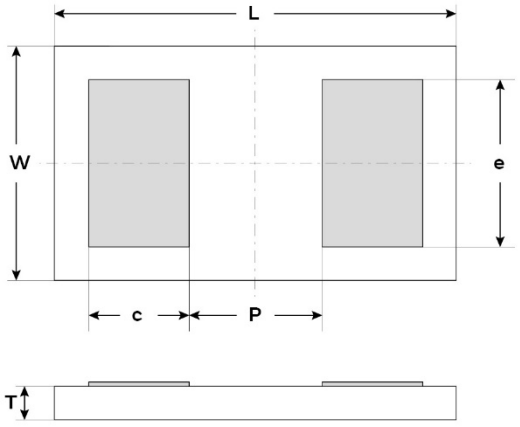

Figure 3 - Package outline drawing

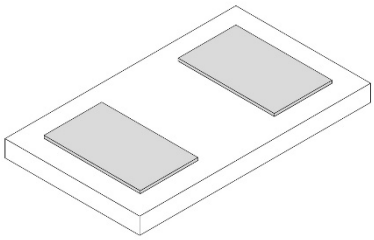

Figure 4 - Package isometric view

L (mm)	W (mm)	T (mm)	c (mm)	P (mm)	e (mm)
1.20 ±0.04	0.70 ±0.04	0.10 ±0.02	0.30	0.40	0.50

Table 4 - Dimensions and tolerances

Assembly

The attachment techniques recommended by Murata on the customer's substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata capacitors **please download the assembly instructions on https://www.murata.com/en-us/products/capacitor/siliconcapacitors and read them carefully.**

Figure 5 Scan this QR Code to access the Murata Silicon Capacitor web page

Packaging format

Please refer to application note 'Products Storage Conditions and Shelf Life'.

Tape and Reel:

Dies are flipped in the tape cavity (bump down) with die ID located near the driving holes of the tape.

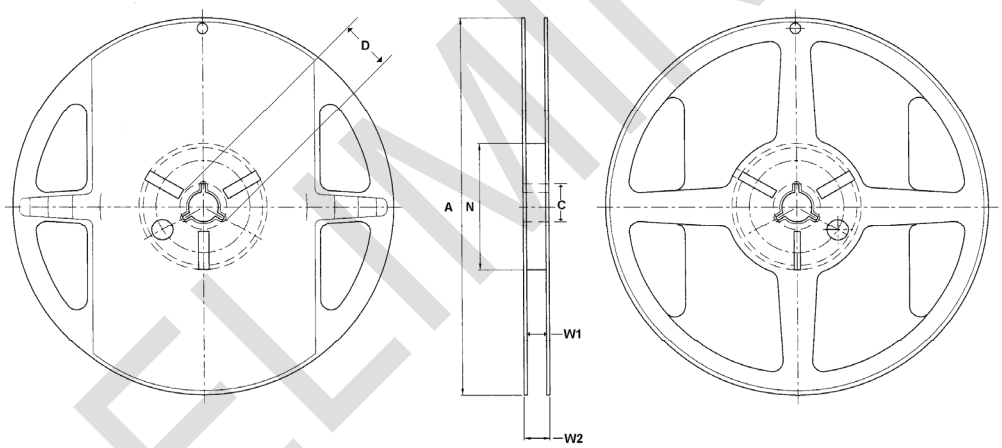

Figure 6 - Reel drawing

Tape Width	Diameter A	C	D	Hub N	W1	W2
8	178 (7 inches)	13.5	20.2	60	9	11.5

Table 5 – Reel dimensions (mm)

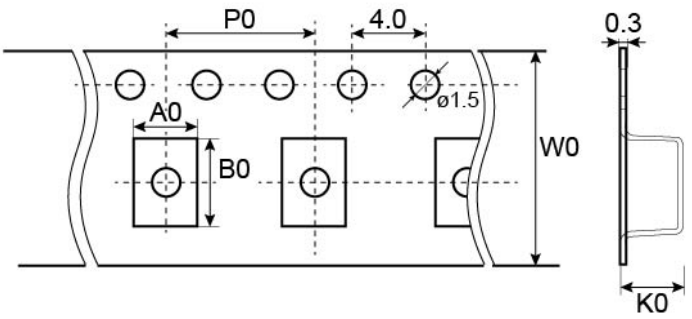

Figure 7 - Tape drawing

Cavity dimensions			Carrier tape width W0	Carrier tape pitch P0
Ao	Bo	Ko		
0.79	1.31	0.33	8	4

Table 6 - Tape dimensions (mm)

Film frame carrier:

Product are delivered as 6” wafers, diced and back-grinded, on UV curable tape (UV curing not performed, tape D510 or equivalent), on 8” FFC.

Good dies are identified using the SINF electronic mapping format. No link is added on wafer to label other dies.

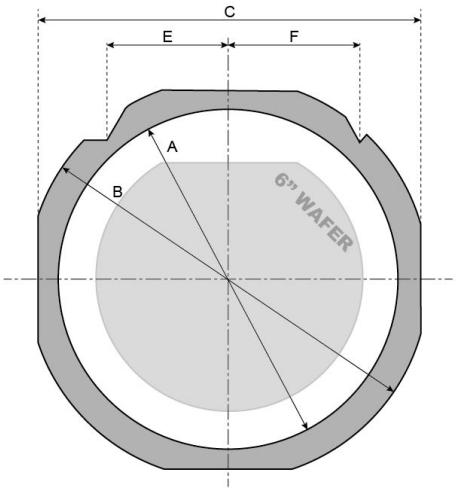

Figure 8 FF070 Frame with a 6" wafer

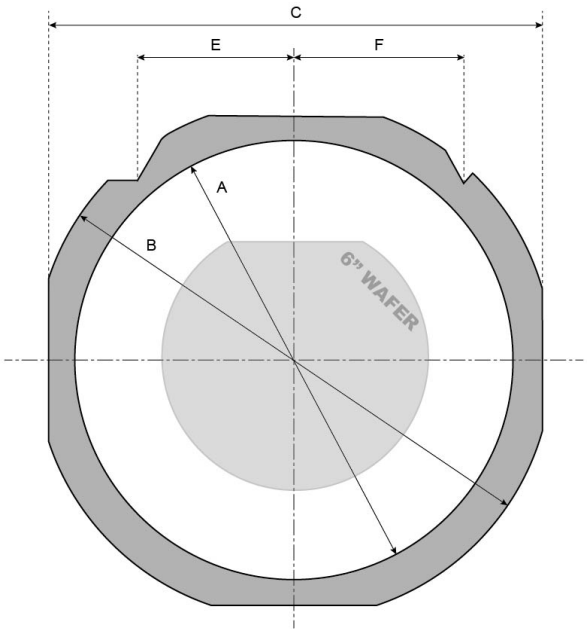

Figure 9 FF108 Frame with a 6" wafer

Frame Reference	Frame Style	Inside diameter A	Outside diameter B	Width C	Thickness	Pin location E	Pin location F
FF108 (1)	DTF-2-8-1	9.842”	11.653”	10.866”	0.048”	2.381”	2.5’’

Table 7 - Frame dimensions (inches)

(1) or equivalent

Definitions

Data sheet status

Objective specification: This data sheet contains target or goal specifications for product development.

Preliminary specification: This data sheet contains preliminary data; supplementary data may be published later.

Product specification: This data sheet contains final product specifications.

Limiting values

Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Electrical performances sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

Revision history

Revision	Date	Description	Author
1.0	13/11/2013	Objective specifications	L Lengignon
2.0	14/12/2020	Content and layout update (maturity level update)	CGU / FNO

Disclaimer / Life support applications

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