

# High Stability Silicon Capacitor HSSC 1812 3.3 $\mu$ F BV11



Rev. 2.00

## General description

HSSC Murata 3D Silicon Capacitor operates from  $-55^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ .

This version based on PICS technology which is the single 3.3 $\mu\text{F}$  Capacitor in size 1812 offering high temperature stability up to  $150^{\circ}\text{C}$ , very low leakage current and high level performances dedicated to industries such as avionic, dowhole, military, and others where integration, temperature and performance play a key role.

With his high stability across temperature range, the 3.3 $\mu\text{F}$  capacitor works efficiently and durably in harsh environments.

**Assembly:** This 1812 3.3 $\mu\text{F}$  has 2 NiAu pads

Other capacitance values and other package size are available as a single die or capacitor array, please feel free to contact us.

## Key features

- High temperature stability (up to  $150^{\circ}\text{C}$ )
  - Temperature  $\pm 0.5\%$  ( $-55^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ )
  - Voltage  $< -0.1\%$ /Volt
  - Negligible capacitance loss through ageing
- Small size : 1812 [4.7mmx3.6mm]
- Low profile (400 $\mu\text{m}$ ).
- Low leakage current  $< 1\text{nA}$
- High reliability
- Compatible with high temperature cycling during manufacturing operations (exceeding  $300^{\circ}\text{C}$ )
- Applicable for almost embedded and wire bonding application

## Key applications

- Any demanding applications, such as medical, aerospace, automotive industrial...
- Supply decoupling / filtering of active device
- High reliability applications
- Devices with battery operations
- High temperature applications
- High volumetric efficiency (i.e. capacitance per unit volume)



## Functional diagram

The next figure provides implementation set-up diagram.



Figure 1 Block Diagram

## Electrical performances

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C	Capacitance value	@+25°C	-	3300	-	nF
$\Delta C_P$	Capacitance tolerance <sup>(1)</sup>	@+25°C	-15	-	+15	%
T <sub>OP</sub>	Operating temperature		-55	20	+150	°C
T <sub>STG</sub>	Storage temperature <sup>(2)</sup>		-70	-	+165	°C
$\Delta C_T$	Capacitance temperature variation	-40°C to +200°C		62		ppm/K
RV <sub>DC</sub>	Rated voltage <sup>(3)</sup>		-	3.3	-	V <sub>DC</sub>
BV	Breakdown voltage	@+25°C	11	-	-	V <sub>DC</sub>
$\Delta C_{RVDC}$	DC Capacitance voltage variation	From 0V to RV <sub>DC</sub> , @22°C	-	-	-0.1	%/V <sub>DC</sub>
IR	Insulation resistance	@ RV <sub>DC</sub> , +22°C, 120s	-	100	-	G $\Omega$
ESR	Equivalent Series Resistance	@+22°C, shunt mode	-	1	-	$\Omega$
ESL	Equivalent Series Inductance		-	100	-	pH

Table 1 - Electrical performances

(1): other tolerance available upon request

(2): without packaging

(3): Lifetime is voltage and temperature dependent, please refer to application note 'Lifetime of 3D capacitors'



## Pinning definition

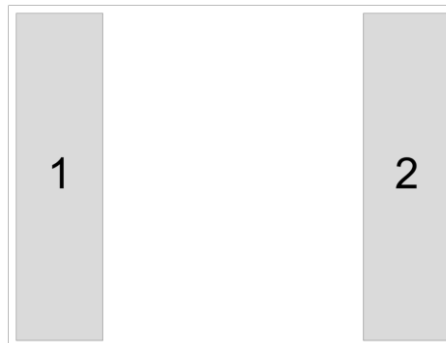


Figure 2 Pinning definition

pin #	Symbol
1	Signal1
2	Signal2

Table 2 - Pinning description.

## Ordering Information

Murata Integrated Passive Devices delivers products with AQL level II (0.65). Tighter quality levels are available upon request.

Part number	Package		
	Packaging	Finishing	Description
935131429733-T3N	Tape & Reel 1000 <sup>(3)</sup>	NiAu <sup>(1)</sup>	High Reliability Silicon Capacitor 3.3uF, -55/+150C, 1812, 4.7 x 3.6 mm, Thickness : 400um, BV: 11V <sup>(2)</sup>

Table 3 - Packaging and ordering information

- (1) detail for pad finishing
- (2) Refer to Package outline
- (3) missing capacitors can reach 0.5% (only applicable to T&R)

Product Name	Die Name	Description
935131429733-T3N	C1812733	High Reliability Silicon Capacitor 3.3uF, -55/+150C, 1812, 4.7 x 3.6 mm, Thickness : 400um, BV: 11V

Table 4 - Die information



## Pad Metallization

The standard pad finishing metallization is NiAu (ENIG).

Other Metallization are possible on request.

Silicon dies are not sensitive to humidity, please refer to applications notes 'Assembly Notes' section 'Handling precautions and storage'.

## Material regulation

This product is RoHS compliant at the time of publication. For further information about regulation compliancy, please ask your sales representative.

## Package outline

The product is delivered as a bare silicon die.

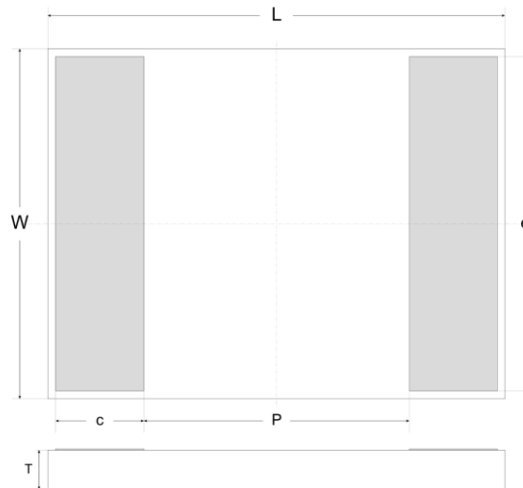


Figure 3 - Package outline drawing

L (mm)	W (mm)	T (mm)	c (mm)	P (mm)	e (mm)
4.66±0.02	3.56±0.02	0.40±0.015	0.90	2.70	3.40

Table 5 - Dimensions and tolerances

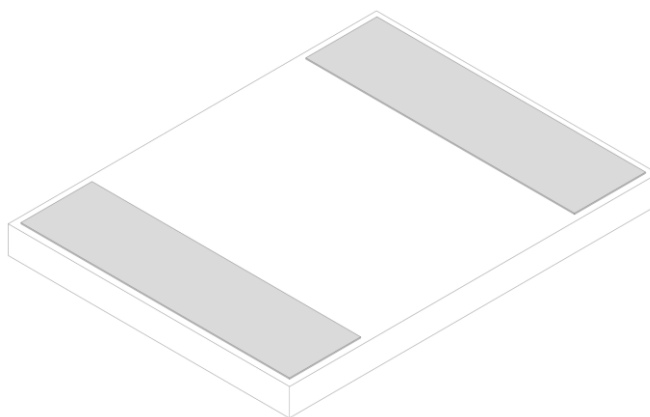


Figure 4: isometric view

PRELIMINARY



## Assembly

The attachment techniques recommended by Murata on the customer's substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata capacitors **please download the assembly instructions on <https://www.murata.com/en-us/products/capacitor/siliconcapacitors> and read them carefully.**



Figure 5 Scan this QR Code to access the Murata Silicon Capacitor web page

## Packaging format

Please refer to application note 'Products Storage Conditions and Shelf Life'.

### Tape and Reel:

Dies are flipped in the tape cavity (bump down) with die ID located near the driving holes of the tape.

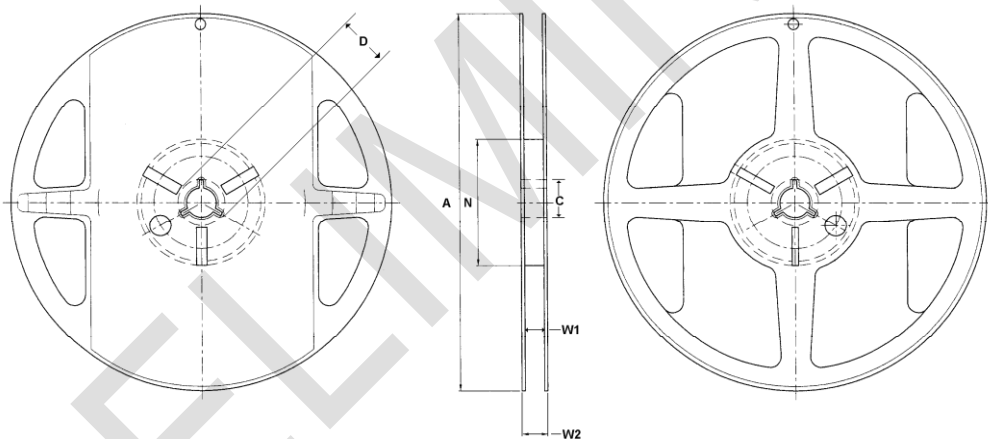


Figure 6 - Reel drawing

Tape Width	Diameter A	C	D	Hub N	W1	W2
8	178 (7 inches)	13.5	20.2	60	9.3	11.5

Table 6 – Reel dimensions (mm)

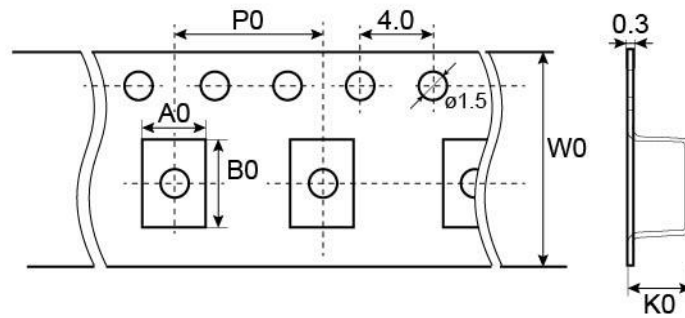


Figure 7 - Tape drawing

Cavity dimensions			Carrier tape width $W_0$	Carrier tape pitch $P_0$	Reel Capacity
$A_0$	$B_0$	$K_0$			
3.8	5.1	0.7	12	8	1000

Table 7 - Tape dimensions (mm)



## Definitions

### Data sheet status

**Objective specification:** This data sheet contains target or goal specifications for product development.

**Preliminary specification:** This data sheet contains preliminary data; supplementary data may be published later.

**Product specification:** This data sheet contains final product specifications.

### Limiting values

Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Electrical performances sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

### Application information

Where application information is given, it is advisory and does not form part of the specification.

## Revision history

Revision	Date	Description	Author
Release 1.0	2013 November 27th	Objective specification	LLE
Release 2.0	2021 January 29 <sup>th</sup>	Preliminary specification	LLE

## Disclaimer / Life support applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Murata customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Murata for any damages resulting from such improper use or sale.

Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent or other industrial or intellectual property rights.

Murata Integrated Passive Solutions S.A. makes no representation that the use of its products in the circuits described herein, or the use of other technical information contained herein, will not infringe upon existing or future patent rights. The descriptions contained herein do not imply the granting of licenses to make, use, or sell equipment constructed in accordance therewith. Specifications are subject to change without notice.



[www.murata.com](http://www.murata.com)

[mis@murata.com](mailto:mis@murata.com)