Low Profile SiCap LPSC 0402 100pF BV11

Rev. 2.1

General description

LPSC 3D Silicon Capacitor targets antenna matching, RF filtering and decoupling of active dies, in applications with height and volume constraints.
This version based on PICS technology, is a single 100pF Capacitor in size 0402 offering low profile (100µm thin), with very high stability upon applied voltage, up to 150°C, with very low leakage current and high level performances dedicated to industries such as Smart Card, RFID tags and others where integration as well as excellent antenna matching play a key role.
The 100pF capacitor works efficiently and durably in RFID environments.
Assembly: Dedicated for wirebonding, Flip Chip or Bumping either in the modules or directly attached to the inlays.
Please refer to our assembly Application note for further recommendations
Pad finishing: nickel/gold electroless (ENiG), other finishing available on request such as aluminum, thin copper, lead-free nickel solder coating or thin gold.
Other capacitance values and other package size are available as a single die or capacitor array, on demand.
Market: All demanding market with space constraint such as RFID Tags, Smart Cards, Telecom and other applications where integration needs to be managed for performances.

Key features

- High stability:
  - Temperature ±0.5% (-55°C to +150°C)
  - Voltage <0.1%/Volts
  - Negligible capacitance loss through ageing
- Small size : 0402
- Low leakage current < 100pA
- High reliability
- Applicable for embedded and wire bonding
- Low profile (100µm)

Key applications

- RFID & Smart Cards Applications:

HF (13.56MHz) & UHF (800/900MHz)

- Decoupling, antenna matching & filtering of active device
- High reliability applications
- Devices with battery operations
- High volumetric efficiency *(i.e. capacitance per unit volume)*

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Functional diagram

The next figure provides implementation set-up diagram.

Figure 1 Block Diagram

Electrical performances

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C	Capacitance value	@+25°C	-	100	-	pF
ΔC_P	Capacitance tolerance (1)	@+25°C	-15	-	+15	%
T_{OP}	Operating temperature		-55	20	+150	°C
T_{STG}	Storage temperature (2)		-70	-	+165	°C
ΔC_T	Capacitance temperature variation	-55°C to +150°C	-0.5	-	+0.5	%
RV_{DC}	Rated voltage (3)		-	-	3.4 (4) 3.8 (5)	V_{DC}
BV	Breakdown voltage	@+25°C	11	-	-	V_{DC}
ΔC_{RVDC}	DC Capacitance voltage variation	From 0V to RV_{DC}, @22°C	-	-	0.1	$\%/V_{DC}$
IR	Insulation resistance	@ RV_{DC}, +22°C, 120s	-	10	-	GΩ
ESR	Equivalent Series Resistance	@+22°C, shunt mode	-	150		mΩ
ESL	Equivalent Series Inductance	@+22°C, SRF shunt mode	-	600		pH
ESD	HBM stress (6)	JS-001-2017	200	-	-	V
SRF	Self Resonance Frequency		550	-	-	MHz

Table 1 - Electrical performances

(1): other tolerance available upon request
(2): without packaging
(3): Lifetime is voltage and temperature dependent, please refer to application note 'Lifetime of 3D capacitors'
(4): 10 years of intrinsic life time prediction at 100°C continuous operation
(5): 10 years of intrinsic life time prediction at 150°C continuous operation
(6): please refer to application note 'ESD Challenge in 3D Murata Integrated Passive technology'

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Frequency response

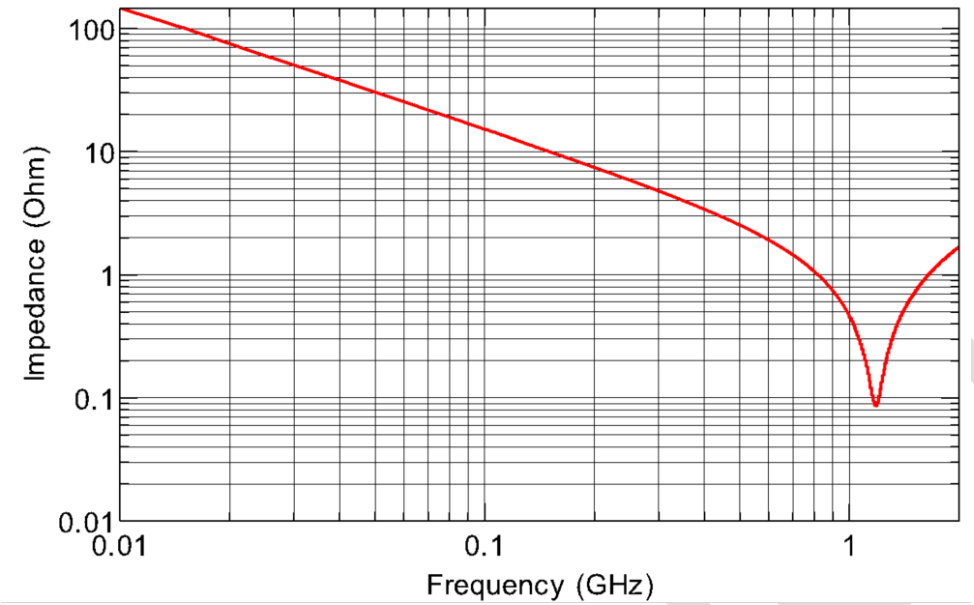

Figure 2 - 100pF frequency response

Pinning definition

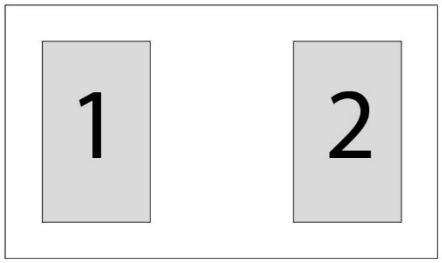

Figure 3 Pinning definition

pin #	Symbol	Coordinates X / Y
1	Signal	-350.0 / 0.0
2	Signal	350.0 / 0.0

Table 2 - Pining description. Reference (0,0) located at the centre of the die.

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Ordering Information

Murata Integrated Passive Devices delivers products with AQL level II (0.65). Tighter quality levels are available upon request.

Part number (16NC)	Package		
	Packaging	Finishing	Description
935 121 424 310-T3N	T&R 1 000units (*)	NiAu (1)	LPSC/0402/100pF/100µm thick/T&R1000/ENIG/BV11 [C0402310]
935 121 424 310-F2N	6” wafer on 8” FFC	NiAu(1)	LPSC/0402/100pF/100µm thick/FF108/ENIG/BV11 [C0402310]
935 121 424 310-F2A	6” wafer on 8” FFC	Alu (2)	LPSC/0402/100pF/100µm thick/FF108/3µmAl/BV11 [C0402310]

Table 3 - Packaging and ordering information

(1) Electroless Nickel – Immersion Gold
(2) Alu (AlSiCu)
(*) missing capacitors can reach 0.5% (only applicable to T&R)

Pad Metallization

The standard pad finishing metallization is NiAu (ENIG).

Other Metallization, such as Copper, Thick Gold or Aluminum pads are possible on request.

Silicon dies are not sensitive to humidity, please refer to applications notes ‘Assembly Notes’ section ‘Handling precautions and storage’.

Material regulation

This product is RoHS compliant at the time of publication. For further information about regulation compliancy, please ask your sales representative.

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Package outline

The product is delivered as a bare silicon die.

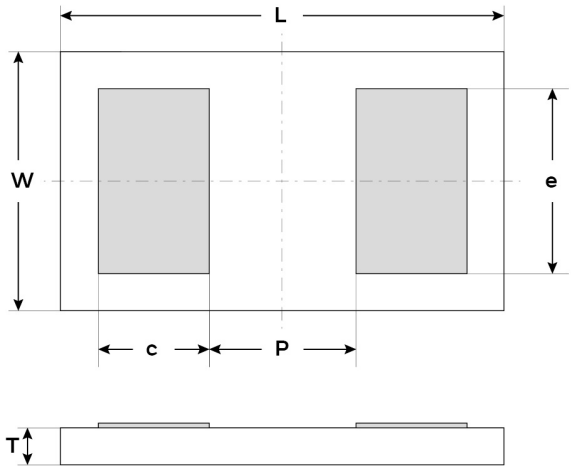

Figure 4 - Package outline drawing

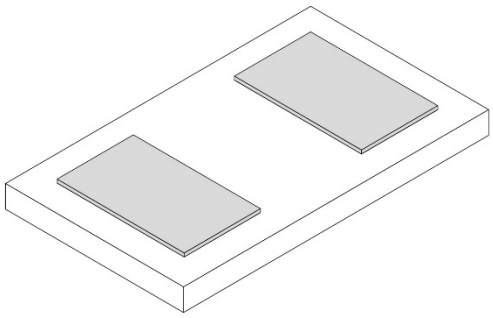

Figure 5 - Package isometric view

L (mm)	W (mm)	T (mm)	c (mm)	P (mm)	e (mm)
1.2 ±0.04	0.70 ±0.04	0.10 ±0.015	0.30	0.40	0.50

Table 4 - Dimensions and tolerances

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Assembly

The attachment techniques recommended by Murata on the customer's substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata capacitors **please download the assembly instructions on https://www.murata.com/en-us/products/capacitor/siliconcapacitors and read them carefully.**

Figure 6 Scan this QR Code to access the Murata Silicon Capacitor web page

Packaging format

Please refer to application note 'Products Storage Conditions and Shelf Life'.

Tape and Reel:

Dies are flipped in the tape cavity (bump down) with die ID located near the driving holes of the tape.

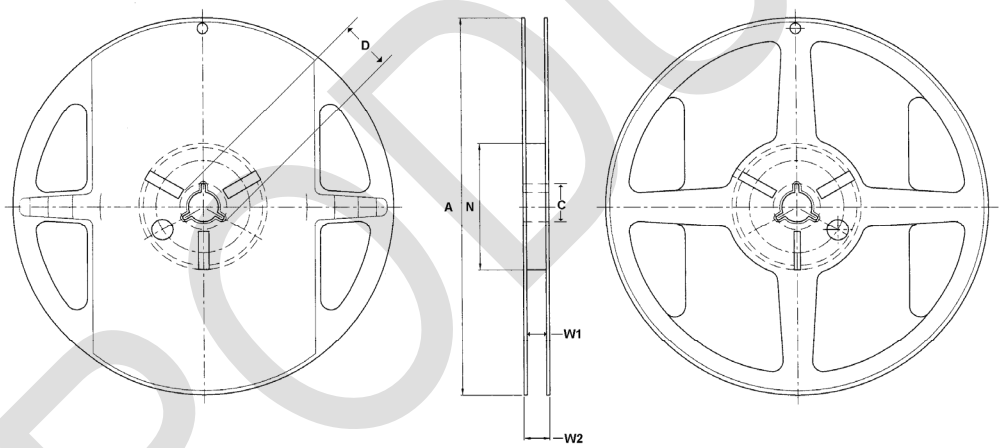

Figure 7 - Reel drawing

Tape Width	Diameter A	C	D	Hub N	W1	W2
8	178 (7 inches)	13.5	20.2	60	9.3	11.5

Table 5 – Reel dimensions (mm)

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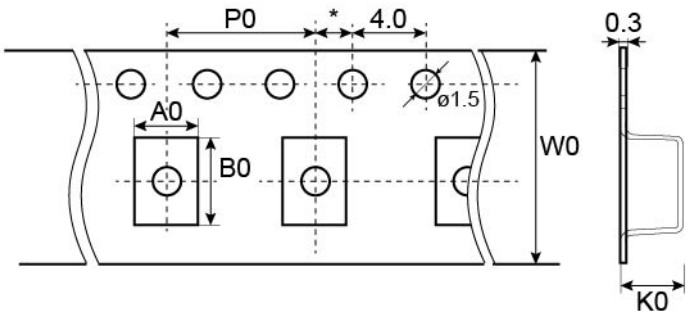

Figure 8 - Tape drawing

Cavity dimensions			Carrier tape width W0	Carrier tape pitch P0	Reel Capacity
Ao	Bo	Ko			
0.92	1.31	0.56	8	2	1 000

Table 6 - Tape dimensions (mm)

Film frame carrier:

With UV curable dicing tape (UV performed).

Good dies are identified using the SINF electronic mapping format. No ink is added on wafer to label other dies.

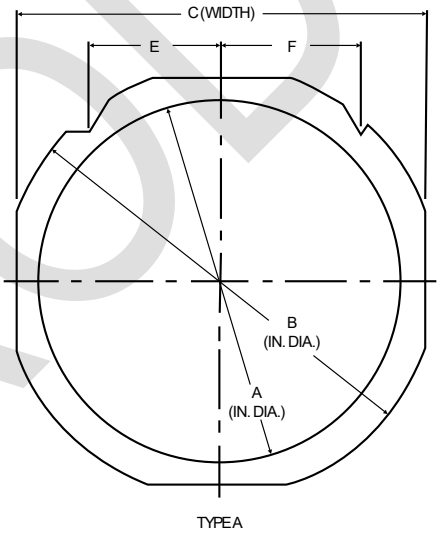

Figure 9 – Film frame drawing

Wafer diameter	Inside diameter A	Outside diameter B	Width C	Thickness	Pin Location E	Pin Location F	Frame style
6''	9.842"	11.653"	10.866"	0.048''	2.381"	2.5''	DTF-2-8-1

Table 7 - Frame dimensions (inches)

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Definitions

Data sheet status

Objective specification: This data sheet contains target or goal specifications for product development.

Preliminary specification: This data sheet contains preliminary data; supplementary data may be published later.

Product specification: This data sheet contains final product specifications.

Limiting values

Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Electrical performances sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

Revision history

Revision	Date	Description	Author
1.0	27/11/201313	Objective specification	LLE
1.1	26/03/2014	Product specification	OGA
1.2	27/03/2014	Update	OGA
2.0	17/07/2020	New template	FN, CGU, SCA
2.1	03/09/2020	Minor changes - Updates	FN, SCA

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