Ultra Broadband Silicon Capacitor UBSC722.410 (1nF / 0201M / BV=30V)

Rev. 1.8

General description

Market: UBSC Capacitor targets Optical communication system such as ROSA/TOSA, SONET and all optoelectronics as well as High speed data system or products.

The UBSC is suitable for DC blocking, feedback, coupling and bypassing applications in all broadband optoelectronics and High-speed data system.

The unique technology of integrated passive device in silicon, developed by Murata Integrated Passive Solutions, offers unique performances with low insertion loss, low reflection and phase stability from 1600 KHz to 60 GHz+.

These capacitors in ultra-deep trenches in silicon have been developed in a semiconductor process, in order to integrate trench MOS capacitor providing high capacitance value of 1nF (for kHz–MHz range) and MIM capacitors for low capacitance value (for GHz range), both in a SMT 0201M (0.6 x 0.3mm).

The UBSC capacitor provides very high stability of the capacitance over temperature, voltage variation as well as a very high reliability.

UBSC capacitors have an extended operating temperature ranging from -55 to 150°C, with very low capacitance change over temperature (+60ppm/K).

Assembly: flip chip applications through existing laminated packages or rigid PCB, ceramic substrate, FR4 or flex platforms suitable.

Bump finishing: SAC305 type 6.

Key features

- Ultra-Broadband performance to 67 GHz
- Resonance free
- Phase stability
- Insertion low < 0.3dB Typ. up to 60 GHz
- Ultra-high stability of capacitance value:
  - Temperature 60ppm/K (-55 °C to +150 °C)
  - Voltage <0.1%/Volts
  - Negligible capacitance loss through ageing
- Low profile: 140µm including bump height
- Break down voltage > 30V
- Low leakage current < 100pA
- High reliability
- High operating temperature (up to 150 °C)
- Compatible with high temperature cycling during manufacturing operations (exceeding 300 °C)
- Compatible with EIA 0201 footprint
- SAC305 40µm bumps after reflow

Key applications

- ROSA/TOSA
- SONET
- High speed digital logic
- Microwave/millimetre system
- Volume limited applications
- Broadband test equipment

Functional diagram

The next figure provides implementation set-up diagram.

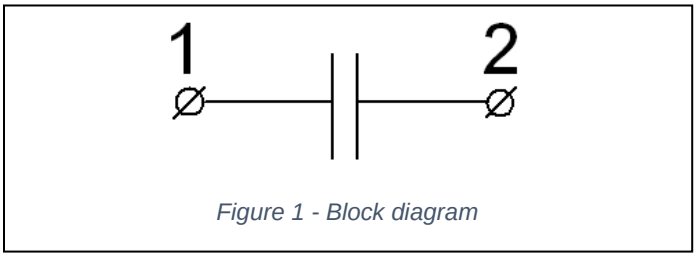


Figure 1 - Block diagram

Electrical performances

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C	Capacitance value	@+25°C	-	1	-	nF
ΔC_P	Capacitance tolerance (1)	@+25°C	-15	-	+15	%
T_{OP}	Operating temperature		-55	20	150	°C
T_{STG}	Storage temperature (2)		-70	-	165	°C
ΔC_T	Capacitance temperature variation	-55 °C to 150 °C	-	60	-	ppm/K
RV_{DC}	Rated voltage (3)		-	10	16(4) 13.6(5)	V_{DC}
BV	Break down voltage	@+25°C	30	-	-	V
ΔC_{RVDC}	Capacitance voltage variation	From 0 V to RV_{DC}, @+25°C	-	-	0.1	%/V_{DC}
IR	Insulation resistor	@RV_{DC}, +25°C, 120s	-	10	-	GΩ
ESR	Equivalent Serial Resistance(6)	@ +25°C, shunt mode	-	-	1.4	Ohm
ESL	Equivalent Serial Inductance(6)	@ +25°C, SRF shunt mode	-	-	100	pH
Fc-3dB	Cut-off frequency at 3dB(6)	@ +25°C	-	1600	1872	kHz
IL	Insertion loss(6)	@ 20 GHz, +25°C	-	0.2	-	dB
		@ 40 GHz, +25°C	-	0.3	-	dB
		@ 60 GHz, +25°C	-	0.3	-	dB
RL	Return loss(6)	Up to 60 GHz, +25°C	13	-	-	dB
ESD	HBM stress (7)	JS-001-2017	8	-	-	kV

Table 1 - Electrical performances

(1): other tolerance available upon request
(2): without packaging
(3): Lifetime is voltage and temperature dependent, please refer to application note 'Lifetime of 3D capacitors'
(4): 10 years of intrinsic life time prediction at 100°C continuous operation
(5): 10 years of intrinsic life time prediction at 150°C continuous operation
(6): Measured
(7): please refer to application note 'ESD Challenge in 3D Murata Integrated Passive technology'

Module S-parameters of 1nF UBSC in transmission mode

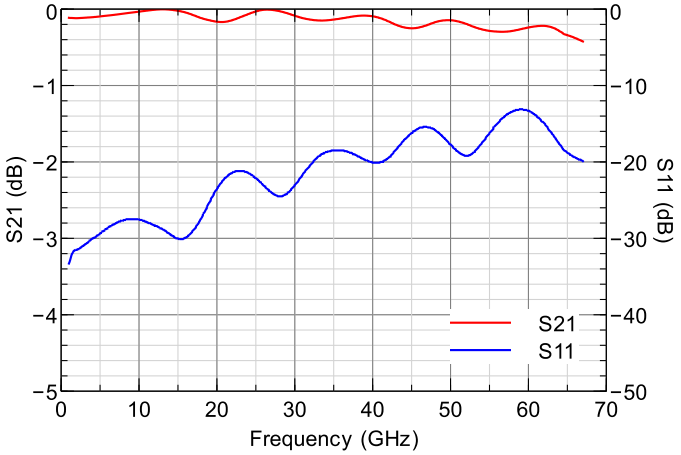


Figure 2 - 1nF UBSC measurement results (module of S-parameters)

Schematic of 1nF UBSC in transmission mode

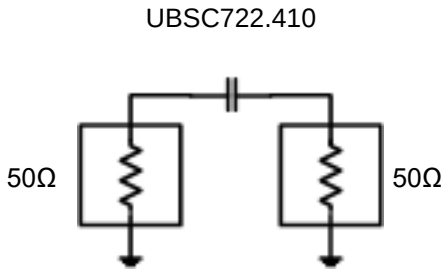


Figure 3 - 1nF UBSC measurement schematic

Capacitance variation versus DC biasing

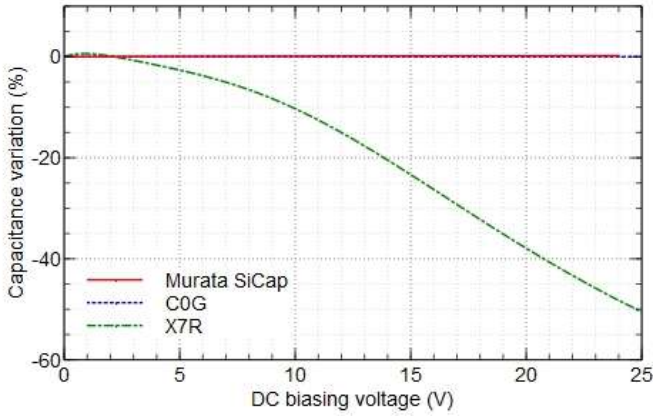


Figure 4 - Capacitance variation versus DC biasing (in function of UBSC and MLCC technology)

Capacitance variation versus operating temperature

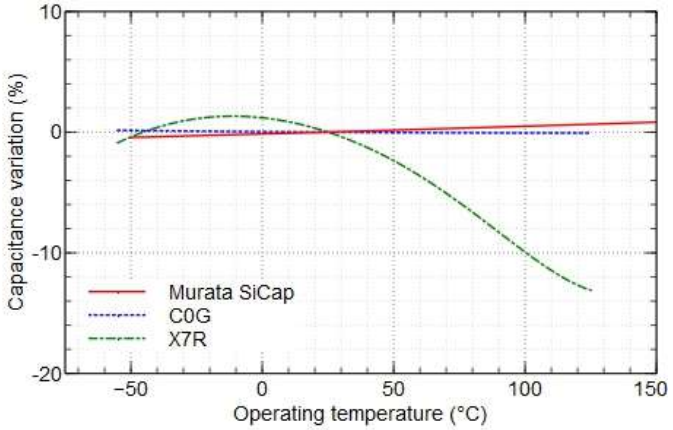


Figure 5 - Capacitance variation versus operating temperature (in function of UBSC and MLCC technology)

Failure Predictions

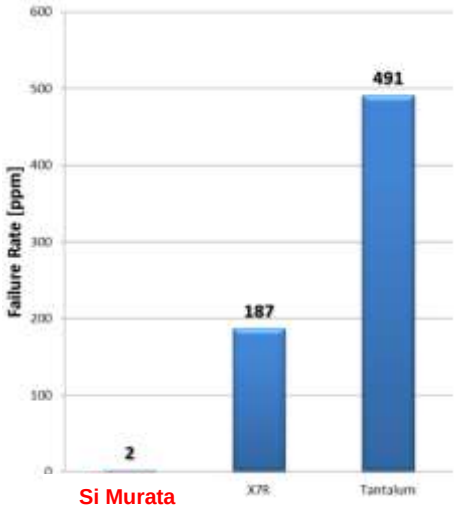
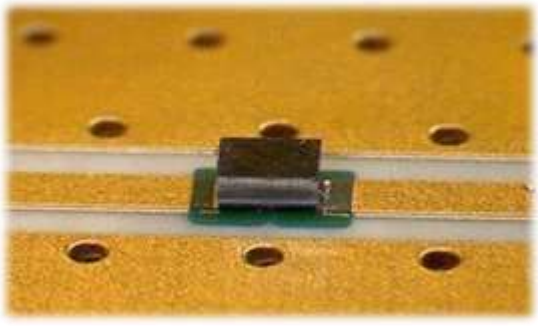


Figure 6 - Projected capacitor Failure Rate in 10 Years at 85°C and 50% of the Rating voltage (in function of UBSC, tantalum and MLCC technology)

Test bench



4-mils Rogers 4350B.
Nominal Pad dimensions – pad length = 0.100 mm, pad width and line width = 0.150mm, pad gap = 0.300 mm. (nominal 50 ohm characteristic impedance).

Figure 7 - test bench picture used for 1nF UBSC characterization

Pinning definition

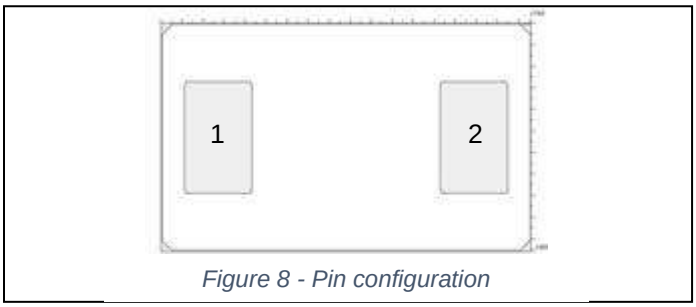


Figure 8 - Pin configuration

pin #	Symbol (optional)	Coordinates X / Y
1	Signal	-150.0 / 0.0
2	Signal	150.0 / 0.0

Table 2 - Pining description. Reference (0,0) located at the centre of the die.

Ordering Information for UBSC722.410

Regardless of packaging, Murata Integrated Passive Devices delivers products with AQL level II (0.65).

Type number (15NC)	Package		
	Packaging	Finishing	Description
935 152 722 410-F1S	6" film frame carrier(1)	SAC(2)	UBSC0201M – 1nF – 2 pads – 0.60mm x 0.30mm x 0.14mm
935 152 722 410-T3S	7" T&R with 1Kpieces / reel (3)	SAC(2)	UBSC0201M – 1nF – 2 pads – 0.60mm x 0.30mm x 0.14mm

(1) Other film frame carrier are possible on request
(2) ENIG (Min 0.1µm Au / 5µm Ni) + SAC305 type 6
(3) missing capacitors can reach 0.5%

Table 3 - Packaging and ordering information

Product Name	Die Name	Description
UBSC722.410	XJM0201410	UBSC 1nF/0201M/BV>30V – 2 pads – 0.6 x 0.3 x 0.14 mm (4)

(4): Capacitor die dimension: 0.56 x 0.26 mm (without scribe line)
Capacitor die size after sawing: 0.6 x 0.3 mm
Scribe line = 80µm (saw lane currently used = 40µm)

Table 4 - Die information

Pad Metallization

The UBSC Capacitor is delivered as standard with SAC305 bumping.

Other Metallization, such as ENIG, Copper, Thick Gold or Aluminum pads are possible on request.

UBSC series is compatible with standard reflow technology.

It is recommended to design mirror pads on the PCB.

Silicon dies are not sensitive to humidity, please refer to applications notes 'Assembly Notes' section 'Handling precautions and storage'.

For further information, please see our mounting application note.

Material regulation

This product is RoHS compliant.

Package outline

The product is delivered as a naked silicon die, with passivation opening for contacts.

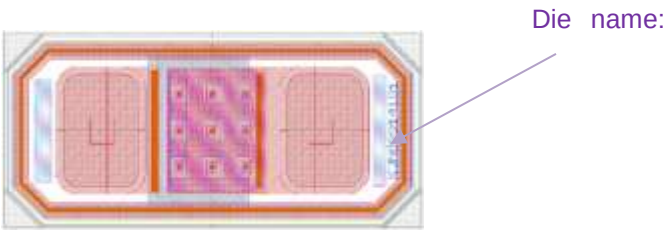


Figure 9 - Micro photography of a 1nF Capacitor

L (mm)	W (mm)	T (mm)	c (mm)	P (mm)	e (mm)	t (mm)
0.60 ±0.02	0.30 ±0.02	0.10 ±0.01	0.10	0.20	0.15	0.04(1)

(1) Solder joint height after reflow on board.

Table 5 - Dimensions and tolerances

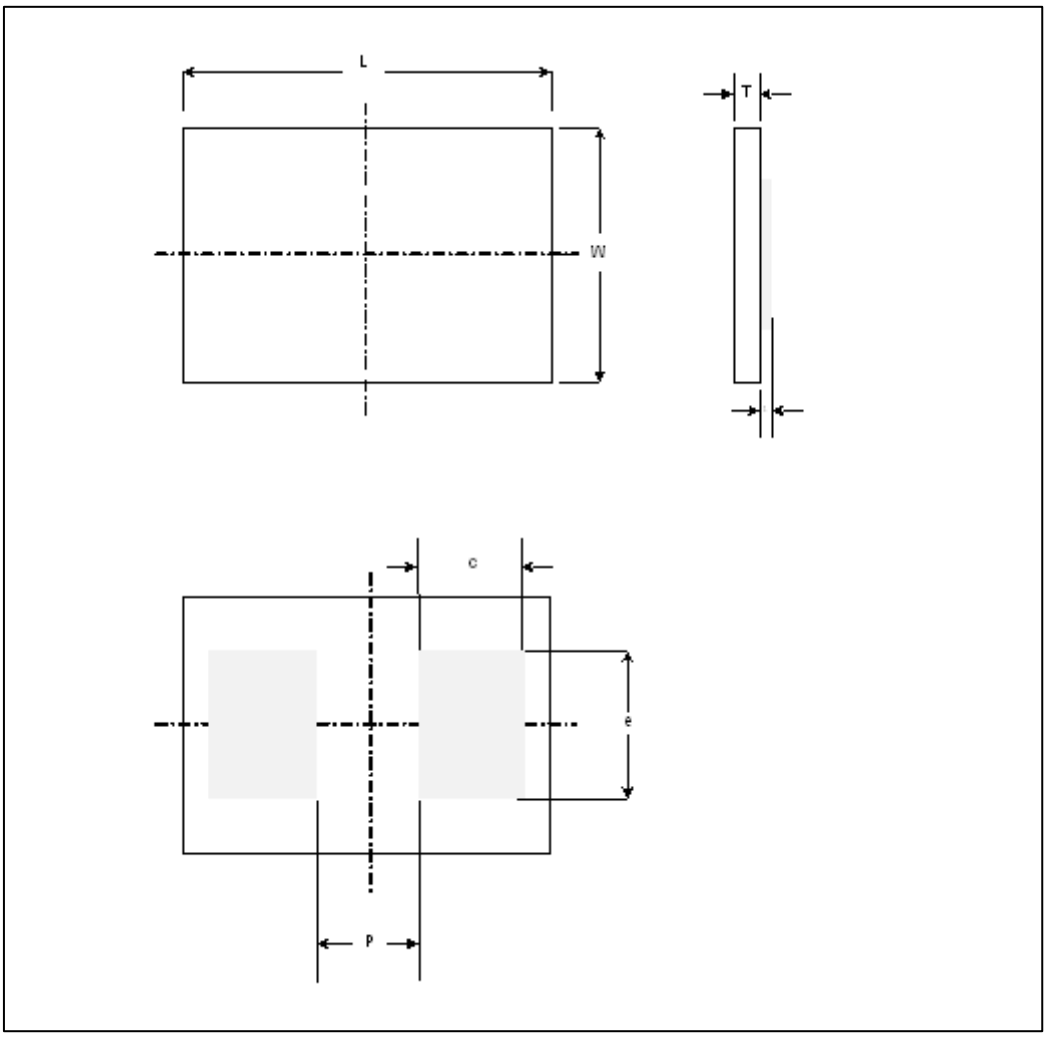


Figure 10 - Package outline 1nF Capacitor

Assembly

The attachment techniques recommended by Murata on the customer's substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata capacitors **please download the assembly instructions on https://www.murata.com/en-us/products/capacitor/siliconcapacitors and read them carefully.**

Packaging format

Please refer to application note 'Products Storage Conditions and Shelf Life'.

Tape and Reel: (Die orientation (flip) within the case related to T&R orientation)

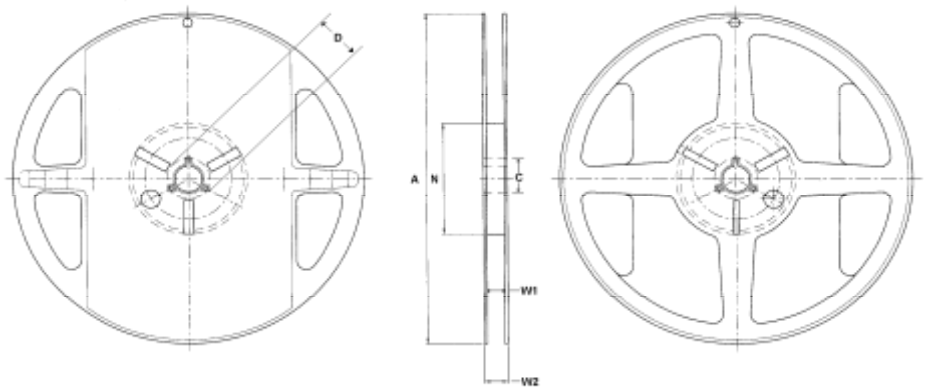


Figure 11 - Reel drawing

Tape Width	Diameter A	C	D	Hub N	W1	W2
8	178 (7 inches)	13.5	20.2	60	93	11.5

Table 6 - Reel dimensions (mm)

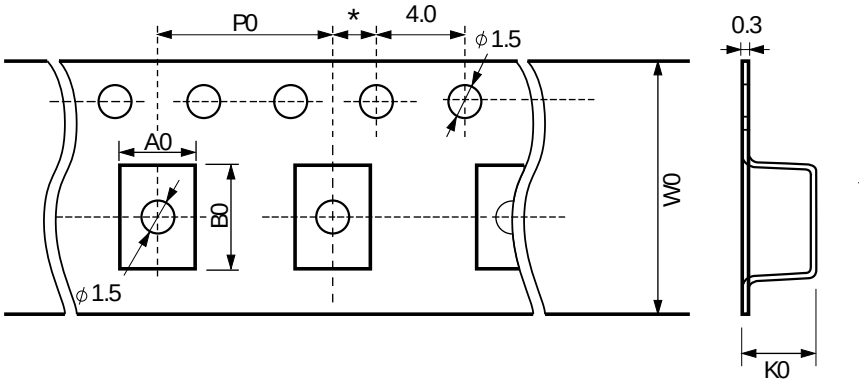


Figure 12 - Tape drawing

Cavity dimensions			Carrier tape width W0	Carrier tape pitch P0	Quantity per reel
A0	B0	K0			
0.36	0.66	0.20	8	2	1 000

Table 7 - Tape dimensions (mm)

Film frame carrier: Ref: FF070 (Perfection products)

With tape Adwill D175 (UV performed) usually used for 400 µm & 250 µm products

With tape Adwill D510 (UV performed) usually used for 100 µm products

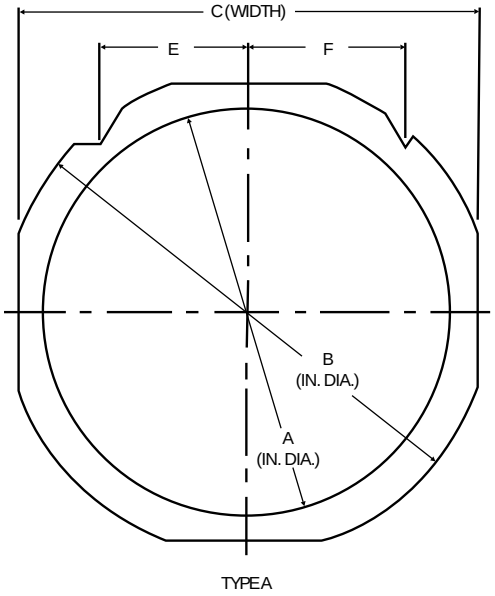


Figure 13 - Film frame drawing

Wafer diameter	Inside diameter A	Outside diameter B	Width C	Thickness	Pin location E	Pin location F	Frame style
6''	7.639"	8.976"	8.346"	0.048''	2.370"	2.5''	DTF-2-6-1

Table 8 - Frame dimensions (inches)

Definitions

Data sheet status

Objective specification: This data sheet contains target or goal specifications for product development.

Preliminary specification: This data sheet contains preliminary data; supplementary data may be published later.

Product specification: This data sheet contains final product specifications.

Limiting values

Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Electrical performances sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

Revision history

Revision	Date	Description	Author.
Release 1.0	**2016 June 28th**	**Objective specification**	**OGA**
Release 1.1	**2016 Sept 22nd**	**Preliminary specification**	**LLR/NNO**
Release 1.2	**2016 Sept 29th**	**Packing update**	**OGA**
Release 1.3	**2017 March 27th**	**Packing update**	**OGA**
Release 1.4	**2017 April 4th**	**Murata version**	**OGA**
Release 1.5	**2017 June 9th**	**Rated voltage update**	**OGA**
Release 1.6	**2018 Jan 15th**	**Update**	**OGA**
Release 1.7	**2018 March 29th**	**Update**	**OGA**
Release 1.8	**2018 April 23th**	**Transfer FBC 0001**	**MSI / OGA**

Disclaimer / Life support applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Murata customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Murata for any damages resulting from such improper use or sale.

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