具有电流检测功能的 TPS7B770x-Q1 车用单通道和双通道天线 LDO

1 特性

- 符合汽车类应用的 要求
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度 1 级：–40°C 至 125°C 的环境运行温度范围
  - 器件人体放电模式 (HBM) 静电放电 (ESD) 分类等级 2
  - 器件组件充电模式 (CDM) ESD 分类等级 C4B
- 具有电流检测和可调节限流功能的单通道和双通道低压降稳压器 (LDO)
- 4.5V 至 40V 宽输入电压范围，45V 负载突降保护
- FB 接至 GND 时进入电源开关模式
- 1.5V 至 20V 可调节输出电压
- 每通道输出电流高达 300mA
- 可通过外部电阻实现可调节限流功能
- 高精度电流检测功能，无需进一步校准即可在低电流下检测天线开路情况
- 高电源抑制比：100Hz 时的典型值为 73dB
- 集成反向极性保护，低至 -40V 且无需外部二极管
- 负载电流为 100mA 时，最大压降电压为 500mV
- 与 2.2μF 至 100μF（ESR 为 1mΩ 至 5Ω）范围内的输出电容器搭配使用时可保持稳定
- 集成了保护和诊断功能
  - 热关断
  - 欠压锁定 (UVLO)
  - 短路保护
  - 反向电池极性保护
  - 反向电流保护
  - 输出端电池短路保护
  - 输出端感性负载钳位
  - 多通道/器件间的电流检测功能复用
  - 能够通过电流检测功能区分所有故障
- 16 引脚 HTSSOP PowerPAD™封装

2 应用

- 信息娱乐系统有源天线电源
- 环视摄像头电源
- 适用于小电流应用的高侧电源 开关

3 说明

TPS7B770x-Q1 系列器件采用具有电流检测功能的单通道和双通道高电压低压差稳压器 (LDO)，适合在 4.5V 至 40V（45V 负载突降保护）的宽输入电压范围内工作。这些器件通过一条每通道电流为 300mA 的同轴电缆为有源天线的低噪声放大器供电。每条通道还可提供 1.5V 至 20V 的可调节输出电压。

这些器件通过电流检测和错误引脚提供诊断。为监视负载电流，高侧电流检测电路提供了与检测的负载电流成比例的模拟输出。电流检测功能非常精确，无需进一步校正即可检测开路、正常和短路条件。可以在通道和器件间对电流检测进行多路复用，以节省模数转换器 (ADC) 资源。每个通道还通过外部电阻实现了可调节限流功能。

集成了反极性二极管，因此无需使用外部二极管。这些器件具有标准热关断功能、输出端电池短路保护功能以及反向电流保护功能。各通道可在电感式开关断开期间为输出端提供内部电感式钳位保护。

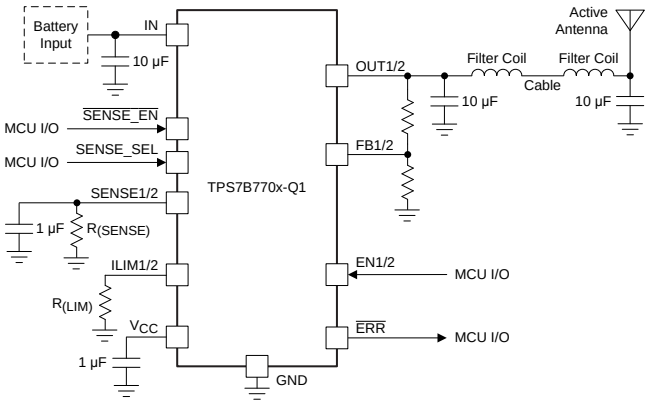
这些器件的工作环境温度范围为 -40°C 至 +125°C。

器件信息(1)

器件型号	封装	通道
TPS7B7701-Q1	HTSSOP (16)	单通道
TPS7B7702-Q1	HTSSOP (16)	双通道

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。

703A I2C



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (November 2015) to Revision C	Page
• Changed NC pin description in *Pin Functions* table to clarify which pins are internally connected	3
• Added row to *Recommended Operating Conditions* for OUT1, OUT2, and OUT regarding switched-mode operation	4
• 已更改 *Current-Limit Resistor Selection* section for clarity	17

Changes from Revision A (May 2015) to Revision B	Page
• Deleted the min and max limits of –4% and 4% from the current-limit threshold voltage parameter in the *Electrical Characteristics* table	6
• Added to the current-limit accuracy table note for the programmable current-limit accuracy parameter in the *Electrical Characteristics* table	6
• 已添加 graphs for the TPS7B7701-Q1 device in the *Typical Characteristics* section	7
• 已删除 the channel 2 PSRR graph in the *Typical Characteristics* section	7
• 已添加 additional test conditions for the *9- to 16-V Line Transient* and *Power Up* graphs in the *Typical Characteristics* section	9
• 已添加 additional test conditions of the *Power Up* graphs in the *Application Curves* section	18

Changes from Original (January 2015) to Revision A	Page
• 发布了完整版数据表	1

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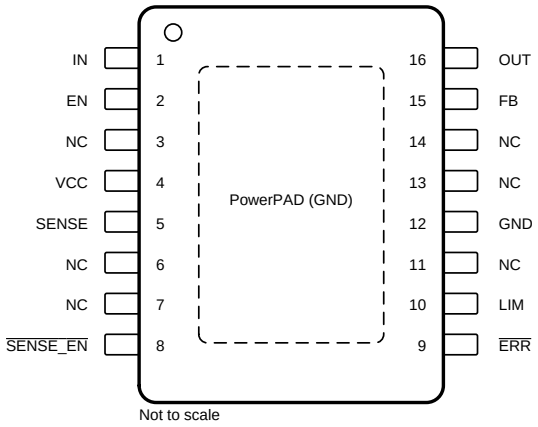
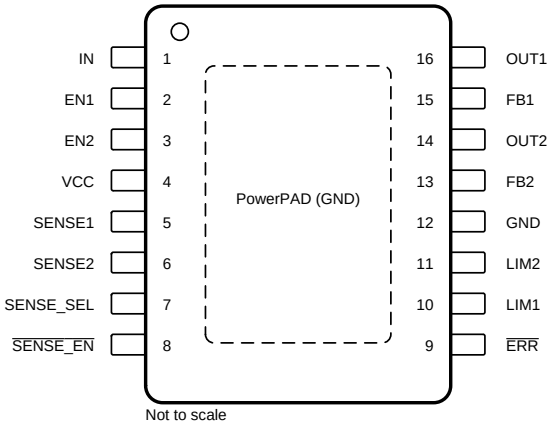
5 Pin Configuration and Functions

Single-Channel TPS7B7701-Q1 PWP Package
16-Pin HTSSOP With PowerPAD
Top View



Dual-Channel TPS7B7702-Q1 PWP Package
16-Pin HTSSOP With PowerPAD
Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	SINGLE-CHANNEL	DUAL-CHANNEL		
EN	2	—	Input	Active-high enable input for the OUT pin with internal pulldown.
EN1	—	2	Input	Active-high enable input for the OUT1 pin with internal pulldown.
EN2	—	3	Input	Active-high enable input for the OUT2 pin with internal pulldown.
$\overline{\text{ERR}}$	9	9	Output	This pin is an open-drain fault indicator for general faults.
FB	15	—	Input	Feedback input for setting OUT voltage. Connect FB to GND for current-limited switch operation.
FB1	—	15	Input	Feedback input for setting OUT1 voltage. Connect FB1 to GND for current-limited switch operation.
FB2	—	13	Input	Feedback input for setting OUT2 voltage. Connect FB2 to GND for current-limited switch operation.
GND	12	12	Ground	Ground reference
IN	1	1	Power	Input power-supply voltage
LIM	10	—	Output	Programmable current-limit pin. Connect a resistor to GND to set the current limitation level. This pin does not need an external capacitor. To set to internal current limit, short this pin to GND.
LIM1	—	10	Output	Programmable current-limit pin for channel 1. Connect a resistor to GND to set the current limitation level for channel 1. This pin does not need an external capacitor. To set to internal current limit, short this pin to GND.
LIM2	—	11	Output	Programmable current-limit pin for channel 2. Connect a resistor to GND to set the current limitation level for channel 2. This pin does not need an external capacitor. To set to internal current limit, short this pin to GND.
NC	3, 13, 14	—	—	Not connected. Connect the NC pins to ground or leave floating.
	6, 7, 11	—	—	Internally connected. These pins must either be floated or connected to GND.
OUT	16	—	Power	Output voltage
OUT1	—	16	Power	Output voltage 1
OUT2	—	14	Power	Output voltage 2
SENSE	5	—	Output	Output of current sense for sensing. To set the SENSE output voltage level, connect a resistor between this pin and GND. In addition, connect a 1-µF capacitor from this pin to GND for frequency compensation of the current-sense loop. Short this pin to GND if not used.
SENSE1	—	5	Output	Output of current sense for sensing. SENSE1 current is proportional to the current flow through OUT1 and SENSE 2 current is proportional to OUT2 current when SENSE_SEL and $\overline{\text{SENSE_EN}}$ are low. To set the SENSEx output voltage level, connect a resistor between this pin and GND. In addition, connect a 1-µF capacitor from the SENSEx pin to GND for frequency compensation of the current-sense loop. Short the SENSEx pin to GND if not used.
SENSE2	—	6	Output	
$\overline{\text{SENSE_EN}}$	8	8	Input	This pin is the enable and disable of the current-sense pin for multiplexing, active-low enable.
SENSE_SEL	—	7	Input	This pin selects the current sense between channel 1 and channel 2. See 表 2 for details.
V_{CC}	4	4	Output	Internal 4.5-V regulator. Connect 1-µF ceramic capacitor between V_{CC} and GND for frequency compensation.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Input voltage	Unregulated input, IN	–40	45	V
	EN, EN1, and EN2	–0.3	45	V
Regulated output[2]	V_{CC}[3][4]	–0.3	6	V
	OUT1 and OUT2	–0.3	45	V
Low-voltage pins	SENSE, SENSE1, and SENSE2[3][4]	–0.3	V_{CC} + 0.3	V
	LIM, LIM1, LIM2, $\overline{\text{SENSE_EN}}$, SENSE_SEL, $\overline{\text{ERR}}$, FB, FB1, and FB2[3][4]	–0.3	7	V
Operating junction temperature, T_J		–40	150	°C
Operating ambient temperature, T_A		–40	125	°C
Storage Temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) There is an internal diode connects between the OUT and GND pins with 300-mA DC current capability for inductive clamp protection.
(3) All voltage values are with respect to GND.
(4) Absolute maximum voltage.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 8, 9, and 16)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_I	Unregulated input		4.5	40	V
	EN, EN1, and EN2		0	40	V
	Low-voltage pins	SENSE, SENSE1, SENSE2, $\overline{\text{SENSE_EN}}$, SEN_SEL , $\overline{\text{ERR}}$, FB, FB1, FB2, LIM, LIM1, LIM2, and V_{CC}	0	5.3	V
	OUT1, OUT2, and OUT	Normal-mode operation	1.5	20	V
		Switched-mode operation	1.5	35	
C_O	Output capacitor stability range		2.2	100	µF
$C_{O(ESR)}$	Output capacitor ESR stability range		0.001	5	Ω
T_J	Junction temperature		–40	150	°C
T_A	Ambient temperature		–40	125	°C

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6.4 Thermal Information

THERMAL METRIC[1]		TPS7B7701-Q1 PWP (HTSSOP) 16 PINS	TPS7B7702-Q1 PWP (HTSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance [2]	45.9	40.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.2	27.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.7	22.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.3	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24.5	22	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.7	2.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The thermal data is based on JEDEC standard high K profile – JESD 51-7. The copper pad is soldered to the thermal land pattern. Also correct attachment procedure must be incorporated

6.5 Electrical Characteristics

at V_I = 14 V and T_J = –40ºC to +150ºC (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT (IN)						
V_I	Input voltage		4.5		40	V
I_Q	Quiescent current	TPS7B7701-Q1: V_I = 4.5 to 40 V, $V_{(EN)}$ ≥ 2 V, $I_{(OUT)}$ = 0.1 mA		0.6	1	mA
		TPS7B7702-Q1: V_I = 4.5 to 40 V, $V_{(EN1)}$ and $V_{(EN2)}$ ≥ 2 V, $I_{(OUT1)}$ and $I_{(OUT2)}$ = 0.1 mA		0.6	1	
$I_{(shutdown)}$	Shutdown current	TPS7B7701-Q1: EN = GND			5	µA
		TPS7B7702-Q1: EN1 = EN2 = GND			5	
I_{nom}	Operating current	TPS7B7701-Q1: $V_{(EN)}$ ≥ 2 V, $I_{(OUT)}$ ≤ 300 mA, GND current			4.5	mA
		TPS7B7702-Q1: $V_{(EN1)}$ and $V_{(EN2)}$ ≥ 2 V, $I_{(OUT1)}$ and $I_{(OUT2)}$ ≤ 300 mA, GND current			6	
$V_{(BG)}$	Bandgap	Reference voltage for FB	–2%	1.233	2%	V
$V_{(UVLO)}$	Undervoltage lockout falling	Ramp IN down until the output turns off			4	V
V_{hys}	Hysteresis			0.4		V
INPUT CONTROL PINS (EN, EN1, EN2, $\overline{\text{SENSE_EN}}$, AND SENSE_SEL)						
V_{IL}	Logic input low level	For EN, EN1, EN2, $\overline{\text{SENSE_EN}}$, and SENSE_SEL	0		0.7	V
V_{IH}	Logic input high level	For EN, EN1, EN2, $\overline{\text{SENSE_EN}}$, and SENSE_SEL	2			V
$I_{I(SENSE_EN)}$	$\overline{\text{SENSE_EN}}$ input current	$V_{(SENSE_EN)}$ = 5 V, $V_{(ENx)}$ ≥ 2 V			10	µA
$I_{I(SENSE_SEL)}$	SENSE_SEL input current	$V_{(SENSE_EN)}$ = 5 V, $V_{(ENx)}$ ≥ 2 V			10	µA
$I_{I(EN)}$	Enable input current	$V_{(ENx)}$ ≤ 40 V			10	µA
REGULATED OUTPUT (OUT, OUT1, AND OUT2)						
V_O	Regulated output	40 V ≥ V_I ≥ V_O + 1.5 V and V_I ≥ 4.5 V, I_O = 1 to 300 mA[1]	–2%		2%	
$\Delta V_{O(\Delta VI)}$	Line regulation	V_I = V_O + 1.5 V to 40 V and V_I ≥ 6 V, I_O = 10 mA, voltage variation on FB pin			10	mV
$\Delta V_{O(\Delta IO)}$	Load regulation	I_O = 1 mA to 200 mA, voltage variation on FB pin			20	mV
$V_{(DROPOUT)}$	Dropout voltage	Measured between IN and OUTx, I_O = 100 mA			500	mV
I_O	Output current	V_O in regulation	0		300	mA
PSRR	Power supply ripple rejection[2]	I_O = 100 mA, C_O = 2.2 µF, f = 100 Hz		73		dB
CURRENT SENSE AND CURRENT-LIMIT						
I_O/I_{SENSE}	OUTx to SENSEx current ratio (I_O / I_{SENSEx})	V_I = 4.5 V to 40 V, 5 mA ≤ I_O ≤ 300 mA		198		

(1) External feedback resistor is not considered.
(2) Design information; specified by design, not production tested.

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Electrical Characteristics (continued)

at V_I = 14 V and T_J = –40ºC to +150ºC (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	OUTx to SENSEx current ratio accuracy	I_O = 100 to 300 mA	–3%		3%	
		I_O = 50 to 100 mA	–5%		5%	
		I_O = 10 to 50 mA	–10%		10%	
		I_O = 5 to 10 mA	–20%		20%	
I_O/I_{LIM}	OUTx to LIMx current ratio (I_O / I_{LIM})	V_I = 4.5 V to 40 V, 50 mA ≤ $I_{(LIMx)}$ ≤ 300 mA		198		
$I_{(LIMx)}$	Programmable current-limit accuracy(3)	V_I = 4.5 V to 40 V, 50 mA ≤ $I_{(LIMx)}$ ≤ 300 mA	–8%		8%	
$I_{L(LIMx)}$	Internal current-limit	LIMx shorted to GND	340		550	mA
I_{lkg}	SENSE, SENSE1, SENSE2, LIM, LIM1, and LIM2 leakage current	ENx = GND, T_A = 25°C			2	µA
$V_{(LIMx_th)}$	Current-limit threshold voltage	Voltage on the LIM, LIM1, and LIM2 pins when output current is limited		1.233		V
$V_{(SENSEx_stb)}$	Current-sense short-to-battery fault voltage	When short-to-battery or reverse current conditions are detected	3.05	3.2	3.3	V
$V_{(SENSEx_tsd)}$	Current-sense thermal shutdown fault voltage	When thermal shutdown is detected	2.7	2.85	3	V
$V_{(SENSEx_cl)}$	Current-sense current-limit fault voltage	When current-limit conditions are detected	2.4	2.55	2.65	V
$I_{(SENSEx_H)}$	Current-sense fault condition current	When short-to-battery, reverse current, thermal shutdown, or current-limit conditions are detected	3.3			mA
FAULT DETECTION						
$V_{(stb_th)}$	Short-to-battery threshold	$V_{(OUTx)}$ – V_I, checked during turnon sequence	–500	–55	110	mV
$I_{(REV)}$	Reverse current detection level	Power FET on (SW or LDO mode)	–100	–40	–1	mA
T_{SD}	Thermal shutdown	Junction temperature		175		°C
$T_{SD(hys)}$	Thermal shutdown hysteresis			15		°C
INTERFACE CIRCUITRY						
V_{OL}	$\overline{ERR}$ output low	$I_{(SINK)}$ = 5 mA			0.4	V
I_{lkg}	$\overline{ERR}$ open-drain leakage current	$\overline{ERR}$ high impedance, 5-V external voltage is applied at $\overline{ERR}$			1	µA
$R_{(OUTx\text{-}off)}$	OUT pulldown resistor(2)	ENx = GND		50		kΩ
$I_{R(lkg)}$	Reverse leakage current	–40 V < V_I < 0 V, reverse current to IN		0.6		mA
V_{CC}	Internal voltage regulator	V_I = 5.5 to 40 V, I_{CC} = 0 mA	4.25	4.5	4.75	V
$I_{CC(lim)}$	Internal voltage-regulator current-limit		15		70	mA

(3) The current-limit accuracy is maintained when the current limit is set between 50 mA and 300 mA, and it includes the deviation of the current-limit threshold voltage $V_{(LIMx_th)}$.

6.6 Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SENSE AND CURRENT-LIMIT						
$t_{d(SENSE_SEL_r)}$	Current-sense delay time from the rising edge of SENSE_SEL(1)	$V_{(ENx)}$ ≥ 2 V, $\overline{SENSE_EN}$ = GND, SENSE_SEL rise from 0 to 5 V		10		µs
$t_{d(SENSE_SEL_f)}$	Current-sense delay time from the falling edge of SENSE_SEL(1)	$V_{(ENx)}$ ≥ 2 V, $\overline{SENSE_EN}$ = GND, SENSE_SEL fall from 5 to 0 V		10		µs
$t_{d(SENSE_EN_r)}$	Current-sense delay time from rising edge of $\overline{SENSE_EN}$(1)	$V_{(ENx)}$ ≥ 2 V, $\overline{SENSE_EN}$ rise from 0 to 5 V		10		µs
$t_{d(SENSE_EN_f)}$	Current-sense delay time from falling edge of $\overline{SENSE_EN}$(1)	$V_{(ENx)}$ ≥ 2 V, $\overline{SENSE_EN}$ fall from 5 to 0 V		10		µs
FAULT DETECTION						
$t_{(PD_RC)}$	Reverse current (Short-to-BAT) shutdown deglitch time	Delay to shut down the switch or LDO after a drop over r_{on} becomes negative, $I_{(OUTx)}$ = –200 mA (typical), T_A = 25°C		5	20	µs
$t_{(BLK_RC)}$	Reverse current blanking time	Blanking time for reverse-current detection after power up, the rising edge of the ENx pin, or the current limiting event is over		16		ms

(1) Design information; specified by design; not production tested.

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6.7 Typical Characteristics

at V_I = 14 V (unless otherwise specified)

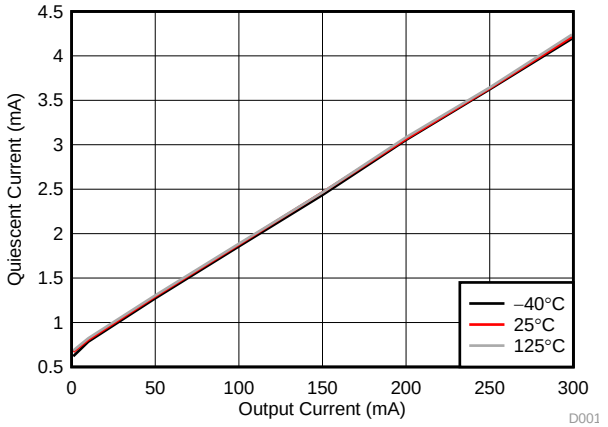


图 1. Quiescent Current vs Output Current (TPS7B7702-Q1)

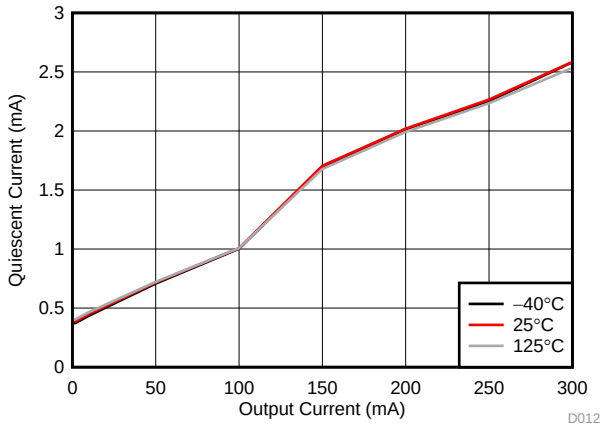


图 2. Quiescent Current vs Output Current (TPS7B7701-Q1)

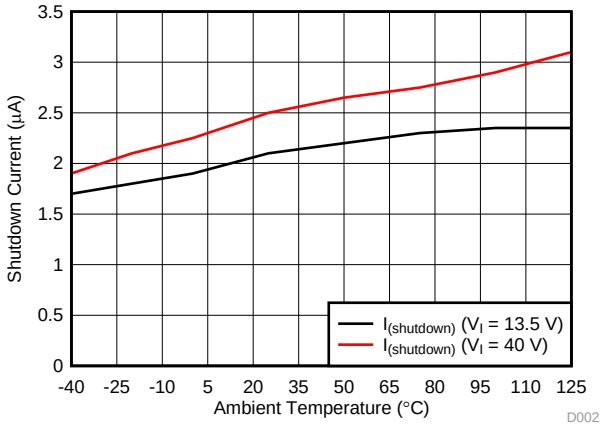
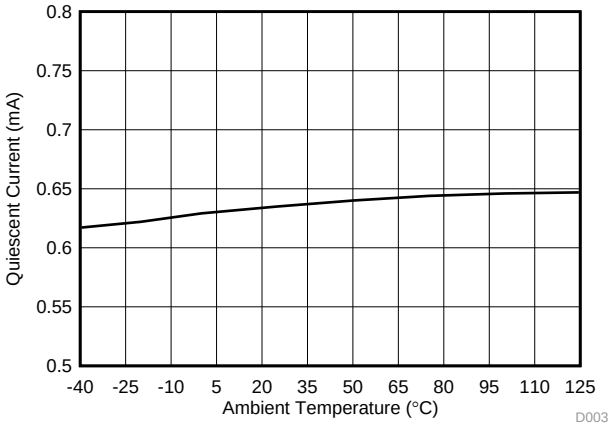
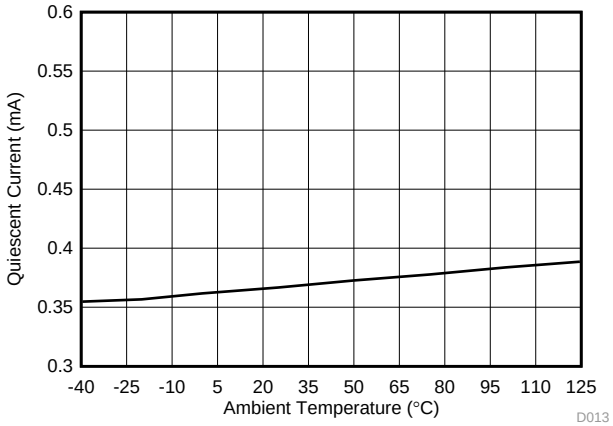


图 3. Shutdown Current vs Ambient Temperature (TPS7B7702-Q1)



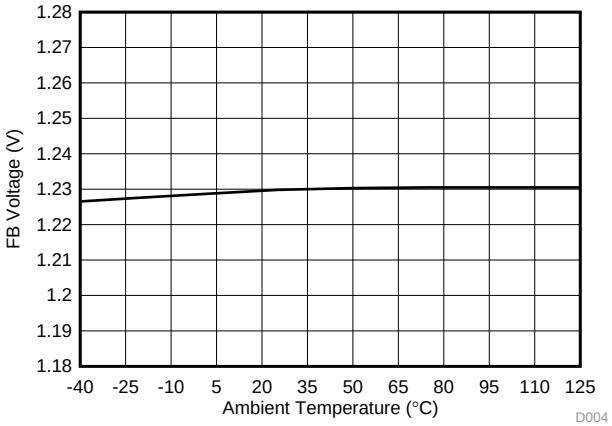
I_O = 0.1 mA

图 4. Quiescent Current vs Ambient Temperature (TPS7B7702-Q1)



I_O = 0.1 mA

图 5. Quiescent Current vs Ambient Temperature (TPS7B7701-Q1)



I_O = 10 mA

图 6. FB Voltage vs Ambient Temperature

Typical Characteristics (接下页)

at V_I = 14 V (unless otherwise specified)

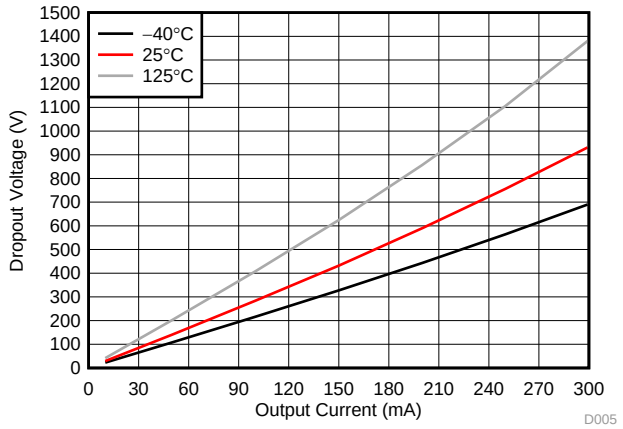
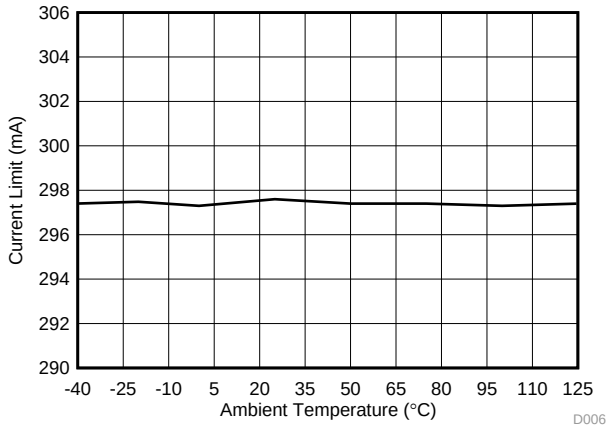
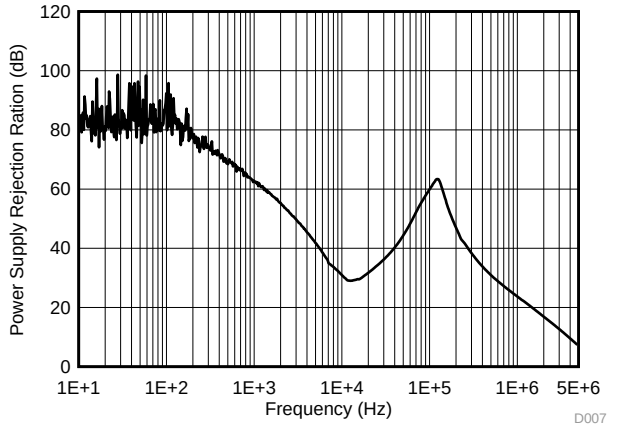


图 7. Dropout Voltage vs Output Current



I_{LIM} = 300 mA

图 8. Current Limit vs Ambient Temperature



C_O = 10 µF I_O = 10 mA

图 9. PSRR TPS7B770x-Q1

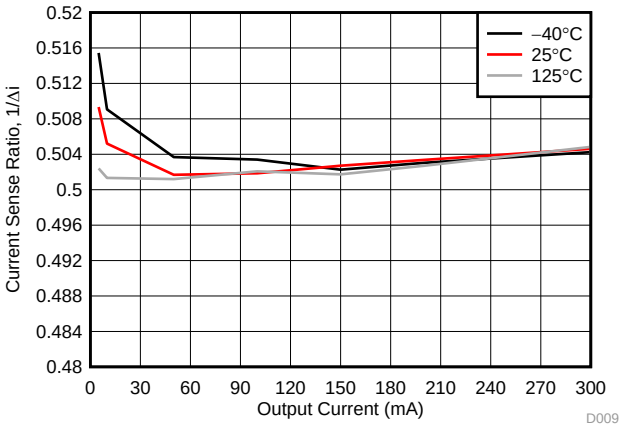


图 10. Current Sense Ratio vs Output Current, TPS7B7702-Q1 Channel 1

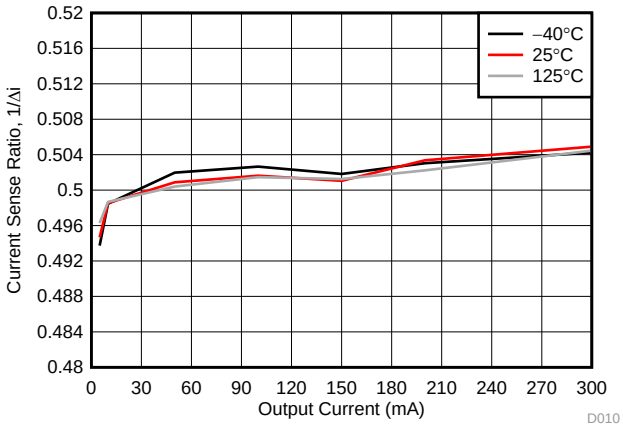
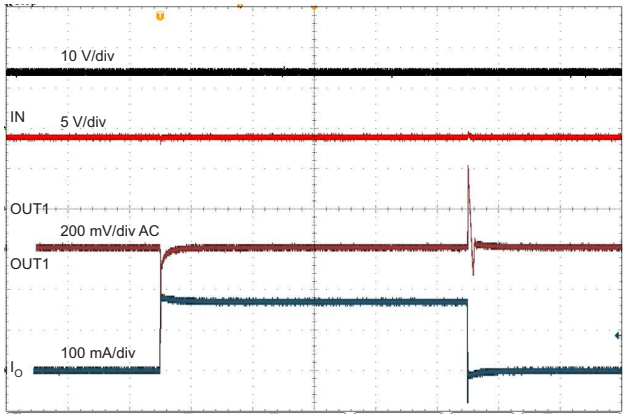


图 11. Current Sense Ratio vs Output Current, TPS7B7702-Q1 Channel 2



V_O = 8.5 V C_O = 10 µF I_O = 1 to 170 mA

图 12. 1-mA to 170-mA Load Transient

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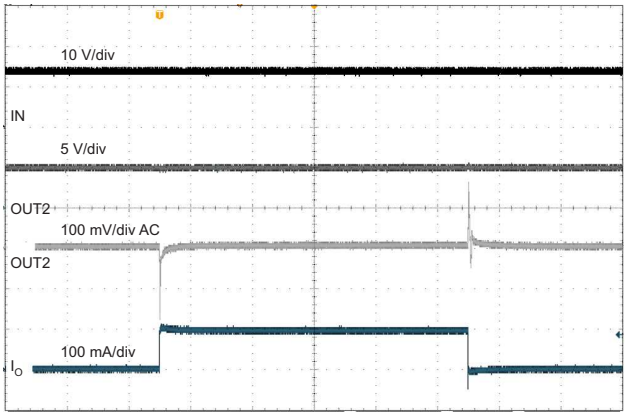
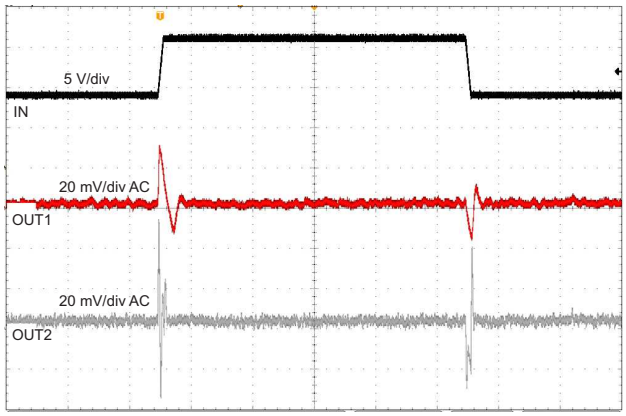
Typical Characteristics (接下页)

at V_I = 14 V (unless otherwise specified)



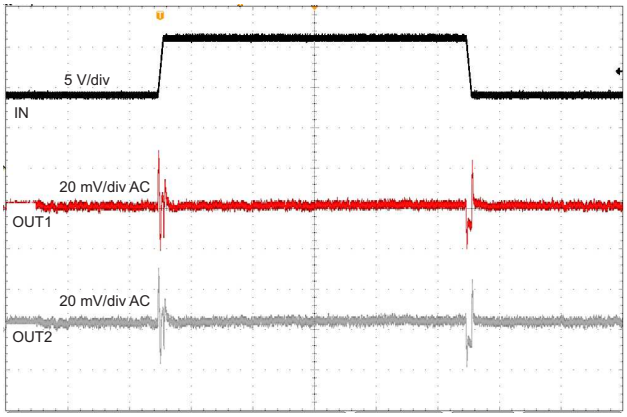
V_O = 5 V C_O = 10 µF I_O = 1 to 100 mA

图 13. 1-mA to 100-mA Load Transient



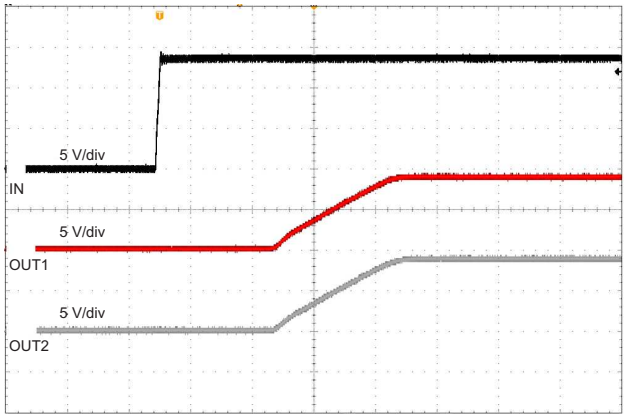
V_O = 8.5 V I_O = 50 mA

图 14. 9-V to 16-V Line Transient (1 V/µs)



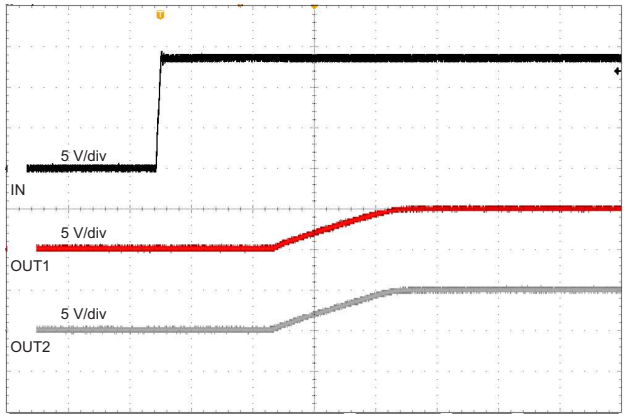
V_O = 5 V I_O = 50 mA

图 15. 9-V to 16-V Line Transient (1 V/µs)



V_O = 8.5 V I_O = 100 mA V_I = 0 to 14 V

图 16. Power Up (1 V/µs)



V_O = 5 V I_O = 100 mA V_I = 0 to 14 V

图 17. Power Up (1 V/µs)

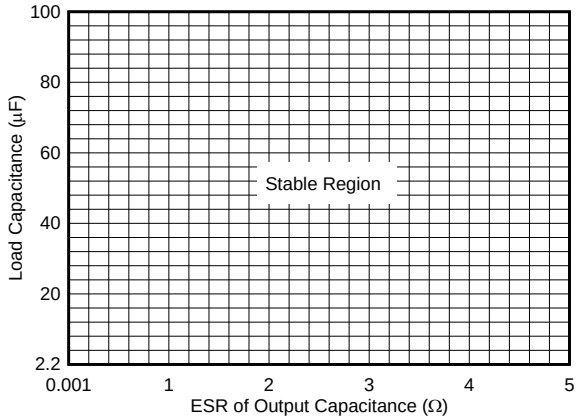


图 18. Load Capacitance vs ESR of Output Capacitance

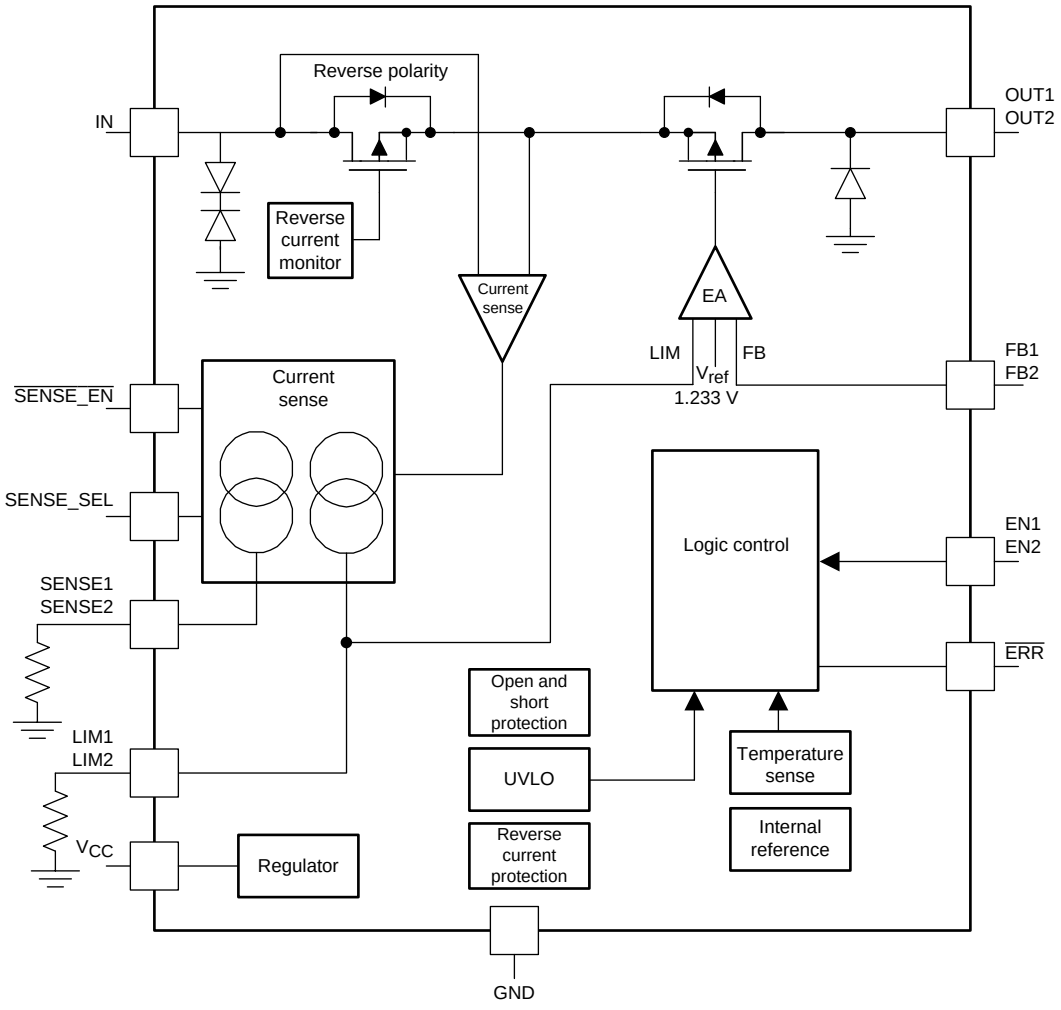
7 Detailed Description

7.1 Overview

The TPS7B770x-Q1 family of devices feature a single- or dual-channel, high voltage LDO with a current-sense function. These devices operate with a wide input-voltage range of 4.5 V to 40 V (45-V load dump protection). These devices also offers protection of antenna lines against electrostatic discharge (ESD) and from short-to-ground, short-to-battery, and thermal overstress. Device output voltage is adjustable from 1.5 V to 20 V through an external resistor divider. Alternatively, each channel can be configured as a switch.

These devices monitor the load. Accurate current sense allows for detection of open, normal, and short-circuit conditions without the need of further calibration. The current sense can also be multiplexed between channels and devices to save ADC resources. Each channel also provides an adjustable current limit with external resistor.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Fault Detection and Protection

The device includes both analog current sense and digital fault pins for full diagnostics of different fault conditions.

The current-sense voltage scale is selected based on the output-current range of interest. 图 19 shows a recommended setting that allows for full diagnostics of each fault. Before the device goes into current-limit mode, the output current-sense voltage is linearly proportional to the actual load current. During a thermal-shutdown (TSD) and short-to-battery (STB) condition, the current-sense voltage is set to the fault voltage level that is specified in the *Electrical Characteristics* table.

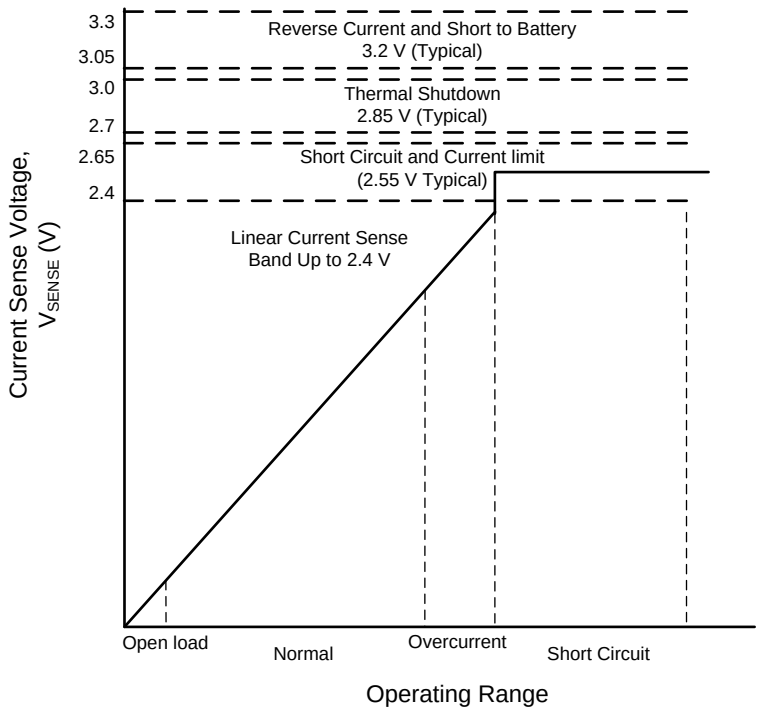

图 19. Functionality of the Current-Sense Output

7.3.2 Short-Circuit and Overcurrent Protection

The current limit on each channel is programmed by selecting the external resistor. The voltage on LIMx pin is compared with an internal voltage reference. When the threshold is exceeded, the current limit is triggered. The output of the current limited channel continues to remain on and the current is limited.

Under current-limit status, the $\overline{\text{ERR}}$ pin asserts low and the SENSE voltage of the fault channel is internally pulled up to a voltage rail between 2.4 V and 2.65 V as shown in 图 19. At this moment, the output voltage is not disabled. The microcontroller (MCU) should monitor the voltage at the SENSEx pin or $\overline{\text{ERR}}$ pin to disable the faulted channel by pulling the $\overline{\text{EN}}$x pin low. If a current-limit condition exists for a long period of time, thermal shutdown can be triggered and shutdown the output.

7.3.3 Short-to-Battery and Reverse Current Detection

Shorting the OUT pin to the battery because of a fault in the system is possible. Each channel detects this failure by comparing the voltage at the OUT and IN pins before the switch turns on. Each time the LDO switch is enabled on the rising edge of the EN pin or during the exiting of the thermal shutdown, the short-to-battery detection occurs. At this moment, if the device detects the short-to-battery fault, the LDO switch is latched off, the $\overline{\text{ERR}}$ pin is asserted low, and the fault-channel SENSE voltage is pulled up internally to a voltage rail between 3.05 V and 3.3 V. The device operates normally when the short-to-battery is removed and the EN pin is toggled.

Feature Description (接下页)

During normal operation if a short-to-battery fault results in reverse current for more than 5 µs (typical), the LDO switch is latched off and the $\overline{ERR}$ pin is asserted low. To remove the latched condition after a short-to-battery (reverse current) fault, the condition must first be removed and then the EN pin must be toggled.

Series inductance and the output capacitor can produce ringing during power up or recovery from current limit, resulting in an output voltage that temporarily exceeds the input voltage. The 16-ms (typical) reverse-current blanking can help filter this ringing.

For the dual-channel antenna LDO application, if both channels are enabled and one channel is shorted to ground after power up, the current drawn from the input capacitor can result in a temporary dip in the input voltage, which can trigger the reverse-current detection fault. To avoid this false trigger event, care must be taken when selecting the input capacitor; an increase of the input capacitor value is recommended.

7.3.4 Thermal Shutdown

The device incorporates a TSD circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output is turned off. When the junction temperature decreases by 15°C (typical) than the TSD trip point, the output is turned on again. The SENSE voltage is internally pulled up to a voltage rail between 2.7 V and 3 V during TSD status.

注

The purpose of the design of the internal protection circuitry of the TPS7B770x-Q1 family of devices is to protect against overload conditions and is not intended as a replacement for proper heat-sinking. Continuously running the device into thermal shutdown degrades device reliability.

7.3.5 Integrated Reverse-Polarity Protection

The device integrates a reverse-connected PMOS to block the reverse current during reverse polarity at the input and output short-to-battery condition. A special ESD structure at the input is specified to withstand –40 V.

7.3.6 Integrated Inductive Clamp

During output turnoff, the cable inductance continues to source the current from the output of the device. The device integrates an inductive clamp to help dissipate the inductive energy stored in the cable. An internal diode is connected between OUT and GND pins with a DC-current capability of 300 mA for inductive clamp protection.

7.3.7 Undervoltage Lockout

The device includes an undervoltage lockout (UVLO) threshold that is internally fixed. The undervoltage lockout activates when the input voltage on the IN pin drops below $V_{(UVLO)}$. The UVLO makes sure that the regulator is not latched into an unknown state during low input-supply voltage. If the input voltage has a negative transient that drops below the UVLO threshold and then recovers, the regulator shuts down and powers up with a normal power-up sequence when the input voltage is above the required levels.

表 1. Fault Table

FAILURE MODE	$V_{(SENSE)}$	$\overline{ERR}$	LDO SWITCH OUTPUT	LATCHED
Open load	$\frac{I_O \times R_{(SENSE)}}{198}$	HIGH	Enabled	No
Normal		HIGH	Enabled	No
Overcurrent		HIGH	Enabled	No
Short-circuit or current limit	2.4 to 2.65 V	LOW	Enabled	No
Thermal shutdown	2.7 to 3 V	LOW	Disabled	No
Output short-to-battery	3.05 to 3.3 V	LOW	Disabled	Yes
Reverse current	3.05 to 3.3 V	LOW	Disabled	Yes

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7.3.8 Enable (EN, EN1, and EN2)

The TPS7B7702-Q1 device features two active-high enable inputs, EN1 and EN2. The EN1 pin controls output voltage 1, OUT1, and the EN2 pin controls output voltage 2, OUT2. The devices consumes a maximum of shutdown current 5-µA when the ENx pins are low. Both the EN1 and EN2 pins have a maximum internal pulldown of 10 µA.

The TPS7B7701-Q1 device features one active-high enable input. The device consumes a maximum shutdown current of 5 µA when the EN pin is low. The EN pin has a maximum internal pull down of 10 µA.

7.3.9 Internal Voltage Regulator (V_{CC})

The device features an internal regulator that regulates the input voltage to 4.5 V to power all internal circuitry. Bypass a 1-µF ceramic capacitor from the V_{CC} pin to the GND pin for frequency compensation. The V_{CC} pin can be used as a power supply for external circuitry with up to 15-mA current capability.

7.3.10 Current Sense Multiplexing

The two, independent current sense pins (one for each channel) provide flexibility in the system design. When the ADC resource is limited, the device allows the multiplexing of the current sense pins by only using one current sense pin and one ADC to monitor all the antenna outputs.

The SENSE_SEL pin (TPS7B7702-Q1 only) selects the channels to monitor the current. The $\overline{\text{SENSE_EN}}$ pin enables and disables the SENSE pin, allowing multiplexing between chips. Therefore, only one ADC and one resistor is needed for current-sense diagnostics of multiple outputs. When the SENSE1 pin is connected to an ADC, the current flow through both channels can be sensed by changing the electrical level at the SENSE_SEL pin.

表 2 lists the selection logic for the current sense.

表 2. $\overline{\text{SENSE_EN}}$ and SEN_SEL Logic Table

$\overline{\text{SENSE_EN}}$	SEN_SEL	SENSE1 Status	SENSE2 Status
LOW	LOW	CH1 current	CH2 current
LOW	HIGH	CH2 current	HIGH impedance
HIGH	—	HIGH impedance	HIGH impedance

图 20 shows the application of four antenna channels sharing one ADC resource.

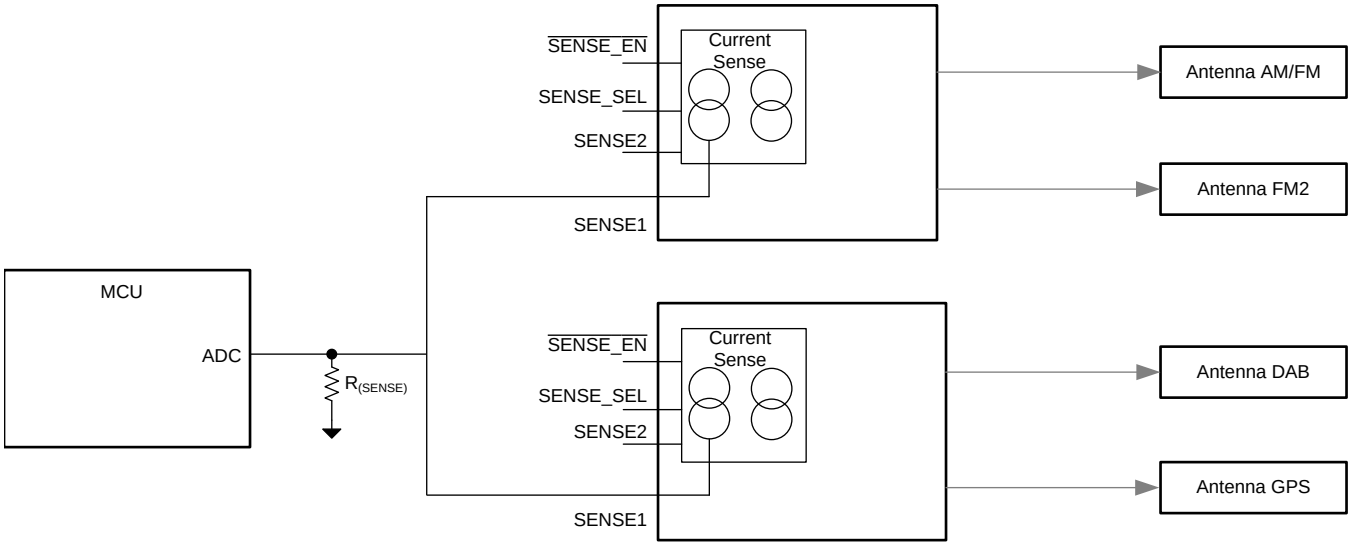

图 20. Current Multiplexing Application Block

7.3.11 Adjustable Output Voltage (FB, FB1, and FB2)

Using an external resistor divider selects an output voltage between 1.5 V and 20 V. Use 表 2 to calculate the output voltage (V_O). The recommended value for both R1 and R2 is less than 100 kΩ.

$$V_O = \frac{V_{(FB)} \times (R1 + R2)}{R2}$$

where

- $V_{(FB)}$ = 1.233 V (1)

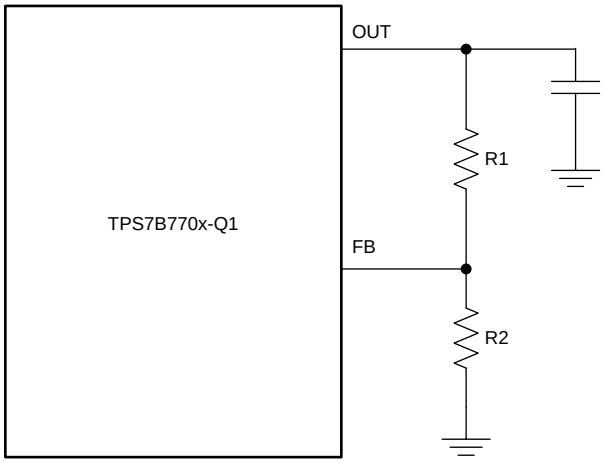

图 21. TPS7B770x-Q1 Output Voltage Setting Connection

The TPS7B770x-Q1 family of devices can also be used as a current-limited switch by connecting the FB pin to the GND pin.

7.4 Device Functional Modes

7.4.1 Operation With IN < 4.5 V

The maximum UVLO voltage is 4 V and the device operates at an input voltage above 4.5V. The device can also operate at lower input voltage. No minimum UVLO voltage is specified. At an input voltage below the actual UVLO voltage, the device does not operate.

7.4.2 Operation With EN Control

The threshold of EN rising edge is 2 V (maximum). With the EN pin held above that voltage and the input voltage above 4.5 V, the device becomes active. The EN falling edge is 0.7 V (minimum). Holding the EN pin below that voltage disables the device which therefore reduces the quiescent current of the device.

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8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7B770x-Q1 family of devices is a single- or dual-channel 300-mA LDO regulator with high, accurate current sense and a programmable current-limit function. Use the PSPICE transient model to evaluate the base function of the devices. Go to www.ti.com to download the PSPICE model and user's guide for the devices.

8.2 Typical Application

图 22 shows the typical application circuit for the TPS7B770x-Q1 family of devices. Different values of external components can be used depending on the end application. An application can require a larger output capacitor during fast load steps to prevent large drops on output voltage. TI recommends a low-ESR ceramic capacitor with a dielectric of type X5R or X7R.

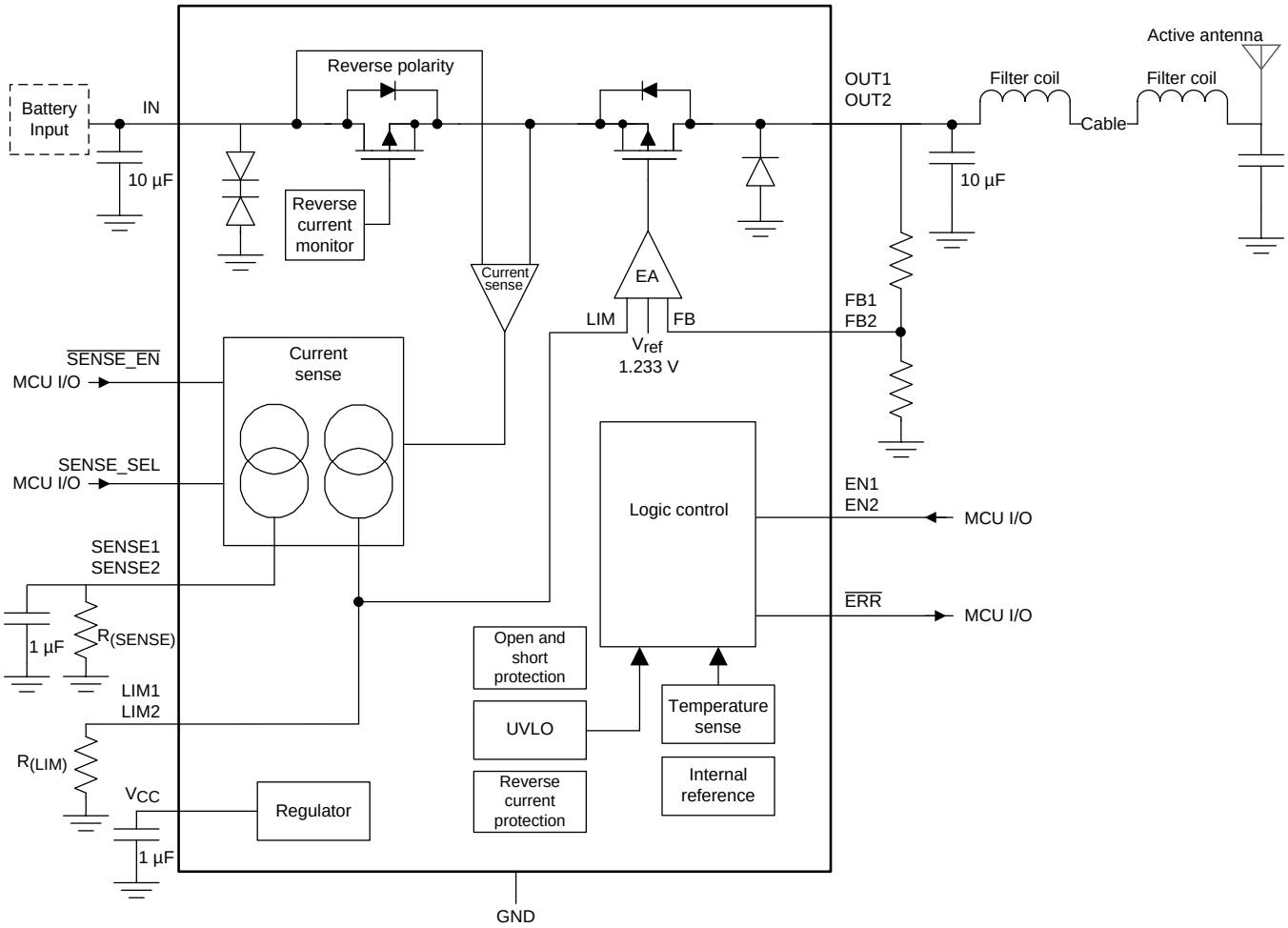

图 22. TPS7B770x-Q1 Typical Application

Typical Application (接下页)

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 3 as the design parameters.

表 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	4.5 to 40 V
Output voltage	1.5 to 20 V
Output capacitor range	2.2 to 100 µF
Output Capacitor ESR range	0.001 to 5 Ω
SENSE resistor	See the *Current Sense Resistor Selection* section
Programmable current limit	50 to 300 mA

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage
- Output voltage
- Output current
- Current limit
- ADC voltage rating

8.2.2.1 Input Capacitor

The device requires an input decoupling capacitor, the value of which depends on the application. The typical recommended value for the decoupling capacitor is 10 µF. The voltage rating must be greater than the maximum input voltage.

8.2.2.2 Output Capacitor

The device requires an output capacitor to stabilize the output voltage. The capacitor value should be between 2.2 µF and 100 µF. The ESR range should be between 1 mΩ and 5 Ω. TI recommends selecting a ceramic capacitor with low ESR to improve the load transient response.

8.2.2.3 Current Sense Resistor Selection

The current-sense outputs, SENSEx (SENSE, SENSE1, and SENSE2), are proportional to the output current at the OUT, OUT1, and OUT2 pins with a factor of 1/198. An output resistor, $R_{(SENSE)}$, must be connected between the SENSEx pin and ground to generate a current sense voltage to be sampled by ADC. Use 公式 2 to calculate the voltage at SENSEx pin ($V_{(SENSEx)}$).

$$V_{(SENSEx)} = I_{(SENSEx)} \times R_{(SENSEx)}$$

where

- $$I_{(SENSEx)} = \frac{I_{(OUTx)}}{198} \quad (2)$$

For this example, select 1.5 kΩ as a value for $R_{(SENSEx)}$. Do not consider the resistor and current-sense accuracy.

For a load current of 198 mA, use 公式 3 to calculate the value of $V_{(SENSEx)}$.

$$I_{(SENSEx)} = \frac{198\text{ mA}}{198} = 1\text{ mA} \rightarrow V_{(SENSEx)} = 1\text{ mA} \times 1.5\text{ k}\Omega = 1.5\text{ V} \quad (3)$$

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To avoid any overlap between normal operation and current-limit or short-to-ground phase, using 公式 4 to select the value of the SENSE resistor is recommended.

$$R_{(SENSEx)} \le \frac{198 \times 2.4\ V}{I_{Omax}}$$

where

- 198 is the output current to current-sense ratio
- 2.4 V is the minimum possible voltage at the SENSEx pin under a short-circuit fault case
- I_{Omax} is the maximum possible output current under normal operation (4)

To stabilize the current-sense loop, connecting a 1-µF ceramic capacitor at the SENSE, SENSE1, or SENSE2 pin is required. 表 4 lists the current sense accuracy across temperature.

表 4. Current Sense Accuracy

OUTPUT CURRENT	CURRENT SENSE ACCURACY
5 mA to 10 mA	20%
10 mA to 50 mA	10%
50 mA to 100 mA	5%
100 mA to 300 mA	3%

8.2.2.4 Current-Limit Resistor Selection

The current at the LIMx pins (LIM, LIM1, and LIM2) is proportional to the load current at the OUTx (OUT, OUT1, and OUT2) pins and is internally connected to a current-limit comparator referenced to 1.233 V. The current limit is programmable through the external resistor connected at LIMx pin. Use 公式 5 to calculate the value of the external resistor, $R_{(LIMx)}$. The programmable current limit accuracy is 8% maximum across all conditions. The internal current limit of the device is set by shorting the LIM pin to ground. Because the current limit varies by 8%, 公式 6 shows how to calculate the minimum current limit value, and 公式 7 shows how to calculate the maximum current limit value.

$$R_{(LIMx)} = \frac{1.233\ V}{I_{(LIMx)}} \times 198$$

where

- $$I_{(LIMx)(typ)} = \frac{1.233\ V}{R_{(LIMx)}} \times 198 \quad (5)$$

$$I_{(LIMx)(min)} = I_{(LIMx)(typ)} \times 0.92 = (0.92)\left(\frac{1.233\ V}{R_{(LIMx)}} \times 198\right) \quad (6)$$

$$I_{(LIMx)(max)} = I_{(LIMx)(typ)} \times 1.08 = (1.08)\left(\frac{1.233\ V}{R_{(LIMx)}} \times 198\right) \quad (7)$$

Select a maximum current-limit value of 200 mA and use 公式 8 to calculate the value of $R_{(LIMx)}$.

$$R_{(LIMx)} = \frac{1.08 \times 198 \times 1.233\ V}{I_{(LIMx)(max)}} \quad (8)$$

Using 公式 8 yields a R_{LIMx} value of 1.318 kΩ. The closest 1% resistor that can be selected is 1.33 kΩ. Now using 公式 7 and plugging in 1.33 kΩ for R_{LIMx} yields a maximum current of 198.2 mA. Keep in mind this result does not include resistor tolerance in the calculation. To make sure that the current does not exceed the set amount, resistor tolerance must also be included in the equation.

8.2.3 Application Curves

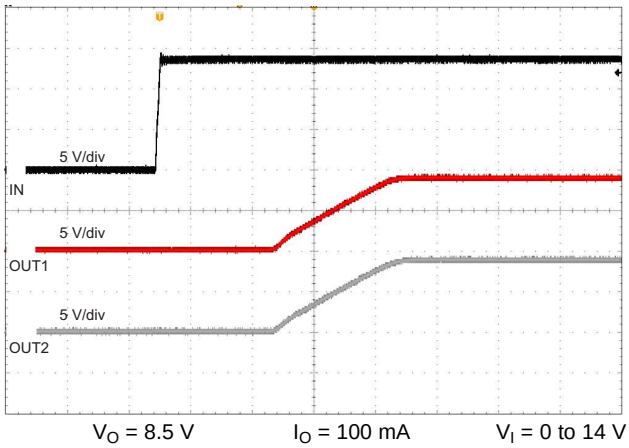

图 23. Power Up (1 V/µs)

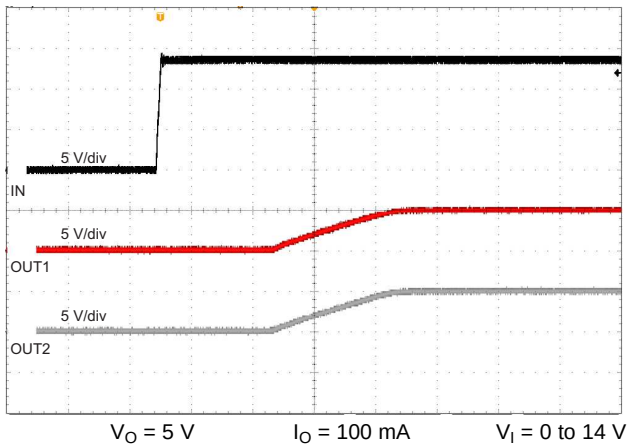

图 24. Power Up (1 V/µs)

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply with a range between 4.5 V and 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B770x-Q1 device, TI recommends adding an 10-µF electrolytic capacitor and a ceramic bypass capacitor at the input.

10 Layout

10.1 Layout Guidelines

For the layout of TPS7B770x-Q1 device, place the input and output capacitors close to the device as shown in 图 25. To enhance the thermal performance, TI recommends surrounding the device with some vias.

Minimize equivalent-series inductance (ESL) and ESR to maximize performance and provide stability. Place every capacitor as close as possible to the device and on the same side of the PCB as the regulator.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. TI strongly discourages the use long traces because they can negatively impact system performance and cause instability.

If possible, and to maintain the maximum performance specified in this device data sheet, use the same layout pattern used for the TPS7B770x-Q1 evaluation board, available online at www.ti.com/tool/TPS7B7702EVM.

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10.2 Layout Example

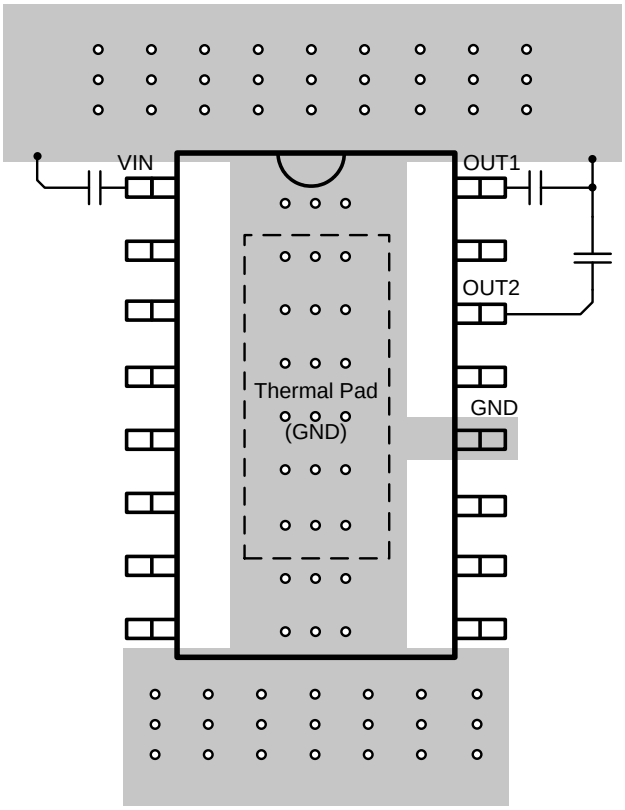

图 25. TPS7B770x-Q1 Layout Example

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

《TPS7B7702-Q1 评估模块用户指南》

11.2 相关链接

表 5 列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 **5.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持和社区
TPS7B7701-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS7B7702-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.5 商标

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7B7701QPWPRQ1	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	7B7701	Samples
TPS7B7702QPWPRQ1	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	7B7702	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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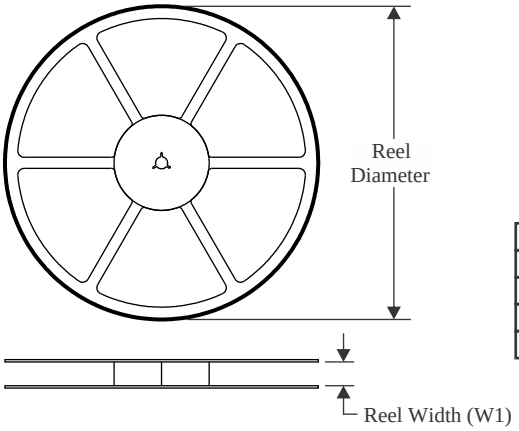
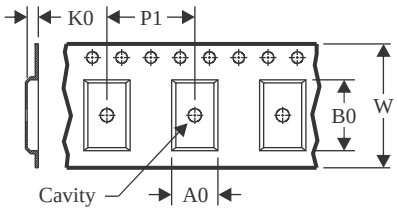
TAPE AND REEL INFORMATION

REEL DIMENSIONS

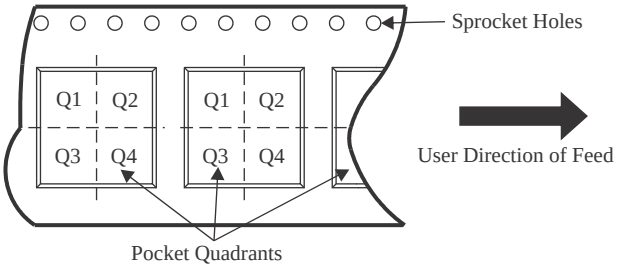


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

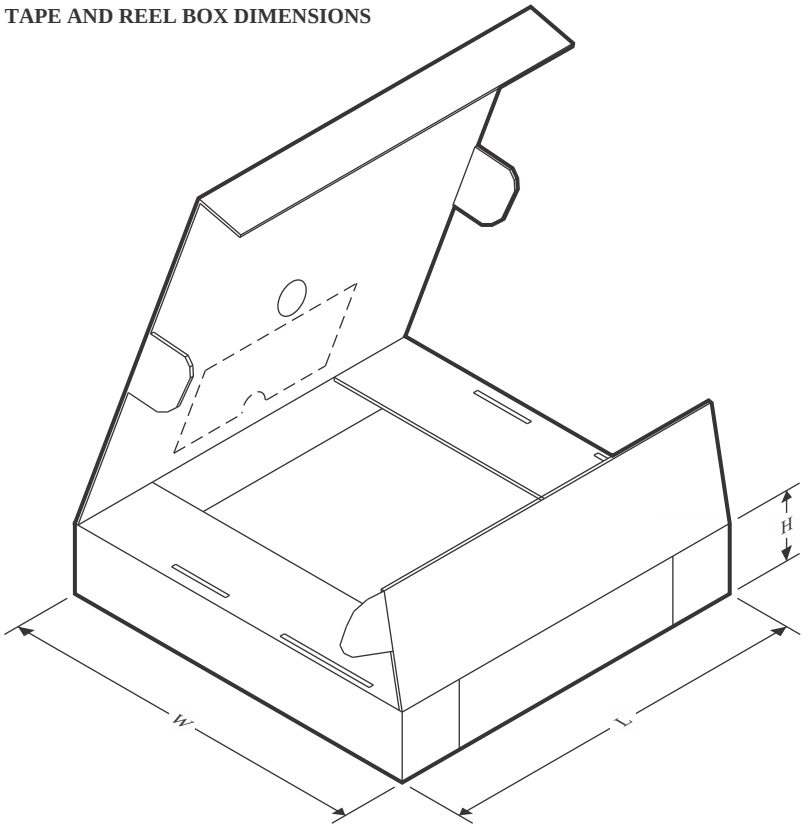
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B7701QPWPRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS7B7702QPWPRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

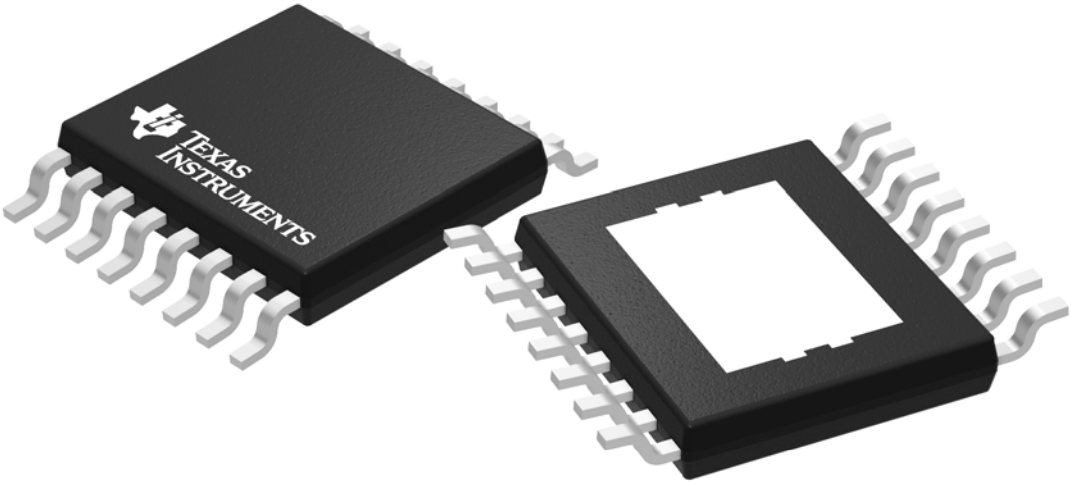


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B7701QPWPRQ1	HTSSOP	PWP	16	2000	350.0	350.0	43.0
TPS7B7702QPWPRQ1	HTSSOP	PWP	16	2000	350.0	350.0	43.0

PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4073225-3/J

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