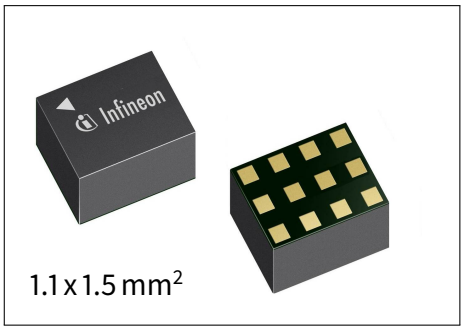
BGM14HBA12

SP4T Low Noise Amplifier Multiplexer Module with Bypass

Features

- Wideband operating frequencies: 1800 - 2700 MHz
- Insertion power gain: 18 dB
- Insertion loss in bypass mode: 4 dB
- Noise figure: 0.8 dB
- Low current consumption: 5 mA
- Multi-state control: OFF- and Multi Gain Modes
- Small ATSLP leadless package



Possible Application

The LTE data rate can be significantly improved by using the LNA Multiplexer Module (LMM). The integrated bypass function increases the overall system dynamic range and leads to more flexibility in the front-end. The LMM offers best Noise Figure to ensure high data rates even on the LTE cell edge. Closer to the basestation the bypass mode can be activated reducing current consumption. Thanks to the MIPI control interface, control lines are reduced to a minimum. Up to four 3GPP LTE bands in the mid- and high-band can be controlled and dynamically amplified with this LMM. This reduces PCB area and system cost.

Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Block diagram

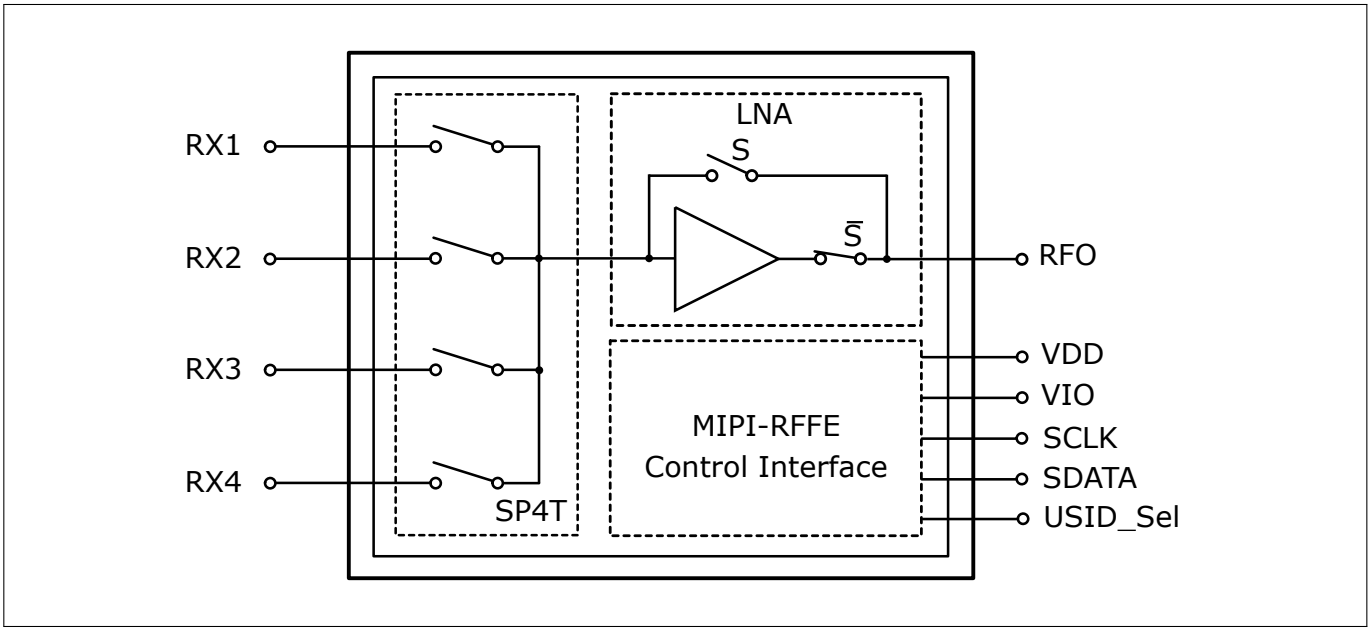
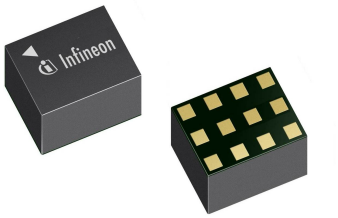


Table of Contents

1 Features



- Power gain: 18 dB
- Low noise figure: 0.8 dB
- Low current consumption: 5 mA
- Wideband frequency range from 1800 to 2700 MHz
- Tunable output tank
- RF output internally matched to 50 Ω
- High port-to-port-isolation: 25 dB
- Suitable for LTE / LTE-Advanced and 3G applications
- No decoupling capacitors required if no DC applied on RF lines
- On chip control logic including ESD protection
- Supply voltage: 1.65 to 3.3 V
- Integrated MIPI RFFE 2.0 interface operating in 1.65 to 1.95 V voltage range
- Software programmable MIPI RFFE USID
- USID select pin
- Small form factor 1.1 mm x 1.5 mm
- High EMI robustness
- RoHS and WEEE compliant package

RoHS Halogen-Free Lead-Free Green

Description

The BGM14HBA12 is a LNA multiplexer module for LTE Mid- and High-band frequencies that increases the data rate while keeping flexibility and low footprint. It is a perfect solution for multimode handsets for 3G, 4G and Carrier Aggregation. The device configuration is shown in Fig. 1.

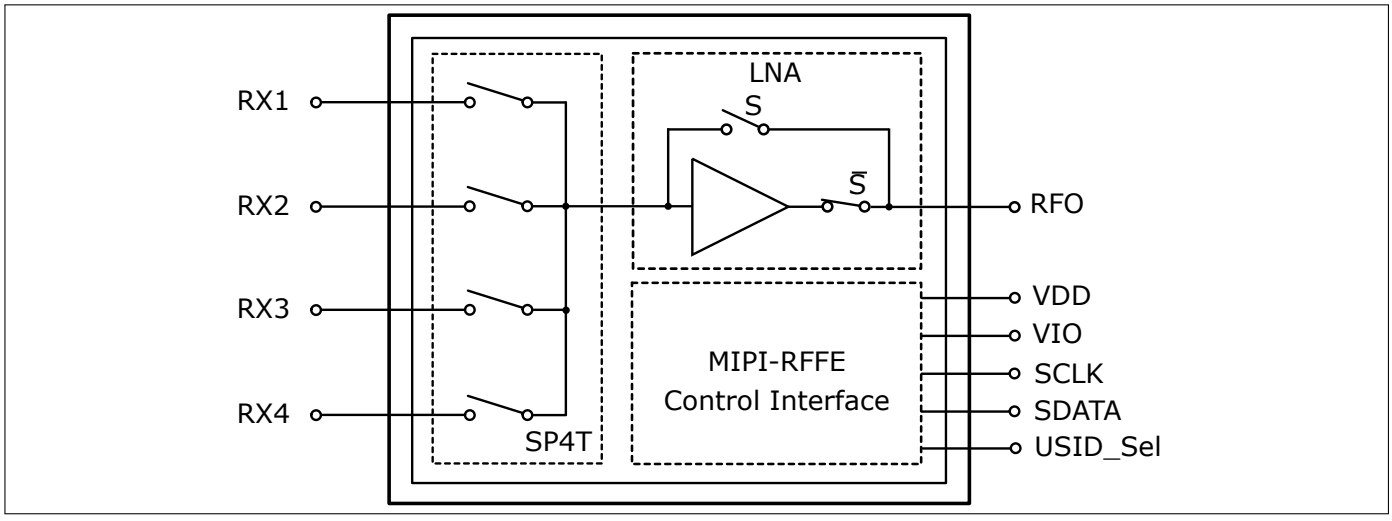


Figure 1: BGM14HBA12 Block diagram

Product Name	Marking	Package
BGM14HBA12	14	PG-ATSLP-12

2 Maximum Ratings

Table 1: Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Voltage VDD [1]	V_{DD}	0.3	–	3.6	V	–
Voltage at RF pins Rx [2]	V_{Rx}	0	–	0	V	–
Voltage at RF output pin RFO	V_{RFO}	0	–	0	V	–
Voltage at GND pins	V_{GND}	0	–	0	V	–
Current into pin VDD	I_{DD}	–	–	16	mA	–
RF input power	P_{IN}	–	–	25	dBm	–
Total power dissipation	P_{tot}	–	–	60	mW	–
Junction temperature	T_J	–	–	150	°C	–
Ambient temperature range	T_A	-40	–	85	°C	–
Storage temperature range	T_{STG}	-55	–	150	°C	–
ESD capability, CDM [3]	V_{ESD_CDM}	-1000	–	1000	V	–
ESD capability, HBM [4]	V_{ESD_HBM}	-2000	–	+2000	V	–
RFFE Supply Voltage	V_{IO}	-0.5	–	2.2	V	–
RFFE Supply Voltage Levels	V_{SCLK}, V_{SDATA}, V_{USID_SEL}	-0.7	–	V_{IO}+0.7 (max. 2.2)	V	–

[1] All voltages refer to GND-Nodes unless otherwise noted
[2] The DC voltage at Rx ports has to be 0V
[3] Field-Induced Charged-Device Model JS-002-2014. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.
[4] Human Body Model ANSI/ESDA/JEDEC JS-001-2014 (R=1.5 kΩ, C=100 pF)

Warning: Stresses above the max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.

3 DC Characteristics

Table 2: DC Characteristics at T_A = 25 °C

Parameter [1]	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Voltage	V_{DD}	1.65	1.8	3.3	V	–
Supply Current	I_{DD}	2.5 (Bias0)	5 (Bias2)	11 (Bias7)	mA	ON Mode, LNA active
		45	50	65	µA	Bypass Mode
		0.1	0.4	1.0	µA	OFF Mode
RFFE supply voltage	V_{IO}	1.65	1.8	1.95	V	–
RFFE input high voltage[2]	V_{IH}	0.7*V_{IO}	–	V_{IO}	V	–
RFFE input low voltage[2]	V_{IL}	0	–	0.3*V_{IO}	V	–
RFFE output high voltage[2]	V_{OH}	0.8*V_{IO}	–	V_{IO}	V	–
RFFE output low voltage[2]	V_{OL}	0	–	0.2*V_{IO}	V	–
RFFE control input capacitance	C_{Ctrl}	–	–	2	pF	–
RFFE supply current	I_{VIO}	–	3	–	µA	Idle State

[1] Based on the application described in Chapter 6
[2] SCLK, SDATA and USID_Sel

4 RF Characteristics

Table 3: RF Characteristics in High Gain Mode at T_A = 25 °C, f = Subband Center Frequency

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion power gain	$\|S_{21}\|^2$	17.0	18.0	19.0	dB	V_{DD} = 1.8 V LNA High Gain Mode Bias 2 (5 mA) Reg0x01: 1000 0010 (see Tab. 13)
Noise figure	*NF*	0.6[1] 0.7[2]	0.8[1] 1.0[2]	1.0[1] 1.3[2]	dB	
Inband input 3rd-order intercept point	*IB_IIP3*	-8[3] -5[4]	-6.5[3] -4.5[4]	-5[3] -4[4]	dBm	
Inband input 1dB compression point	IP_{1dB}	-16	-15	-14	dBm	

Table 4: RF Characteristics in Low Gain Mode at T_A = 25 °C, f = Subband Center Frequency

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion power gain	$\|S_{21}\|^2$	15.0	16.0	17.0	dB	V_{DD} = 1.8 V LNA Low Gain Mode Bias 2 (5 mA) Reg0x01: 1001 0010 (see Tab. 13)
Noise figure	*NF*	0.7[1] 0.8[2]	0.9[1] 1.1[2]	1.1[1] 1.3[2]	dB	
Inband input 3rd-order intercept point	*IB_IIP3*	-5[3] -4[4]	-3.5[3] -2.5[4]	-3[3] -2[4]	dBm	
Inband input 1dB compression point	IP_{1dB}	-14	-13	-12	dBm	

Table 5: RF Characteristics in Bypass Mode at T_A = 25 °C, f = Subband Center Frequency

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion power gain	$\|S_{21}\|^2$	-5.0	-4.0	-3.0	dB	LNA Bypass Mode Bias x (60 µA) Reg0x01: 1100 0xxx (see Tab. 13)
Noise figure	*NF*	4.0[1] 4.5[2]	4.5[1] 5.5[2]	6.5[1] 7.0[2]	dB	
Inband input 3rd-order intercept point	*IB_IIP3*	17[3] 17[4]	21[3] 21[4]	23[3] 23[4]	dBm	

[1] Subbands 1 and 2 (see Table 14)
[2] Subbands 3 and 4 (see Table 14)
[3] Input power = −30 dBm for HG and LG, −15 dBm for Bypass, 1 MHz tone distance
[4] Input power = −30 dBm for HG and LG, −15 dBm for Bypass, 10 MHz tone distance

Table 6: Common RF Characteristics at T_A = 25 °C, f = Subband Center Frequency

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input return loss	RL_{in}	9	10	11	dB	Common for all LNA Modes
Output return loss	RL_{out}	16	18	21	dB	
Reverse isolation RFO to RX port	$1/\lvert S_{12}\rvert^2$	37	38	39	dB	
Isolation RX to RX port	ISO	20	35	54	dB	
Isolation RX to RFO port	ISO	18	27	32	dB	
Stability	k	>1	–	–		f=140 MHz–3.25 GHz
Power Up Settling Time	T_{PUP}	–	10	20	µs	See Fig. 2
Turn On Time Band Select Switch		1.3	1.4	1.5	µs	Time between end of MIPI write enabling the switch and the selected path in through position
Band Select Switching Time		0.7	1.0	1.5	µs	Time to change between switch states when active
LNA Enable/Disable Time		1.8	2.3	3.5	µs	Time required after RFFE register write to LNA is enabled/disabled
LNA Gain Switching Time		1.8	2.3	3.5	µs	Time required after RFFE register write changing LNA gain state (and bias if applicable) between any two gain states to LNA gain and phase settled

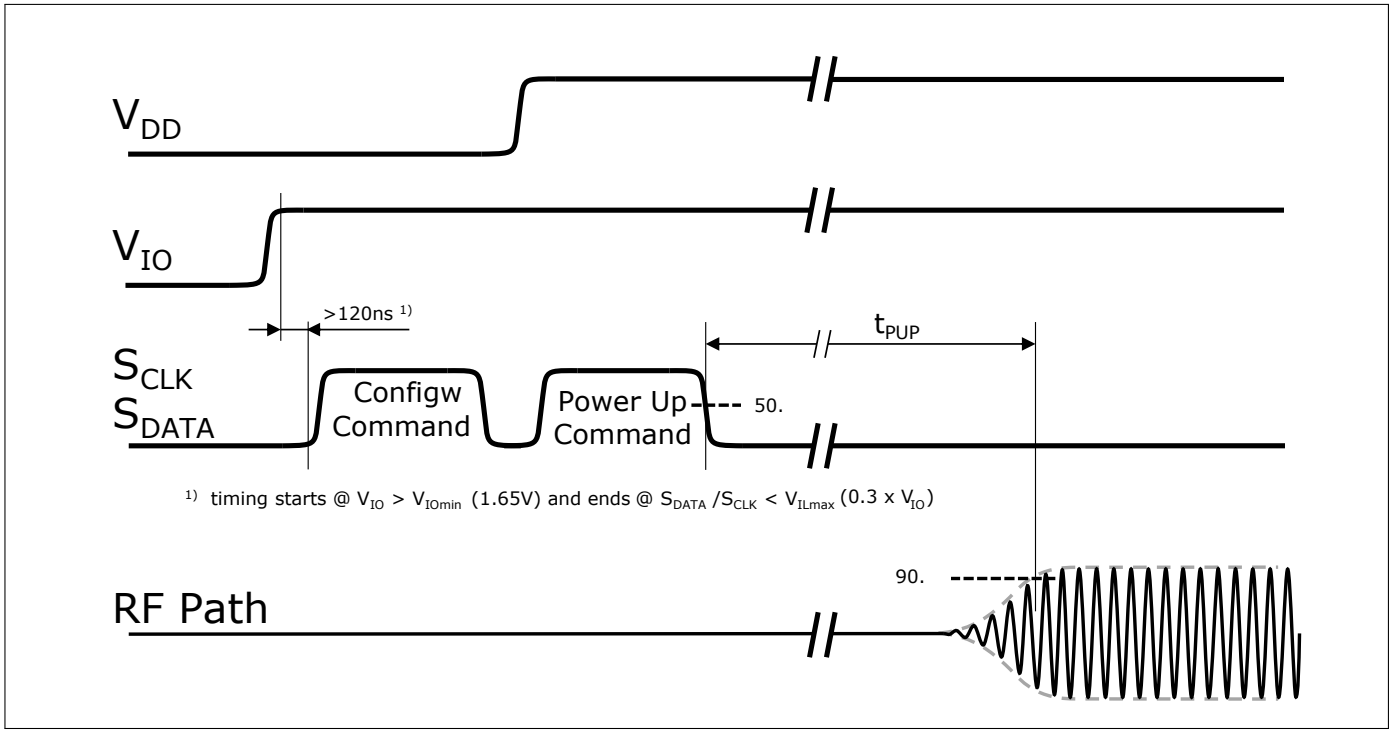


Figure 2: Power Up Settling Time

5 MIPI RFFE Specification

All sequences are implemented according to the 'MIPI Alliance Specification for RF Front-End Control Interface' document version 2.0 - 25. September 2014.

Table 7: MIPI Features

Feature	Supported	Comment
MIPI RFFE 2.0 standard	Yes	
Register 0 write command sequence	Yes	
Register read and write command sequence	Yes	
Extended register read and write command sequence	Yes	
Support for standard frequency range operations for SCLK	Yes	Up to 26 MHz for read and write
Support for extended frequency range operations for SCLK	Yes	Up to 52 MHz for write
Half speed read	Yes	
Full speed read	Yes	
Full speed write	Yes	
Programmable Group SID	Yes	
Programmable USID	Yes	Support for three registers write and extended write sequences
Trigger functionality	Yes	
Broadcast / GSID write to PM TRIG register	Yes	
Reset	Yes	Via VIO, PM TRIG or software register
Status / error sum register	Yes	
Extended product ID register	Yes	
Revision ID register	Yes	
Group SID register	Yes	
USID_Sel pin	Yes	See Tab. 11
USID selection via SDATA / SCLK swap feature	No	–

Table 8: Startup Behavior

Feature	State	Comment
Power status	Low power	Lower power mode after start-up
Trigger function	Enabled	Enabled after start-up. Programmable via behavior control register

Table 9: Register Mapping, Table I

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x00	REGISTER_0	7:0	MODE_CTRL	Switch control	00000000	No	Trigger1	R/W
0x01	REGISTER_1	7:0	MODE_CTRL	Switch control	00000000	No	Trigger2	R/W
0x1C	PM_TRIG	7	PWR_MODE(1), Operation Mode	0: Normal operation (ACTIVE)	1	Yes	No	R/W
				1: Low Power Mode (LOW POWER)				
		6	PWR_MODE(0), State Bit Vector	0: No action (ACTIVE)	0			
				1: Powered Reset (STARTUP to ACTIVE to LOW POWER)				
		5	TRIGGER_MASK_2	0: Data masked (held in shadow REG)	0	No		
				1: Data not masked (ready for transfer to active REG)				
		4	TRIGGER_MASK_1	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		3	TRIGGER_MASK_0	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		2	TRIGGER_2	0: No action (data held in shadow REG)	0	Yes		
				1: Data transferred to active REG				
		1	TRIGGER_1	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		0	TRIGGER_0	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
0x1D	PRODUCT_ID	7:0	PRODUCT_ID	This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	1110101	No	No	R
0x1E	MAN_ID	7:0	MANUFACTURER_ID [7:0]	This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value.	00011010	No	No	R
0x1F	MAN_USID	7:6	RESERVED	Reserved for future use	00	No	No	R
		5:4	MANUFACTURER_ID [9:8]	These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value.	01			
		3:0	USID[3:0]	Programmable USID. Performing a write to this register using the described programming sequences will program the USID in devices supporting this feature. These bits store the USID of the device.	See Tab. 11	No	No	R/W

Table 10: Register Mapping, Table II

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x20	EXT_PRODUCT_ID	7:0	EXT_PRODUCT_ID		00000000	No	No	R
0x21	REV_ID	7:4	MAIN_REVISION		0001	No	No	R/W
		3:0	SUB_REVISION		0000			
0x22	GSID	7:4	GSID0[3:0]	Primary Group Slave ID.	0000	No	No	R/W
		3:0	RESERVED	Reserved for secondary Group Slave ID.	0000			
0x23	UDR_RST	7	UDR_RST	Reset all configurable non-RFFE Reserved registers to default values. 0: Normal operation 1: Software reset	0	No	No	R/W
		6:0	RESERVED	Reserved for future use	0000000			
0x24	ERR_SUM	7	RESERVED	Reserved for future use	0	No	No	R
		6	COMMAND_FRAME_PARITY_ERR	Command Sequence received with parity error — discard command.	0			
		5	COMMAND_LENGTH_ERR	Command length error.	0			
		4	ADDRESS_FRAME_PARITY_ERR	Address frame with parity error.	0			
		3	DATA_FRAME_PARITY_ERR	Data frame with parity error.	0			
		2	READ_UNUSED_REG	Read command to an invalid address.	0			
		1	WRITE_UNUSED_REG	Write command to an invalid address.	0			
		0	BID_GID_ERR	Read command with a BROADCAST_ID or GROUP_ID.	0			

Table 11: USID Selection

USID Pin	USID Value
0	0011
1	0100

Table 12: Modes of Operation (Truth Table, Register_0)

		REGISTER_0 Bits							
		Reserved	Reserved	Reserved	Input Select				
State	Mode	B7	B6	B5	B4	B3	B2	B1	B0
1	Isolation	x	x	x	x	0	0	0	0
2	RX1-RFO	x	x	x	x	0	0	0	1
3	RX2-RFO	x	x	x	x	0	0	1	0
4	RX3-RFO	x	x	x	x	0	1	0	0
5	RX4-RFO	x	x	x	x	1	0	0	0

Table 13: Modes of Operation (Truth Table, Register_1)

		REGISTER_1 Bits							
		LNA Enable	LNA Bypass Mode	LNA High Gain Mode	LNA Attenuator Mode		LNA Bias States		
State	Mode	B7	B6	B5	B4	B3	B2	B1	B0
1	LNA Disabled	0	x	x	x	x	x	x	x
2	LNA Enabled	1	x	x	x	x	x	x	x
3	LNA High Gain	1	0	0	x	x	x	x	x
4	LNA Low Gain	1	0	1	x	x	x	x	x
5	LNA Bypass	1	1	0	x	x	x	x	x
6	LNA 0dB Atten.	1	x	x	0	0	x	x	x
7	LNA 3dB Atten.	1	x	x	0	1	x	x	x
8	LNA 5dB Atten.	1	x	x	1	0	x	x	x
9	LNA Bias0, 3mA	1	x	x	x	x	0	0	0
10	LNA Bias1, 4mA	1	x	x	x	x	0	0	1
11	LNA Bias2, 5mA	1	x	x	x	x	0	1	0
12	LNA Bias3, 6mA	1	x	x	x	x	0	1	1
13	LNA Bias4, 7mA	1	x	x	x	x	1	0	0
14	LNA Bias5, 8mA	1	x	x	x	x	1	0	1
15	LNA Bias6, 9mA	1	x	x	x	x	1	1	0
16	LNA Bias7, 10mA	1	x	x	x	x	1	1	1

Table 14: Band Tuning (Truth Table, Register_3)

This register has to be programmed only once after power up!			REGISTER_3 Bits							
			Band Tuning Select							
State	Mode	Subband	B7	B6	B5	B4	B3	B2	B1	B0
1	RX1 Tuning	1: 1800 - 2025 MHz	x	x	x	x	x	x	0	0
2		2: 2025 - 2250 MHz	x	x	x	x	x	x	0	1
3		3: 2250 - 2475 MHz	x	x	x	x	x	x	1	0
4		4: 2475 - 2700 MHz	x	x	x	x	x	x	1	1
5	RX2 Tuning	1: 1800 - 2025 MHz	x	x	x	x	0	0	x	x
6		2: 2025 - 2250 MHz	x	x	x	x	0	1	x	x
7		3: 2250 - 2475 MHz	x	x	x	x	1	0	x	x
8		4: 2475 - 2700 MHz	x	x	x	x	1	1	x	x
9	RX3 Tuning	1: 1800 - 2025 MHz	x	x	0	0	x	x	x	x
10		2: 2025 - 2250 MHz	x	x	0	1	x	x	x	x
11		3: 2250 - 2475 MHz	x	x	1	0	x	x	x	x
12		4: 2475 - 2700 MHz	x	x	1	1	x	x	x	x
13	RX4 Tuning	1: 1800 - 2025 MHz	0	0	x	x	x	x	x	x
14		2: 2025 - 2250 MHz	0	1	x	x	x	x	x	x
15		3: 2250 - 2475 MHz	1	0	x	x	x	x	x	x
16		4: 2475 - 2700 MHz	1	1	x	x	x	x	x	x

6 Application Information

Pin Configuration and Function

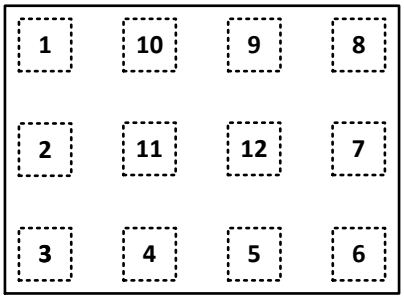


Figure 3: BGM14HBA12 Pin Configuration (top view)

Table 15: Pin Definition and Function

Pin No.	Name	Function
1	RFO	RF output port
2	VDD	Power supply
3	RX1[1]	RF input port 1
4	RX2[1]	RF input port 2
5	RX3[1]	RF input port 3
6	RX4[1]	RF input port 4
7	USID_Sel	USID Select
8	SDATA	MIPI RFFE data
9	SCLK	MIPI RFFE clock
10	VIO	MIPI RFFE supply
11	GND	Ground
12	GND	Ground

[1] Leave unconnected if not used (do NOT connect to GND)

Application Board Configuration

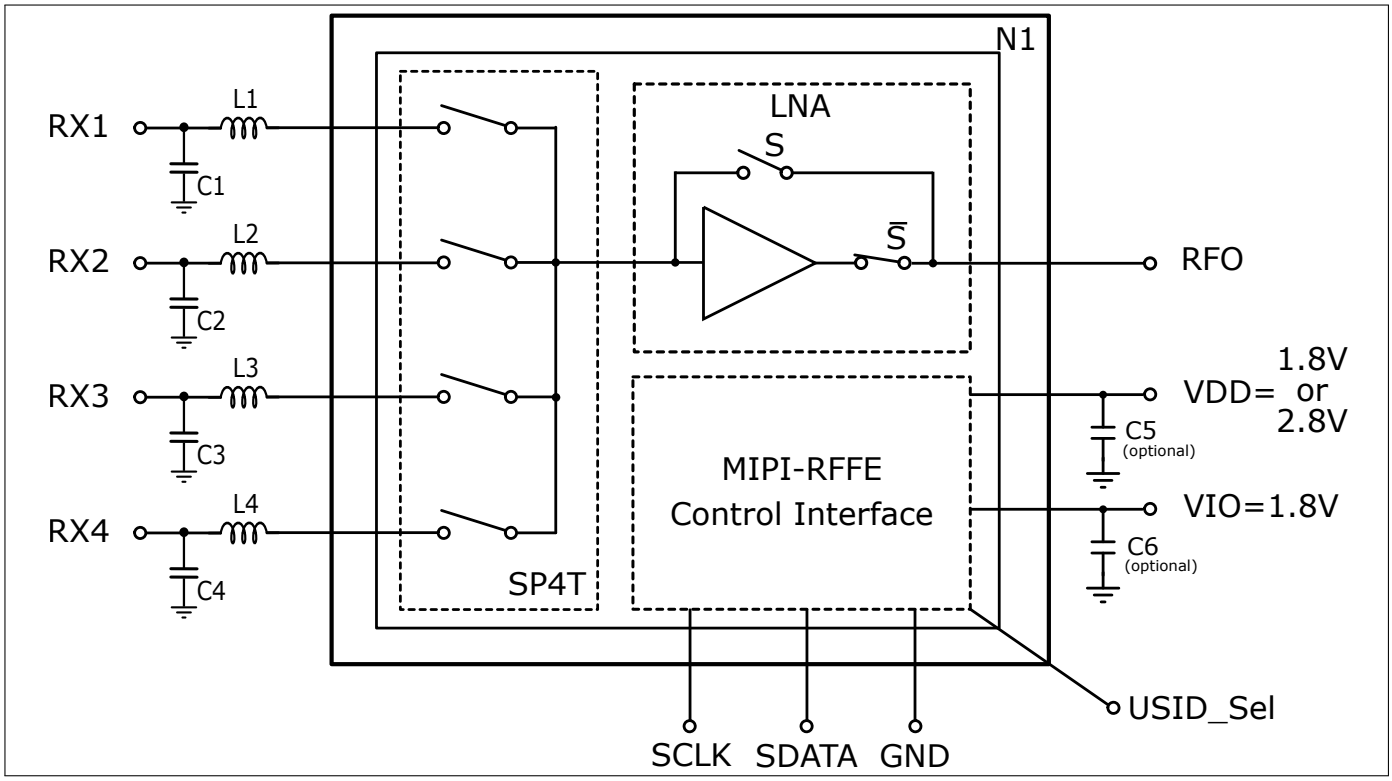


Figure 4: BGM14HBA12 Application Schematic

Table 16: Bill of Materials Table

Name	Value	Package	Manufacturer	Function
C1...C4	tbd	0402	Various	Input matching[1]
C5-C6 (optional)	≥ 1nF	0402	Various	RF bypass[2]
L1...L4	tbd	0402	Murata LQW15 type	Input matching[1]
N1	BGM14HBA12	PG-ATSLP-12	Infineon	LNA Multiplexer Module

[1]The matching elements must be optimized with reference to the frequency band of interest. Each band can be arbitrarily assigned to an RF port.
[2]RF bypass recommended to mitigate power supply noise.

7 Package Information

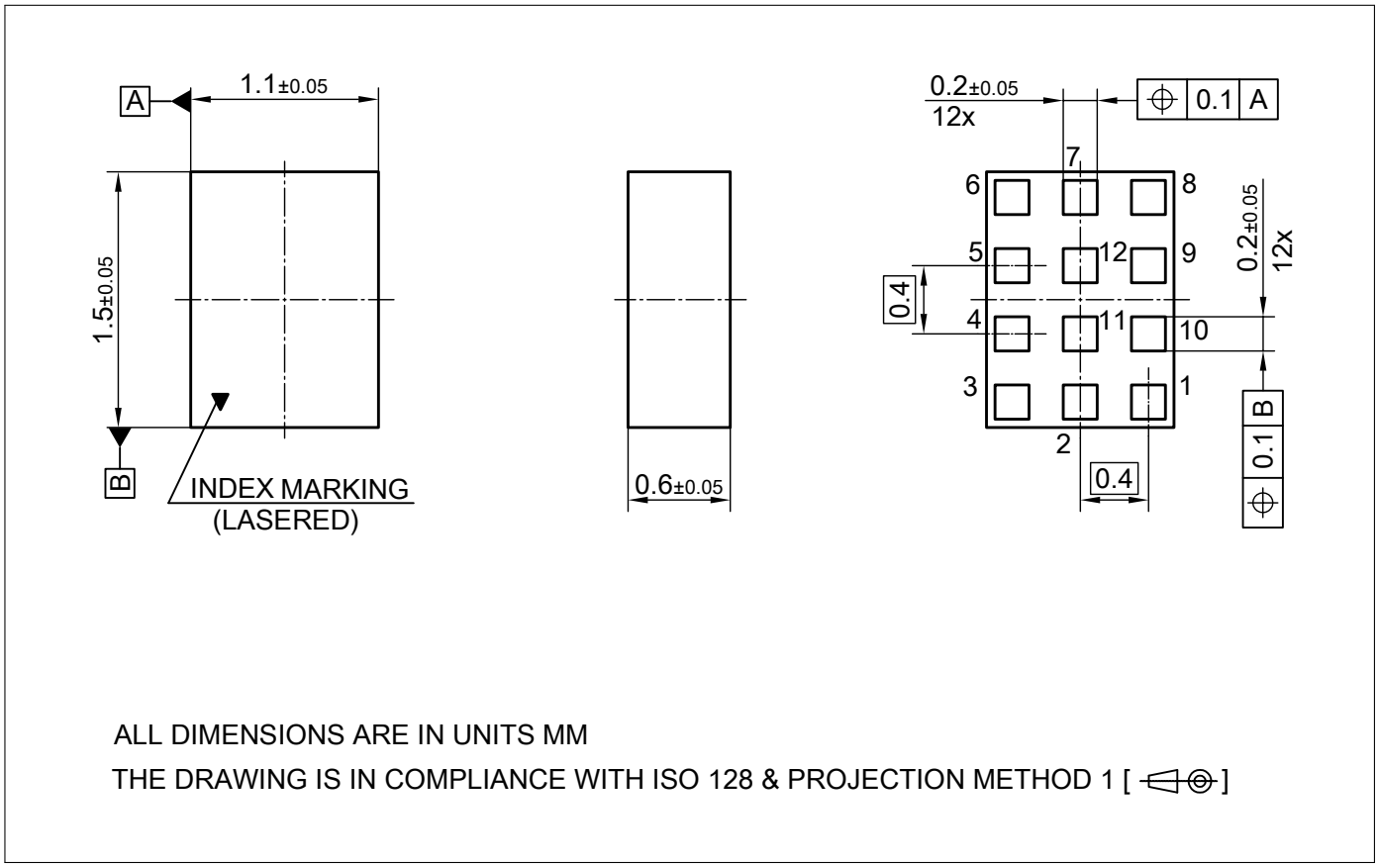


Figure 5: PG-ATSLP-12 Package Outline (top, side and bottom views)

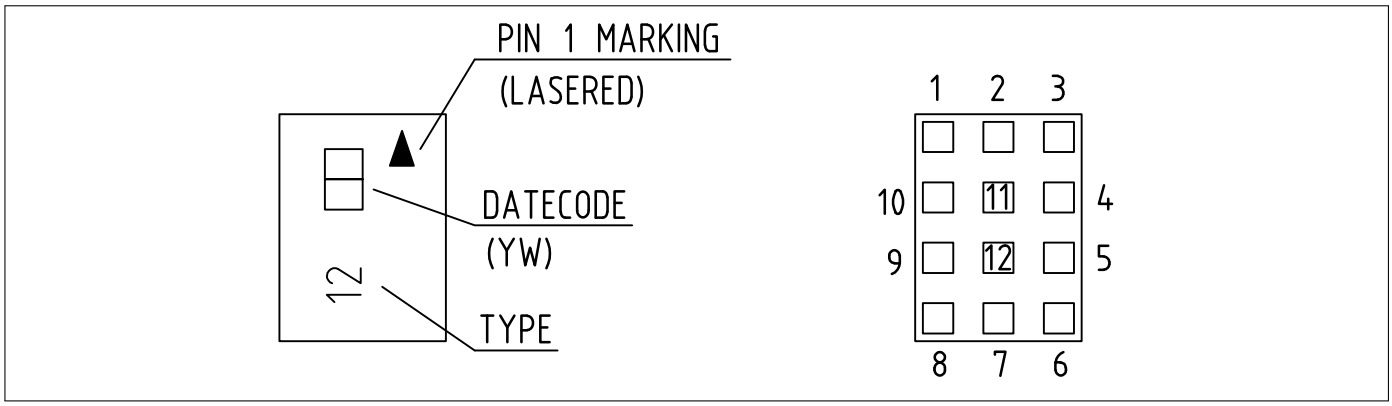


Figure 6: Marking Specification (top view)

Table 17: Year date code marking - digit "Y"

Year	"Y"	Year	"Y"	Year	"Y"
2010	0	2020	0	2030	0
2011	1	2021	1	2031	1
2012	2	2022	2	2032	2
2013	3	2023	3	2033	3
2014	4	2024	4	2034	4
2015	5	2025	5	2035	5
2016	6	2026	6	2036	6
2017	7	2027	7	2037	7
2018	8	2028	8	2038	8
2019	9	2029	9	2039	9

Table 18: Week date code marking - digit "W"

Week	"W"	Week	"W"	Week	"W"	Week	"W"	Week	"W"
1	A	12	N	23	4	34	h	45	v
2	B	13	P	24	5	35	j	46	x
3	C	14	Q	25	6	36	k	47	y
4	D	15	R	26	7	37	l	48	z
5	E	16	S	27	a	38	n	49	8
6	F	17	T	28	b	39	p	50	9
7	G	18	U	29	c	40	q	51	2
8	H	19	V	30	d	41	r	52	3
9	J	20	W	31	e	42	s		
10	K	21	Y	32	f	43	t		
11	L	22	Z	33	g	44	u		

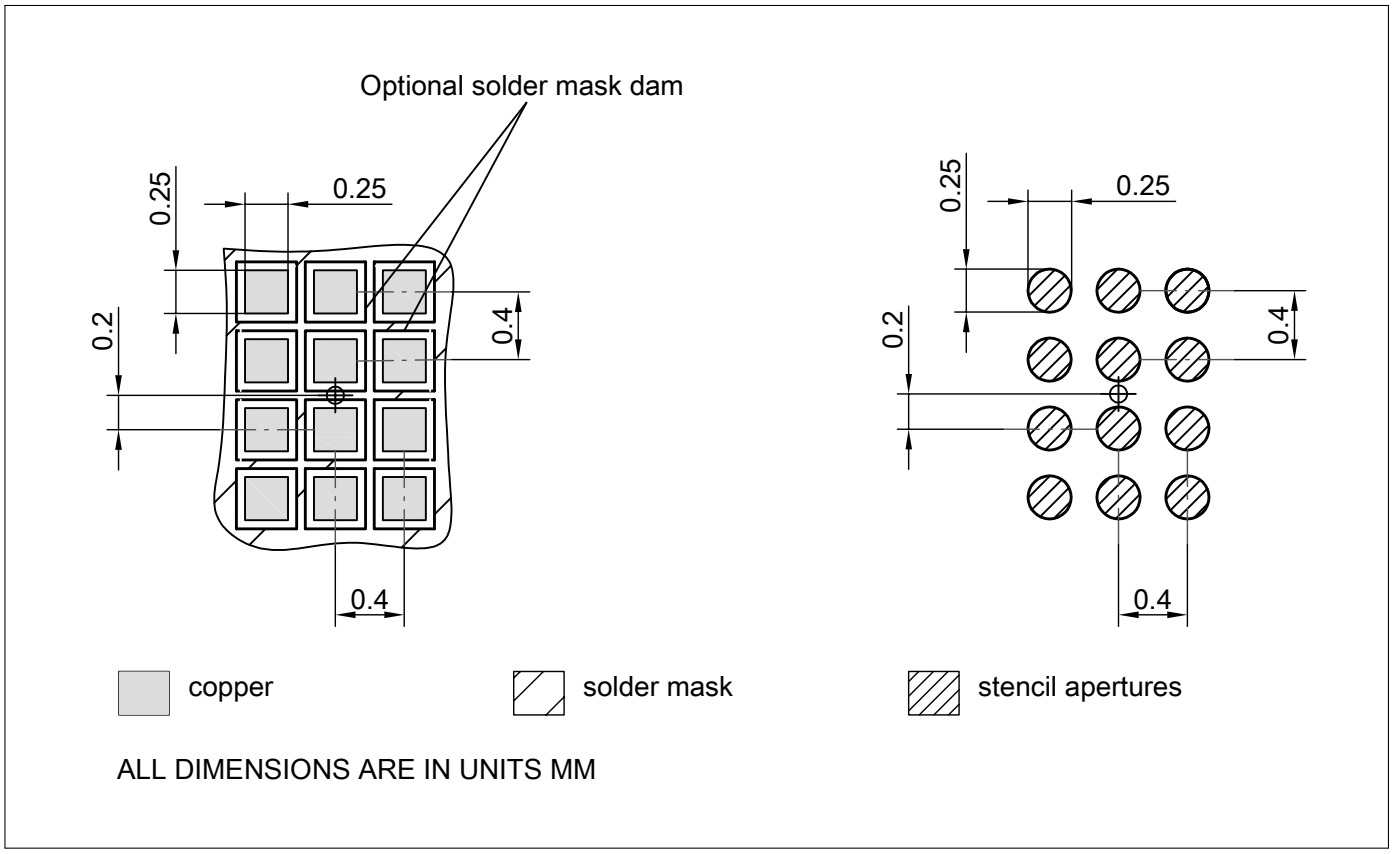


Figure 7: Footprint Recommendation

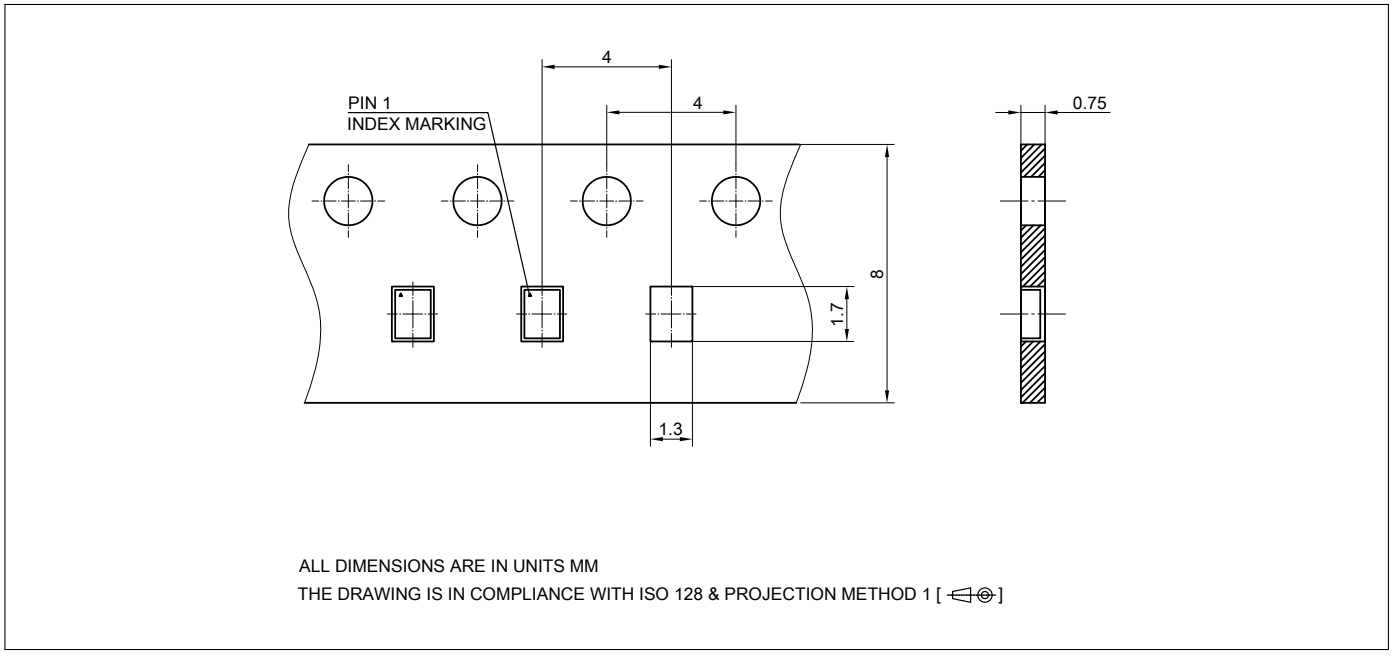


Figure 8: PG-ATSLP-12 Carrier Tape

Revision History	
v2.1	
Page or Item	**Subjects (major changes since previous revision)**
Revision 2.2, 2019-11-11	
Revision History	
3	Updated ESD HBM

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2019-11-11
Published by
Infineon Technologies AG
81726 Munich, Germany

Do you have a question about any aspect of this document?
Email: erratum@infineon.com

Document reference
Doc_Number

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie"). With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party. In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications. The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.