

IGC54T65T8RM

IGBT3 Chip Medium Power

Features:

- 650V Trench & Field Stop technology
- high short circuit capability, self limiting short circuit current
- positive temperature coefficient
- easy paralleling
- Qualified according to JEDEC for target applications

Recommended for:

• power modules

Applications:

drives



Chip Type	V _{CE}	<i>I</i> _{Cn}	Die Size	Package
IGC54T65T8RM	650V	100A	5.97 x 8.97 mm ²	sawn on foil

Mechanical Parameters

Wechanical Laramet	0.0				
Die size		5.97 x 8.97			
Emitter pad size (incl.	gate pad)	See chip drawing			
Gate pad size		1.615 x 0.817			
Area total		53.6			
Thickness		80	μm		
Wafer size		200	mm		
Max.possible chips pe	er wafer	486	486		
Passivation frontside		Photoimide			
Pad metal		3200 nm AlSiCu			
Backside metal		Ni Ag –system			
Die bond		Electrically conductive epoxy glue and soft solder			
Wire bond		Al, <500μm			
Reject ink dot size		Ø 0.65mm ; max 1.2mm			
	for original and sealed MBB bags	Ambient atmosphere air, Temperature 17°C – 25°C, < 6 month			
Storage environment	for open MBB bags	Acc. to IEC62258-3: Atmosphere >99% Nitrogen or inert gas, Humidity <25%RH, Temperature 17°C – 25°C, < 6 month			



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Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-Emitter voltage, $T_{\rm vj}$ =25 °C	V _{CE}	650	V
DC collector current, limited by $T_{\rm vj\;max}$	I _C	1)	А
Pulsed collector current, t_p limited by $T_{vj \max}^{2}$	$I_{c,puls}$	300	А
Gate emitter voltage	V _{GE}	±20	V
Operating junction temperature	T _{vj}	-40 +175	°C
Short circuit data $^{2)3)}$ $V_{GE} = 15V$, $V_{CC} = 360V$, $T_{Vj} = 150$ °C	tsc	10	μs

¹⁾ depending on thermal properties of assembly

Static Characteristics (tested on wafer), T_{vj} =25 °C

Parameter	Symbol	Conditions	Value			Unit
Tarameter	Cymbol	Conditions	min.	typ.	max.	0
Collector-Emitter breakdown voltage	V _{(BR)CES}	$V_{\rm GE}$ =0V , $I_{\rm C}$ =4 mA	650			
Collector-Emitter saturation voltage	V _{CEsat}	V _{GE} =15V, I _C =90A	1.08	1.55	1.82	V
Gate-Emitter threshold voltage	$V_{\rm GE(th)}$	$I_{\rm C}$ =1.6mA , $V_{\rm GE}$ = $V_{\rm CE}$	5.1	5.8	6.4	
Zero gate voltage collector current	I _{CES}	V_{CE} =650V , V_{GE} =0V			0.54	μΑ
Gate-Emitter leakage current	I _{GES}	V_{CE} =0V , V_{GE} =20V			600	nA
Integrated gate resistor	$r_{\rm G}$			2		Ω

Electrical Characteristics (not subject to production test - verified by design / characterization)

Parameter		Symbol	Conditions	Value			Unit
				min.	typ.	max.	Oiiit
Collector-Emitter saturation	<i>T</i> _{vj} =25 °C	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	V _{GF} =15V, I _C =100A		1.55	1.95	W
voltage	<i>T</i> _{vj} =150 °C	· V _{CEsat}	V _{GE} =13V, I _C =100A		1.75		V
Input capacitance		C _{ies}	$V_{CE}=25V$, $V_{GE}=0V$, $f=1MHz$		6160		pF
Reverse transfer capacitance		C _{res}	$T_{\text{vj}} = 25 ^{\circ}\text{C}$		183		Ρ'

²⁾ not subject to production test - verified by design/characterization

³⁾ allowed number of short circuits: <1000; time between short circuits: >1s.



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Further Electrical Characteristic

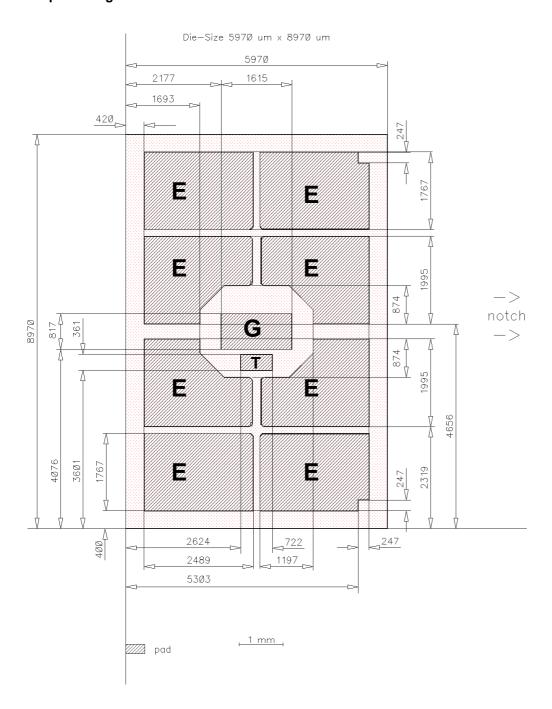
Switching characteristics and thermal properties are depending strongly on module design and mounting technology and can therefore not be specified for a bare die.

This chip data sheet refers to the device data sheet	FS100R07N2E4	Rev 2.0



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Chip Drawing



E = Emitter

G = Gate

T = Test pad do not contact



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Description
AQL 0,65 for visual inspection according to failure catalogue
Electrostatic Discharge Sensitive Device according to MIL-STD 883

Revision History

Version	Subjects (major changes since last revision)	Date

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