OptiMOS® Power-Transistor

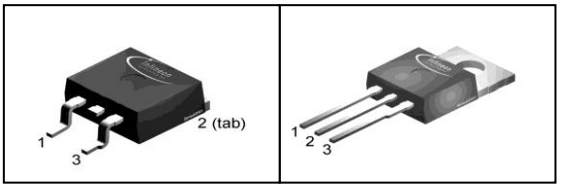
Features

- N-channel - Enhancement mode
- Automotive AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green package (lead free)
- Ultra low Rds(on)
- 100% Avalanche tested

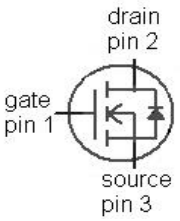
Product Summary

V_{DS}	55	V
$R_{DS(on),max}$ (SMD version)	4.7	mΩ
I_D	100	A

PG-TO263-3-2 PG-TO220-3-1



Type	Package	Marking
IPB100N06S2-05	PG-TO263-3-2	PN0605
IPP100N06S2-05	PG-TO220-3-1	PN0605



Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current[1]	I_D	T_C=25 °C, V_{GS}=10 V	100	A
		T_C=100 °C, V_{GS}=10 V[2]	100	
Pulsed drain current[2]	$I_{D,pulse}$	T_C=25 °C	400	
Avalanche energy, single pulse[2]	E_{AS}	I_D= 80 A	810	mJ
Gate source voltage[4]	V_{GS}		±20	V
Power dissipation	P_{tot}	T_C=25 °C	300	W
Operating and storage temperature	T_j, T_{stg}		-55 ... +175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics[2]						
Thermal resistance, junction - case	R_{thJC}		-	-	0.5	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}		-	-	62	
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm^2 cooling area[5]	-	-	40	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D= 1 mA	55	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250 µA	2.1	3.0	4.0	
Zero gate voltage drain current	I_{DSS}	V_{DS}=55 V, V_{GS}=0 V, T_j=25 °C	-	0.01	1	µA
		V_{DS}=55 V, V_{GS}=0 V, T_j=125 °C[2]	-	1	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=80 A	-	4.0	5.0	mΩ
		V_{GS}=10 V, I_D=80 A, SMD version	-	3.7	4.7	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics[2]						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=25 V, f=1 MHz	-	5110	-	pF
Output capacitance	C_{oss}		-	1330	-	
Reverse transfer capacitance	C_{rss}		-	320	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=30 V, V_{GS}=10 V, I_D=80 A, R_G=2.2 Ω	-	21	-	ns
Rise time	t_r		-	31	-	
Turn-off delay time	$t_{d(off)}$		-	59	-	
Fall time	t_f		-	30	-	
Gate Charge Characteristics[2]						
Gate to source charge	Q_{gs}	V_{DD}=44 V, I_D=100 A, V_{GS}=0 to 10 V	-	27	35	nC
Gate to drain charge	Q_{gd}		-	53	80	
Gate charge total	Q_g		-	130	170	
Gate plateau voltage	$V_{plateau}$		-	5.4	-	V
Reverse Diode						
Diode continous forward current[2]	I_S	T_C=25 °C	-	-	100	A
Diode pulse current[2]	$I_{S,pulse}$		-	-	400	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=80 A, T_j=25 °C	0.6	0.9	1.3	V
Reverse recovery time[2]	t_{rr}	V_R=30 V, I_F=I_S, di_F/dt=100 A/µs	-	60	75	ns
Reverse recovery charge[2]	Q_{rr}	V_R=30 V, I_F=I_S, di_F/dt=100 A/µs	-	130	160	nC

[1] Current is limited by bondwire; with an R_{thJC} = 0.5 K/W the chip is able to carry 170 A at 25°C. For detailed information see Application Note ANPS071E at *www.infineon.com/optimos*

[2] Defined by design. Not subject to production test.

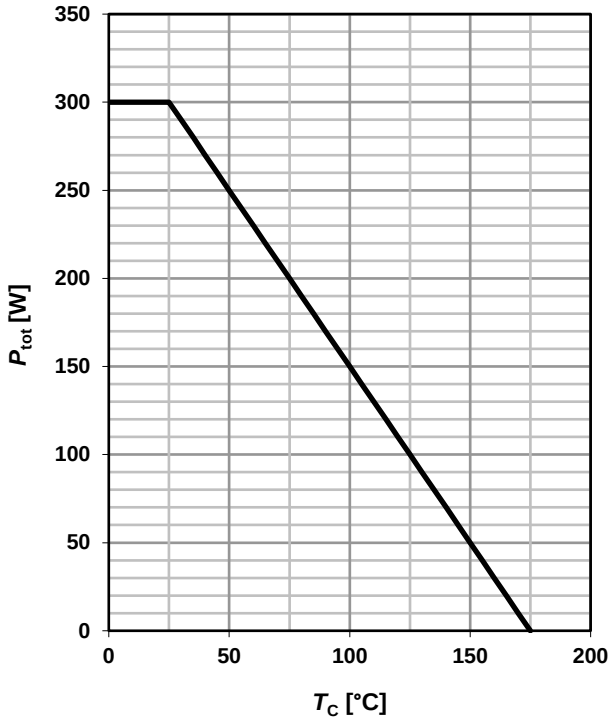
[3] See diagram 13.

[4] Qualified at -20V and +20V.

[5] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

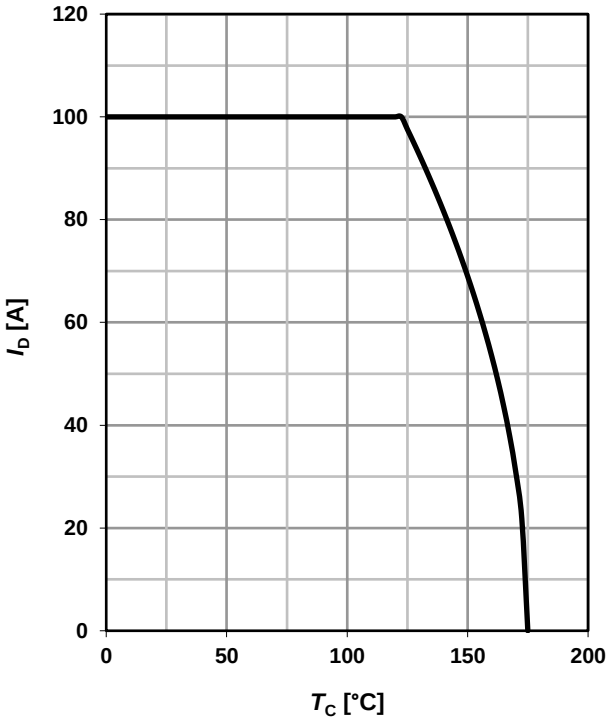
1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} \geq 6$ V



2 Drain current

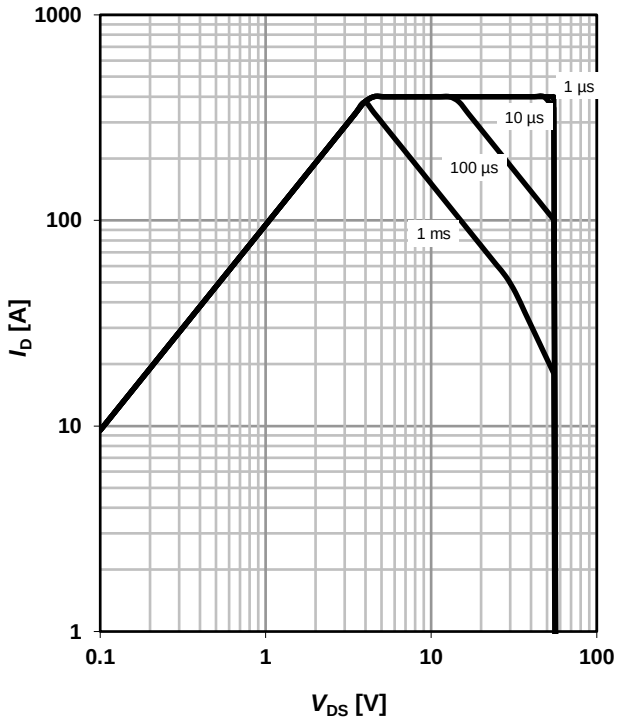
$I_D = f(T_C)$; $V_{GS} \geq 10$ V



3 Safe operating area

$I_D = f(V_{DS})$; $T_C = 25$ °C; $D = 0$

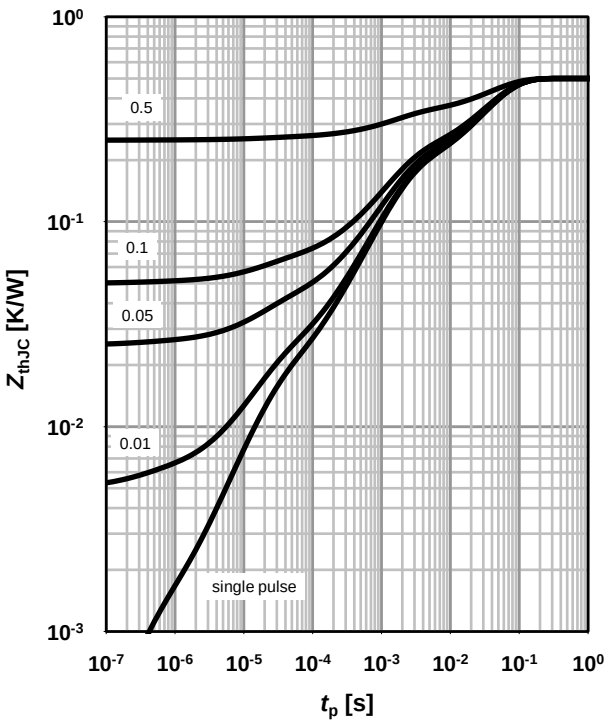
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

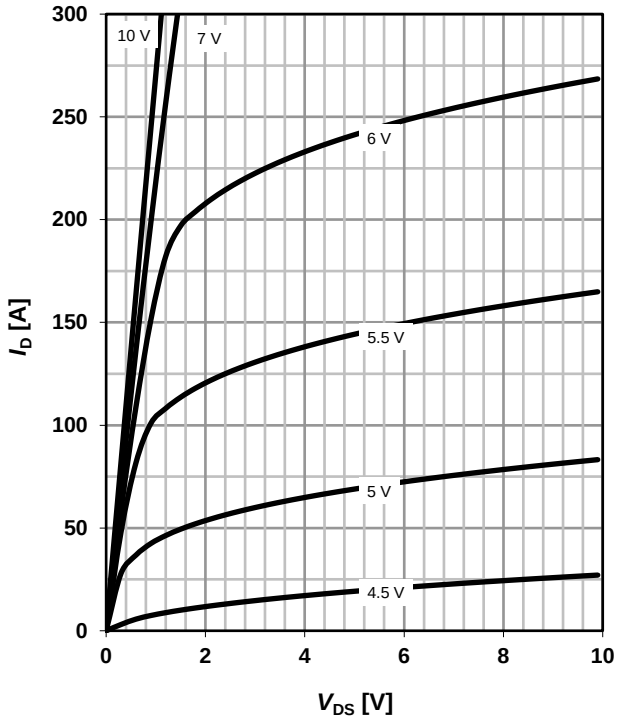
parameter: $D = t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS})$; $T_j = 25$ °C

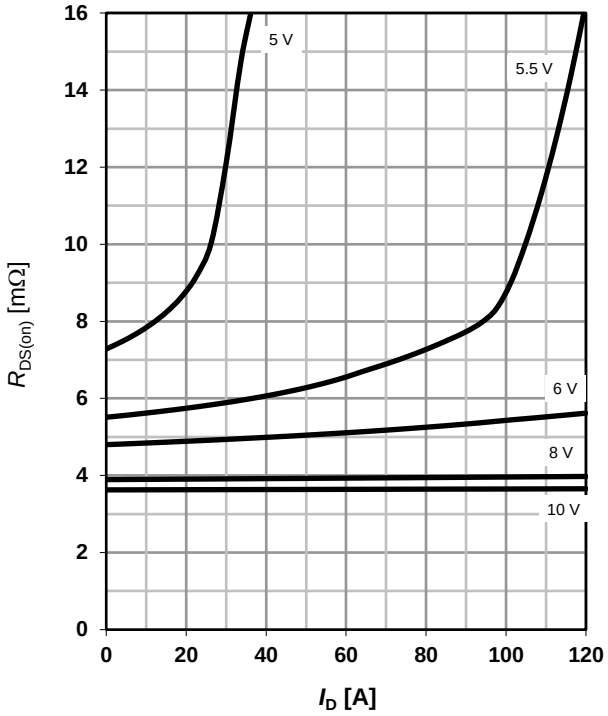
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = (I_D)$; $T_j = 25$ °C

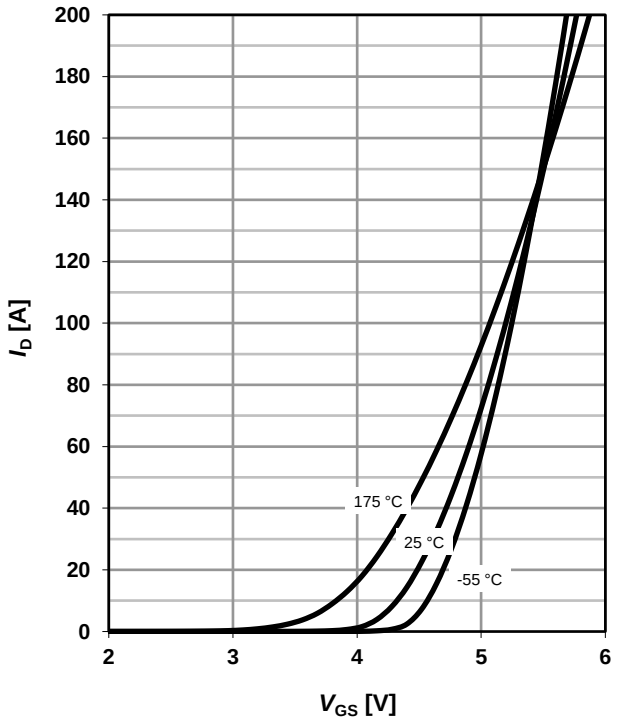
parameter: V_{GS}



7 Typ. transfer characteristics

$I_D = f(V_{GS})$; $V_{DS} = 6$V

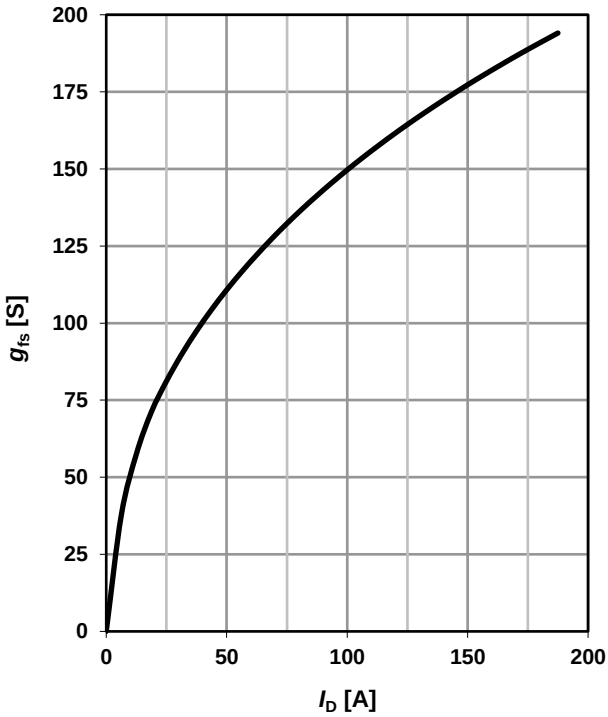
parameter: T_j



8 Typ. Forward transconductance

$g_{fs} = f(I_D)$; $T_j = 25$°C

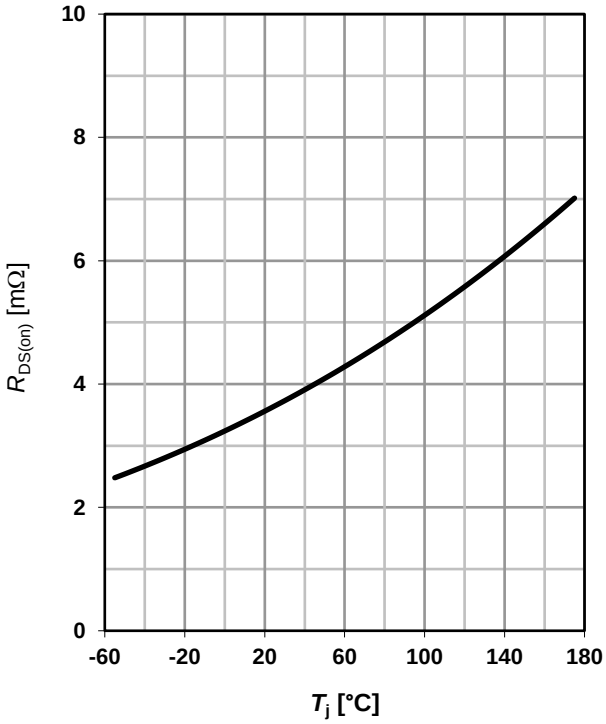
parameter: g_{fs}



9 Typ. Drain-source on-state resistance

$R_{DS(ON)} = f(T_j)$

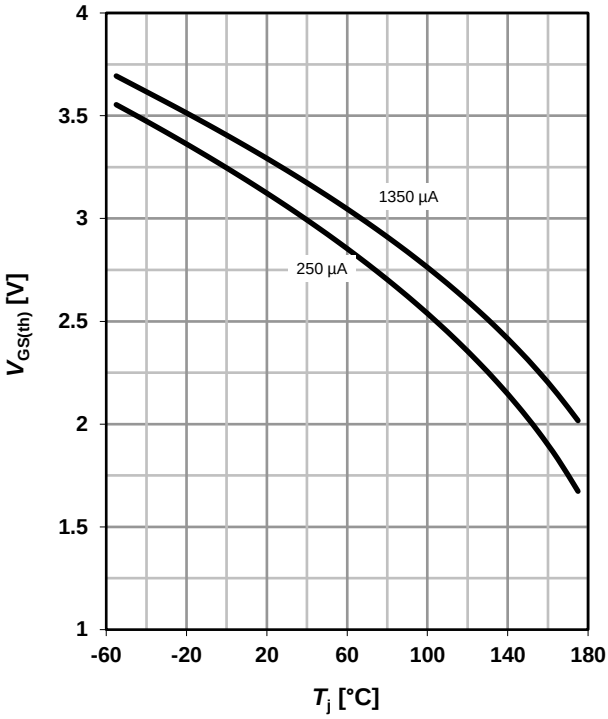
parameter: $I_D = 80$ A; $V_{GS} = 10$ V



10 Typ. gate threshold voltage

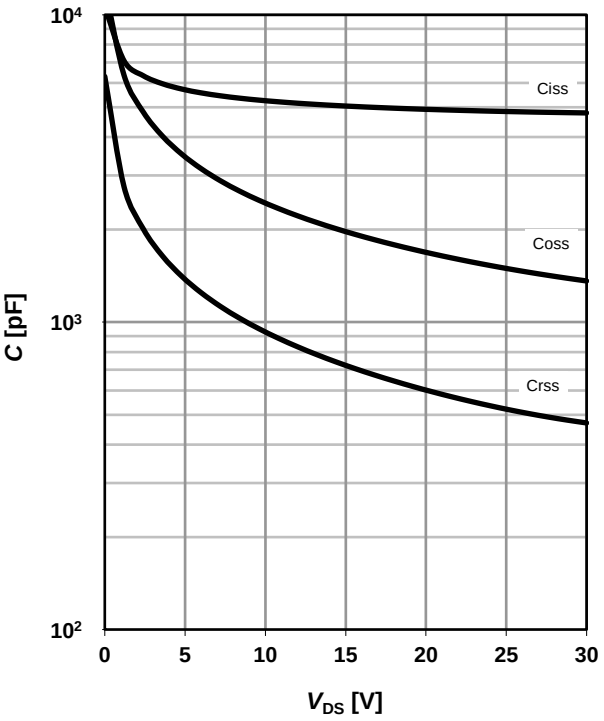
$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$

parameter: I_D



11 Typ. capacitances

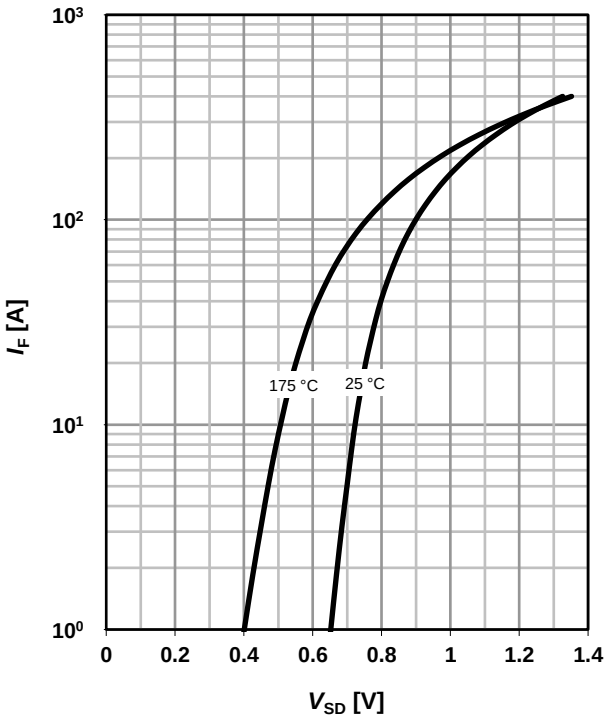
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



12 Typical forward diode characteristicis

IF = f(V_{SD})

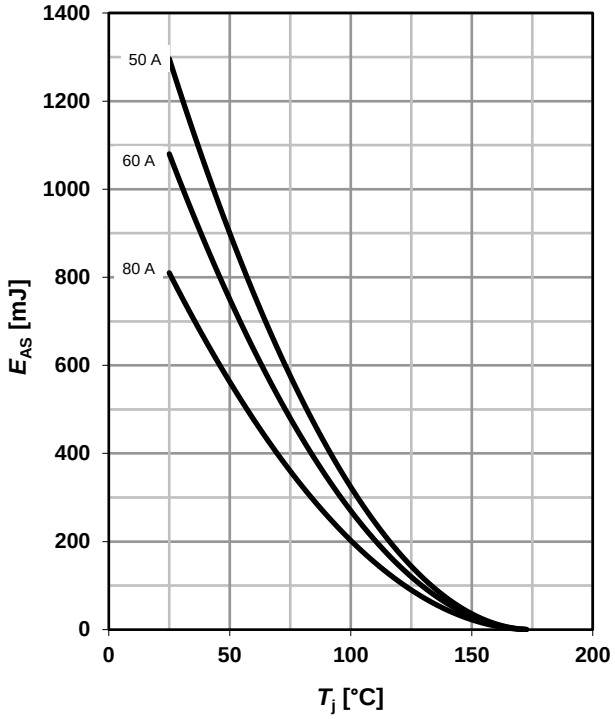
parameter: T_j



13 Typical avalanche energy

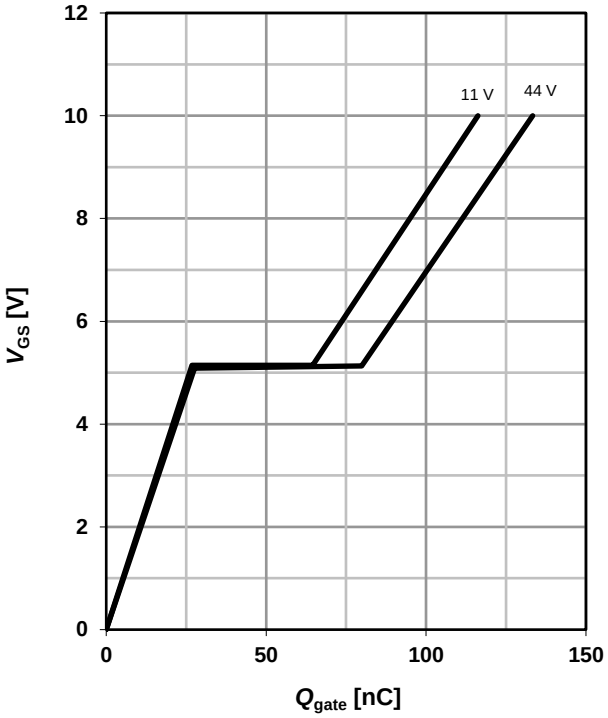
$E_{AS} = f(T_j)$

parameter: I_D



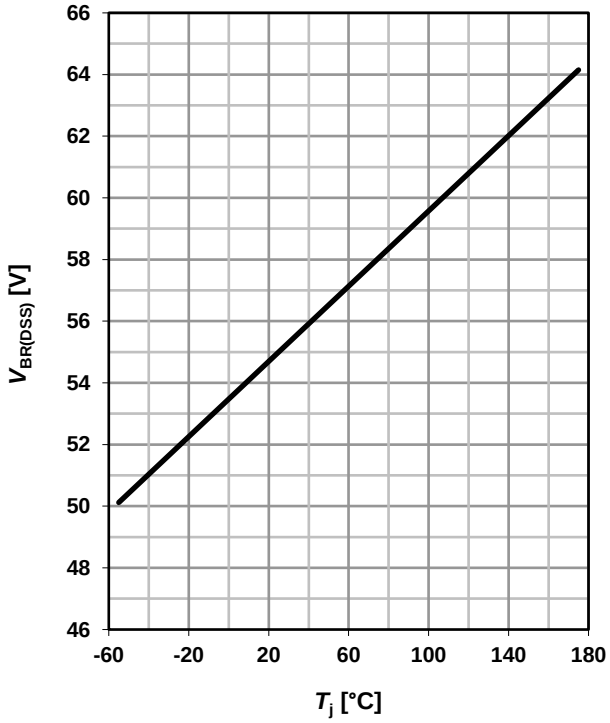
14 Typ. gate charge

$V_{GS} = f(Q_{gate})$; $I_D = 80$ A pulsed

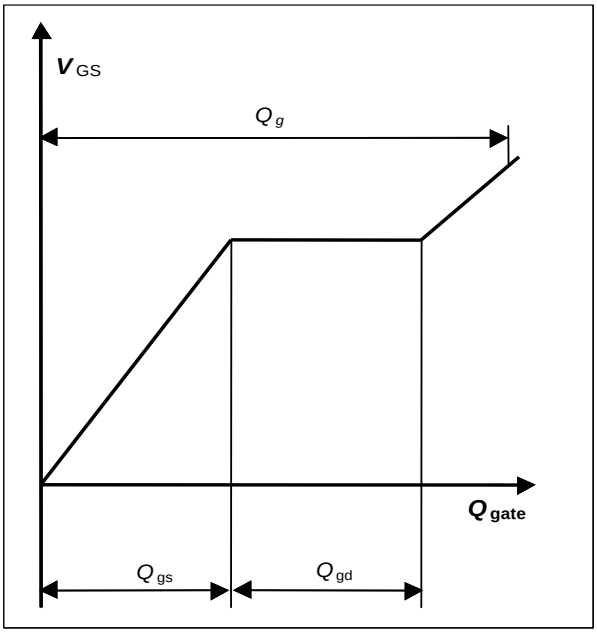


15 Typ. drain-source breakdown voltage

$V_{BR(DSS)} = f(T_j)$; $I_D = 1$ mA

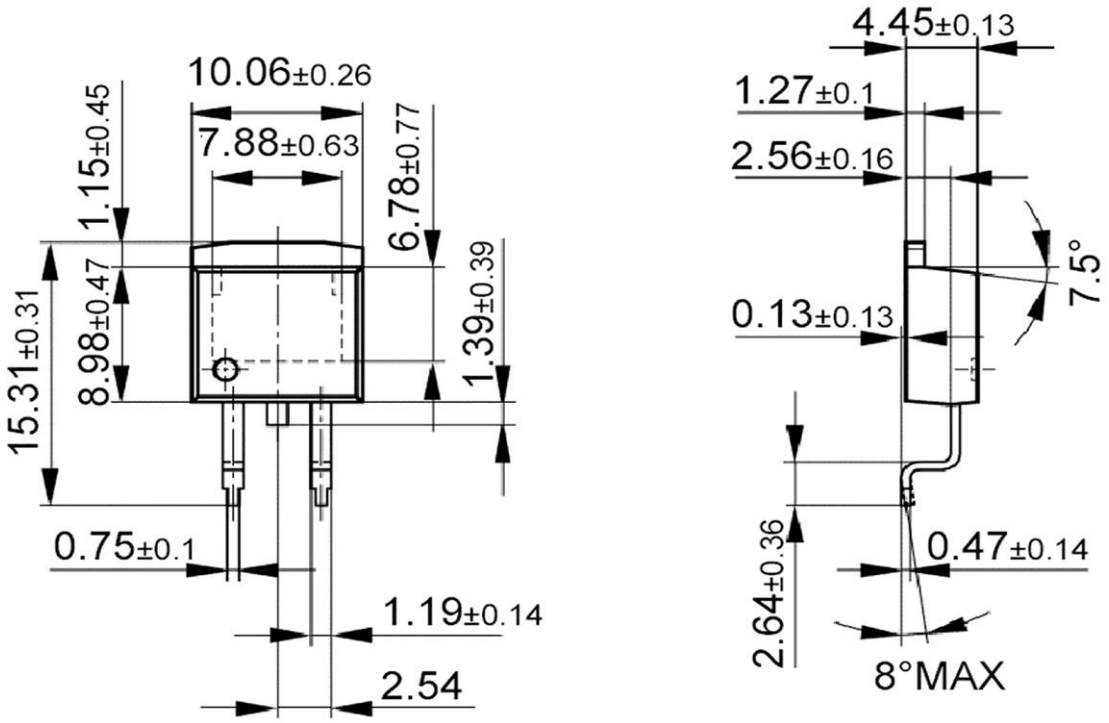


16 Gate charge waveforms

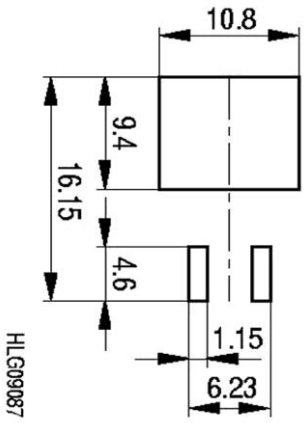


Package Outline

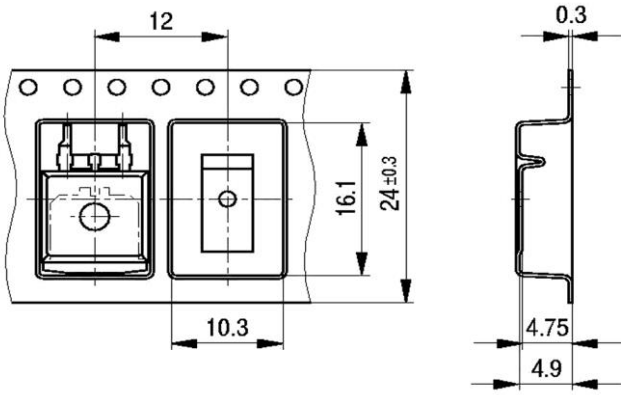
P-TO263-3-2: Outline



Footprint

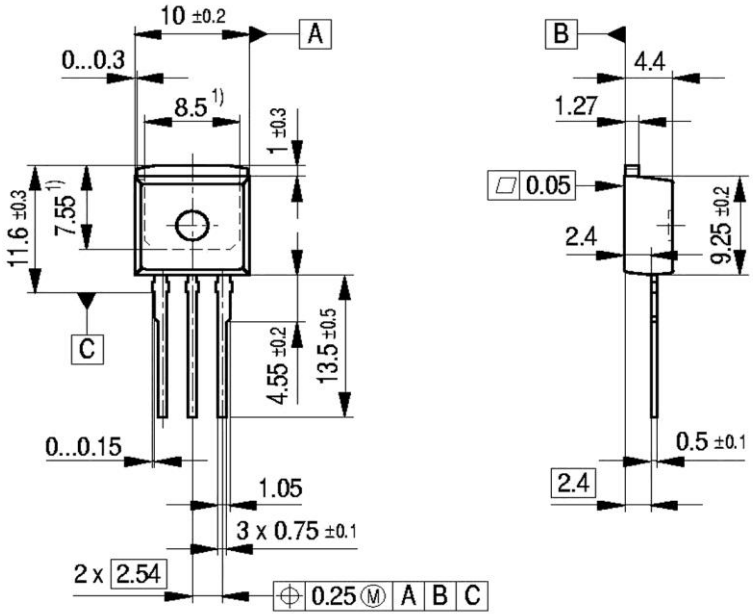


Packaging



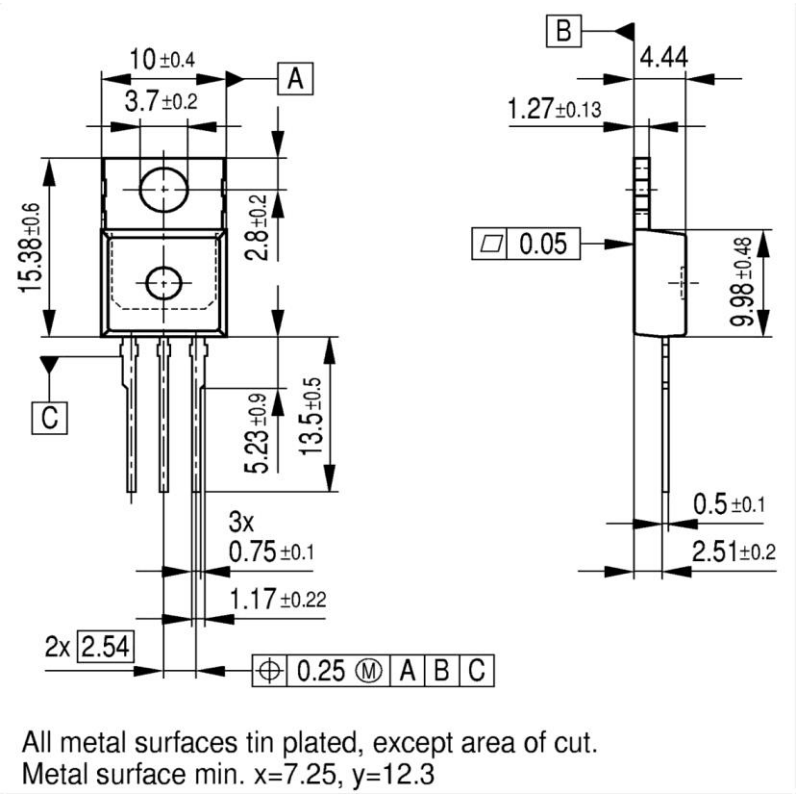
Dimensions in mm

P-TO262-3-1: Outline



1) Typical
Metal surface min. X = 7.25, Y = 6.9
All metal surfaces tin plated, except area of cut.

P-TO220-3-1: Outline



All metal surfaces tin plated, except area of cut.
Metal surface min. x=7.25, y=12.3

Packaging

Dimensions in mm

Published by
Infineon Technologies AG
81726 Munich, Germany

Legal Disclaimer
The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information
For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

Warnings
Due to technical requirements, components may contain dangerous substances.
For information on the types in question, please contact the nearest Infineon Technologies Office.
Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life.
If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Revision History

Version	Date	Changes
Version 1.0	13.03.2006	Final Data Sheet
Version 1.01	24.08.2020	Removal of ordering code Correction of condition parameter I_D related to $V_{GS(th)}$ in figure 10