International
IOR Rectifier

Data Sheet No. PD60163-U

IR2109(4) (S) & (PbF)

HALF-BRIDGE DRIVER

Features

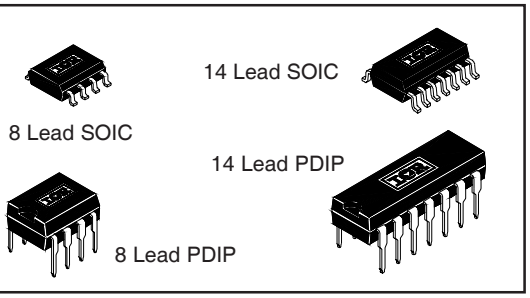
- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V, 5V and 15V input logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- High side output in phase with IN input
- Logic and power ground +/- 5V offset.
- Internal 540ns dead-time, and programmable up to 5us with one external R_{DT} resistor (IR21094)
- Lower di/dt gate driver for better noise immunity
- Shut down input turns off both channels.
- Available in Lead-Free

Product Summary

V_{OFFSET}	600V max.
I_O+/-	120 mA / 250 mA
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	750 & 200 ns
Dead Time	540 ns

(programmable up to 5uS for IR21094)

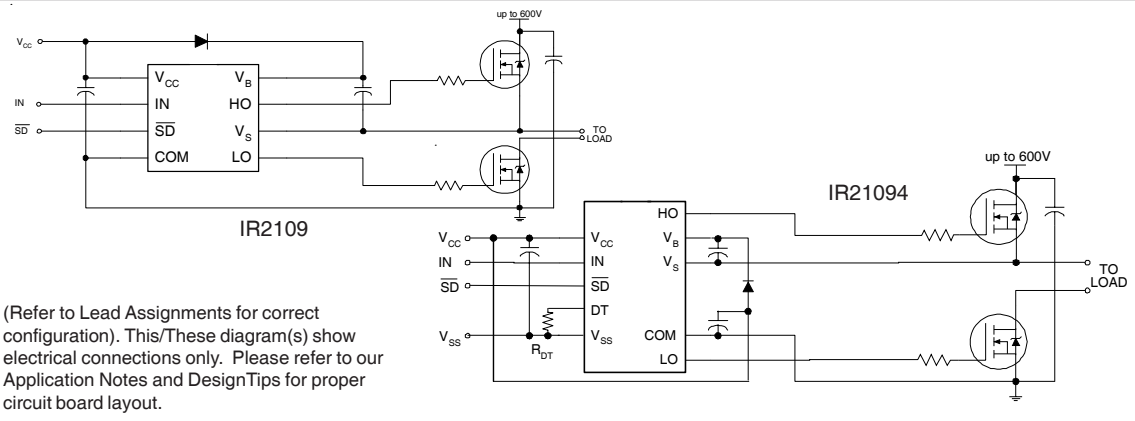
Packages



Description

The IR2109(4)(S) are high voltage, high speed power MOSFET and IGBT drivers with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Typical Connection



(Refer to Lead Assignments for correct configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating absolute voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
DT	Programmable dead-time pin voltage (IR21094 only)		V_{SS} - 0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (IN & $\overline{SD}$)		V_{SS} - 0.3	V_{CC} + 0.3	
V_{SS}	Logic ground (IR21094/IR21894 only)		V_{CC} - 25	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(8 Lead PDIP)	—	1.0	W
		(8 Lead SOIC)	—	0.625	
		(14 lead PDIP)	—	1.6	
		(14 lead SOIC)	—	1.0	
Rth_{JA}	Thermal resistance, junction to ambient	(8 Lead PDIP)	—	125	°C/W
		(8 Lead SOIC)	—	200	
		(14 lead PDIP)	—	75	
		(14 lead SOIC)	—	120	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-50	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
VB	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (IN & $\overline{SD}$)	V_{SS}	V_{CC}	
DT	Programmable dead-time pin voltage (IR21094 only)	V_{SS}	V_{CC}	
V_{SS}	Logic ground (IR21094 only)	-5	5	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to -V_{BS}. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, C_L = 1000 pF, T_A = 25°C, DT = VSS unless otherwise specified.

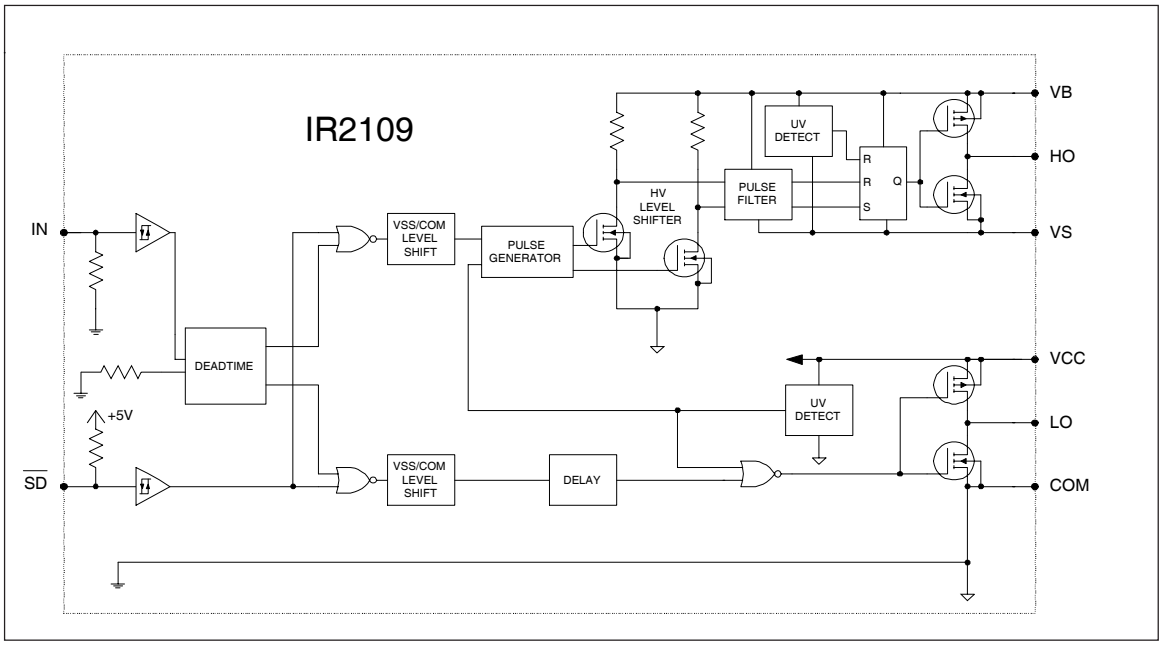
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	750	950	nsec	V_S = 0V
t_{off}	Turn-off propagation delay	—	200	280		V_S = 0V or 600V
t_{sd}	Shut-down propagation delay	—	200	280		
MT	Delay matching, HS & LS turn-on/off	—	0	70		
t_r	Turn-on rise time	—	150	220		V_S = 0V
t_f	Turn-off fall time	—	50	80		V_S = 0V
DT	Deadtime: LO turn-off to HO turn-on(DT_{LO-HO}) &	400	540	680		RDT= 0
	HO turn-off to LO turn-on (DT_{HO-LO})	4	5	6	usec	RDT = 200k (IR21094)
MDT	Deadtime matching = $DT_{LO\ -\ HO}$ - DT_{HO-LO}	—	0	60	nsec	RDT=0
		—	0	600		RDT = 200k (IR21094)

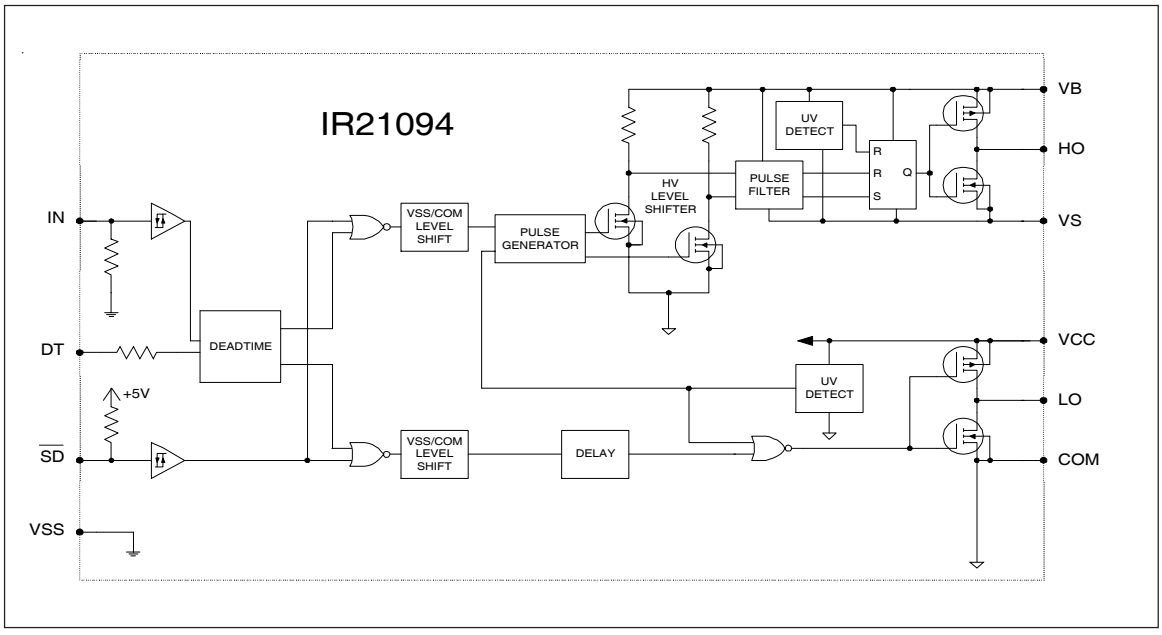
Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, DT= V_{SS} and T_A = 25°C unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to V_{SS} /COM and are applicable to the respective input leads: IN and $\overline{SD}$. The V_O, I_O and Ron parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage for HO & logic "0" for LO	2.9	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic "0" input voltage for HO & logic "1" for LO	—	—	0.8		V_{CC} = 10V to 20V
$V_{SD,TH+}$	$\overline{SD}$ input positive going threshold	2.9	—	—		V_{CC} = 10V to 20V
$V_{SD,TH-}$	$\overline{SD}$ input negative going threshold	—	—	0.8		V_{CC} = 10V to 20V
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	0.8	1.4		I_O = 20 mA
V_{OL}	Low level output voltage, V_O	—	0.3	0.6		I_O = 20 mA
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current	20	75	130		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} supply current	0.4	1.0	1.6	mA	V_{IN} = 0V or 5V RDT = 0
I_{IN+}	Logic "1" input bias current	—	5	20	µA	IN = 5V, $\overline{SD}$ = 0V
I_{IN-}	Logic "0" input bias current	—	—	2		IN = 0V, SD = 5V
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0		
V_{CCUVH} V_{BSUVH}	Hysteresis	0.3	0.7	—		
I_{O+}	Output high short circuit pulsed vurrent	120	200	—	mA	V_O = 0V, PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	250	350	—		V_O = 15V,PW ≤ 10 µs

Functional Block Diagrams

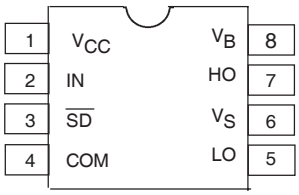




Lead Definitions

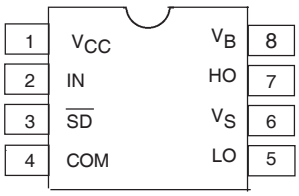
Symbol	Description
IN	Logic input for high and low side gate driver outputs (HO and LO), in phase with HO (referenced to COM for IR2109 and VSS for IR21094)
$\overline{SD}$	Logic input for shutdown (referenced to COM for IR2109 and VSS for IR21094)
DT	Programmable dead-time lead, referenced to VSS. (IR21094 only)
VSS	Logic Ground (21094 only)
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



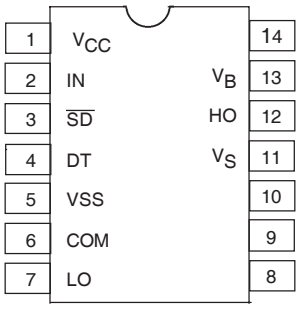
8 Lead PDIP

IR2109



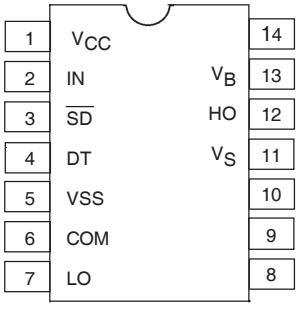
8 Lead SOIC

IR2109S



14 Lead PDIP

IR21094



14 Lead SOIC

IR21094S

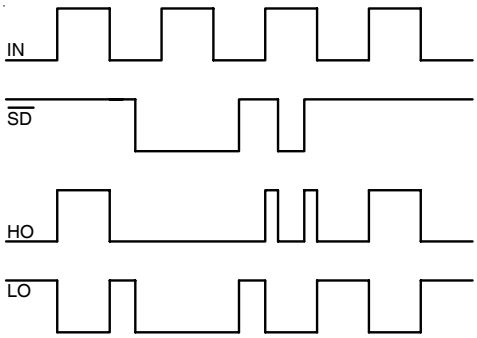


Figure 1. Input/Output Timing Diagram

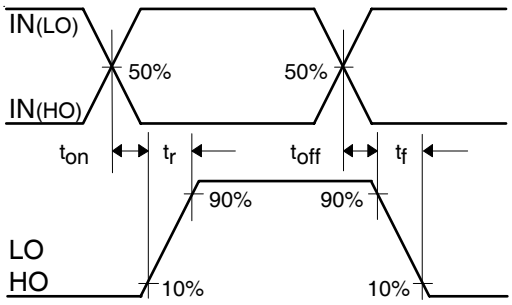


Figure 2. Switching Time Waveform Definitions

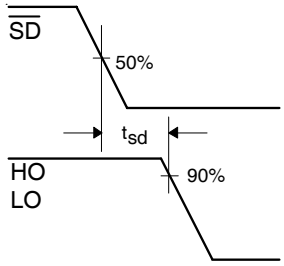


Figure 3. Shutdown Waveform Definitions

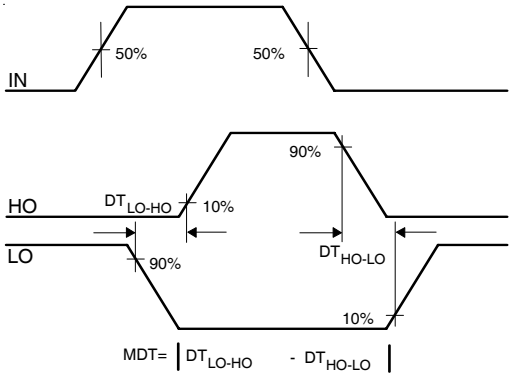


Figure 4. Deadtime Waveform Definitions

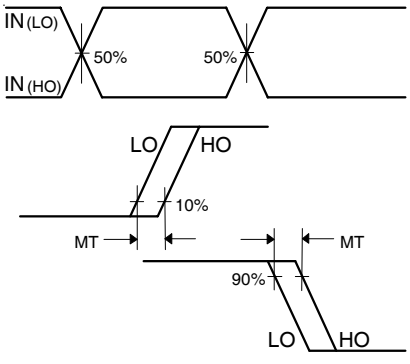


Figure 5. Delay Matching Waveform Definitions

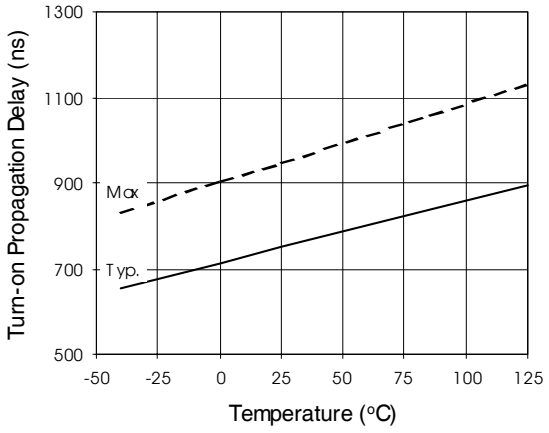


Figure 6A. Turn-on Propagation Delay vs. Temperature

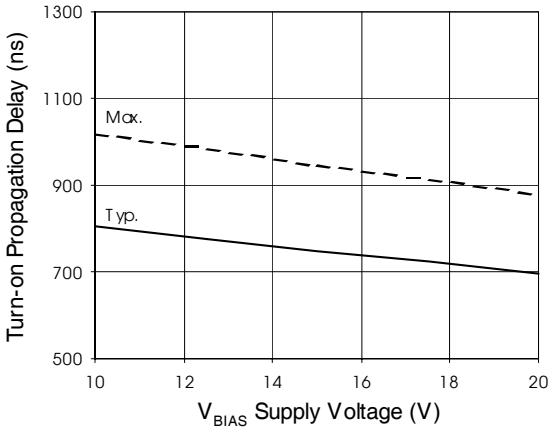


Figure 6B. Turn-on Propagation Delay vs. Supply Voltage

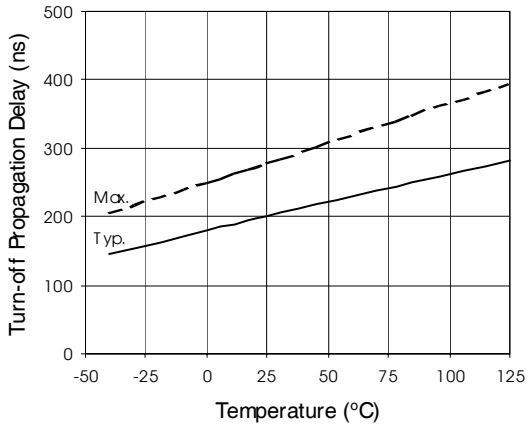


Figure 7A. Turn-off Propagation Delay vs. Temperature

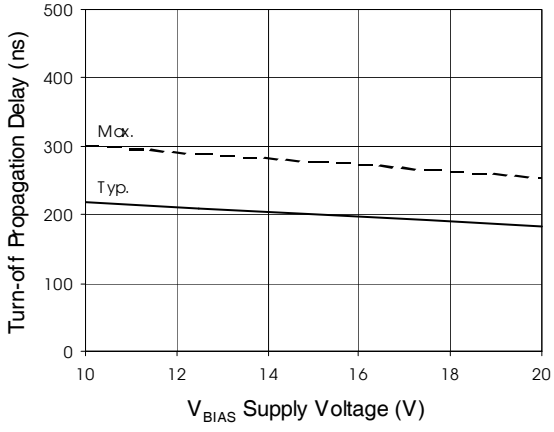


Figure 7B. Turn-off Propagation Delay vs. Supply Voltage

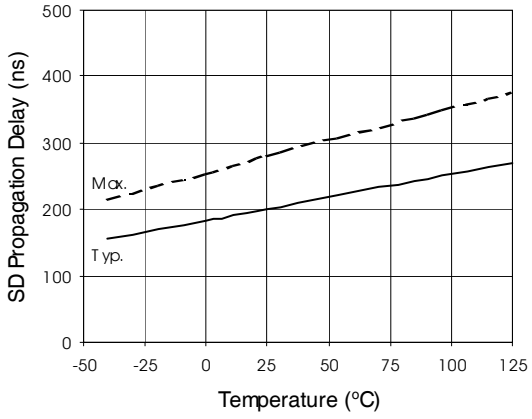


Figure 8A. SD Propagation Delay vs. Temperature

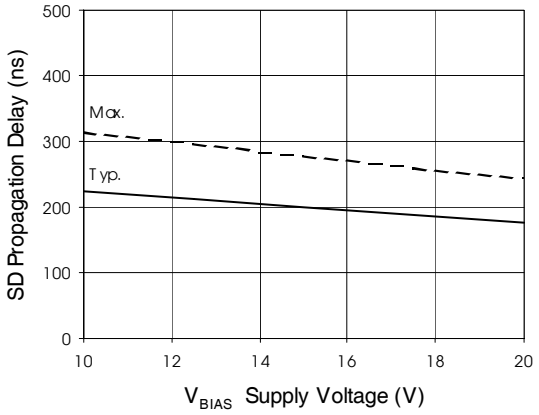


Figure 8B. SD Propagation Delay vs. Supply Voltage

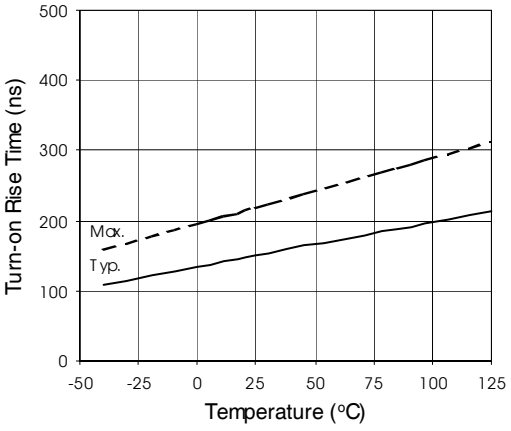


Figure 9A. Turn-on Rise Time vs. Temperature

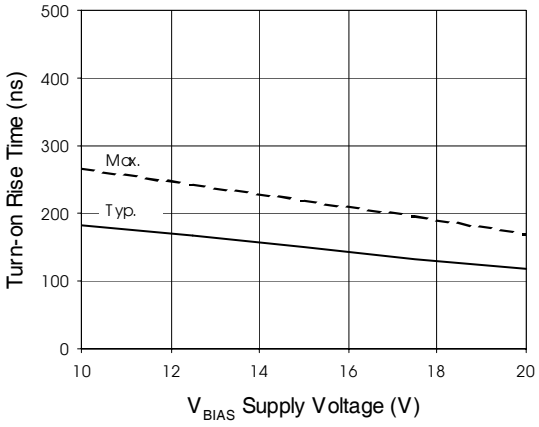


Figure 9B. Turn-on Rise Time vs. Supply Voltage

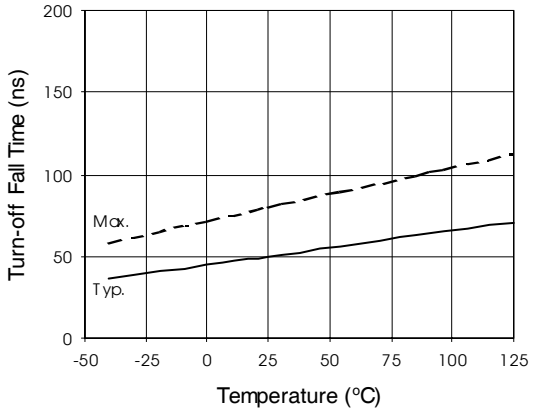


Figure 10A. Turn-off Fall Time vs. Temperature

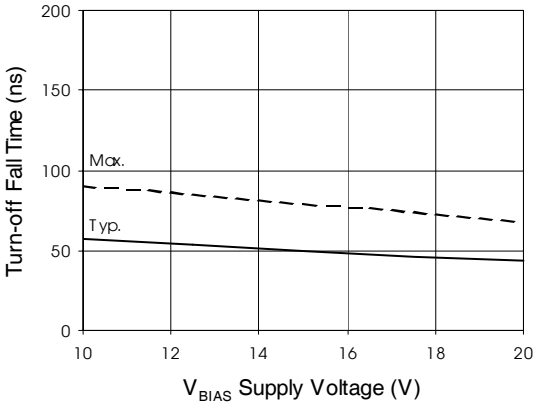


Figure 10B. Turn-off Fall Time vs. Supply Voltage

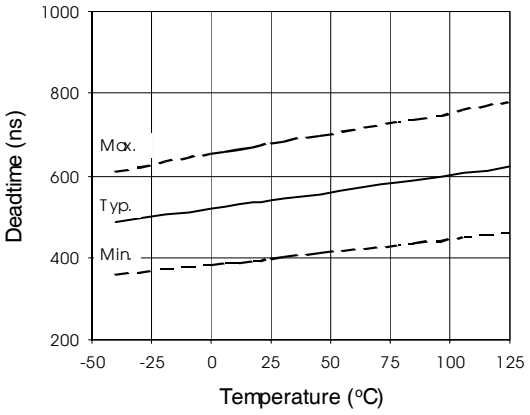


Figure 11A. Deadtime vs. Temperature

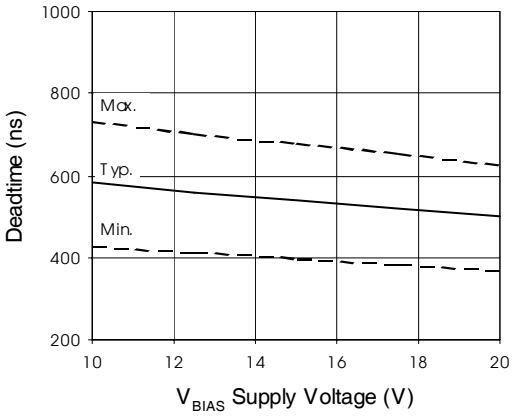


Figure 11B. Deadtime vs. Supply Voltage

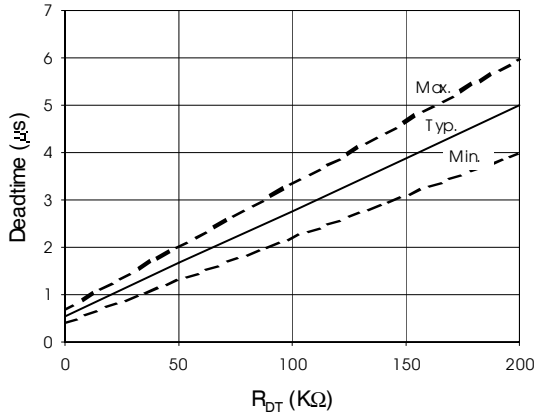


Figure 11C. Deadtime vs. R_{DT} (IR21094 only)

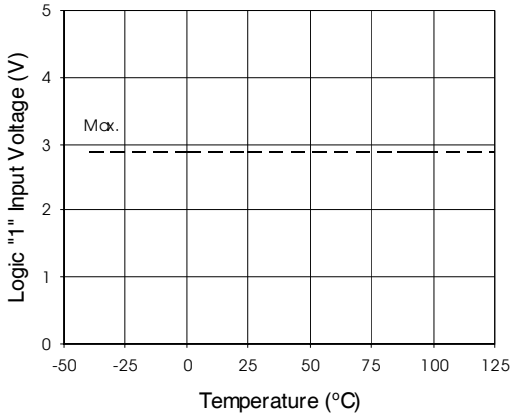


Figure 12A. Logic "1" Input Voltage vs. Temperature

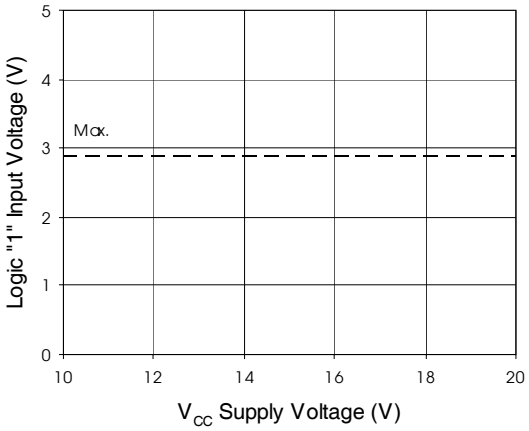


Figure 12B. Logic "1" Input Voltage vs. Supply Voltage

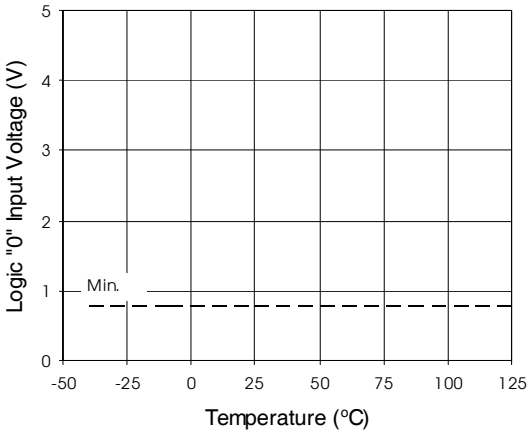


Figure 13A. Logic "0" Input Voltage vs. Temperature

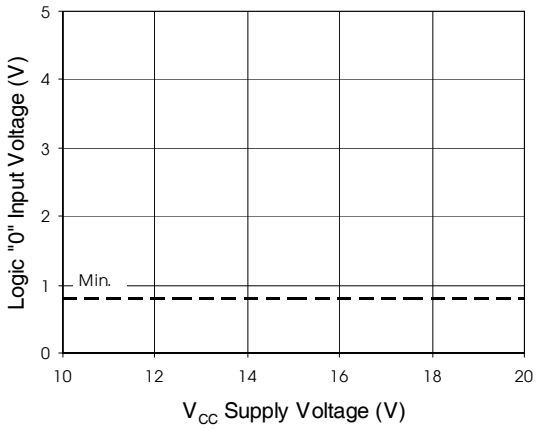


Figure 13B. Logic "0" Input Current vs. Supply Voltage

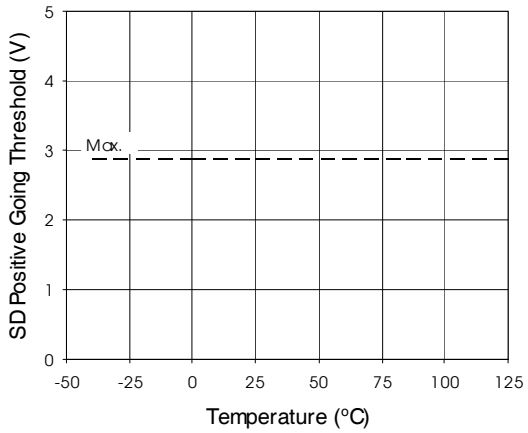


Figure 14A. SD Positive Going Threshold vs. Temperature

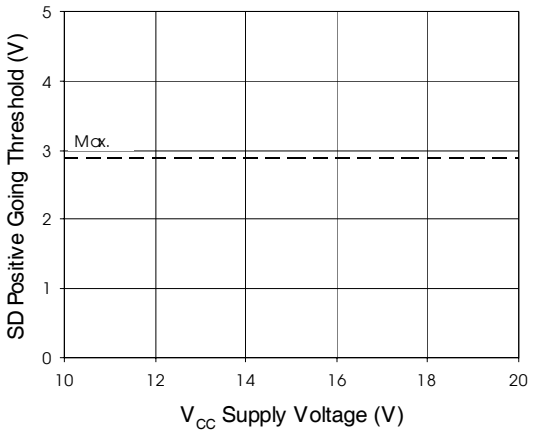


Figure 14B. SD Positive Going Threshold vs. Supply Voltage

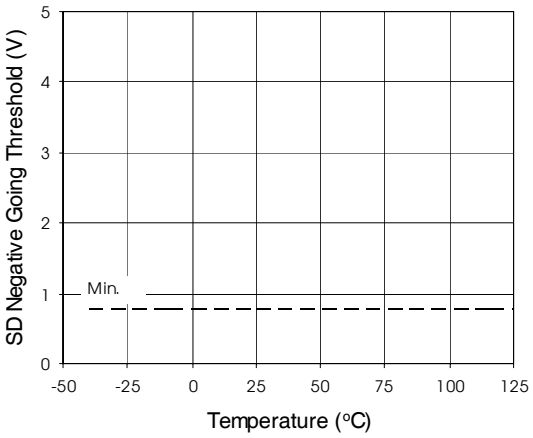


Figure 15A. SD Negative Going Threshold vs. Temperature

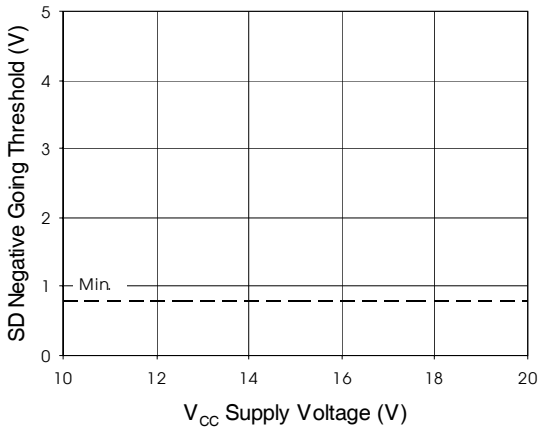


Figure 15B. SD Negative Going Threshold vs. Supply Voltage

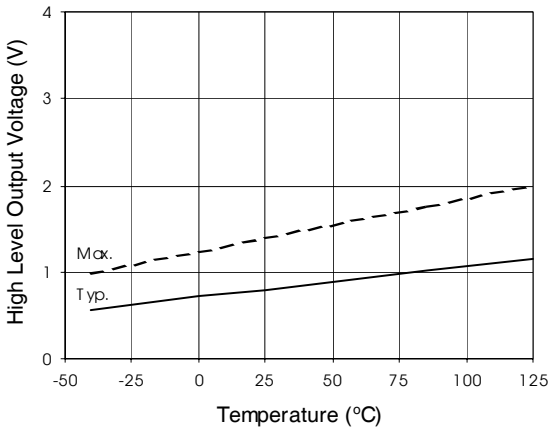


Figure 16A. High Level Output Voltage vs. Temperature

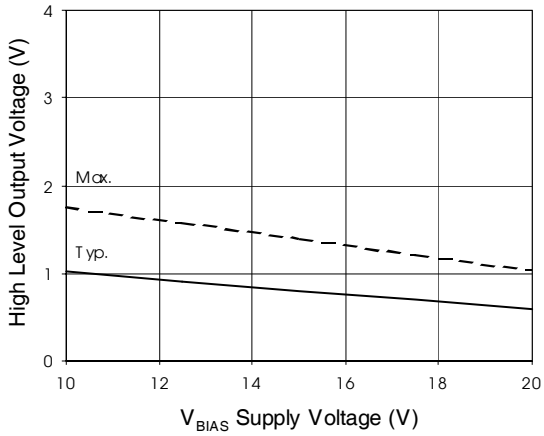


Figure 16B. High Level Output Voltage vs. Supply Voltage

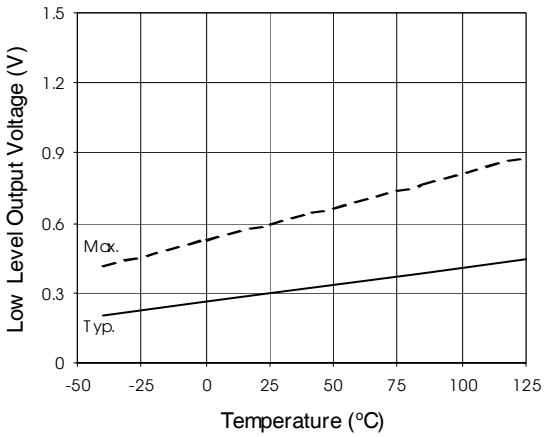


Figure 17A. Low Level Output Voltage vs. Temperature

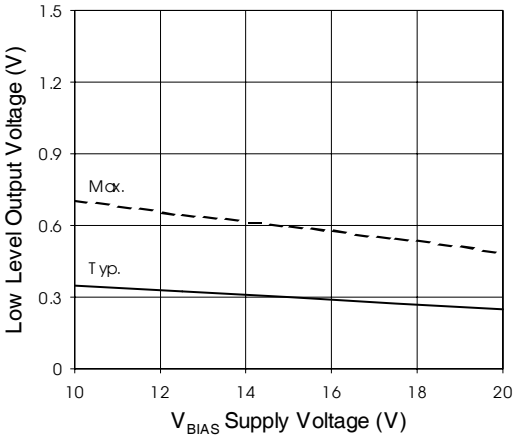


Figure 17B. Low Level Output Voltage vs. Supply Voltage

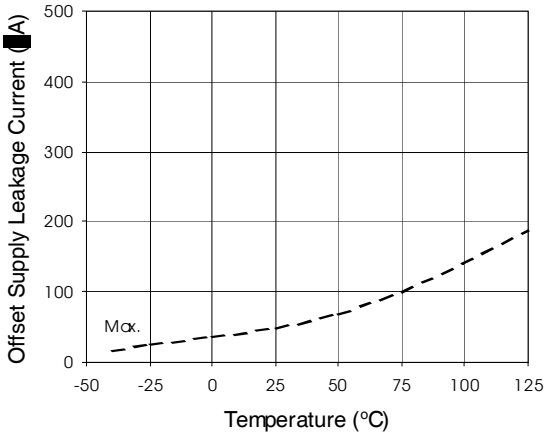
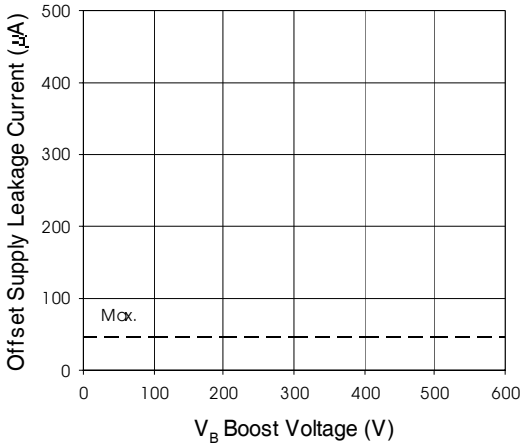


Figure 18A. Offset Supply Leakage Current vs. Temperature



igure 18B. Offset Supply Leakage Current vs. Boost Voltage

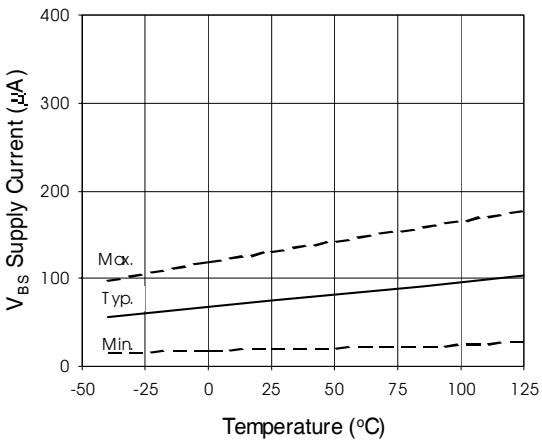


Figure 19A. V_{BS} Supply Current vs. Temperature

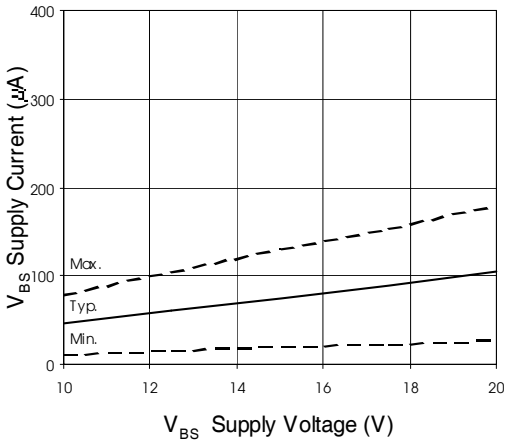


Figure 19B. V_{BS} Supply Current vs. Supply Voltage

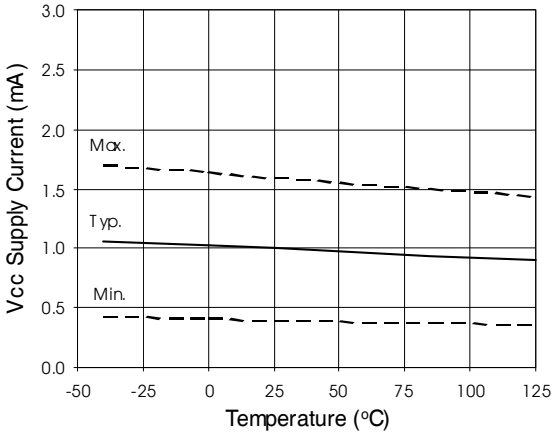


Figure 20A. V_{CC} Supply Current vs. Temperature

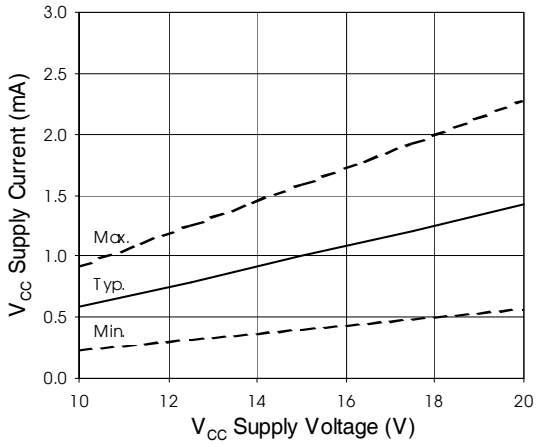


Figure 20B. V_{CC} Supply Current vs. V_{CC} Supply Voltage

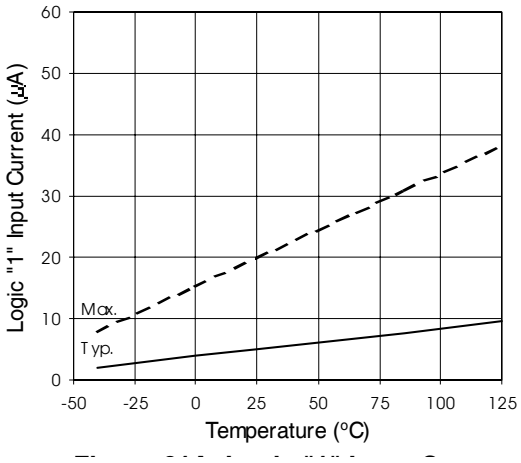


Figure 21A. Logic "1" Input Current vs. Temperature

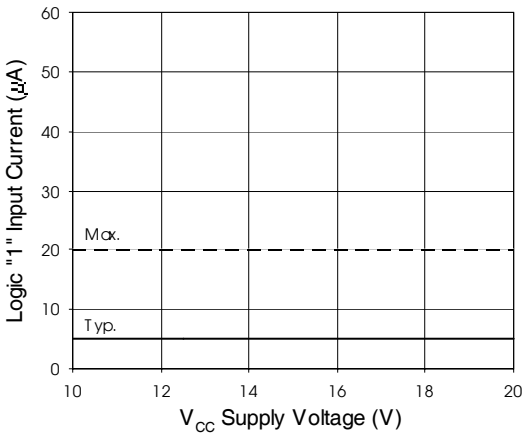


Figure 21B. Logic "1" Input Current vs. Supply Voltage

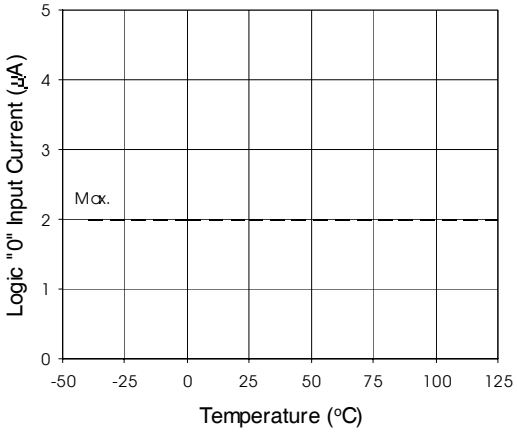


Figure 22A. Logic "0" Input Current vs. Temperature

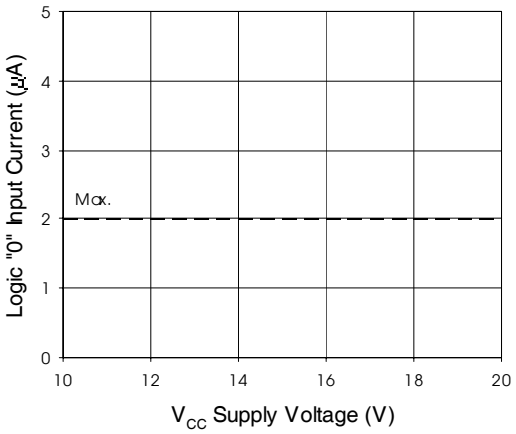


Figure 22B. Logic "0" Input Currentt vs. Supply Voltage

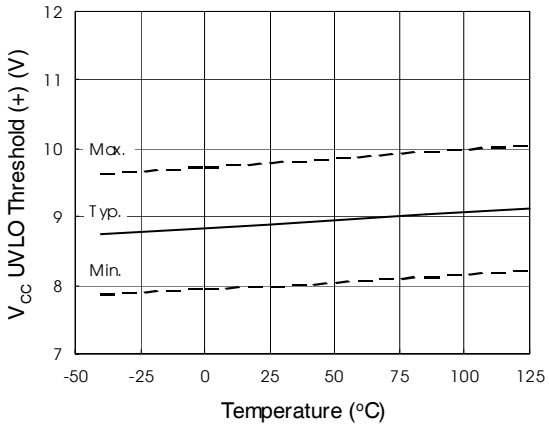


Figure 23. VCC Undervoltage Threshold (+) vs. Temperature

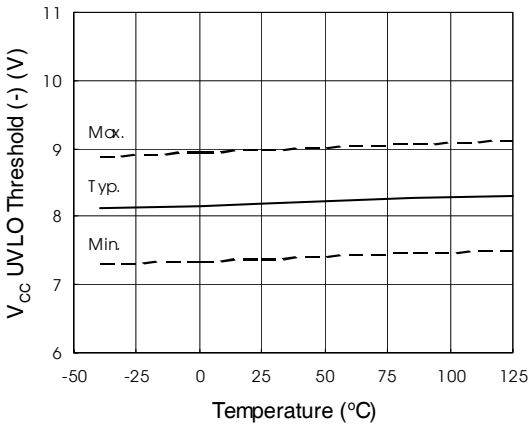


Figure 24. V_{CC} Undervoltage Threshold (-) vs. Temperature

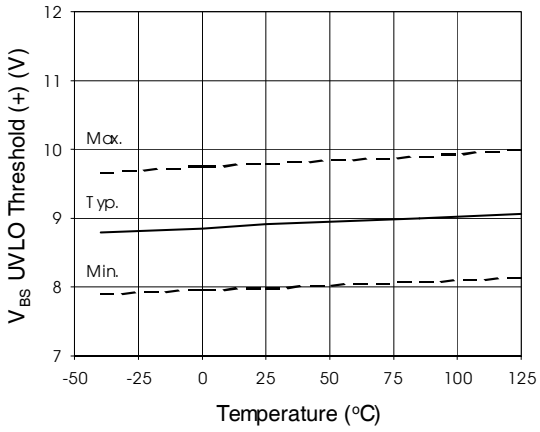


Figure 25. V_{BS} Undervoltage Threshold (+) vs. Temperature

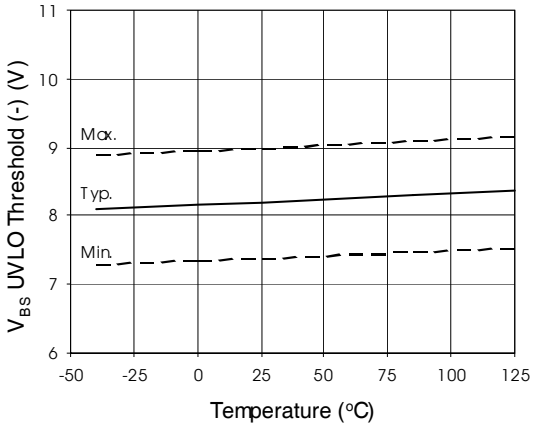


Figure 26. V_{BS} Undervoltage Threshold (-) vs. Temperature

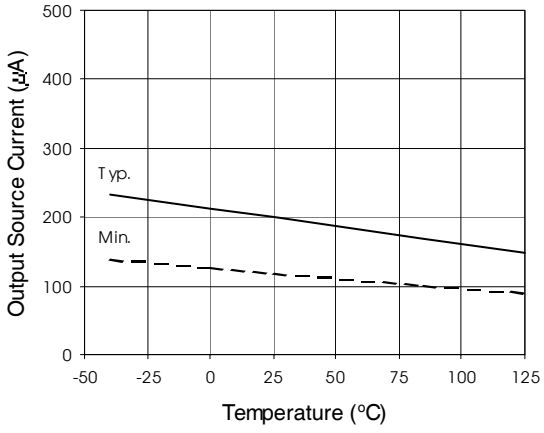


Figure 27A. Output Source Current vs. Temperature

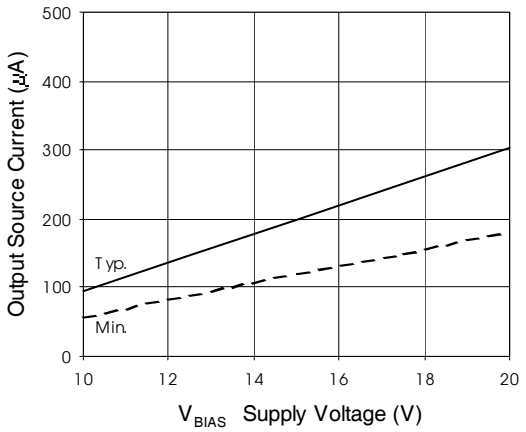


Figure 27B. Output Source Current vs. Supply Voltage

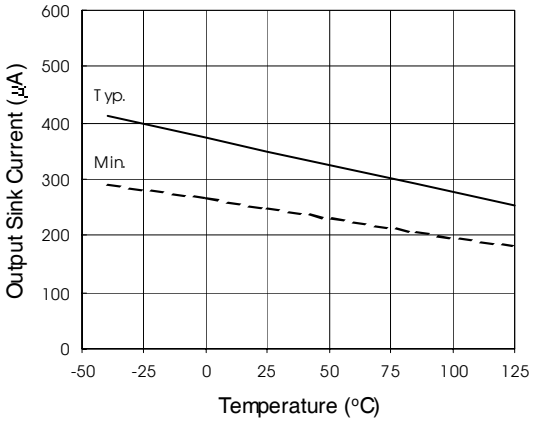


Figure 28A. Output Sink Current vs. Temperature

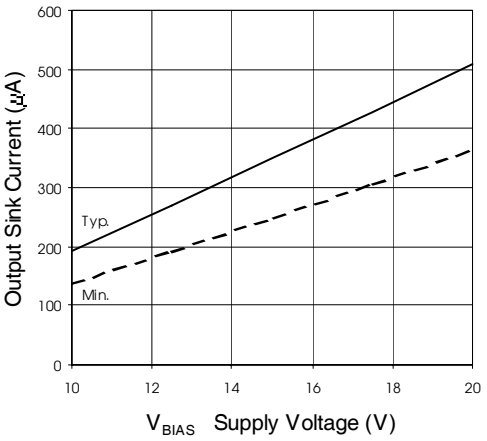


Figure 28B. Output Sink Currentt vs. Supply Voltage

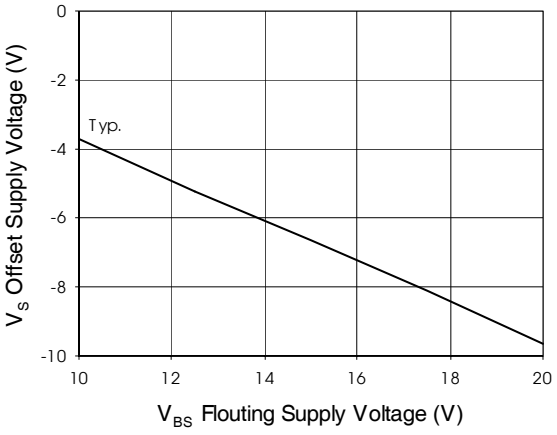


Figure 29. Maximum VS Negative Offset vs. Supply Voltage

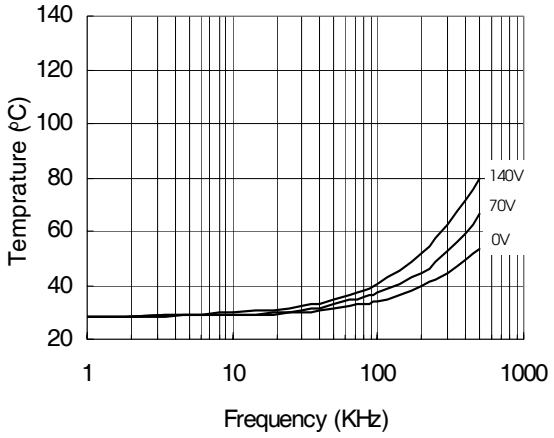


Figure 30. IR2109 vs Frequency (IRFBC20)
R_{gate} = 33Ω, V_{CC} = 15V

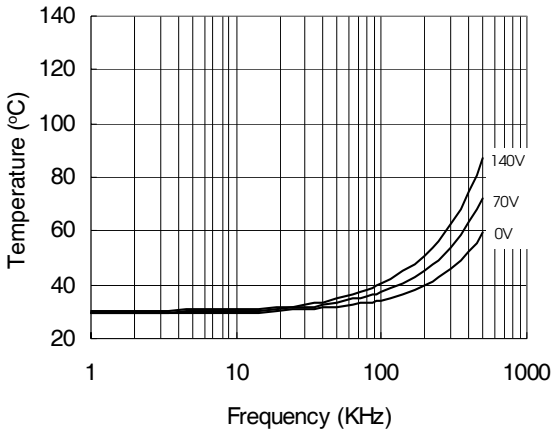


Figure 31. IR2109 vs Frequency (IRFBC30)
R_{gate} = 22Ω, V_{CC} = 15V

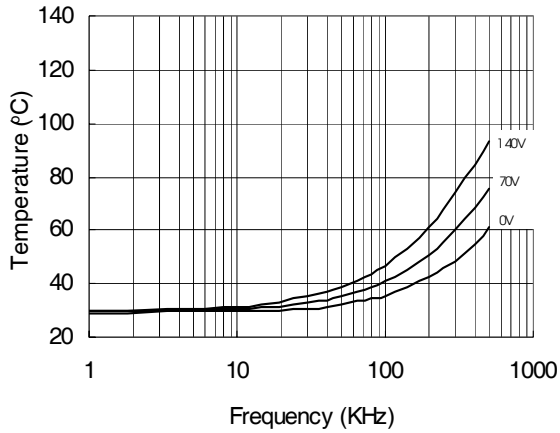


Figure 32. IR2109 vs Frequency (IRFBC40)
R_{gate} = 15Ω, V_{CC} = 15V

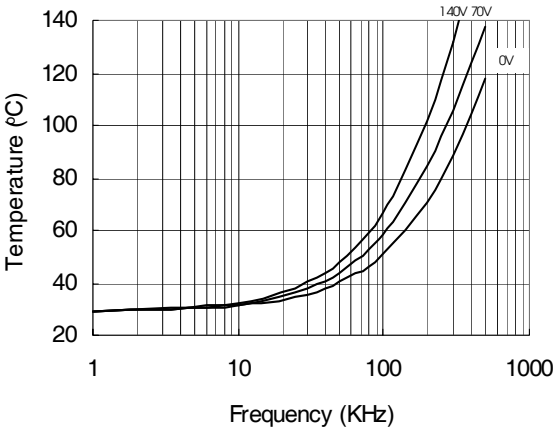


Figure 33. IR2109 vs Frequency (IRFPE50)
R_{gate} = 10Ω, V_{CC} = 15V

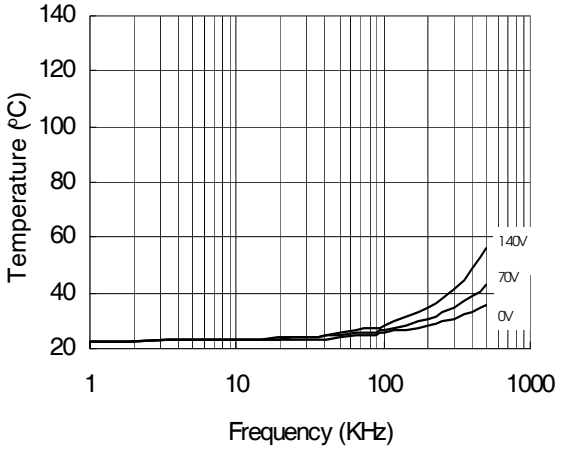


Figure 34. IR21094 vs. Frequency (IRFBC20), R_{gate}=33Ω, V_{CC}=15V

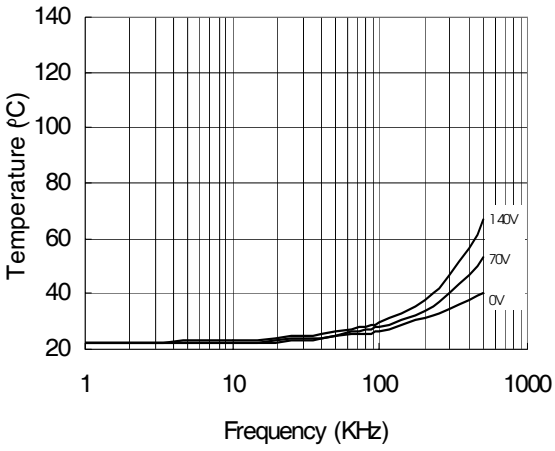


Figure 35. IR21094 vs. Frequency (IRFBC30), R_{gate}=22Ω, V_{CC}=15V

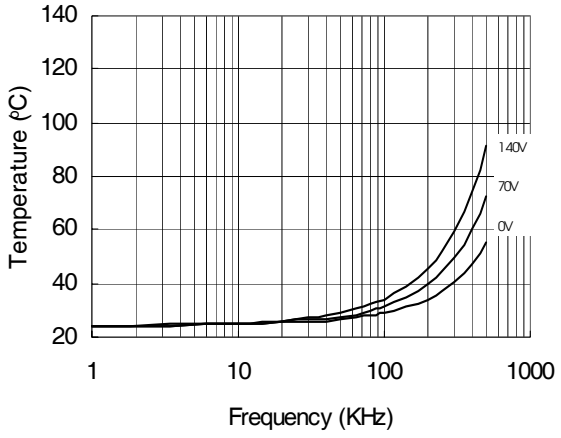


Figure 36. IR21094 vs. Frequency (IRFBC40), R_{gate}=15Ω, V_{CC}=15V

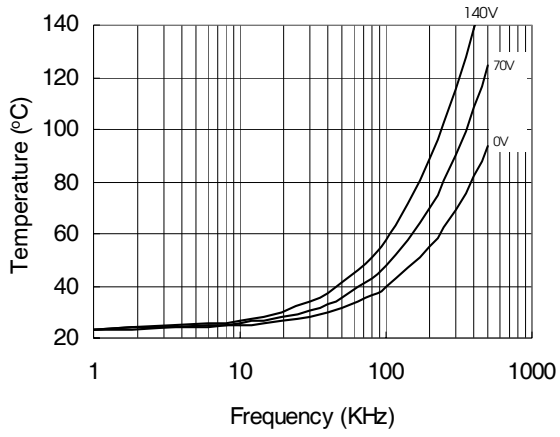


Figure 37. IR21094 vs. Frequency (IRFPE50), R_{gate}=10Ω, V_{CC}=15V

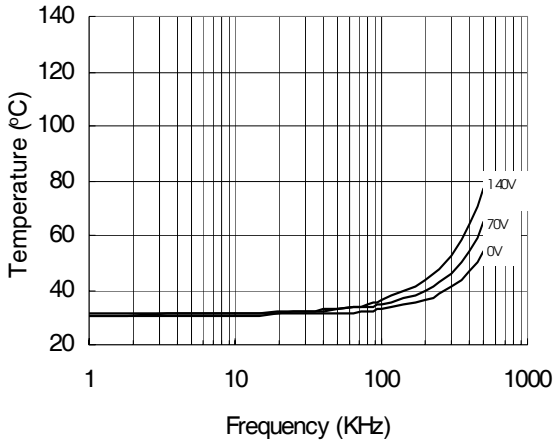


Figure 38. IR2109S vs. Frequency (IRFBC20), R_{gate}=33Ω, V_{CC}=15V

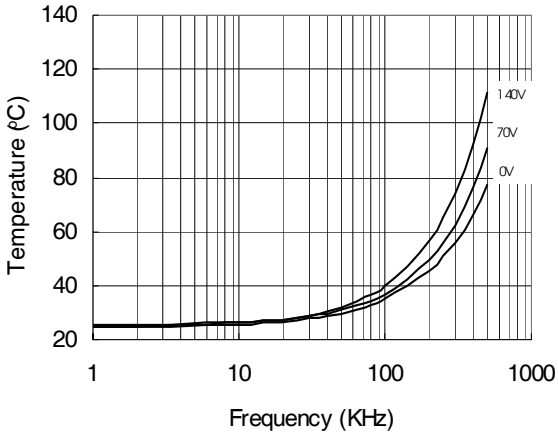


Figure 39. IR2109S vs. Frequency (IRFBC30), R_{gate}=22Ω, V_{CC}=15V

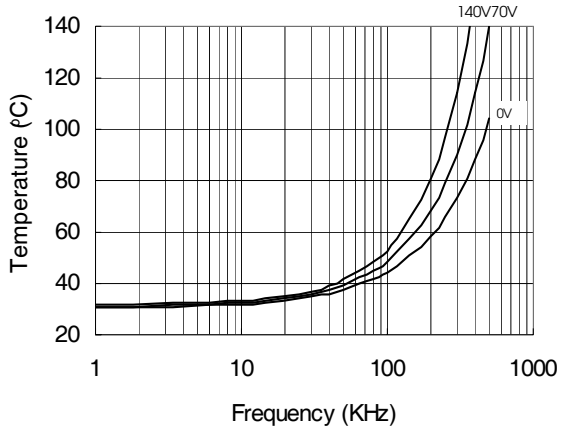


Figure 40. IR2109S vs. Frequency (IRFBC40), R_{gate}=15Ω, V_{CC}=15V

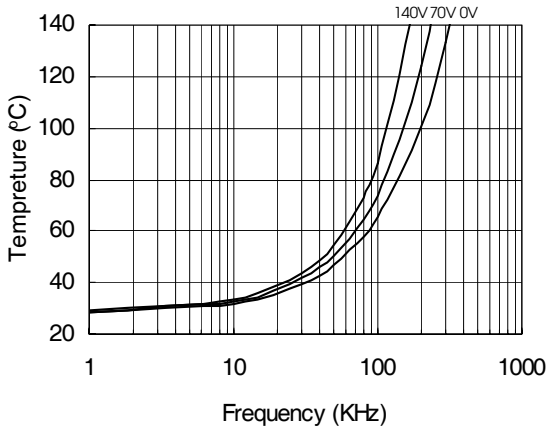


Figure 41. IR2109S vs. Frequency (IRFPE50), R_{gate}=10Ω, V_{CC}=15V

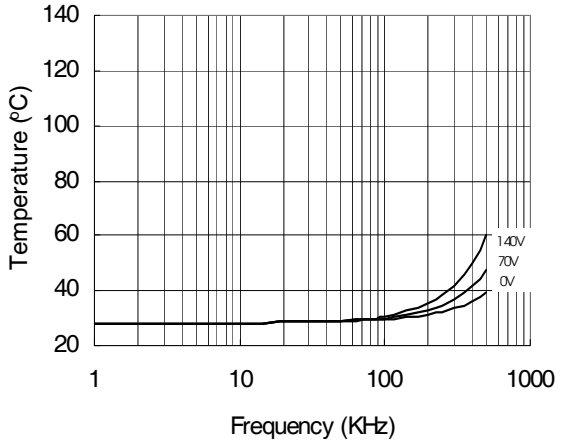


Figure 42. IR21094S vs. Frequency (IRFBC20), R_{gate}=33Ω, V_{CC}=15V

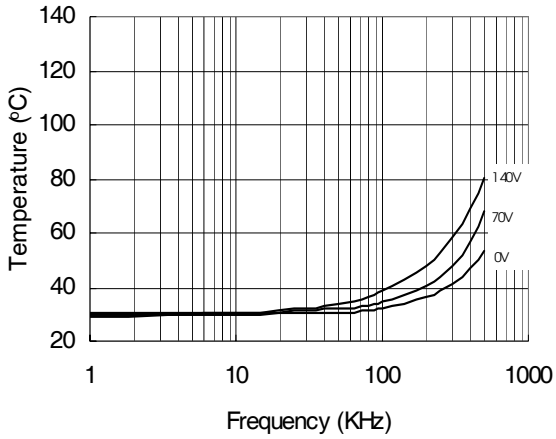


Figure 43. IR21094S vs. Frequency (IRFBC30), R_{gate}=22Ω, V_{CC}=15V

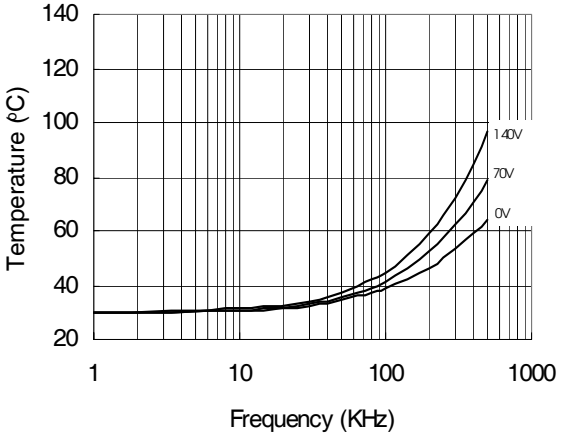


Figure 44. IR21094S vs. Frequency (IRFBC40), R_{gate}=15Ω, V_{CC}=15V

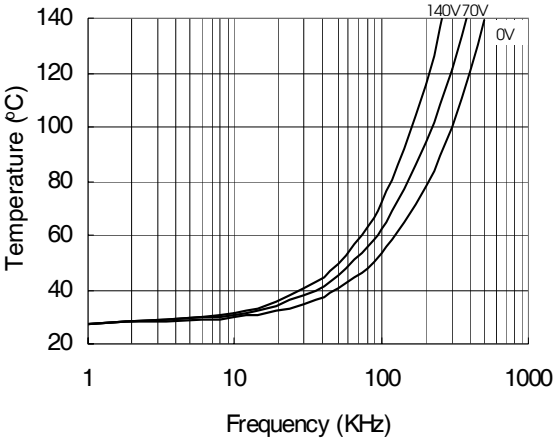
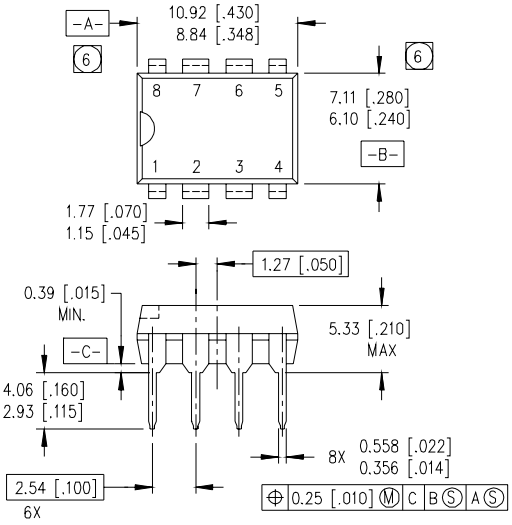
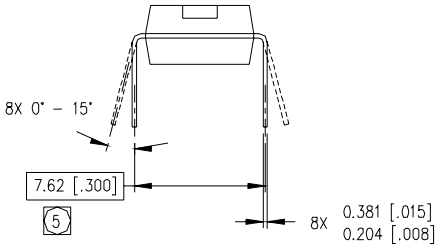


Figure 45. IR21094S vs. Frequency (IRFPE50), R_{gate}=10Ω, V_{CC}=15V

Case Outlines

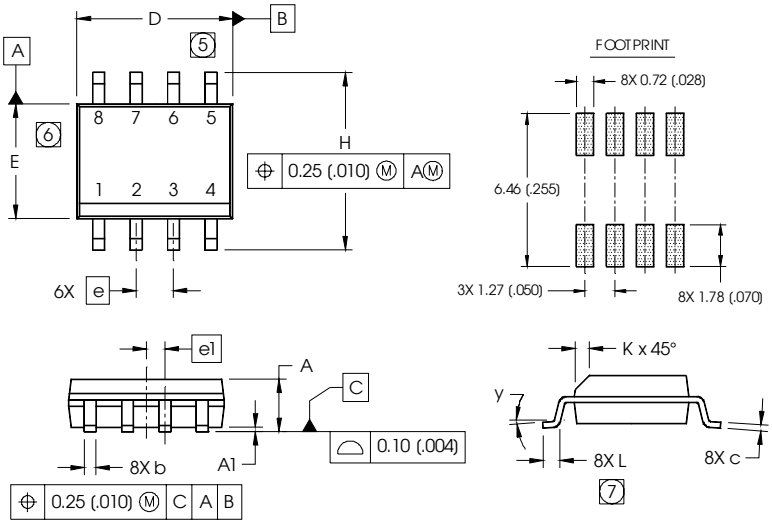


NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



8 Lead PDIP

01-6014
01-3003 01 (MS-001AB)

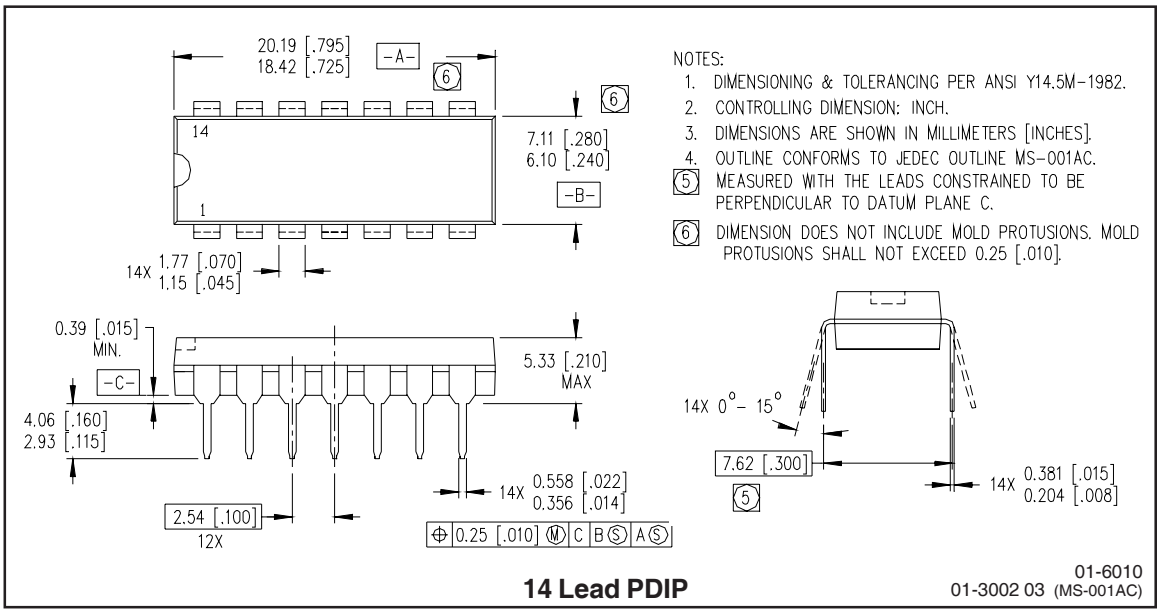


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 (.006).
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.010).
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

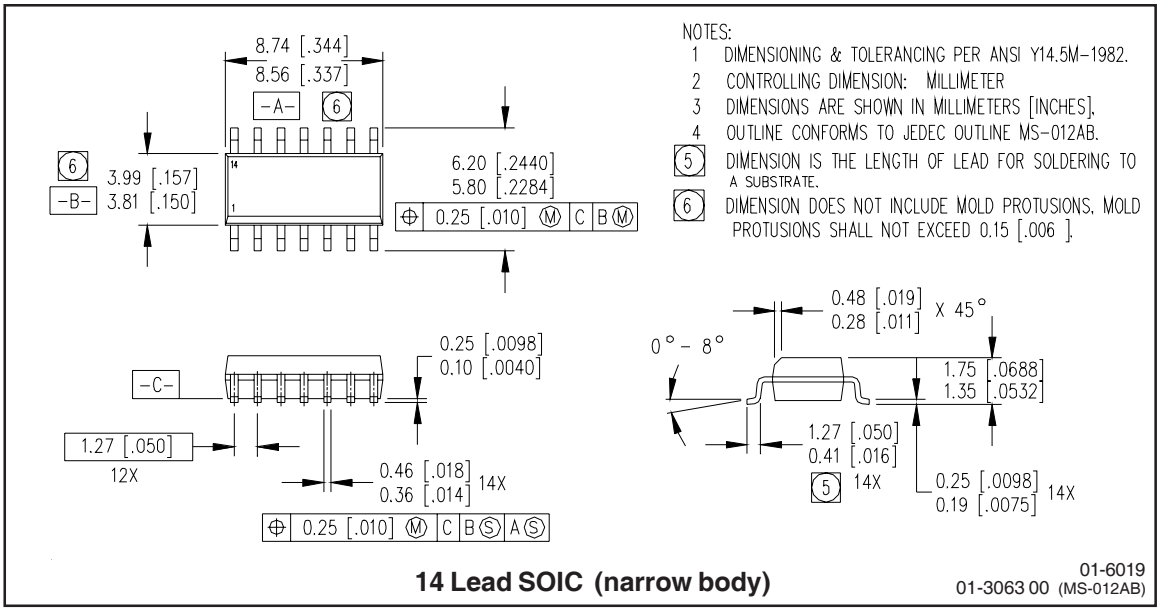
8 Lead SOIC

01-6027
01-0021 11 (MS-012AA)



14 Lead PDIP

01-6010
01-3002 03 (MS-001AC)

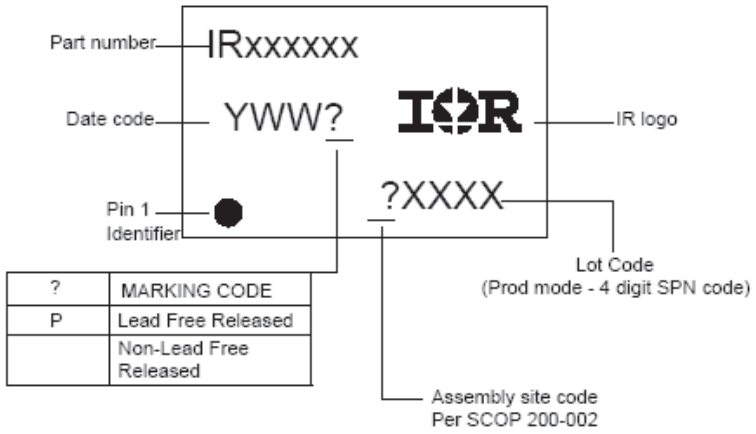


14 Lead SOIC (narrow body)

01-6019
01-3063 00 (MS-012AB)

Data and specifications subject to change without notice. 7/11/2003

LEADFREE PART MARKING INFORMATION



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

Basic Part (Non-Lead Free)

8-Lead PDIP	IR2109	order	IR2109
8-Lead SOIC	IR2109S	order	IR2109S
14-Lead PDIP	IR21094	order	IR21094
14-Lead SOIC	IR21094S	order	IR21094S

Lead-Free Part

8-Lead PDIP	IR2109	order	IR2109PbF
8-Lead SOIC	IR2109S	order	IR2109SPbF
14-Lead PDIP	IR21094	order	IR21094PbF
14-Lead SOIC	IR21094S	order	IR21094SPbF

International
IOR Rectifier

This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Website.
Data and specifications subject to change without notice.

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