XDPP1100

Digital power supply controller with PMBus interface & ARM CORTEX™ M0

Features

- Digital controller assisted high performance analog front ends and fully programmable ARM® Cortex™-M0 processor
  - 100 MHz clock, 32-bit
  - 64 kB OTP
  - 32 kB RAM
  - 80 kB ROM
  - Firmware based system configuration management and command execution
- Programmable to support one or two fully digital controlled voltage rails
- High performance, low latency digital hardware control loop
- Secondary side regulation with primary-side current signal emulation and primary voltage sensing via transformer winding
- High-speed voltage sense
  - 100 MHz 11-bit ADC with 1.25 mV/ LSB
  - Up to 2.1 V differential voltage range
  - Auto calibrated offset
  - Setpoint accuracy within +/-1% over temperature range at 1.2 V to 2.1 V
  - 200 MHz edge detection comparator
  - Low latency protection comparators for OVP and UVP
  - Up to 3 differential sense channels for output voltage and transformer rectifier voltage sensing
- High-speed current sense
  - 25 MHz 9-bit ADC with selectable gain from 100 µV/LSB and 1.45 mV/LSB
  - Support current sense of integrated power stage
  - Low latency protection comparators for OCP and positive/negative peak current limit
  - Up to 2 differential sense channels for secondary current, primary current or second-loop current sensing
- Up to 12 high resolution Digital Pulse Width Modulated (DPWM) outputs
  - 78.125 ps pulse width resolution
  - Adjustable phase shift between outputs
  - PWMx remappable
  - Cycle-by-cycle duty-cycle matching
  - Adjustable dead-time between pairs for both rising and falling edges
  - Dead-time resolution 1.25 ns
  - Up to 2 MHz switching frequency
  - Frequency/period resolution 20ns
- Configurable PWM edge alignment

Features

  - Trailing modulation (leading edge aligned)
  - Leading modulation (trailing edge aligned)
  - Triangular modulation (center aligned PWM)
- Configurable feedback control
  - Voltage mode
  - Peak current mode
  - Constant current mode
  - Constant power mode
- Configurable modulation methods
  - Pulse width modulation
  - Phase shift modulation
- Up to 16 GPIO pins
- Soft start/ Stop with and without prebias
- Feed forward compensation without primary voltage sensing
- High efficiency and light load management
  - Burst mode
  - Diode emulation
  - Low standby power
- Copper trace current sensing
  - Temperature compensation 3900 ppm/˚C
- Flux balancing
- Phase current balancing
- Feature rich fault protections
  - Programmable over and under voltage protection (OVP, UVP) thresholds and response
  - Programmable over and under current protection (OCP, UCP) thresholds and response
  - Programmable over and under temperature protection (OTP, UTP) thresholds and hysteresis
  - Programmable positive/ negative peak current limit threshold
  - Internal and external temperature sensor
  - SR negative current protection
  - Feedback open loop protection
  - Programmable blanking time
- Synchronization with external clock
- 6-channel, 9-bit, 1Msps general purpose ADC
- Communication peripherals
  - 1 MHz I^2C/PMBUS with customizable command set
  - Optional support for secondary serial port: I^2C M/S
  - Full duplex UART
- Firmware enhanced capability for application features customization
  - PMBus commands
  - GPIO functionality
  - Protection and fault detection/ monitoring
  - Control enhancement

Typical applications

- System monitoring
- Built-in watchdog
- Extreme low operation and quiescent current
- 40-pin and 24-pin VQFN packages
- Operating temperature: -40 ˚C to 125 ˚C
- Debug interface
  - GUI interface for configurable interface, control and protection features for fast and robust design-in

Typical applications

- Isolated/ non-isolated DC-DC Brick modules
- Intermediate bus converters
- Non-isolated buck-boost converters
- Optimized Power supplies for Telecom infrastructure
- Standard 48V to 12V isolated DC-DC converters
- Smart power systems for Industrial applications

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Table 1 ESD and MSL ratings

ESD	Charge Device Model	Class C3 (1000V) (per JEDEC standard JS-002)
	Human Body Model	Class 2 (2000V) (per EIA/JEDEC standard EIA/ JS-001)
Moisture Sensitivity Level		MSL2 (per IPC/JEDEC J-STD-020E)

Ordering information

Table 2 Ordering information

Base Part Number	Package Type	Standard Pack Form and Qty		Orderable Part Number
XDPP1100-Q024	VQFN (24), 4 mm x 4 mm	Tape & Reel	5000	XDPP1100Q024XUMA1
XDPP1100-Q040	VQFN (40), 6 mm x 6 mm	Tape & Reel	4000	XDPP1100Q040XUMA1

Description

The XDPP1100 device is a highly integrated and programmable digital power supply controller from Infineon Technologies. This device offers advanced power control solution for a wide variety of DC-DC power applications using isolated and non-isolated topologies. Thanks to Infineon's advanced design technology, the XDPP1100 offers industry's smallest digital power controller solution in a 4mm^2 QFN package.

The XDPP1100 device has a unique architecture that includes many optimized power-processing digital blocks to enhance the performance of Isolated DC-DC converters, reduce external components and minimize firmware development effort. For advance power conversion and monitoring, the XDPP1100 device also provides accurate telemetry and power management bus (PMBus™) interface for system communication. These advanced features make it an ideal power controller for modern high-end power systems employed in Telecom infrastructure, 48V server motherboards, datacenter and Industrial 4.0 applications.

The XDPP1100 controller is highly programmable and versatile device. Many optimized features and innovative regulation algorithms are included in its digital design to allow faster time to market, however the versatile nature of the XDPP1100 allows designers to customize and differentiate their solutions based on application needs. Infineon offers support tools such as a complementary Graphic User Interface (GUI) that allows customers to configure and monitor key parameters. In addition, developers have full control of their application and firmware development process. Infineon allows system designers to develop and compile their customized firmware in any commonly used ARM™ based development environment.

The XDPP1100 device is a dual independent loop controller, wherein the loop peripherals include the state of the art analog front-end (AFE) implementation. The AFE senses input/output voltage and current measurements by using dedicated high-speed voltage and current sense Analog-to-Digital converters (ADCs) and comparators. There are up to three high speed 100 MHz, 11-bit voltage sense ADCs that provide excellent feed-forward performance, load transient response and dynamic SR dead-time optimization. There are also up to two 9-bit high-resolution current sense ADCs with 25MHz clocking speed and support differential sensing. This device also contains a 9-bit general purpose ADC with up to six useable channels that helps implement active current sharing, primary voltage sensing and temperature sensing. The information from AFE is fed to the digital core of the XDPP1100, which generates the programmable PWM signals for regulation and control. There are up to 12 digitally modulated PWMs with 78.125 ps of pulse width resolution and a PID-based digital compensator providing an origin pole, 2 high frequency poles and 2 zeros. With a finite state machine based configurable control loop architecture, the XDPP1100 device supports various modes of operation including voltage, peak current, constant current and constant power modes.

To facilitate system level communication, this controller supports PMBus™1.3 subsets and includes other interfaces such as UART and I2C. PMBus™ command set is runtime programmable, which allows config the commands on the fly.

The XDPP1100 includes a 32-bit, 100 MHz ARM® Cortex™-M0 RISC microcontroller sub-system that can be used for enhanced control, real-time monitoring, configuration of peripheral, and managing communications. It also allows firmware-based customization and implementation of housekeeping functions such as sequencing, optimization and interfacing. Infineon pre-programmed many basic and advance power control functions in the device ROM. Additional programs can be stored and executed out of the nonvolatile memory as well as on-chip RAM and OTP.

The XDPP1100 device has many pre-programmed power management peripherals including:

- Light load burst mode
- Synchronous rectification
- Input voltage feed forward
- Temperature compensated copper trace current sensing using dedicated current sense ADC

Description

- Diode emulation
- Flux balancing
- Soft start with pre-bias
- Fault management
- Secondary side input voltage sensing
- A revolutionary transient protection scheme called Fast Transient Response (FTR)

The device ROM contains regulation algorithms patented by Infineon that contribute to enhancing converter efficiency, and power density for space constrained power modules. Sophisticated fault management and protection features improve system health and lifetime. The XDPP1100 device supports many commonly used DC-DC topologies such as, hard-switched full bridge and half bridge, phase shifted full bridge, active clamp forward, full-bridge and half-bridge current doubler rectifier, interleaved active clamp forward, interleaved half bridge, and interleaved full-bridge. Dual-rail version also supports pre-buck or post-buck configuration.

This unique combination of high performance analog front end, state machine based digital control loop and a microcontroller integrated in a single chip makes XDPP1100 a highly integrated, programmable and fastest time to market technology for power modules development.

The XDPP1100 is offered in two packages.

Table 3 XDPP1100 device packages

Part number	Package type	Size	Application
XDPP1100-Q024	VQFN (24)	4.00 mm × 4.00 mm	Single-rail control with 6 PWM outputs
XDPP1100-Q040	VQFN (40)	6.00 mm × 6.00 mm	Dual-rail control with 12 PWM outputs

Figure 1 shows a typical application implementation of the XDPP1100 device in an isolated full-bridge DC to DC step down converter:

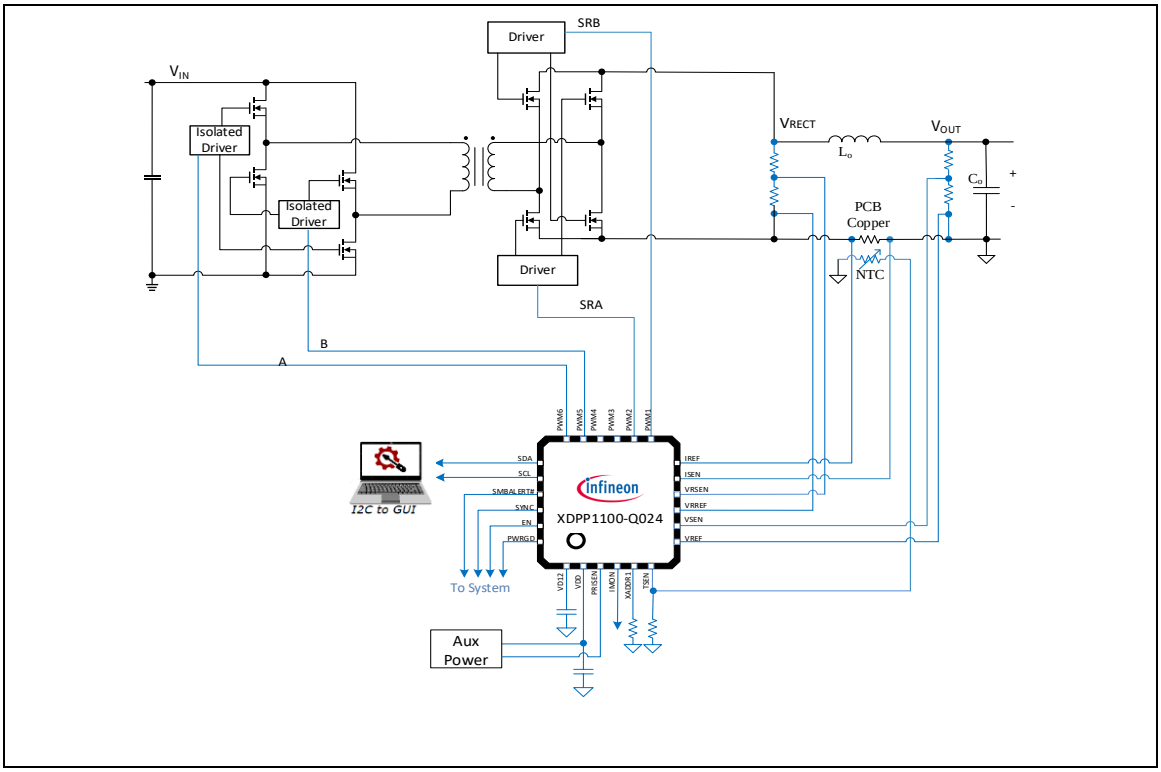

Figure 1 Typical application diagram

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1 Functional Block Diagram

Figure 2 shows a functional block diagram of the XDPP1100 device architecture.

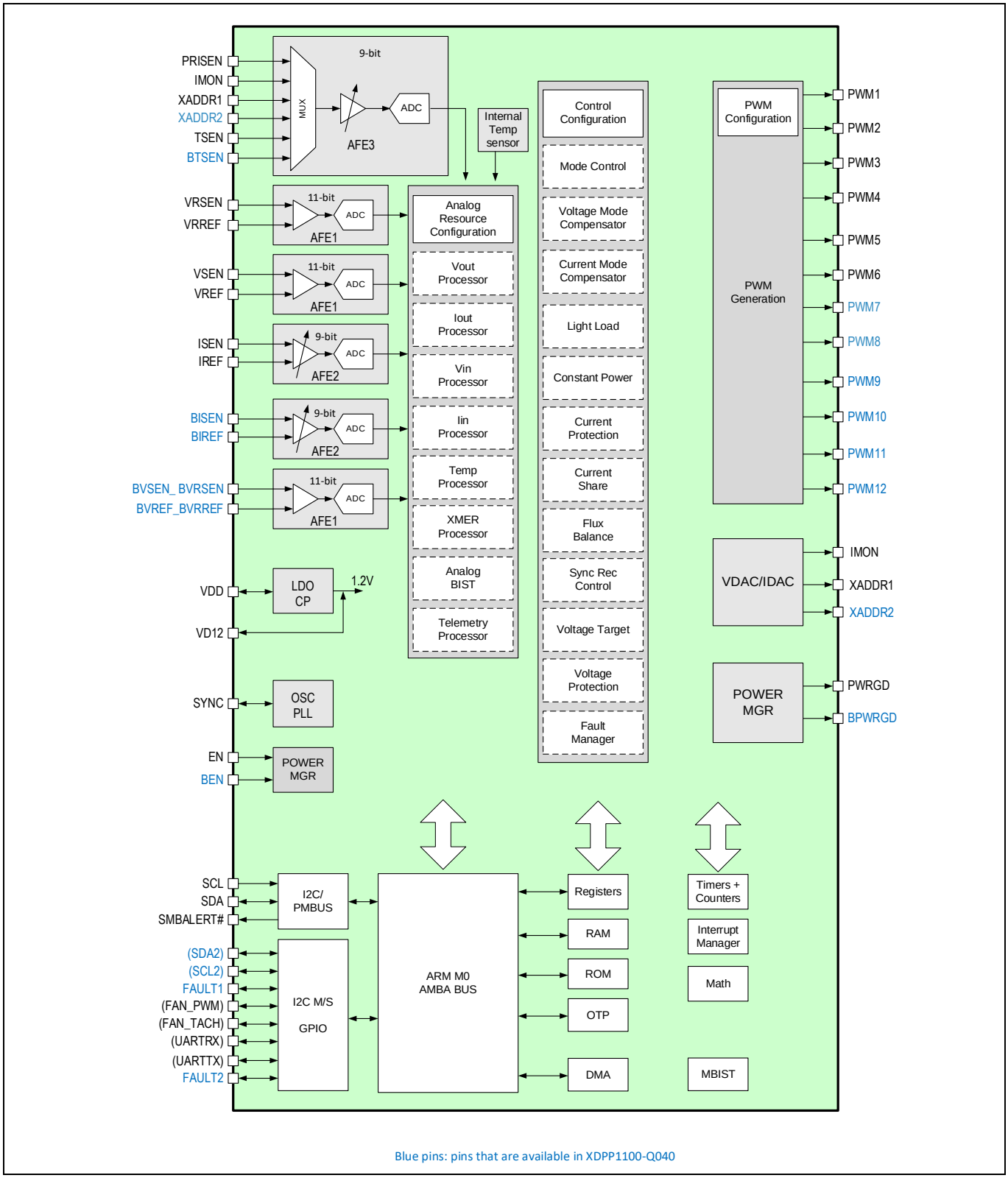

Figure 2 Block diagram

2 Product Selection Matrix

Table 4 Product selection table

FEATURE	XDPP1100-Q040	XDPP1100-Q024
ARM M0 core processor	100 MHz	100 MHz
High resolution DPWM outputs (78.125ps resolution)	12	6
Number of high-speed independent feedback rails	2	1
Number of voltage sense ADC	3	2
Number of current sense ADC	2	1
9-bit, 1Msps, general purpose ADC channels	6	4
OTP	64 kB	64 kB
RAM	32 kB	32 kB
ROM	80 kB	80 kB
DPWM switching frequency	Up to 2 MHz	Up to 2 MHz
Secondary serial bus (I^2C M/S)	Yes	No
UART	Yes	Yes
PMBus	Yes	Yes
Watchdog	Yes	Yes
On chip oscillator	Yes	Yes
Sync in and sync out functions	Yes	Yes
Temperature sense inputs	2	1
Enable inputs	2	1
Power good outputs	2	1
Total GPIO (General purpose I/O pins)	16	11
Package offering	VQFN-40 (6x6 mm^2)	VQFN-24 (4x4 mm^2)

3 Terminal Configuration and Functions

3.1 XDPP1100-Q040 Package

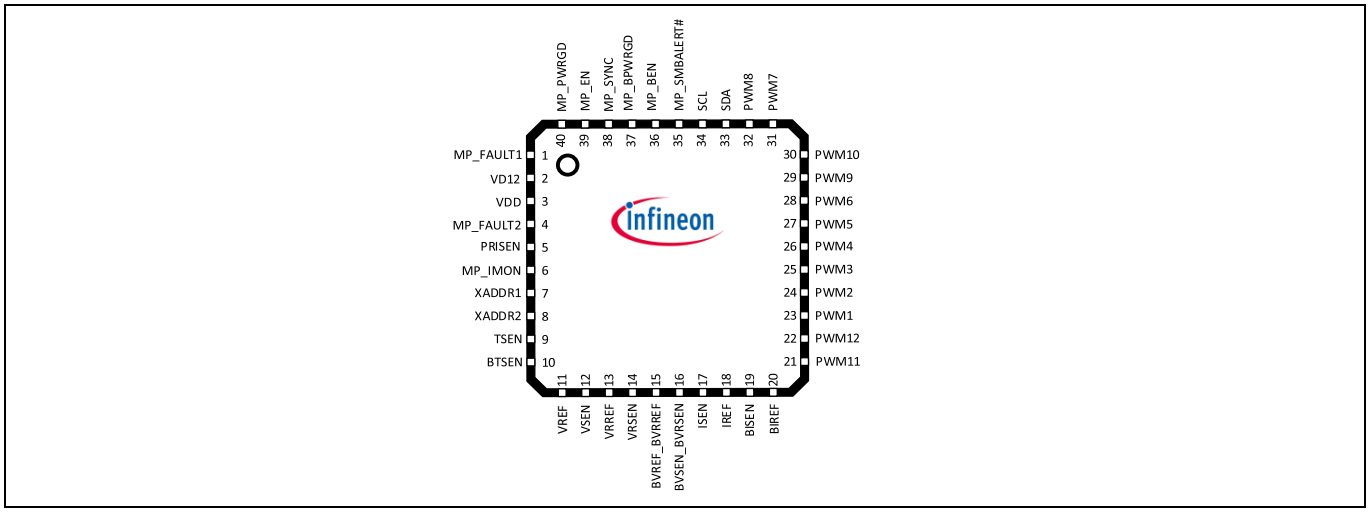

Figure 3 XDPP1100-Q040 pin assignment

Table 5 XDPP1100-Q040 pin definition

Pin No.	Name	Primary Assignment	Alternate assignment	Configurable GPIO?
1	MP_FAULT1	Fault 1	SYNC/ FAN2_PWM/ SDA2/ UARTRX	Yes
2	VD12	1.2V supply bypass		
3	VDD	3.3V main supply input		
4	MP_FAULT2	Fault 2	SYNC/FAN2_TACH/ SCL2/ UARTTX	Yes
5	PRISEN	Primary voltage sensing input	GPA1	
6	MP_IMON	Current monitor output	GPA2/ SYNC/ FAN1_TACH	Yes
7	XADDR1	Address 1	GPA3	
8	XADDR2	Address 2	GPA4	
9	TSEN	Temperature sensing input of the first rail	GPA5	
10	BTSEN	Temperature sensing input of the second rail	GPA6	
11	VREF	Differential voltage sensing of the first rail, negative input		
12	VSEN	Differential voltage sensing of the first rail, positive input		
13	VRREF	Transformer winding voltage sense, negative input		

Pin No.	Name	Primary Assignment	Alternate assignment	Configurable GPIO?
14	VRSEN	Transformer winding voltage sense or primary input voltage sense, positive input		
15	BVREF_BVRREF	Differential voltage sensing of the second rail, negative input	Transformer winding voltage sense return of the second rail	
16	BVSEN_BVRSEN	Differential voltage sensing of the second rail, positive input	Transformer winding voltage sense of the second rail	
17	ISEN	Differential current sensing of the first rail, positive input		
18	IREF	Differential current sensing of the first rail, negative input		
19	BISEN	Differential current sensing of the second rail, positive input		
20	BIREF	Differential current sensing of the second rail, negative input		
21	PWM11	PWM11 output	SYNC/ FAN1_PWM	Yes
22	PWM12	PWM12 output	SYNC/ FAN1_TACH	Yes
23	PWM1	PWM1 output	SYNC	Yes
24	PWM2	PWM2 output	SYNC	Yes
25	PWM3	PWM3 output	SYNC	Yes
26	PWM4	PWM4 output	SYNC	Yes
27	PWM5	PWM5 output	SYNC/ UARTRX	Yes
28	PWM6	PWM6 output	SYNC/ UARTTX	Yes
29	PWM9	PWM9 output	SYNC	Yes
30	PWM10	PWM10 output	SYNC	Yes
31	PWM7	PWM7 output	SYNC/ FAN2_PWM	Yes
32	PWM8	PWM8 output	SYNC/ FAN2_TACH	Yes
33	SDA	I^2C serial data line		
34	SCL	I^2C serial clock line		
35	MP_SMBALERT#	PMBus alert	SYNC	Yes
36	MP_BEN	Enable input of the second rail	SYNC/ SDA2/ UARTRX	Yes
37	MP_BPWRGD	Power good output of the second rail	SYNC / SCL2/ UARTTX	Yes
38	MP_SYNC	Synchronize pin	FAN1_PWM	Yes
39	MP_EN	Enable input of the first rail	SYNC	Yes
40	MP_PWRGD	Power good output of the first rail	SYNC	Yes
	GND	Ground pin		

Note: GND is the metal pad under the chip

3.2 XDPP1100-Q024 Package

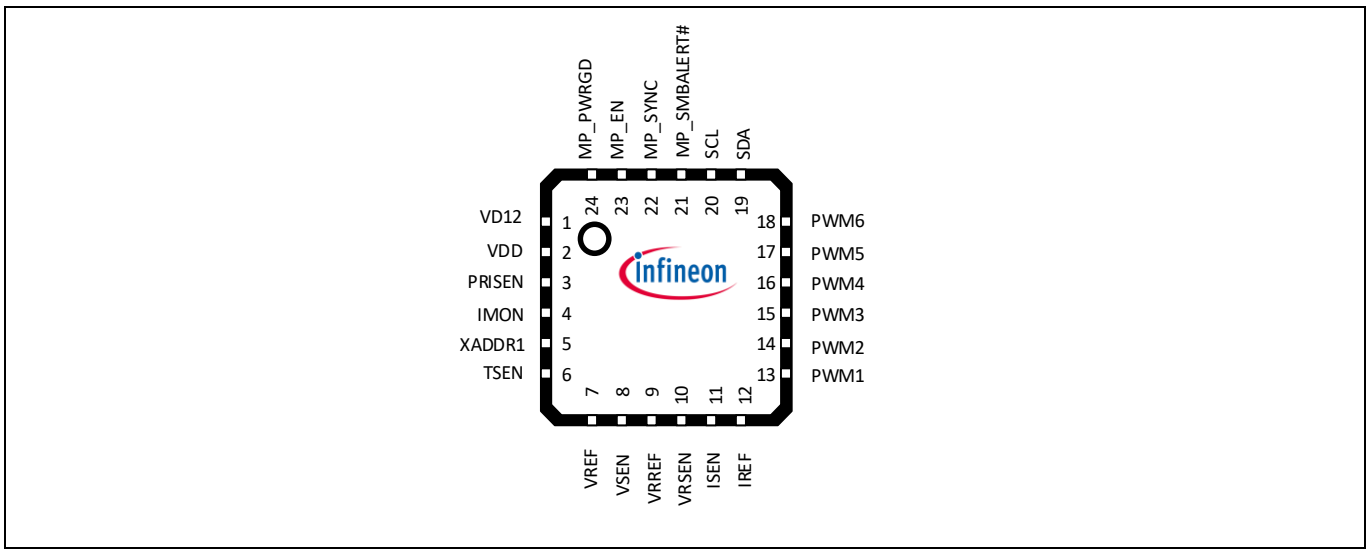

Figure 4 XDPP1100-Q024 pin assignment

Table 6 XDPP1100-Q024 pin definition

Pin No.	Name	Primary Assignment	Alternate assignment	Configurable GPIO?
1	VD12	1.2V supply bypass		
2	VDD	3.3V main supply input		
3	PRISEN	Primary voltage sensing input	GPA1	
4	MP_IMON	Output current monitor	GPA2/ SYNC/ FAN1_TACH	Yes
5	XADDR1	Address 1	GPA3	
6	TSEN	Temperature sensing input	GPA4	
7	VREF	Differential voltage sensing, negative input		
8	VSEN	Differential voltage sensing, positive input		
9	VRREF	Transformer winding voltage sense, negative input		
10	VRSEN	Transformer winding voltage sense or primary input voltage sense, positive input		
11	ISEN	Differential current sensing, positive input		
12	IREF	Differential current sensing, negative input		
13	PWM1	PWM1 output	SYNC	Yes
14	PWM2	PWM2 output	SYNC	Yes
15	PWM3	PWM3 output	SYNC	Yes
16	PWM4	PWM4 output	SYNC	Yes

Pin No.	Name	Primary Assignment	Alternate assignment	Configurable GPIO?
17	PWM5	PWM5 output	SYNC/ UARTRX	Yes
18	PWM6	PWM6 output	SYNC/ UARTTX	Yes
19	SDA	I^2C serial data line		
20	SCL	I^2C serial clock line		
21	MP_SMBALERT#	PMBus alert	SYNC	Yes
22	MP_SYNC	Synchronize pin	FAN1_PWM	Yes
23	MP_EN	Enable input	SYNC	Yes
24	MP_PWRGD	Power good output	SYNC	Yes
	GND	Ground pin		

Note:

1. *GND is the metal pad under the chip*
2. *NC: no connection pin*
3. *SDA and SCL are Open Drain I/O pins*
4. *All digital GPIO pins are 3.3V level CMOS, the outputs are programmable to be CMOS or Open Drain*

4 Specifications

4.1 Absolute Maximum Ratings

Subjecting the controller to stresses above those listed in *Table 7 Absolute Maximum Rating* may cause permanent damage to the device. These are absolute stress ratings only and functional operation of the device is not implied or recommended at these or any other conditions in excess of those given in the *Recommended Operating Conditions* sections of this specification. Exposure to absolute maximum ratings for extended periods may adversely affect the operation and reliability of the device.

Table 7 Absolute maximum rating

Parameters	Symbol	Min.	Max.	Units	Remarks
VDD Supply Voltage	V_{DD}	-0.3	4	V	Instantaneous voltage, see Note
			3.7	V	Continuous voltage
VSEN, VRSEN, BVSEN_BVRSEN		-0.3	3.7*	V	*The lesser of 3.7V or VDD+0.2V
VREF, VRREF, BVREF_BVRREF		-0.3	0.5	V	
ISEN, BISEN, IREF, BIREF		-0.3	3.7*	V	*The lesser of 3.7V or VDD+0.2V
		-0.3	2.0	V	IPS mode
1.2V Supply	V_{D12}	-1	1	mA	
All other pins		-0.3	3.7*	V	*The lesser of 3.7V or VDD+0.2V
Operating Junction Temperature	T_J	-40	150	°C	
Storage Temperature	T_S	-65	150	°C	

Note: The absolute maximum VDD supply voltage is 4.0V with the conditions that the junction temperature range is maintained between -40˚C < T_J < +125˚C and the product is not operated at the absolute maximum VDD supply voltage for more than 24 hours cumulatively over the lifetime of the product.

4.2 Thermal Characteristics

Table 8 Thermal Impedance

Parameters	Symbol	Value	Units	Remarks
Thermal Resistance, Junction to Ambient, at 0 lfm	$R_{\theta JA}$	30.3	°C/W	QFN-40 6x6
		53.5		QFN-24 4x4
Thermal Resistance, Junction to Ambient, at 200 lfm	$R_{\theta JA}$	26.2		QFN-40 6x6
		36.9		QFN-24 4x4
Thermal Resistance, Junction to Ambient, at 500 lfm	$R_{\theta JA}$	23.4		QFN-40 6x6
		30.3		QFN-24 4x4
Thermal Resistance, Junction to Case (top)	$R_{\theta JC}$	2.8		QFN-40 6x6
		3.7		QFN-24 4x4

4.3 Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

Table 9 Recommended operating conditions

Parameters	Symbol	Min.	Nom.	Max.	Units	Remarks
Supply Voltage	V_{DD}	3	3.3	3.6	V	
Junction Temperature	T_J	-40	25	125	°C	

4.4 Electrical Characteristics

VDD=3.0 V to 3.6 V, 1 µF capacitor from VD12 to GND, T_J = -40 °C to 125 °C unless otherwise specified.

Table 10 Electrical characteristics of power supply section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Supply current	I_{DD0}		11	16.5	mA	Both loops in off mode
Supply current	I_{DD1}		21			Single-loop operation, 4 PWMs switching at 250 kHz without any load
Supply current	I_{DD2}		24			Dual-loop operation, all 12 PWMs switching at 250 kHz without any load
VDD UVLO threshold	$V_{DD\ rising}$		2.78	2.95	V	
	$V_{DD\ falling}$	2.5	2.7			
VDD UVLO hysteresis			80		mV	

Table 11 Voltage ADC AFE1 section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Input differential voltage range		0.25		2.1	V	Voltage below 0.5 V is not production tested
Error voltage digital resolution			1.25		mV	
Input impedance	R_{EA}		> 1		MΩ	
Sample rate			100		MHz	
VS ADC Accuracy (Note 5)		-1	±0.75	1	%	Setpoint 1.2 V to 2.1 V, -40 °C <T_A < 125 °C, 3.0 V < V_{DD} < 3.6 V, Typ = 3 σ
		-1.4	±1.0	1.4	%	Setpoint 1.0 V, -40 °C <T_A < 125 °C, 3.0 V < V_{DD} < 3.6 V, Typ = 3 σ
		-1.8	±1.2	1.8	%	Setpoint 0.8 V, -40 °C <T_A < 125 °C, 3.0 V < V_{DD} < 3.6 V, Typ = 3 σ
			±0.45		%	Setpoint 1.2 V to 2.1 V, T_A = 25 °C, V_{DD} = 3.3 V, Typ = 3 σ

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
			±0.65		%	Setpoint 1.0 V, T_A = 25 °C, V_{DD} = 3.3 V, Typ = 3 σ
			±0.9		%	Setpoint 0.8 V, T_A = 25 °C, V_{DD} = 3.3 V, Typ = 3 σ
			±10.5		mV	Setpoint 0.25 V to 0.5 V, -40 °C <T_A < 125 °C, 3.0 V < V_{DD} < 3.6 V, Typ = 3 σ

Table 12 Current ADC AFE2 section (high gain)

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Input differential voltage range		-22		22	mV	Voltage below -3 mV is not production tested
Error voltage digital resolution			100		µV	
Input impedance	R_{EA}		> 1		MΩ	
IS ADC Offset	V_{OFFSET}	-4		4	LSB	
Sample rate			25		MHz	
IS ADC accuracy		-4	±2.7	4	%	11 mV differential input, Typ = 3 σ
		-3.5	±2.4	3.5	%	22 mV differential input, Typ = 3 σ

Table 13 Current ADC AFE2 section (low gain)

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Input differential voltage range		-280		395	mV	Voltage below -50 mV is not production tested
Error voltage digital resolution			1.45		mV	
Input impedance	R_{EA}		> 1		MΩ	
IS ADC Offset	V_{OFFSET}	-2.5		2.5	LSB	
Sample rate			25		MHz	
IS ADC accuracy		-3	±1.5	3	%	200 mV differential input, Typ = 3 σ
		-2	±1.2	2	%	395 mV differential input, Typ = 3 σ

Table 14 Current ADC AFE2 section (IPS mode)

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Input common voltage range		1.11		1.3	V	
Input differential voltage range		-200		425	mV	Voltage below -50 mV is not production tested
Error voltage digital resolution			1.45		mV	
Input impedance	R_{EA}		> 1		MΩ	
IS ADC Offset	V_{OFFSET}	-2.5		2.5	LSB	
Sample rate			25		MHz	

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
IS ADC accuracy		-3	±1.4	3	%	200 mV differential input, Typ = 3 σ
		-1.7	±1.1	1.7	%	395 mV differential input, Typ = 3 σ

Table 15 General ADC AFE3 section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Input differential voltage range			0 – 1.2		V	
Error voltage digital resolution			2.344		mV	
Input impedance	R_{EA}		> 1		MΩ	
TS ADC offset error	V_{OFFSET}	-2		2	LSB	
Sample rate			1		MHz	
TS ADC Gain error		-1		1	%	

Table 16 IMON DAC section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Output current range			0-640		µA	
Output current resolution			10		µA	
TSIDAC accuracy		-3		3	%	Tested at 100 µA

Table 17 XADDR1, XADDR2 pins

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Current measurement			0-640		µA	

Table 18 GPIO Inputs/Outputs (FAULT1/2, IMON, PWM1-5, PWM7-10, PWM12, EN, BEN, SYNC)

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Low-level output voltage	V_{OL}			0.4	V	I_{OL} = 5 mA
High-level output voltage	V_{OH}	2.6				I_{OH} = -5 mA
Low-level input voltage	V_{IL}			1.0		
High-level input voltage	V_{IH}	2.1				
Leakage current	I_{OZ}	-1		1	µA	

Table 19 GPIO Inputs/Outputs (PWRGD, BPWRGD, PWM6, PWM11)

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Low-level output voltage	V_{OL}			0.4	V	I_{OL} = 5 mA
High-level output voltage	V_{OH}	2.6				I_{OH} = -5 mA
Low-level input voltage	V_{IL}			0.3 VDD		
High-level input voltage	V_{IH}	0.7 VDD				
Leakage current	I_{OZ}	-1		1	µA	

Table 20 SDA, SCL, SMBALERT pins

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Output low voltage	V_{OL}			0.4	V	IOL = 20 mA
Low-level input voltage	V_{IL}			1.0		Configured as 3.3V buffer

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
High-level input voltage	V_{IH}	2.1				
Low-level input voltage	V_{IL}			0.6		
High-level input voltage	V_{IH}	1.35				Configured as 1.8V buffer
Leakage current	I_{OZ}	-1		1	µA	
Pin capacitance	C_{PIN}		1.5		pF	

Table 21 System performance

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Processor master clock			100		MHz	
Internal oscillator frequency		190	200	210	MHz	
Switching Frequency	Fsw		100-2000		kHz	
Switching Period time resolution			20		ns	
Sync Frequency range			+/-6.25		%	

Table 22 Temperature sensor

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Input Voltage Range			0 – 1.2		V	ATSEN, BTSEN
Bias Current			100		µA	Source current to measure external NTC or PTC resistor, can be disabled
Accuracy of internal temperature sensor			±5		˚C	

Note:

5. The VS ADC accuracy applies to the VSEN and BVSEN_BVRSEN voltage sense

5 Function Overview

5.1 Introduction

Isolated DC-DC power converters are defined as power converters that use a transformer to provide electrical isolation between the input and output terminals of the converter. The controller can either be placed on the primary side of the transformer with direct connection to the input voltage, or on the secondary-side of the transformer. In the case of primary-side control, analog controllers are often used for their low cost, simple yet effective protection features, voltage feed-forward capability, and proven reliability through decades of use in the industry.

However, digital power conversion methods have been gaining popularity in major applications such as Telecom and computing in recent years. These applications require system level communication (i.e. PMBus) and accurate telemetry, which makes digital controller-based converters more attractive. Digital power controllers are typically implemented on the secondary side of the transformer to reduce isolation circuitry. Unlike analog PWM controllers, a digital controller provides digital PWMs and requires external gate drivers for power MOSFETs and auxiliary power supply.

The XDPP1100 is a flexible, feature-rich digital secondary side controller, optimized for isolated dc-to-dc applications and facilitates designs with minimum component count and maximizes system flexibility with a microcontroller based sub-system. The XDPP1100 is designed to enable flexibility and provide excellent digital control for both, transformer based isolated DC to DC converters and non-isolated topologies. It works for all the major fixed frequency topologies: pulse width modulation (PWM) half-bridge (HB), PWM full-bridge (FB), phase-shift full-bridge (PSFB), active clamp forward (ACF), open loop fix-frequency resonant half-bridge or full-bridge (FF LLC), non-isolated Buck, Boost and Buck-boost. The XDPP1100 supports interleaved operation of any of the topologies mentioned. The dual-loop version XDPP1100-Q040 also offers post-buck or post–boost regulation. The control loop PID digital filter and compensation terms are integrated and can be programmed over the I^2C port. The industry-standard PMBus interface also provides access to the many monitoring and system control functions. The integrated ARM COTEX™ M0 microcontroller and built-in non-volatile memory provide extensive programming and customization of functions such as, the integrated loop filter, PWM signal timing, non-linear transient suppression schemes, soft start timing and sequencing. The XDPP1100 requires a 3.3 V auxiliary supply for operation.

5.1.1 ARM® Cortex™ –M0 core

The XDPP1100 chip embeds the smallest ARM processor – the ARM® Cortex®-M0 processor. It is a cost-competitive, high performance 32-bit processor with exceptionally low gate count, minimal power requirements, and reduced code footprint. It is an optimized interrupt controller, allows to be used in hard real-time applications. The XDPP1100 ARM® Cortex® -M0 processor clock frequency is 100 MHz.

5.1.2 Memories

The XDPP1100 has 80 kB Boot ROM that contains the initial firmware startup routines for PMBUS communication. This boot ROM is executed after power-up-reset checks. The XDPP1100 also supports customization of the boot program by allowing an alternative boot routine to be executed from the one-time programmable (OTP) nonvolatile memory (NVM). Control registers can be reprogrammed in the field via the serial communication (I^2C) bus and stored into the OTP NVM. For run time data storage and scratchpad memory, a 32 kB RAM is available.

5.1.3 Communication ports

The device provides a primary I²C, a secondary I²C, and UART communication ports.

5.1.3.1 I²C/PMBus

All operating parameters in the device are configurable via the primary I²C serial interface (SDA, SCL). The secondary I²C offers additional communication port, for example to access external memory. The SDA, SCL support two logic levels, 3.3 V and 1.8 V. The device supports all three speeds I²C: standard (100 kHz), fast (400 kHz) and fast mode plus (1 MHz) operating frequency. The speed of the I²C is configurable through the Graphic User Interface (GUI).

The XDPP1100 device is compliant to PMBus™ Power System Management Protocol Specification, revision 1.3.1. The I²C/PMBus interface allows user to configure the device as well as monitoring fault status, voltage, current, power, and temperature telemetry.

5.1.3.2 UART

A full duplex Universal Asynchronous Receiver/Transmitter (UART) interface is included in the device. The baud rate, word size, buffer depth, IrDA, modem operation is configurable through registers. A loop back feature can also be setup for firmware verification.

The UARTTX and UARTRX pin sets can be configured using assigned GPIO pins. See Table 26 for the list of GPIO pins and the pre-defined functions of each of them.

5.1.3.3 Address offset

The XDPP1100-Q040 uses two pins, XADDR1 and XADDR2, for I²C/PMBus address decoding. The XDPP1100-Q024 has one address pin XADDR1, and it allows to modify the function of IMON pin to do address decoding via FW patch when two XADDR pins are desired. FW patch examples are available on Infineon website.

The base address of I²C and PMBus should be configured by MFR PMBus command 0xC9 FW_CONFIG_PMBUS. The address offset of the I²C and PMBus can be configured either by the address offset fields of 0xC9 or can be decoded via the XADDR1 and XADDR2 pins by connecting resistors from the XADDR1 or XADDR2 to ground. To use resistor address offset, the corresponding bit must be enabled by FW_CONFIG_PMBUS. The XDPP1100 measures XADDR resistor offset during initialization state, and doesn't support on the fly modification. The configuration of FW_CONFIG_PMBUS must be stored in OTP memory and recycling VDD is required to have the modifications taking effect.

The XDPP1100 device supports 16-valent or 8-valent address table as shown in Table 23 and Table 25. To properly set the device addresses, resistors with 1% tolerance must be connected. The programming resistors are designed to allow using E12 resistors for system cost saving. The recommended series combination of E12 resistors are shown in Table 24.

Table 23 I²C/PMBus address offset of 16-segment decode

Resistor-to-GND (1%)		Address offset
XADDR1, or XADDR2	780Ω	0x0F
	1.10 kΩ	0x0E
	1.50 kΩ	0x0D
	2.02 kΩ	0x0C
	2.70 kΩ	0x0B

	3.52 kΩ	0x0A
	4.70 kΩ	0x09
	6.07 kΩ	0x08
	8.00 kΩ	0x07
	10.20 kΩ	0x06
	13.20 kΩ	0x05
	17.20 kΩ	0x04
	22.47 kΩ	0x03
	29.20 kΩ	0x02
	39.00 kΩ	0x01
	56.00 kΩ (or open)	0x00

Table 24 Recommended E12 resistor for XADDR 16-segment decode

XADDR Resistance (Ω)	R1	R2
780	680	100
1100	1000	100
1500	1500	0
2020	1800	220
2700	2700	0
3520	3300	220
4700	4700	0
6070	5600	470
8000	6800	1200
10200	10000	200
13200	12000	1200
17200	15000	2200
22470	22000	470
29200	27000	2200
39000	39000	0
56000	56000	0

If only 8-segment decode is desired, the XDPP1100 also can be configured per Table 25. All the resistors are 1% E12 resistors. Register xv_decode_sel config the xValent selection.

Table 25 I²C/PMBus address offset of 8-segment decode

Resistor-to-GND (1%)		Address offset
XADDR1, or XADDR2	1.20 kΩ	0x07
	1.80 kΩ	0x06
	2.70 kΩ	0x05
	3.90 kΩ	0x04
	6.80 kΩ	0x03
	10.00 kΩ	0x02
	18.00 kΩ	0x01
	47.00 kΩ (or Open)	0x00

5.1.4 GPIO

The XDPP1100 provides up to 16 general purpose inputs/outputs (GPIOs). Each of the GPIO pins can be configured by software as input (with or without pull-up or pull-down) or as output (push-pull or open-drain). All the GPIO pins are shared with alternative functions. The I/O configuration can be locked if needed to follow a specific function. The GPIO configuration is programmed by the function register of each GPIO pin named xxxx_func, and the FW_CONFIG_PMBUS command.

Table 26 shows the multi-purpose GPIO function mapping.

Table 26 GPIO multi-purpose pin

Name	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
MP_FAULT1	IO:GPIO0[2] (FAULT1)	IO:GPIO0[2]	IO:GPIO1[2]	IO:SYNC	O:FAN2_PWM	IO:SDA2	UARTRX	na
MP_FAULT2	IO:GPIO1[2] (FAULT2)	IO:GPIO0[2]	IO:GPIO1[2]	IO:SYNC	I:FAN2_TACH	IO:SCL2	UARTTX	na
MP_IMON	A:IMON	IO:GPIO0[3]	IO:GPIO1[3]	IO:SYNC	I:FAN1_TACH	na	na	na
PWM11	O:PWM11	IO:GPIO0[6]	IO:GPIO1[6]	IO:SYNC	O:FAN1_PWM	na	na	na
PWM12	O:PWM12	IO:GPIO0[7]	IO:GPIO1[7]	IO:SYNC	I:FAN1_TACH	na	na	na
PWM1	O:PWM1	IO:GPIO0[5]	IO:GPIO1[5]	IO:SYNC	na	na	na	na
PWM2	O:PWM2	IO:GPIO0[7]	IO:GPIO1[7]	IO:SYNC	na	na	na	na
PWM3	O:PWM3	IO:GPIO0[1]	IO:GPIO1[1]	IO:SYNC	na	na	na	na
PWM4	O:PWM4	IO:GPIO0[2]	IO:GPIO1[2]	IO:SYNC	na	na	na	na
PWM5	O:PWM5	IO:GPIO0[3]	IO:GPIO1[3]	IO:SYNC	UARTRX	na	na	na
PWM6	O:PWM6	IO:GPIO0[4]	IO:GPIO1[4]	IO:SYNC	UARTTX	na	na	na
PWM9	O:PWM9	IO:GPIO0[4]	IO:GPIO1[4]	IO:SYNC	na	na	na	na
PWM10	O:PWM10	IO:GPIO0[5]	IO:GPIO1[5]	IO:SYNC	na	na	na	na
PWM7	O:PWM7	IO:GPIO0[5]	IO:GPIO1[5]	IO:SYNC	O:FAN2_PWM	na	na	na
PWM8	O:PWM8	IO:GPIO0[6]	IO:GPIO1[6]	IO:SYNC	I:FAN2_TACH	na	na	na
MP_SMBALERT#	IO:SMBALERT_N	IO:GPIO0[6]	IO:GPIO1[6]	IO:SYNC	IO:GPIO0[7]	IO:GPIO1[7]	na	na
MP_BEN	IO:GPIO1[0] (BEN)	IO:GPIO0[0]	IO:GPIO1[0]	IO:SYNC	UARTRX	IO:SDA2	na	na
MP_ BPWRGD	IO:GPIO1[1] (BPWRGD)	IO:GPIO0[1]	IO:GPIO1[1]	IO:SYNC	UARTTX	IO:SCL2	na	na
MP_SYNC	na	IO:GPIO0[7]	IO:GPIO1[7]	IO:SYNC	O:FAN1_PWM	na	na	na
MP_EN	IO:GPIO0[0](EN)	IO:GPIO0[0]	IO:GPIO1[0]	IO:SYNC	na	na	na	na
MP_PWRGD	IO:GPIO0[1] (PWRGD)	IO:GPIO0[1]	IO:GPIO1[1]	IO:SYNC	na	na	na	na

Note:

1. Shaded rows available in all packages
2. Analog functions prefixed with "A:"
3. Digital inputs prefixed with "I:", outputs prefixed with "O:", inouts prefixed with "IO:"
4. Input priority by lowest pin # (e.g., if MP_FAULT1 and PWM11 both programmed to SYNC, the input is taken from MP_FAULT1 due to lower pin #)

5.1.5 Register Map

The XDPP1100 device is configured by application specific parameter settings loaded into control registers. The access to control register map can be achieved over I^2C and PMBus. Module manufacturer could use I^2C to set up controller features and parameters. PMBus commands allow end user to customize system applications. The access to register map is supported by the XDPP1100 GUI. Details of the register map can be found in Register Descriptions document which comes along with the GUI installation package.

For typical applications, the control registers are pre-programmed at the factory and stored in the on-chip nonvolatile memory (NVM), which is then downloaded to the control registers during initialization of the controller as it powers up. Control registers can be reprogrammed in the field via the serial communication (I2C) bus and stored into the NVM. The XDPP1100 controllers support multiple reprogramming cycles which is easily accomplished with the XDPP1100 GUI or System Programmer software.

In addition to supporting multiple reprogramming cycles, the XDPP1100 controllers also support storing multiple configurations in NVM, where the initialization settings is selected from one of these stored configurations depending on the value of an external resistor connect to the XADDR pin. This capability is referred to as multi-config. This allows a single configuration file to support multiple applications, which is useful when multiple controllers are used in a system, but require different configurations because they support multiple types of output rails. With multi-config, the XDPP1100 controllers are capable of storing up to 16 configurations, and these configurations may be reprogrammed if needed. The controller identifies the proper configuration to load based on information stored in the configuration, namely an indicator bit identifying a multi-config should be used and a pointer to the location of the multi-config space in the NVM.

5.2 Analog Blocks and Subsystems

5.2.1 Power Supply

Operating from a single +3.3 V (VDD) supply to the controller, an on-chip low drop-out (LDO) regulator generates an internal +1.2 V voltage at VD12 pin. Both VDD and VD12 pin should have 1 µF+0.1 µF ceramic bypass capacitors for noise filtering. Place the bypass capacitors as close as possible to VDD and VD12 pins. Do not apply voltage to or ground VD12 pin. VD12 pin is also not intended to be used as 1.2 V reference.

5.2.2 Oscillator and PLL

A 200 MHz internal PWM oscillator is incorporated in the device. With a 6-bit interpolator, the XDP device offers high PWM resolution as small as 78.125 ps, using 11-bit time-based period and frequency control. The maximum pulse width that the XDPP1100 supports is 10.24 µs (2048 x 5ns); this limits the minimum switching frequency to approximately 100 kHz. The maximum switching frequency is 2 MHz and the frequency resolution is 20 ns. With the 20 ns resolution, the target frequency could not be configured linearly within the 100 kHz to 2 MHz range. For example, set switching frequency to 350 kHz (Ts = 2857 ns), will result 352 kHz with the switching period rounded down to 2840 ns. The XDPP1100 GUI could help user to find out the actual switching frequency when using FREQUENCY_SWITCH command.

A typical PWM generation waveform is shown in Figure 5. The top axis shows analog behavioral waveforms of a dual-edge modulator (Vmod) and compensated error signal (i.e. PID output). The second axis shows the resulting PWM waveform, followed by the inverted PWM signal. The signals on the bottom 8 axes have hatched lines indicating where dead-time is applied to the signals.

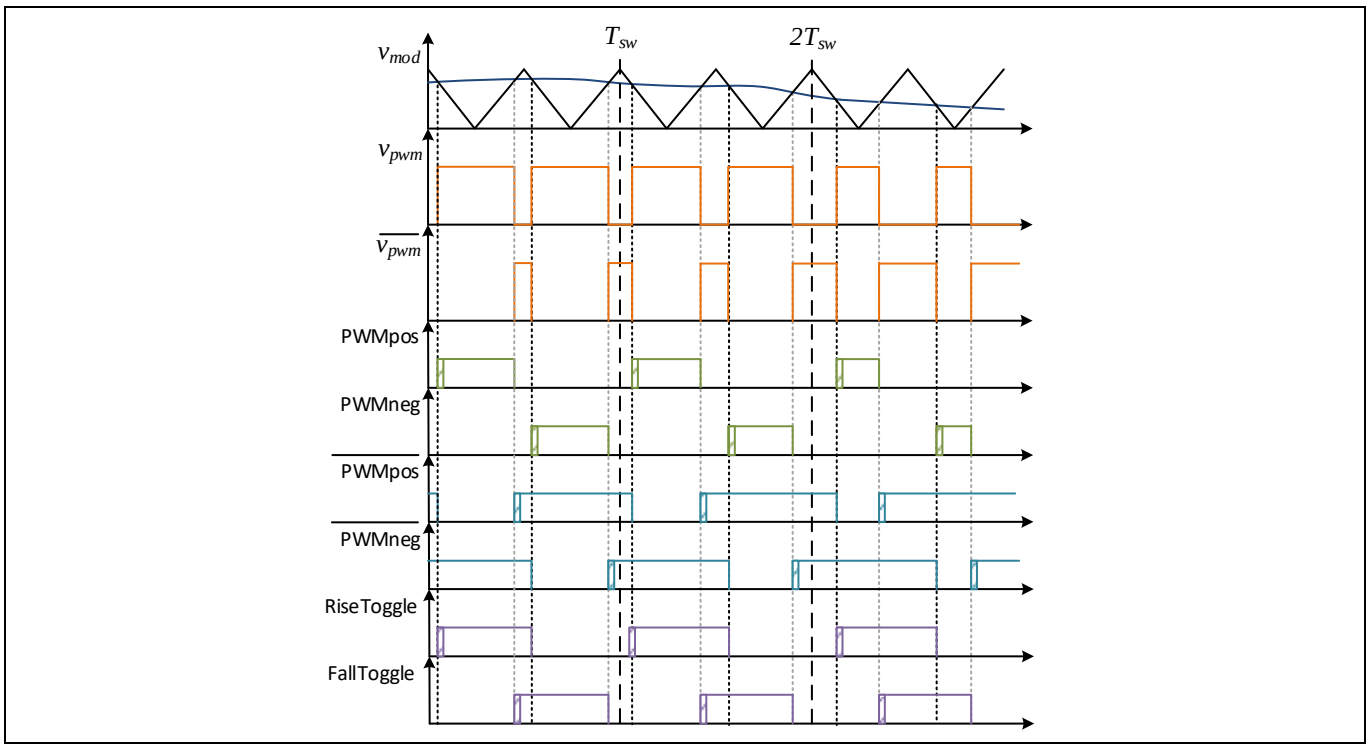

Figure 5 PWM Generation

Dead-time refers to the amount of time between the turning-off of one switch to the turning-on of another switch where both are off to prevent unintentional short circuit conditions. The standard way of implementing dead-time is to use leading edge-blanking. Each signal of the PWM generator will be capable of blanking the rising edge by a programmable amount of 0-318.75 ns in 1.25 ns increments. The XDPP1100 also support to adjust the falling edge of each PWM if additional blanking time is required. The value of dead-time is changeable during normal operation to allow power supply efficiency optimization.

PWM outputs are 3.3 V compatible signals which are set to high impedance during reset, configuration, and initialization. The PWM outputs that are mapped to a Loop to drive MOSFETs will be pulled low after firmware completed the configuration and initialization. It is not mandatory to use an external pull-down resistor at PWM pins.

The multi-purpose MP_SYNC pin can be configured as an input to allow synchronization to an external clock signal, or as an output to provide a clock that other converters synchronize to. For the best flexibility, all GPIO pins can be configured as SYNC pin.

When SYNC pin is configured as an input, the PLL receives a periodic signal that can be assigned to either loop (in the packages that support dual-loop operation). The input signal will be limited to +/-6.25% of the programmed switching frequency to lock the sync clock. Once locked, the sync input signal can wander to +/-12.5% of the programmed frequency.

The SYNC signal output is set when the ramp timer crosses a programmed threshold. This allows setting the phase of the SYNC signal. The sync function would provide a signal indicating successfully synchronization, as well as a fault if it cannot synchronize.

5.2.3 Voltage Sense AFE1

The XDPP1100 offers 3 dedicated high speed voltage analog/digital converters (ADC) as Analog Front End (AFE1). By function, the voltage sense AFE1 can be used as voltage sense processor (VSP) or rectified voltage sense processor (VRSP).

The major functions of the VSP and its accociated blocks are:

- Voltage ADC full rate interface to the digital domain
- Voltage ADC gain and offset trim (digital trim)
- Voltage scaling (external resistor divider)
- Output voltage computation
- Output Over/Under Voltage Protection comparators and fault
- Fast transient (FTR) mode and FTR exit comparators
- Open sense protection and fault comparators
- Burst mode and burst mode exit comparators

The VRSP and its accociated blocks have the following functions in addition to the above:

- 200 MHz edge comparator with digital de-glitcher
- Measure V_{RECT} voltage of the even and odd half cycles of bridge topologies
- Measure V_{RECT} voltage on the even cycle for non-bridge topologies
- Average the measured even and odd V_{RECT} voltage
- Flux balancing circuit
- Input voltage processing

The simplified VSADC block diagram is shown Figure 6.

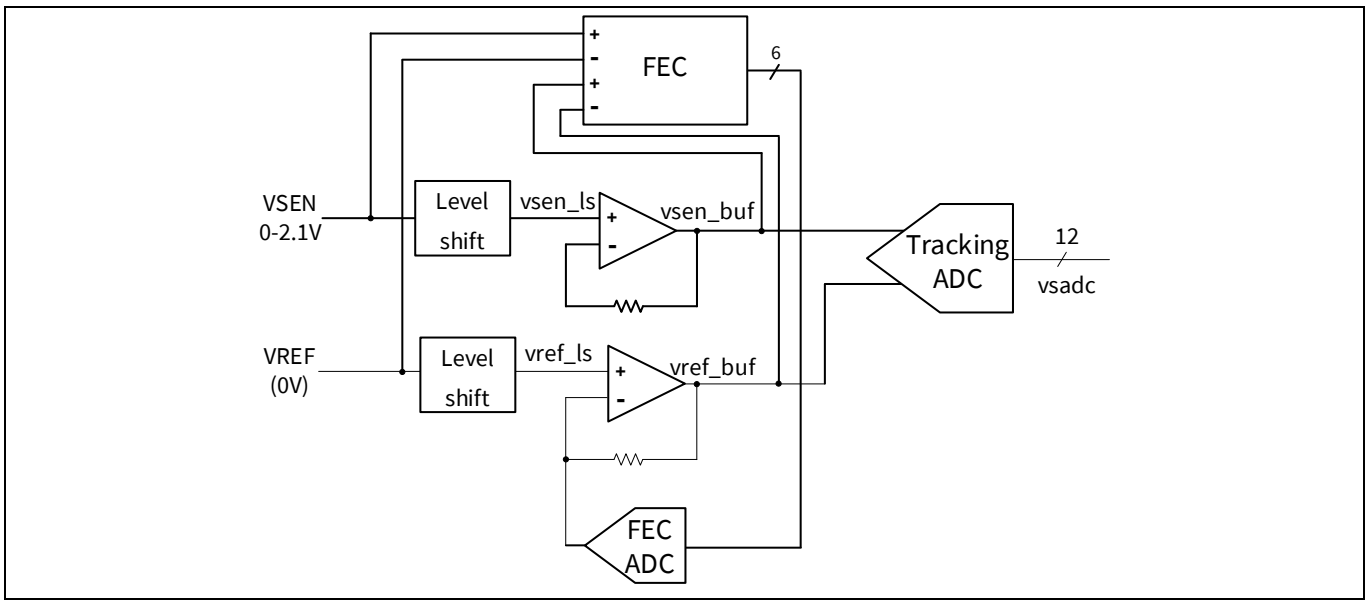

Figure 6 Voltage sense ADC block diagram

The level shifters allow wide input voltage range, 0.0 to 2.1V, as well as provide a high input impedance. The unity gain buffers provide additional drive strength to the tracking ADC input stage. The front end offset compensator (FEC) is to reduce the effects of temperature, stress and lifetime offset-drift in the AFE.

Simplified block diagram of the tracking ADC is shown in Figure 7. The summing amplifier amplifies the difference between the buffered differential sensed voltage and the DAC output voltage.

The output of the summing amplifier drives the comparator whose output determines the size and direction of the next step for the tracking integrator. The tracking integrator output represents the analog to digital converted sensed voltage. It is also used to drive the DAC whose output is summed in the summing amplifier.

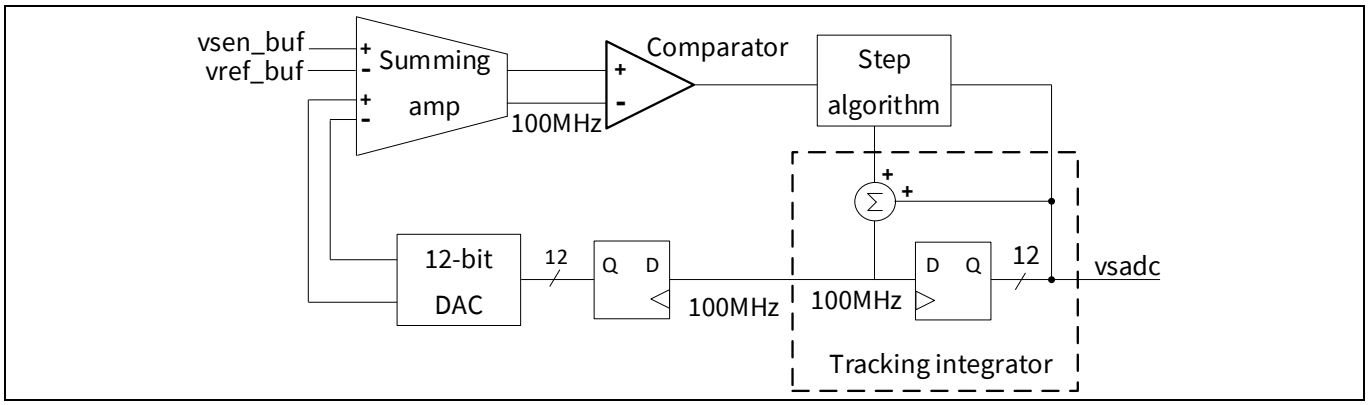

Figure 7 Tracking ADC block diagram.

Tracking ADC resolution is 12 bits with an input referred LSB weight of 1.25mV. Note that the AFE input range is restricted to maximum of 2.1V, meaning only the lower 11 bits of the ADC output are actually used. For output voltage sensing, 3-bit modulation is added to the reference voltage to achieve 156 µV resolution.

The voltage sense input has a nominal input impedance of 1 MΩ. The ADC is clocked at 100 MHz and a voltage sense front-end amplifier process the voltage at 50 MHz. There is no need for an anti-alias filtering, but it may be advantageous to add a higher bandwidth external RC filter network to increase the attenuation of high frequency noise that may couple onto the voltage sense lines. This additional filter provides minimal phase margin impact on the feedback loop. If such an additional filter is used, it is recommended that values of R_{EXT} = 10 Ω and C_{EXT} = 220 pF be used.

If the external feedback loop is failed to connect, VSEN/ BVSEN is able to detect open sense lines. More details of the open sense fault protection can be found in application note.

The VRSP is responsible for controlling the VRSEN ADCs when they are used to measure the rectified voltage waveform (V_{RECT}). Figure 8 presents waveforms to illustrate how sampling of the V_{RECT} waveform. Noise has been added to the ideal V_{RECT} waveform to highlight the importance of sampling window timing. The AFE1 has an edge detector working at 200 MHz clock. It senses the rising and falling edges of V_{RECT} waveform. T_{detect} waveform is the output of edge detector logic. The rising-edge of the rectified voltage waveform is detected and some programmable blanking window is added to it. The blanking time should be configured longer than the voltage spike and ringing duration. The blanking time should also be set longer than 250 ns for the tracking ADC to settle. After the blanking window, sampling of the rectified voltage can occur (shown as the T_{sample} waveform). The comparator for the VRS is prepositioned to the value of the last cycle to minimize the time required for the ADC to properly track the voltage. The sampling window ends when the associated PWM signal goes low.

Faults and warnings including input overvoltage and undervoltage would be detected by the VRSP when it is being used for input voltage sensing. These are set by PMBus commands; and the response is handled by the CPU.

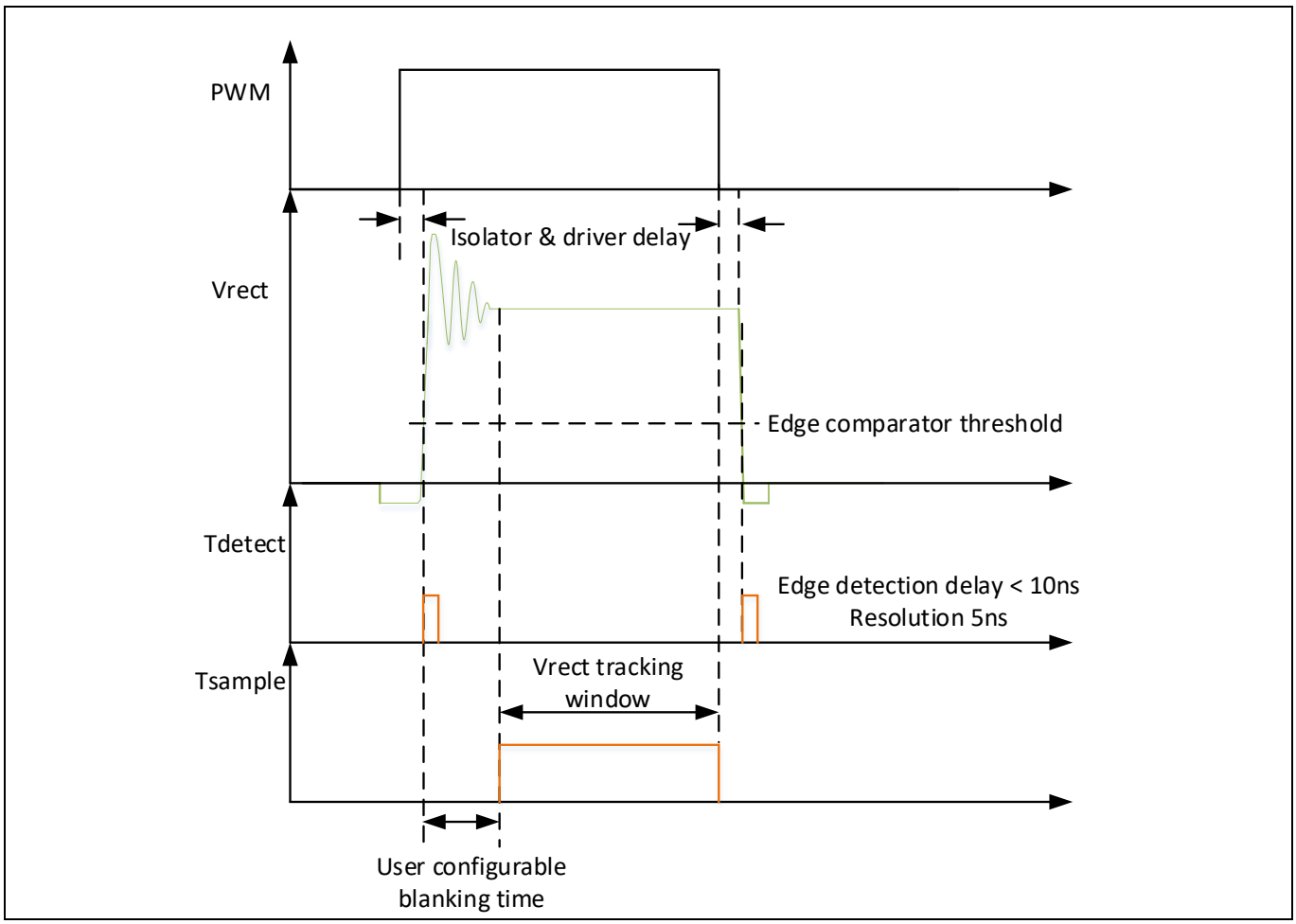

Figure 8 VRSP sampling window

The timing of the rising and falling edges of the rectified voltage waveform, along with the magnitude, is used for transformer protection. i.e. in full-bridge voltage mode converter, the V_{RECT} timing and amplitude is used for volt-second flux balancing. To avoid waveform distortion or timing delay, it is not recommended to add any filter to the input of VRSEN when it is used V_{RECT} sensing mode.

5.2.4 Current Sense AFE2

The dedicated differential current sense ADC (AFE2) is designed to sense output current via low ohmic sense resistor or PCB copper trace. The ISADC (ISEN, BISEN) is 9.25-bit tracking ADC and is interpolated to 13-bit through current emulation. It operates at 25 MHz and could provide high speed cycle-by-cycle peak current limiting. The peak current limit comparator works at 100 MHz clock, provides fast protection to the system.

Simplified block diagram of the current sense ADC is shown in Figure 9. The first sub-block, programmable gain OTA converts the current sense voltage to a current that is summed with the DAC current. The gain level for OTA is programmable as well as the reference level for current sense voltage. The high-gain mode has 100 µV /LSB and the low-gain mode has 1.45 mV/LSB. The reference level is ground except IPS mode.

The second sub-block, 9.25 bit DAC, has 640 quantization levels. However, some of the bits are used for offset correction and the effective bits are less, depending on the OTA gain setting. The effective ISADC input voltage range of each gain setting is specified in Table 12, Table 13, and Table 14.

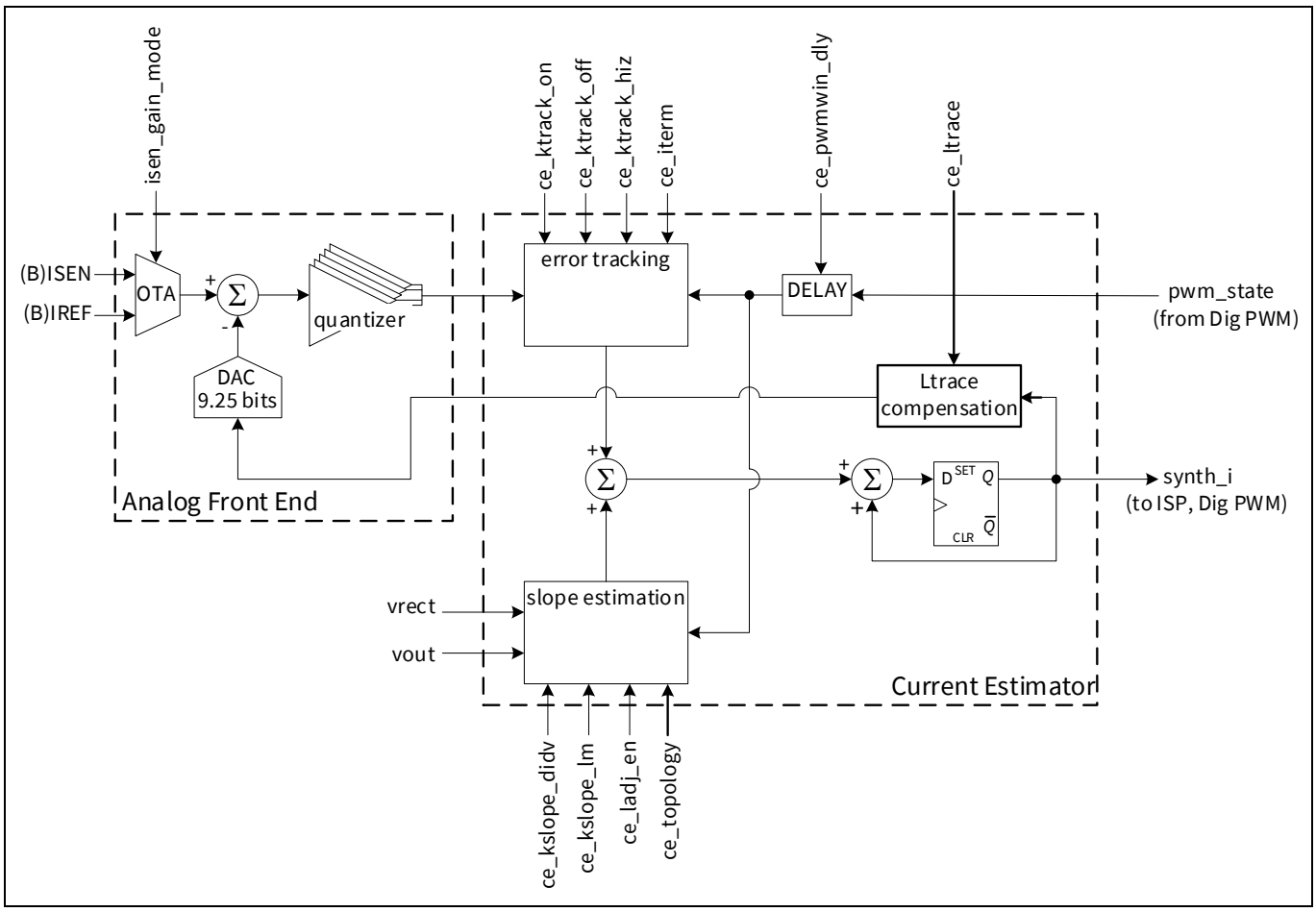

Figure 9 Simplified block diagram of the current sense ADC.

The quantizer consists of five comparators which generate 6-level (±1, ±3, ±5) error tracking signal used by the current estimator to correct current estimation.

The current estimator provides a digital reconstruction of the secondary side inductor current or the primary side current, depending on the current sense input pin configuration. The shape of this current is obtained through slope estimation function. The detail of current estimator can be find in the XDPP1100 technical reference manual.

If PCB copper traced is used for current sensing, temperature compensation should be considered to compensate the temperature shift of the copper trace. The controller continuously monitors temperature and uses this information to digitally compensate for resistance changes over temperature based on temperature coefficient of copper. The temperature compensated current readings are also used to determine fault status.

The controller provides several mechanisms for improving the current sense accuracy. To reduce the effect of board noise on the current sense, leading edge blanking and trailing edge blanking time are implemented at PWM transition. The blanking time can be configured from 0 to 280 ns. Exceptional noise immunity is achieved by the use of the internal phase current estimator. Based on the state of the PWM pulse, the controller continuously predicts each individual phase DC and ripple current. The result of the prediction is combined with the actual measured phase current to be processed by the controller. Hence, the instantaneous noise in the measurement can be filtered out without losing the valuable ripple current information. In addition, the XDPP1100 makes multiple current measurements and the readings are averaged over every switching cycle. To

improve the current sense accuracy, the XDPP1100 also allows to compensate the parasitic inductance of current sense resistor.

The XDPP1100 controllers can be configured to operate with integrated power stage (IPS), which incorporates integrated current sense features (for example, Infineon's IR3555A). When the current sense is set to IPS mode, a 1.2 V common mode voltage should be applied to the current reference pin as shown in Figure 10. The advantages of using integrated current sense over traditional DCR current sense include:

1. Superior part-to-part current sense gain control: integrated power stage has much lower gain variation compared with PCB copper trace.
2. Superior current sense accuracy over temperature: current mirror sensing ideally tracks the signal over temperature.

Please note only PWM6 and PWM11 support tri-state output. If the integrated power stage requires tri-state to turn both MOSFETs off for Body-Breaking™ or phase dropping, please use PWM6 or PWM11 pin to drive the power stage. For other PWM outputs, firmware change is required to force individual PWM output to HiZ to enable tri-state.

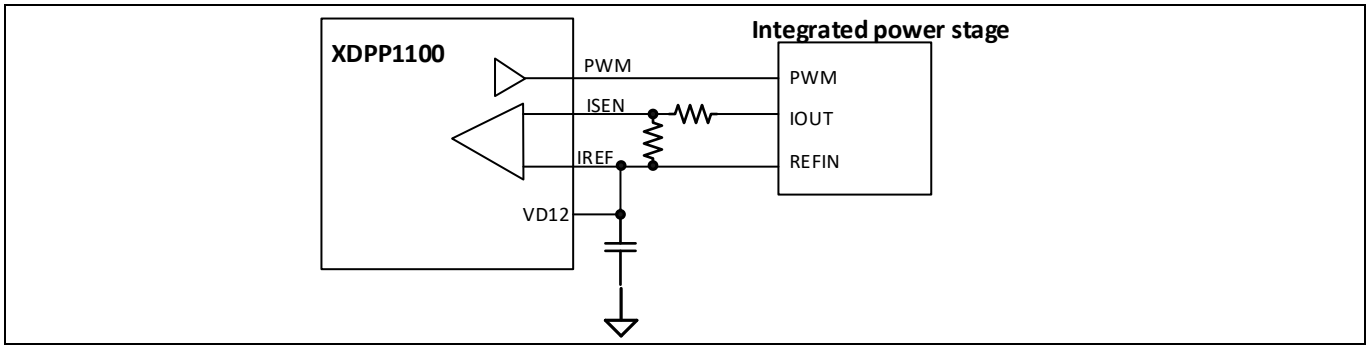

Figure 10 Integrated current sense

The major functions of the current sense processor (ISP) and its associated blocks are:

- Current ADC full rate interface to the digital domain
- Current ADC gain and offset trim (digital trim)
- Current scaling
- Output current computation
- Output current shunt temperature compensation
- Output Over/Under Current Protection comparators and fault
- Input current estimation
- Input Over Current Protection comparators and fault (during PCMC)
- Cycle-by-cycle peak current limit

5.2.5 General Purpose AFE3

The general-purpose ADC AFE3, also referred to as telemetry ADC (TS ADC), is a 9-bit, high speed analog to digital converter. Voltage resolution of the general-purpose ADC is 2.344 mV, with a sample frequency 1 MHz. The general-purpose ADC block consists 8 channels and 6 channels are usable as shown in Figure 11. It can be configured to digitize voltage, current, impedance, and temperature.

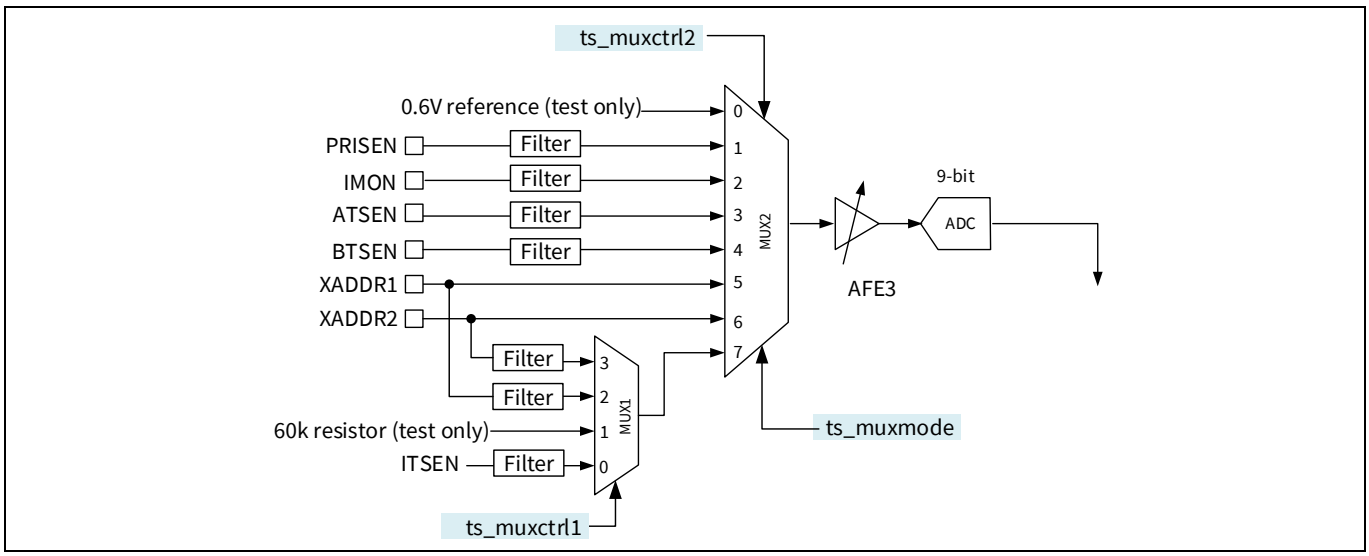

Figure 11 Telemetry sense block

The conversion sequence of channels can be defined by user or can be set to auto sequencing per mux control registers.

5.2.5.1 IMON and Active Current Sharing

IMON pin has an analog DAC output representing the output current. IMON could be used for output current monitor, and for active current balancing between multi parallel modules. An internal current source proportional to the output current of loop0 is sourced from IMON pin. IMON current DAC (IDAC) is 6-bit DAC with output current range is 0 to 640 µA. There are 4-bit accumulated dithering driving an extra LSB input to the DAC for extra resolution (total 6+4 bit). The gain of the current source is configurable which allows user to scale the current source per application. The maximum source current is 640 µA. At no load, this source current is 320 µA. IMON source current lower than 320 µA indicates negative current in this module.

A 1.875 kΩ precision resistor (R_{ishare}) connected between IMON and ground will present a voltage proportional to output current of each module. To smooth the IDAC dithering ripple, it is suggested to put a 1 nF capacitor in parallel with the R_{ishare}. At full load, the IMON voltage will be 1.2 V (640 µA x 1.875 kΩ); and at no load, IMON voltage is 0.6 V.

Connecting the IMON of paralleled converters together allows the IC detecting the level of averaging current. Each power supply converter would compare its own output current with the average current and make corresponding adjustment. To prevent oscillation on small error current, a dead zone applies to the current sharing block. When the error current is less than the dead zone, current sharing is inactive.

The XDPP1100 provides both positive and negative clamps to voltage adjustment during active current sharing. This guardbands the output voltage in a safe range. If the output voltage reaches the clamping level and the current error is still larger than the dead zone, current share fault will be reported.

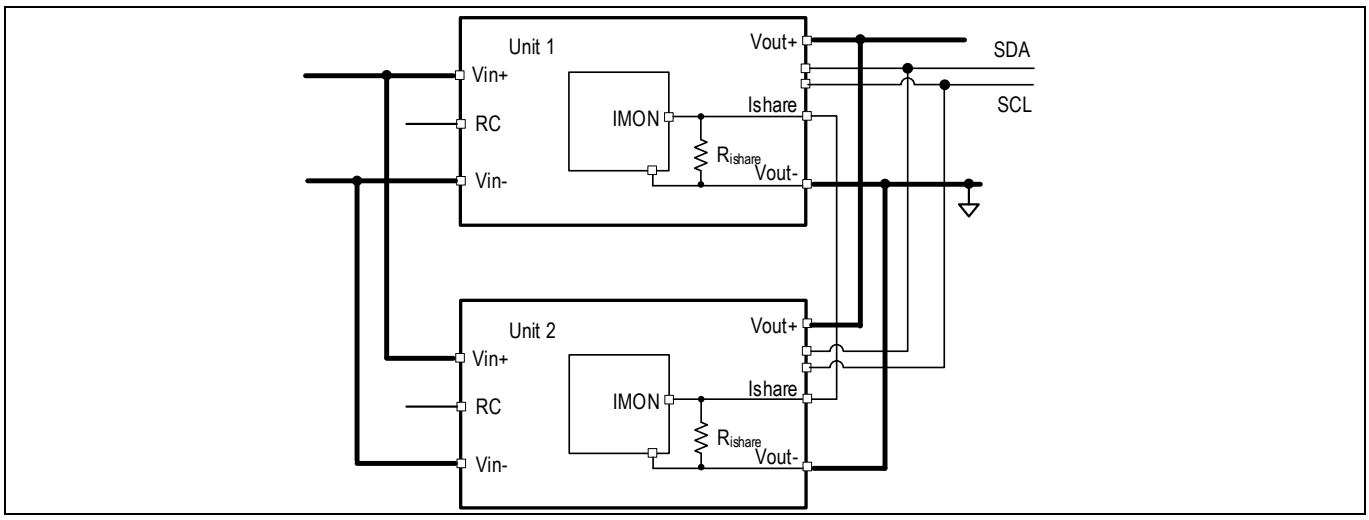

Figure 12 Parallel module current sharing

5.2.5.2 Temperature sense

The XDPP1100 supports both, external and internal temperature sensing for protection and monitoring. External temperature sensing is performed with a thermistor connected between TSEN or BTSEN to ground. IC supports external temperature sensor using inexpensive NTC thermistor method. The external sensor component should be placed close to and tightly coupled to the element of interest, for example the power stage components or the current sense resistor.

The xTSEN pin should be connected to the NTC through a network consisting of a parallel resistor and filter capacitor, as shown in Figure 13 below. The NTC terminals should be routed differentially to the xTSEN signal line back to the controller ground. The temperature is sensed by injecting a 100 µA current and measuring the voltage on xTSEN. The temperature is used to effectively compensate for the temperature coefficient of the current sense element and to provide over temperature protection by generating warning and fault signals. If the temperature sensor is not required, the xTSEN pin must be tied to GND.

The XDPP1100 controller includes a pre-programmed look-up table that is optimized for the recommended NTC options Murata NCP15WB473F03RC or Panasonic ERT-J0EP473J, with nominal value of 47 KΩ and in parallel with a fixed 12 KΩ resistor. It also supports user defined temperature lookup table if other temperature sense device is preferred, such as PTC or Vbe temperature sense.

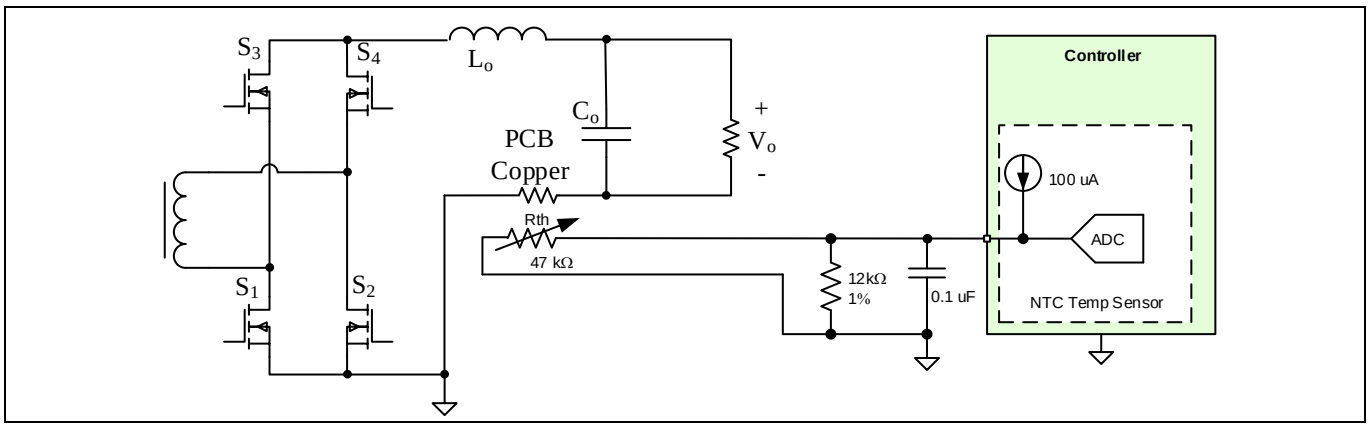

Figure 13 NTC Temperature sensing

Extra care should also be taken in the PCB layout to ensure that routing of the temperature sense traces is isolated from noise sources.

The internal temperature sensor is a PTAT (Proportional to Absolute Temperature) voltage generated within the controller die which reflects the junction temperature of the controller.

5.2.5.3 PRISEN

PRISEN is used to sense primary voltage for input voltage telemetry and feedforward compensation. In isolated application, the V_{IN} voltage should be sensed at primary side and feed to PRISEN pin through isolated amplifier. The slope and offset of the PRISEN could be configured by vin_pwl_slope and vin_trim registers.

The input voltage telemetry and protection could be configured to use either PRISEN or VRSEN as the input voltage signal source. The differences are shown below.

V_{IN} sense by PRISEN: uses General ADC (1MHz sample rate) and sample rate is shared with 5 other inputs (temperature sense, IMON, etc.). PRISEN is always enabled even when converter is in OFF mode. The feedforward response is slower than VRSEN based input voltage sensing.

V_{IN} sense by VRSEN: uses high speed ADC (50 MHz sample rate), provides very fast feedforward response and OV/UV protection. When using VRSEN for V_{IN} telemetry, it can be configured to sense DC input voltage by setting the vsp1_vrs_sel register to “general purpose ADC mode” or to sense transformer secondary winding by setting the vsp1_vrs_sel register to “V_{RECT} sense (VRS) mode”. When set to “V_{RECT} sense mode”, the V_{IN} telemetry is not active when converter is not in switching.

The PRISEN and VRSEN voltage sensing could be combined for the best system performance. The XDPP1100 allows to configure the input voltage telemetry and input voltage feedforward independently. Using PRISEN for input voltage telemetry allows continuous input voltage monitoring and pre-startup protections; using V_{RECT} sensing through VRSEN for fast feedforward response and flux balancing functions.

5.3 Control Loop Subsystems

5.3.1 State diagram

The state diagram is shown in Figure 14.

Controller operation is initialized by a power-on UVLO circuit with internal threshold. During controller configuration, the content of the OTP NVM is downloaded onto the control registers. During this period, the GPIO pins are held in high impedance (Hi-Z) state, allowing board pull-up or pull-down resistors to set the correct default levels for static input signals such as the I^2C address (XADDR1, XADDR2).

During the Initialization state, the controller measures the internal and external temperatures, input and output voltage, and executes the various calibration routines within the IC. Prior to exiting the Initialization state, the controller performs the external resistor pin set measurements used to set the I^2C serial addresses. Once a valid I^2C address has been determined, communication with the controller can established via the I^2C bus of the controller.

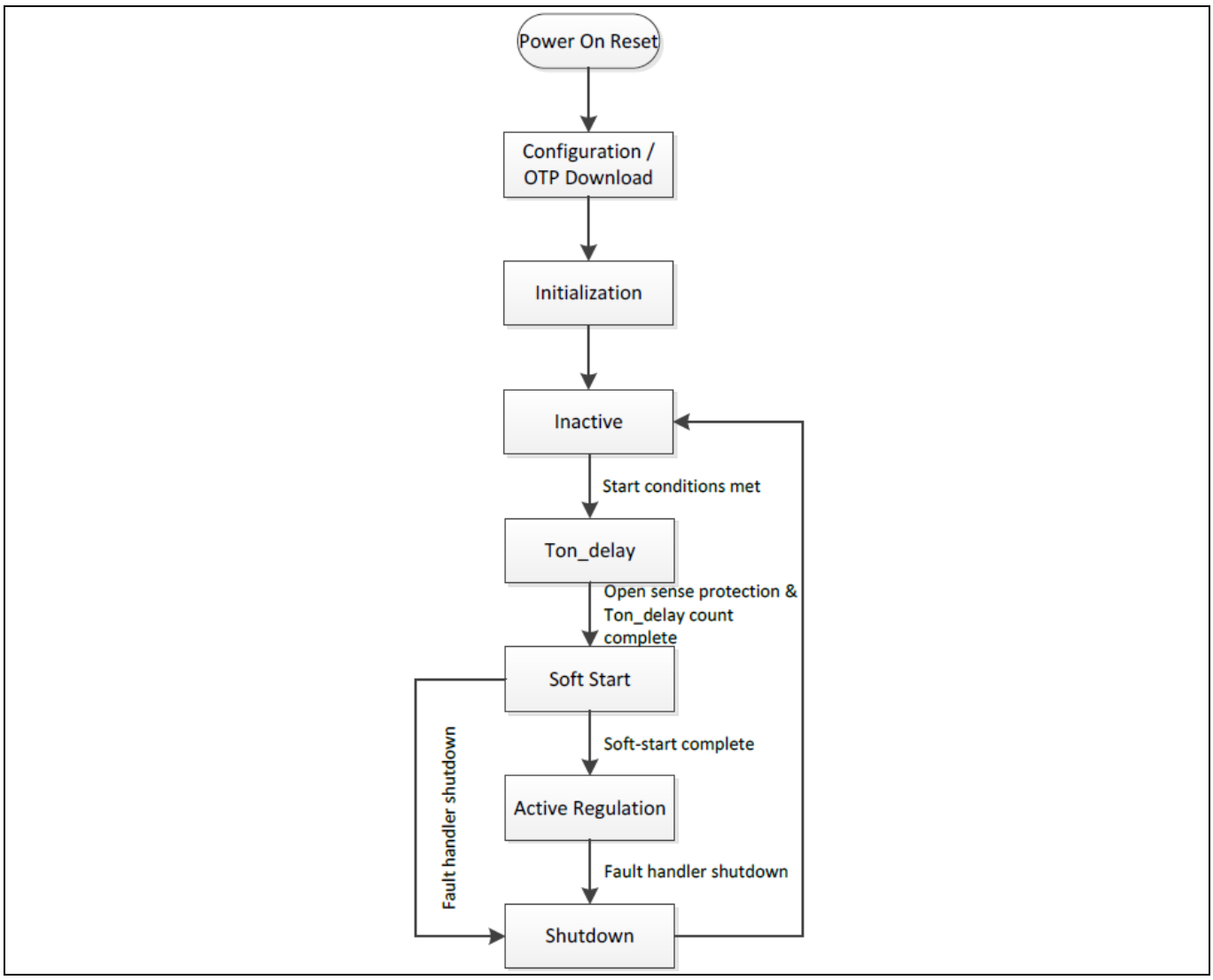

Figure 14 State Diagram

Upon completion of the Initialization process, the controller will enter the Inactive state. Controller will verify that the following conditions are satisfied before initiating the system:

1. Valid VDD: The voltage applied to VDD must exceed +2.78 V for the internal power valid signal to be asserted. Otherwise, a VDD UVLO fault will be issued.
2. No shutdown faults are asserted that are defined in the programmed shutdown mask.
3. Enable (EN/BEN) is asserted if the ON_OFF_CONFIG is set to “response to EN”. It is recommended that EN/BEN be asserted only after VDD, V_{IN} and power supplies for the power stages are ready.
4. TSEN/BTSEN inputs and the internal temperature are within operation range.

Once the above startup conditions are satisfied, the controller will wait for a programmable period of time (TON_DELAY) before ramping up the output voltage.

5.3.2 Soft start

Prior to entering the active regulation state, the controller performs a controlled, monotonic soft start ramp of the voltage output. During Soft Start, the controller will perform a pre-bias condition measurement of the

output voltage. The controller could disable synchronous rectifier outputs (diode emulation mode) so that it will not sink current from the pre-biased output. The diode emulation mode in startup can be configured using PMBus commands. Soft start is performed by actively regulating the output voltage while digitally ramping up a reference voltage from the measured pre-biased voltage to its final target value. Target output voltage, slew rate, turn-on rise time, as well as number of turn-on trials can be configured during a soft start ramp.

The transition from diode rectification (DE) to synchronous rectification (SR) is seen by the control loop as a load release. To avoid voltage glitch, the control loop resets the PID accumulate error and use the feed-forward duty-cycle when the SRs are enabled. Thus, by the time the SRs turned on, the loop has a corrected duty-cycle immediately, which avoid the slow response of the feedback loop. This feature applies to the voltage mode control.

When the converter completes the initial output ramp to the target output voltage, it enters active regulation state. The power good signal PWRGD is asserted indicating the output voltage is within the regulation window.

5.3.3 Voltage Mode Control (VMC)

Voltage mode control (VMC) is the most fundamental control mode supported in the XDPP1100, and is shown for dual loop operation in Figure 15. The output voltage for each loop is compared to its desired voltage (vref) to generate an error voltage that is fed into the PID compensation network. The output of the PID is used by the PWM Gen block to create the required signals for the given topology.

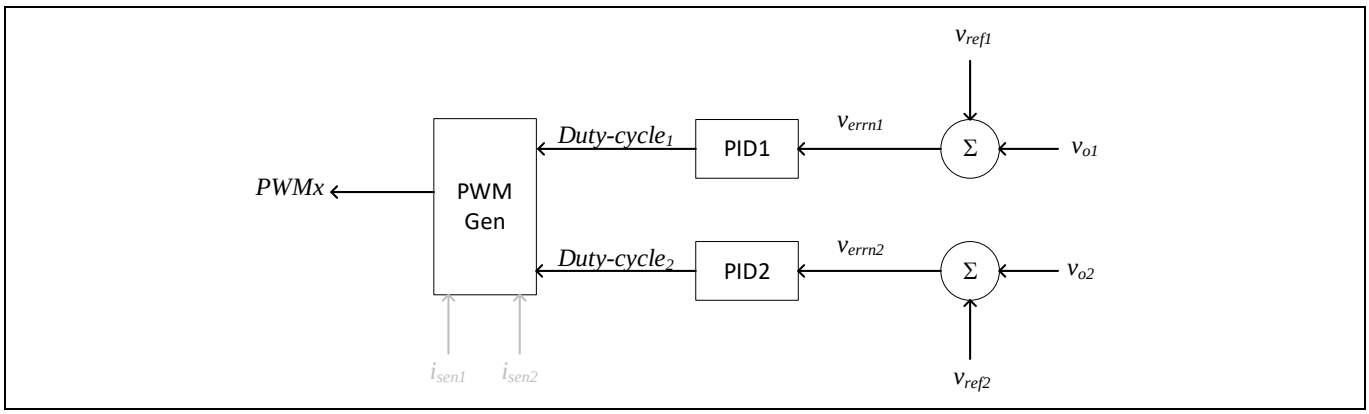

Figure 15 Voltage mode control loop

VMC supports three pwm modulation modes: dual-edge (DE) modulation, trailing-edge (TE) modulation, and leading-edge (LE) modulation. These modulation schemes are shown in Figure 16.

The first modulation waveform in Figure 16 a) shows the trailing edge (TE) modulation case. The PWM pulse has a fixed leading edge and a modulated trailing edge.

The second modulation scheme is leading edge (LE) modulation, shown in Figure 16 b). The PWM pulse has a fixed trailing edge and a modulated leading edge.

The last modulation scheme is dual edge (DE) modulation, shown in Figure 16 c). In this modulation, the timing markers t1 and t2 are both modulated.

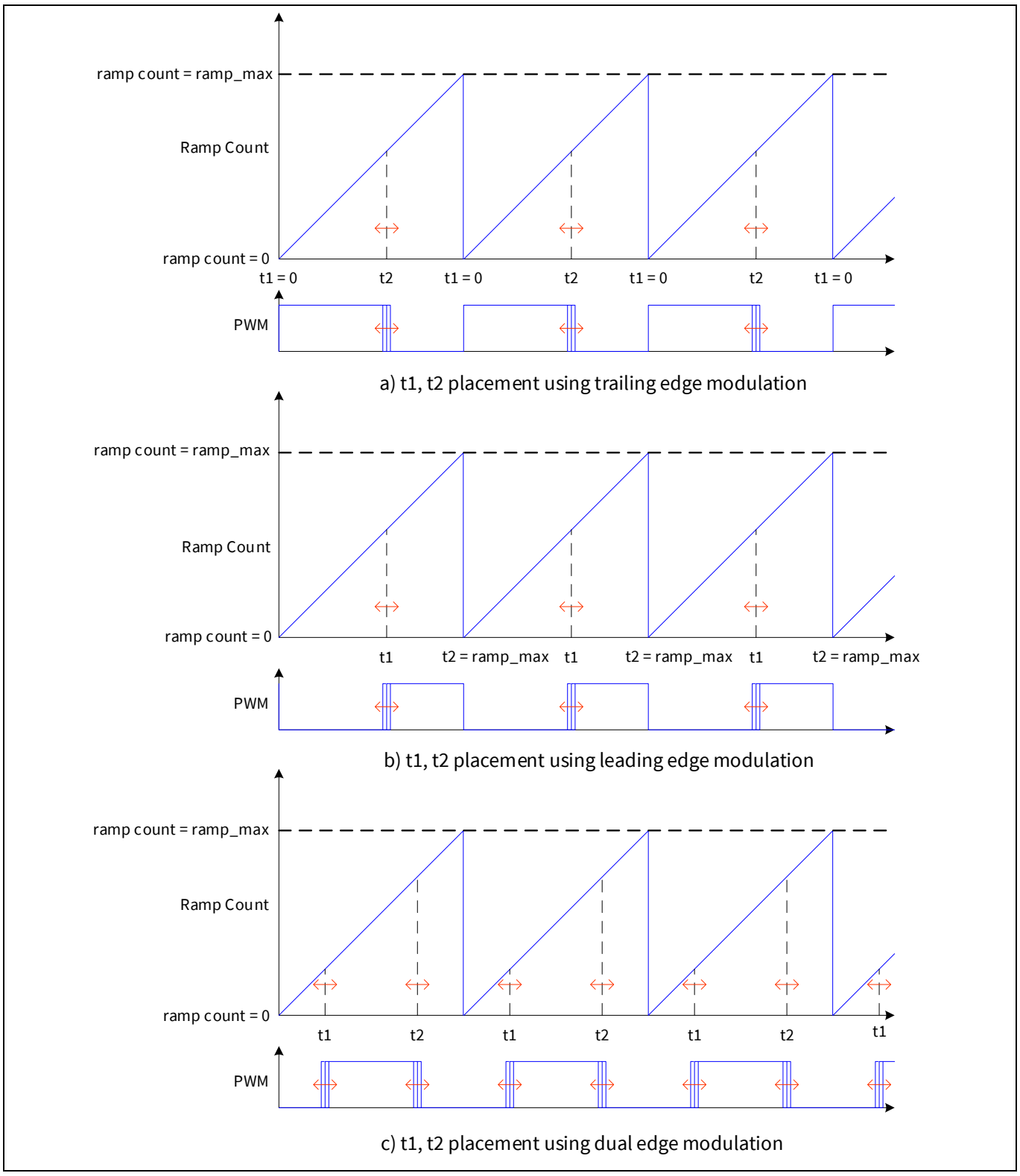

Figure 16 T1 and t2 placement for TE, LE and DE modulation.

5.3.4 Peak Current Mode Control (PCMC)

In peak current mode control (PCMC), the current is sensed and shut off when it reaches a given threshold. The compensated error voltage defines that threshold value. What is important to note is that to implement

primary side PCMC, the sensed current is not the output current (as in VMC). Instead, the current in the primary devices is sensed and fed across the isolation barrier by a current transformer or isolation amplifier. Secondary side PCMC is compensated similarly to primary side PCMC, the main difference being the sense current in this case is the output (inductor) current.

With PCMC, the derivative of the compensator network is not needed, leaving only a PI for the compensation network.

One issue with PCMC is subharmonic oscillation with duty cycles greater than 50% causing disturbances to grow instead of decay. To overcome this, an auxiliary ramp is added. The slope of the ramp is user selectable by register compensation_slope from V_O/L, $V_O/2L$, $V_O/4L$.

During startup and controlled shutdown when the duty-cycle is narrow, primary current signal is weak. It is suggested to enable the minimum pulse width register (rampX_min_pw_state = 1) to avoid cycle skipping. It is also possible to disable the peak current mode control and use the voltage mode control during startup and switch to PCMC when the output voltage reaching a target window.

PCMC only supports trailing edge modulation.

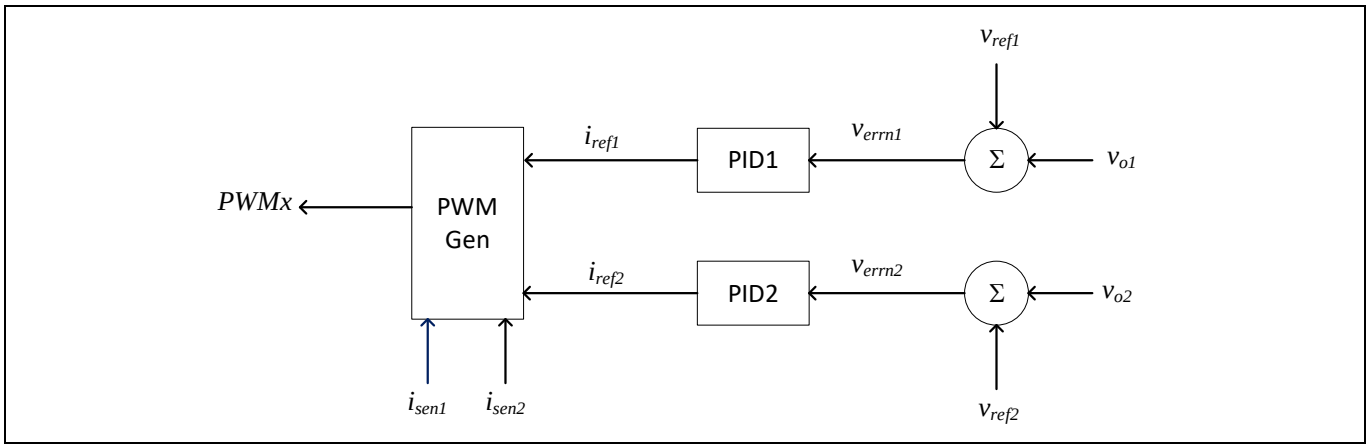

Figure 17 Peak current mode control loop

5.3.5 PID and Control Loops

Each loop of the controller implements a fixed switching frequency, digital PID voltage loop, and dual-edge PWM architecture. During operation, the output voltage is sensed differentially and digitized by a precision analog-to digital converter (ADC). The voltage is compared to reference voltage to generate an error voltage. The resultant digital error signal is then fed into a digital PID compensator with the effective transfer function given by:

$$H_{PID}(z) = \left[\left(K_P + K_D(1-z^{-1})\right)\left(\frac{K_{fp2}}{1-(1-K_{fp2})z^{-1}}\right) + \frac{K_i}{1-z^{-1}}\right]\left[\frac{K_{fp1}}{1-(1-K_{fp1})z^{-1}}\right]z^{-1}$$

The locations of the poles and zeroes are determined by the digital loop coefficients Kp, Ki, Kd, and Kfp, which are the PID (proportional, integral, derivative) and low pass filter pole terms, respectively. It creates the equivalent of type III compensation network. In current mode control, phase lead is not required, so the derivative term Kd is zeroed out.

The ARM M0 has access to the PID coefficients and is able to optimize the values during different operating modes, i.e. soft start, steady state, load transient, and power saving states.

The output of each loop's digital PID compensator is converted to a PWM pulse using a digital dual-edge pulse width modulator. The maximum duty cycle limit is programmable up to 99.6%. In addition to using the PID compensator for regulation, the controller has nonlinear control mechanisms such as fast transient response (5.3.9), and input voltage feedforward (5.3.10), to minimize voltage excursions during transient events.

5.3.6 Shutdown

The shutdown state can be entered from either soft start or active regulation states through user intervention (de-asserting EN) or through a detected fault. Here are the example of some fault conditions: over-temperature (OTP), over current (OCP), input under voltage (IUVP), input over voltage (IOVP), output overvoltage (OOVP), flux balance fault. The voltage loops may be programmed to shut down together or independently in case of a fault condition.

The XDPP1100 supports two user selectable shutdown options in response to de-assertion of EN. The first option is a closed-loop shutdown where the controller ramps down the output voltage at a user defined slew rate. The second option is a hot-shutdown (Hi-Z) response, where the output stage power FETs are immediately switched off. If immediate shut-down is required, TOFF_DELAY should be set to 0ms. For cases where the shutdown is caused by a fault, the resultant shutdown response is always Hi-Z.

Once shutdown has occurred, firmware will handle the subsequent response. The shutdown may be final; or the converter may enter a finite or infinite hiccup mode.

5.3.7 Current Sense Estimator

The current sense estimator (CE) samples the inductor current and provides slope estimation and tracking. Based on the state of the PWM pulse, the controller continuously predicts each individual DC and ripple current. The result of the prediction (estimation) is combined with the actual measured current (tracking) to be processed by the controller. The weight of tracking over estimation can be defined by user through register ceX_ktrack_hiz, ceX_ktrack_off, ceX_ktrack_on. These registers set the tracking gain in HiZ state, off state and on state respectively. It can be configured as estimation only, tracking only or the combination of estimation and tracking.

When used for output current sensing, slopes during the energy transfer interval depend on the value of the rectified voltage, which is a function of input voltage and turns ratio; the filter inductance, and the output voltage. The freewheeling interval can be split up into two parts: the first where the SR body diode conducts, and the second where the SR is on so the channel conducts. In the first case, the slope is a function of the output voltage, inductor, and forward voltage of the diode. In the second case, the slope is a function of the output voltage and filter inductance. Register ceX_kslope_didv defines the normalized output inductor value for slope estimation.

The output current could be sensed before the output capacitor bank, which is the inductor current with ripple; or could be sensed after the output cap which is DC current without ripple. Sensing the inductor current enables the capability of secondary peak current mode control. Sensing DC output current couldn't use the secondary PCMC or cycle-by-cycle peak current limit.

When used for primary-side PCMC, the CE estimates the slope of the current during the energy transfer interval. The slope is a function of input voltage, output inductance, output voltage, turn ratio N, and magnetizing inductance of the transformer. The primary-side current is sensed through a current transformer and fed to the ISEN inputs of the chip; which means the turn ratio of the current transformer, along with its termination resistor introduces a gain scaling term. Register ceX_kslope_lm defines the normalized transformer primary magnetizing inductance.

If the ripple current magnitude falls outside of a configurable range, a current sense tracking fault will be issued. The enable of current track fault is user configurable.

The CE supports compensation of the following non-idealities associated with typical brick converter current sense schemes:

- The step induced by the parasitic inductance of the current sense trace resistor
- Output inductor variation with output current
- Leading-edge and falling-edge blanking time due to noise after PWM toggles

5.3.8 Load-line (Droop)

The XDPP1100 supports VOUT_DROOP in LINEAR11 format with exponent configurable from -7 to +2, which corresponds resolution from 0.0078125 mΩ to 4 mΩ. Each loop has the VOUT_DROOP configured independently. Each loop implements the droop calculation based on its own output current value.

The multi-segment droop is implemented for constant current and constant power operation. Multi-segment droop is a type of non-linear droop that allows user to define different droop resistance under different load current. If the loadline resistor is set high, output voltage will sag quickly when the current exceeds the set threshold, behavior similarly to constant current (CC) or constant power (CP) operation.

Figure 18 shows the behavior of multi-segment load-line. A load-line value of $R_{LL,neg}$ is used when the output current I_o is less than zero. This is meant to help current balancing in parallel module application. $R_{LL,1}$ is the regular droop resistance that defined by standard PMBus command VOUT_DROOP. From I_{thr_seg2} to I_{thr_seg3}, $R_{LL,2}$ is used to emulate constant current operation. From I_{thr_seg3} until the overcurrent shut down threshold $I_{OC,SD}$, $R_{LL,3}$ is used for approximate constant power operation. $I_{OC,SD}$ equals to the IOUT_OC_FAULT_LIMIT.

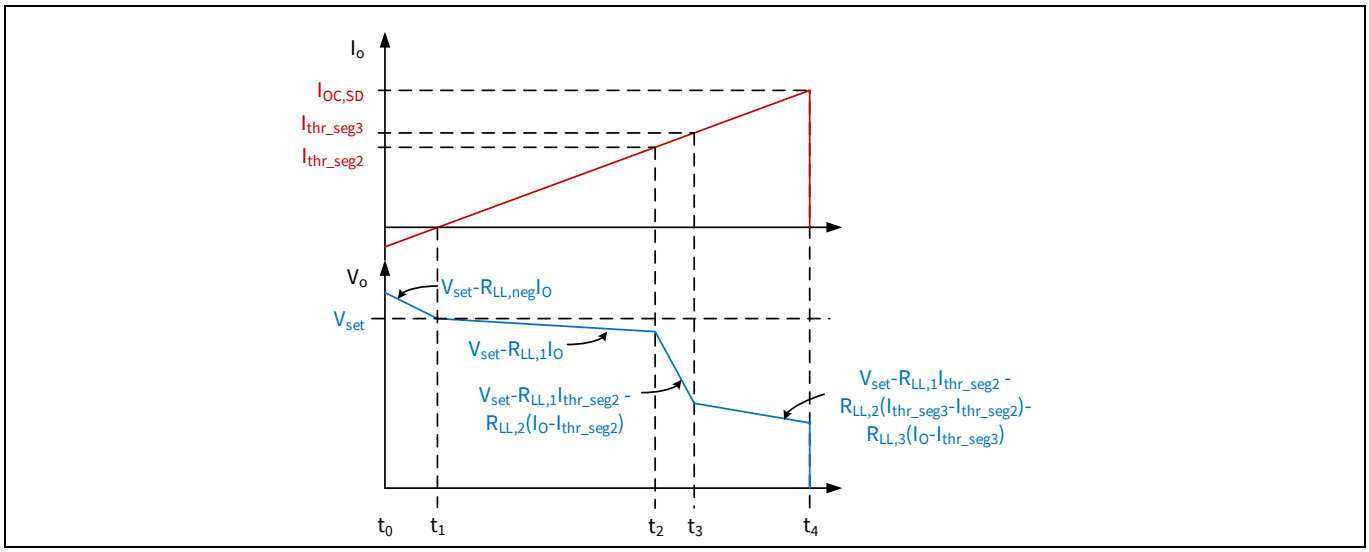

Figure 18 Load-line implementation for over-current protection

5.3.9 Fast Transient Response

The XDPP1100 implements fast transient response to half-bridge and full-bridge topologies. Upon the detection of a positive load transient the converter effectively saturates the rectified voltage by changing the switching period from T_{sw} to $2T_{on}$ where T_{on} is the product of duty cycle D and switching period. Since D varies with input voltage, the operating frequency during the transient is also dependent on input voltage.

Transient detection can be achieved by threshold voltage detection in the Vo sense as shown in Figure 19, or threshold of the derivative of the error voltage (not shown), or a combination of the two. The peak inductor current (i_L) depends on the load step Δi_o and input voltage (which determines the rate of rise of the inductor current.

Output voltage starts recover after a couple of FTR cycles when the current in output inductor is higher than load current. To avoid overshoot, the converter should exit FTR mode before Vout getting back to the set target voltage. The XDPP1100 exits FTR mode at a configurable error voltage threshold which is always below target Vout. The error voltage is defined as (target voltage - sense voltage). When the error voltage is smaller than the set threshold, the XDPP1100 exits FTR mode. At FTR exit, the XDPP1100 would complete the present FTR cycle then resume switching period back to T_{SW}, the linear loop then takes over for regulation.

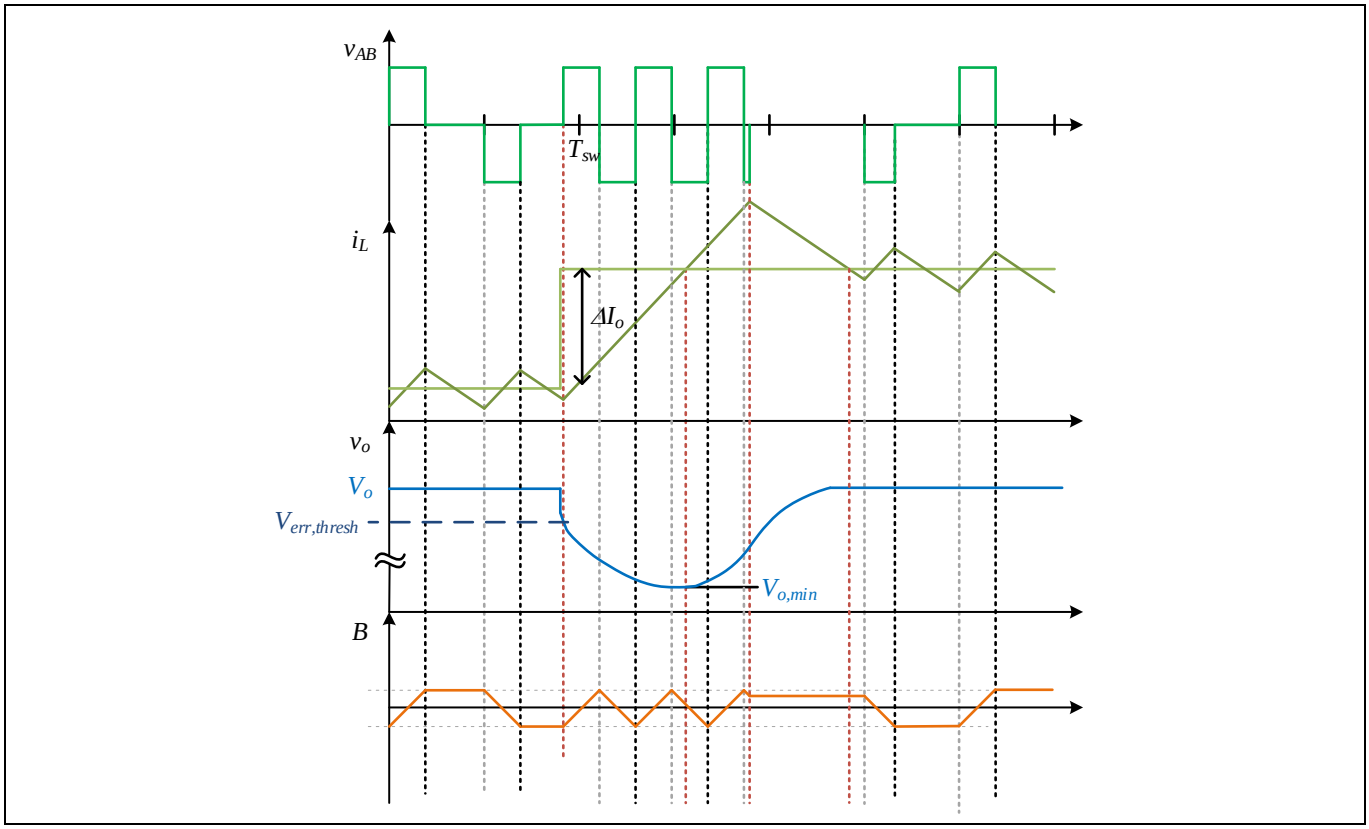

Figure 19 Waveforms of fast transient response with transformer protection

5.3.10 Input Voltage Feedforward

Input voltage feedforward involves using input and output voltage measurements to set the nominal duty cycle for the given conditions. Upon sensing a changing of input voltage, the XDPP1100 could quickly compensate duty cycle based on input voltage, output voltage, and the SRs condition. In an input voltage transient condition, feedforward response is much faster than output linear loop. In isolated converter with controller sitting at the secondary side, fast and accurate VRS sensing is critical to achieve high performance feedforward.

The XDPP1100 allows user to select one of the following sources for the feedforward computation.

- Sensed V_{RECT} on VRSEN inputs
- Sensed V_{RECT} on BVRSEN inputs
- Sensed V_{IN} on the PRISEN input (Telemetry sense V_{IN})
- pid_ff_vrect_override is provided for FW override of sensed V_{RECT}

Feedforward duty cycle calculation varies with topology, as defined in the equations below. The input voltage is measured, while target output voltage ($V_{o,target}$) and turns ratio are register settings.

$$D_{HB} = \frac{2 \times N \times V_{o,\,target}}{V_{in}}$$

$$D_{FB,\,ACF} = \frac{N \times V_{o,\,target}}{V_{in}}$$

$$D_{Buck} = \frac{V_{o,\,target}}{V_{in}}$$

HB: Half-bridge, FB: Full-Bridge, ACF: Active Clamp Forward.

5.3.11 Current Balancing

Current balancing is required for interleaved topologies. A PI compensation network is used in the current balance circuit. The current through each 'phase' is measured and compared to half the total. The error is compensated by the PI network which then adjusts the duty cycle appropriately.

An enable threshold applies to current balancing block. Current balancing only activates when the total current is higher than the enable threshold which has options of 0 A, 3 A and 5 A.

5.3.12 Current Sharing

Current sharing refers to balancing the current of individual power supplies that provide a common output voltage. One way to implement current sharing is to use IMON (section 5.2.5.1), shown in Figure 12 where the Ishare pin of each converter are connected and feed an external resistor R_{ishare}. The IDAC outputs a current proportional to the load current of the module. The sum of the currents generates a voltage across the resistor that is measured by the general ADC and used to identify how equal the current is shared between the two modules. Current sharing is a slow loop (ex. 10% of voltage loop bandwidth).

The second method of current sharing is passive and uses load-line (Section 5.3.8).

5.3.13 Flux Balancing

In full-bridge converters, timing mismatch can cause the applied volt-seconds across transformer during one half cycle to be greater than the volt-seconds during the opposite half cycle. This places a dc voltage across the transformer core leading to saturation due to 'flux walkaway.' To avoid this, PWM timing must be adjusted to balance each half cycle to account for practical timing differences.

The XDPP1100 implemented volt-second based flux balancing. It uses input voltage measurement and timing measurement during each half cycle. Error between the volt-second product of each half cycle is fed to a PI compensation network for duty cycle augmentation. The XDPP1100 use the rectified voltage (V_{RECT}) for voltage and timing measurement. The high speed edge comparator has 5ns accuracy for timing measurement, enables high performance flux balancing. The edge comparator has two configurable reference voltage thresholds: 500mV and 300mV. To have proper voltage sensing, the V_{RECT} voltage should be scaled properly. The recommended voltage range of VRSEN is 600 mV to 2 V.

Failure to achieve flux balance within a programmable number of cycles would generate a fault. More details of flux balancing and flux balance fault protection can be found in application note.

For V_{RECT} sensing, do not put filter cap to VRSEN pin to avoid waveform distortion. Route the VRSEN and VRREF in pairs for Kelvin sensing; keep the route away from other switching node to avoid noise coupling.

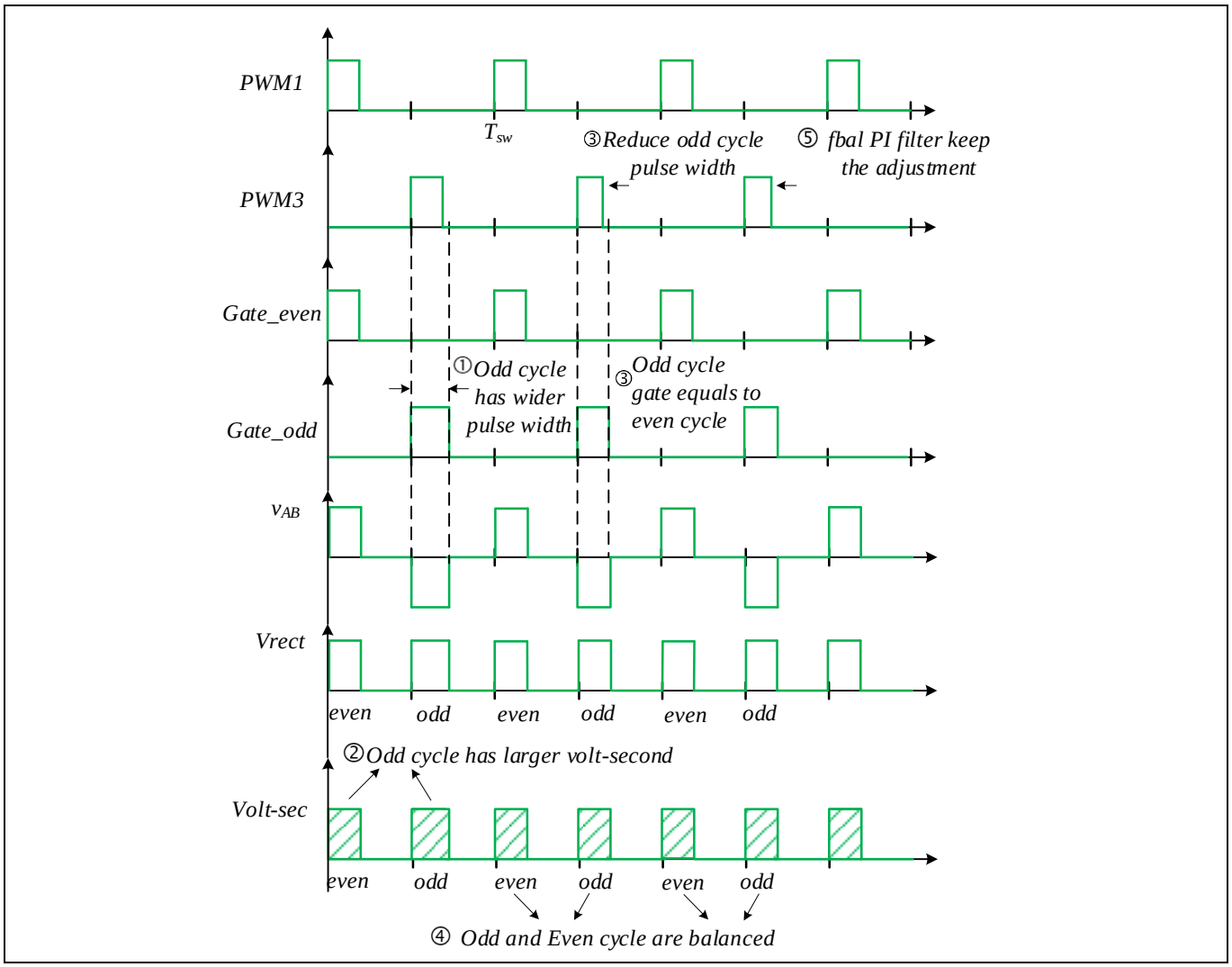

Figure 20 Volt-second flux balancing

5.3.14 Burst Mode

To increase light load efficiency, converter could enter burst mode to reduce switching losses. When the load current falls below the desired entry current level, the converter should enter burst mode operation. Converter stops switching when entering burst (burst-off). Switching is resumed when output voltage drops to a target level (burst-on). This target level defines output voltage ripple in burst mode. In burst mode, PID output is frozen to the value prior entering burst. Thus during burst-on period, converter works in constant on time mode. The SRs are turned off during burst mode. The frequency of the PWM bursts will be same as the switching frequency. Representative waveforms are shown in Figure 21. More details of the burst operation can be found in application note.

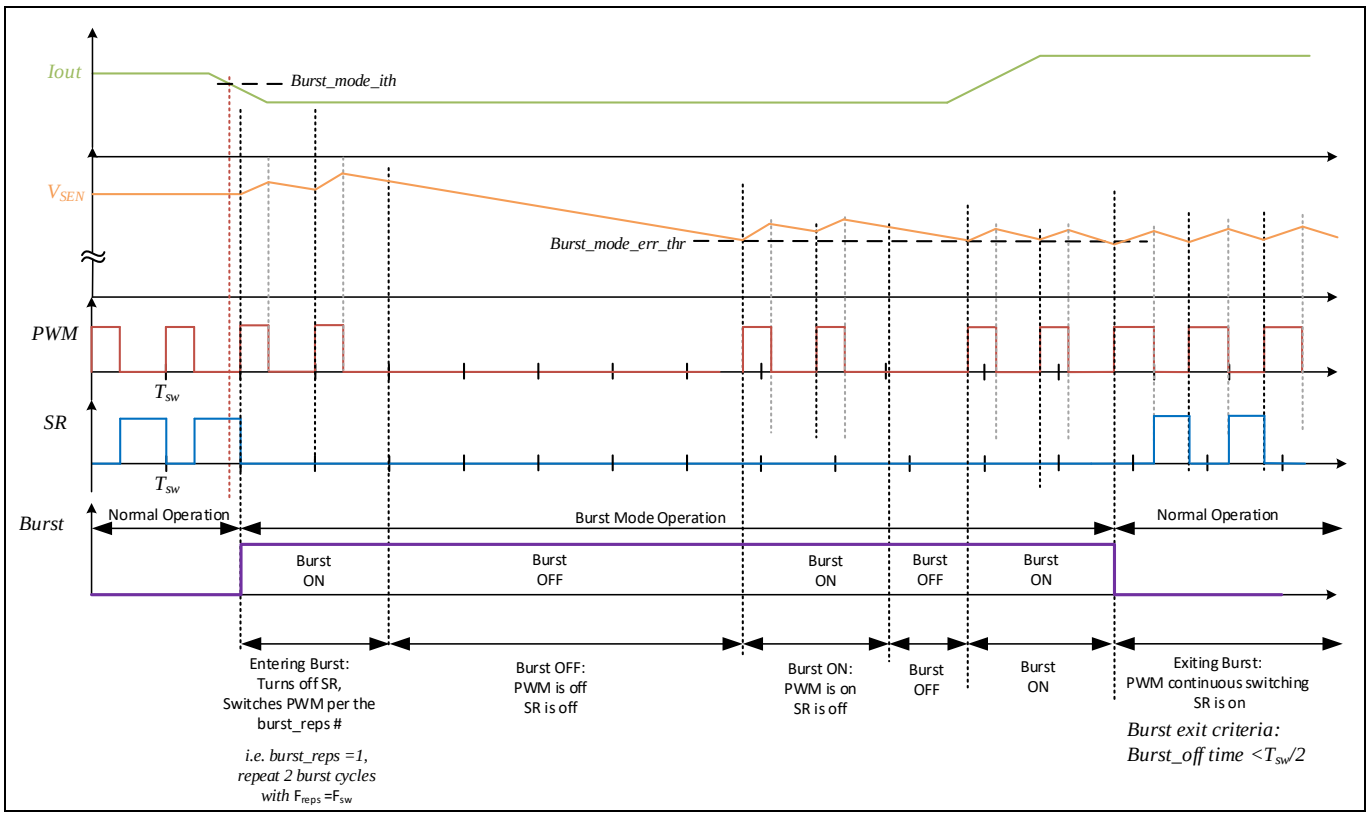

Figure 21 Waveforms in burst mode operation

5.4 Protection and Fault

The fault protection system has the following functions:

- Controller VDD under-voltage lock out (VDD UVLO)
- Input under/over-voltage protection (VIN_UV/VIN_OV)
- Input over current protection (IIN_OC)
- Input over power warning (PIN_OP)
- Output under/over-voltage protection (VOUT_UV/VOUT_OV)
- Output under/over-current protection (IOUT_UC/ IOUT_OC)
- Output over power warning (POUT_OP)
- Pulse-by-pulse peak current limit protection (PCL)
- Short circuit protection (SCP)
- Internal/external temperature protection (OT/ UT)
- Open/short sense line protection
- Flux balance fault
- Sync fault
- Current sharing fault
- SMBALERT#
- Configuration (CRC) failure
- I^2C communication failure

The protection block diagram is shown in Figure 22. The XDPP1100 implements all the fault protections without the need of using external comparators. More details of the fault protections can be found in application note.

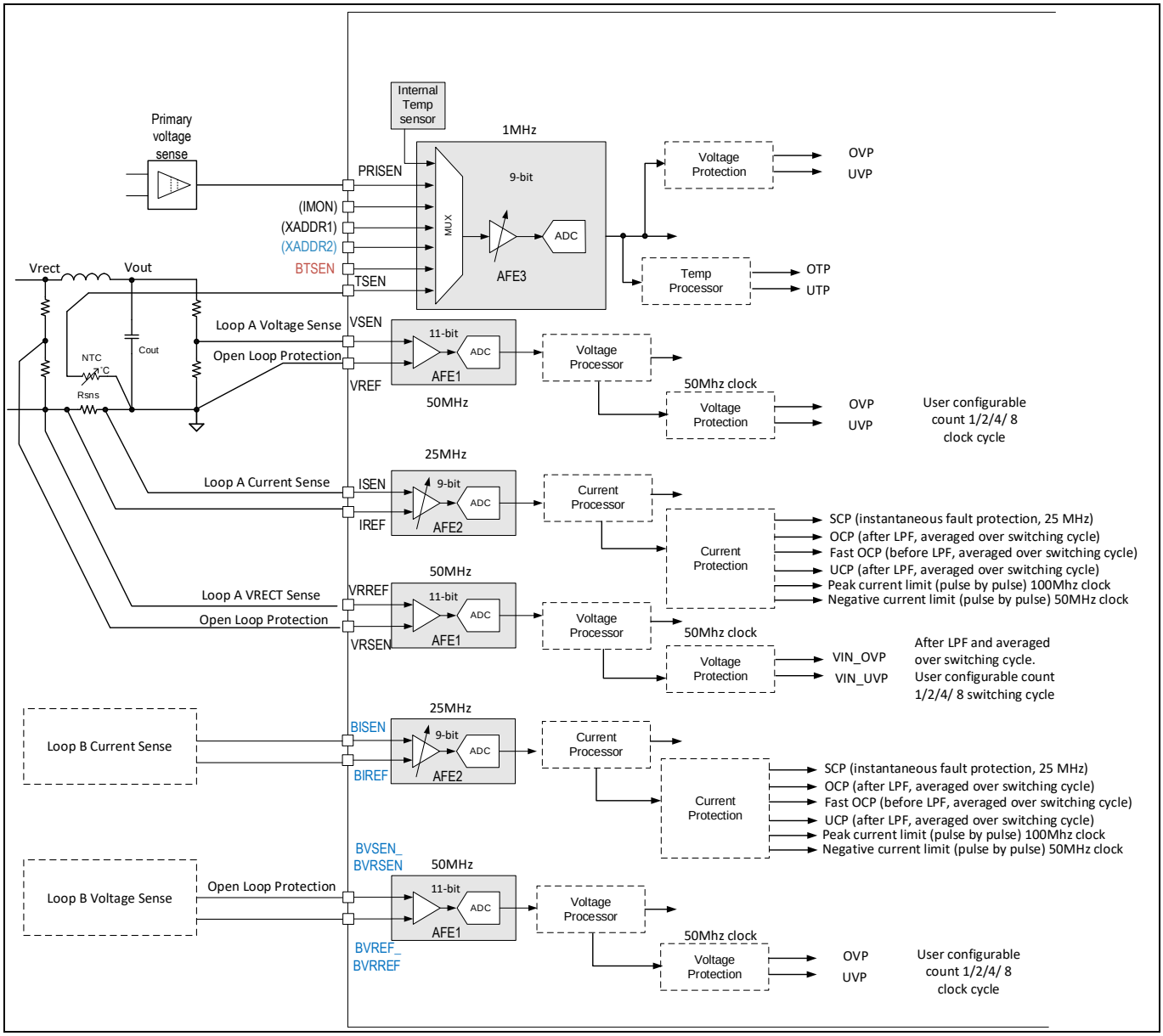

Figure 22 Protection block diagram

6 Application Information

All the topologies listed in this section are the standard topologies that the IC supports. The loop and PWM timing control of these topologies are pre-defined in the chip, reducing the users' effort on programming.

6.1 PWM full-bridge converter

6.1.1 PWM full-bridge with center tapped output in VMC

Typical connection of full-bridge converter with center tapped rectifier is shown in Figure 23:

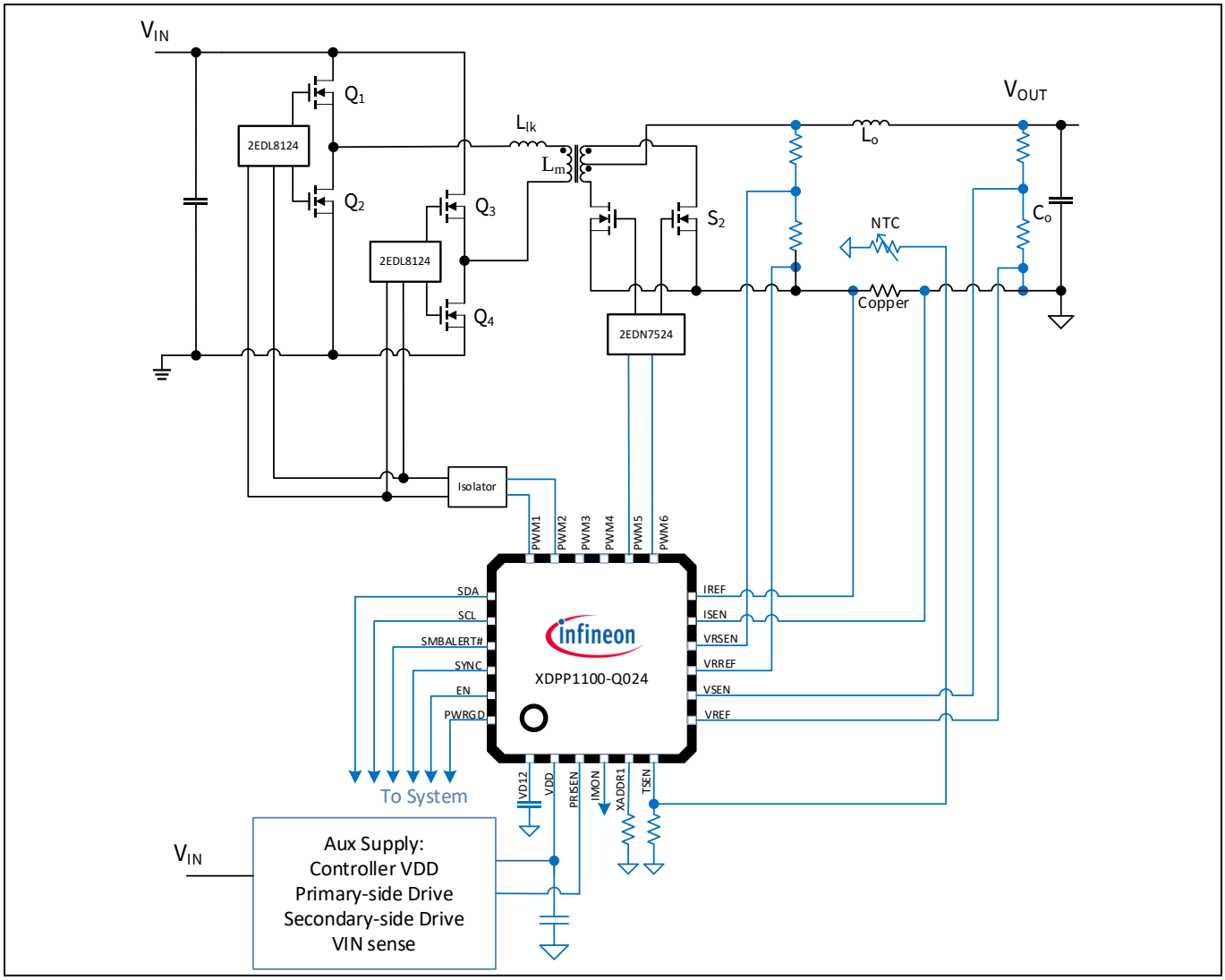

Figure 23 Full-bridge converter with center-tapped output in VMC

The XDPP1100 supports voltage mode control with flux balancing for full-bridge converter. The XDPP1100-Q024 is capable to control full-bridge converter with 2 PWM outputs driving primary MOSFETs, another 2 PWMs driving the secondary synchronous rectifier MOSFETs. The ISEN ADC is used for output current sensing.

The output voltage is differentially sensed and feed to VSEN the voltage ADC. The secondary current is sensed through PCB copper trace, with a temperature sensor put close to the copper trace to compensate the temperature shift of the resistance. The high precision current ADC provides 100 µV/LSB accuracy, allows

connecting the current sense signal directly to ISEN; eliminates the need of using external amplifier. Input voltage is sensed from the auxiliary power supply for telemetry as well as sensed at the transformer secondary side at the center-tapped point V_{RECT}. The V_{RECT} sensing is required for flux balancing and high performance voltage feed forward function. The XDPP1100 allows to config the input voltage telemetry and input voltage feedforward with different input source.

6.1.2 PWM full-bridge with PCMC

Typical connection of full-bridge converter with full-bridge rectifier in PCMC is shown in Figure 24.

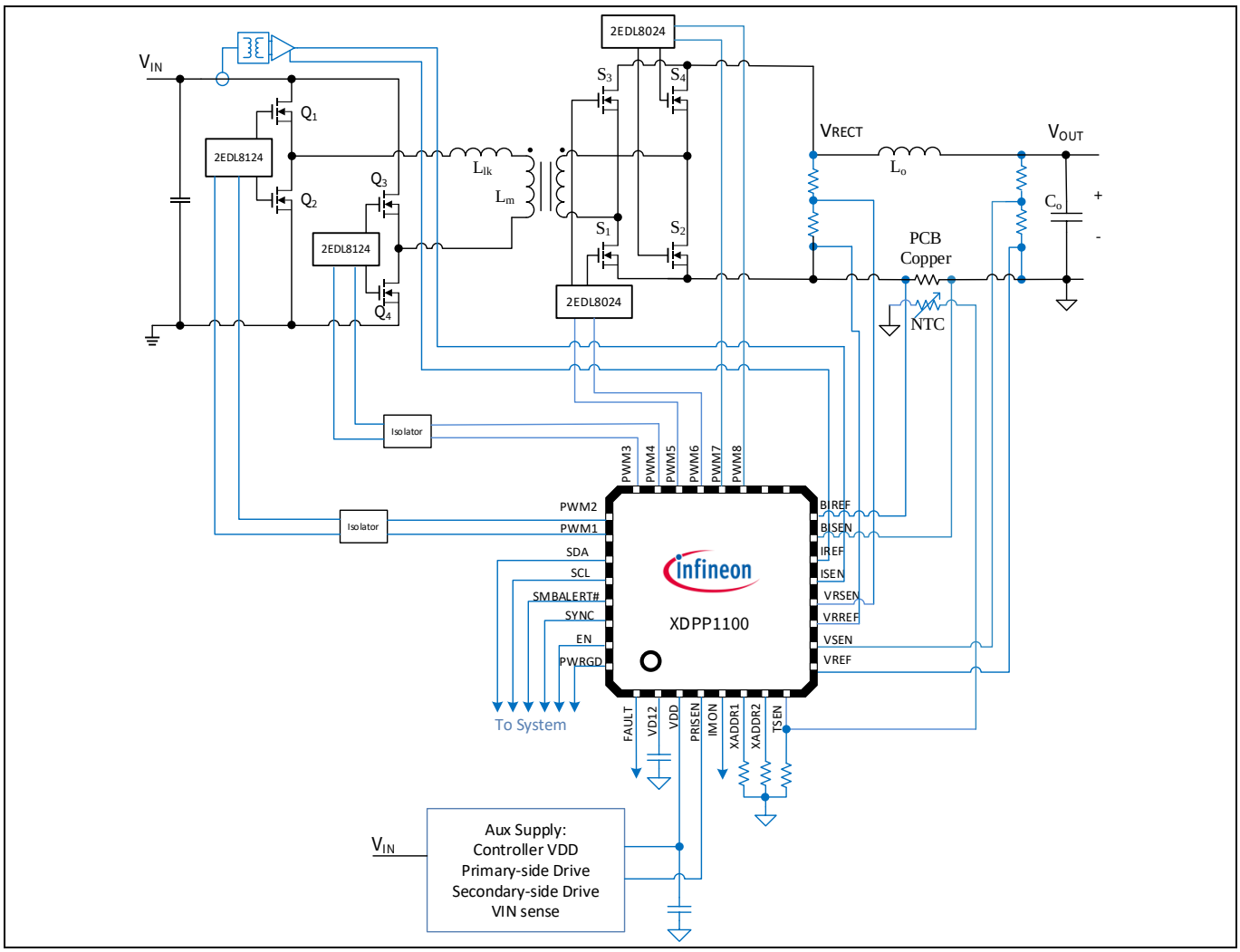

Figure 24 Full-bridge converter with full-bridge rectification PCMC

For full-bridge peak current mode control, XDPP1100-Q040 is recommended which enables both primary and secondary current sensing, as well as allows to program dead-time of each of the switches. In this diagram, 4 PWM outputs are used to drive primary MOSFETs, another 4 PWMs drive the secondary SR MOSFETs. Each MOSFET could have independent dead-time adjustment.

The primary current is sensed via current transformer and feeds to the ISEN/IREF inputs, enabled primary PCMC.

6.2 PWM half-bridge converter

Typical connection of half-bridge converter with center-tap output is shown in Figure 25.

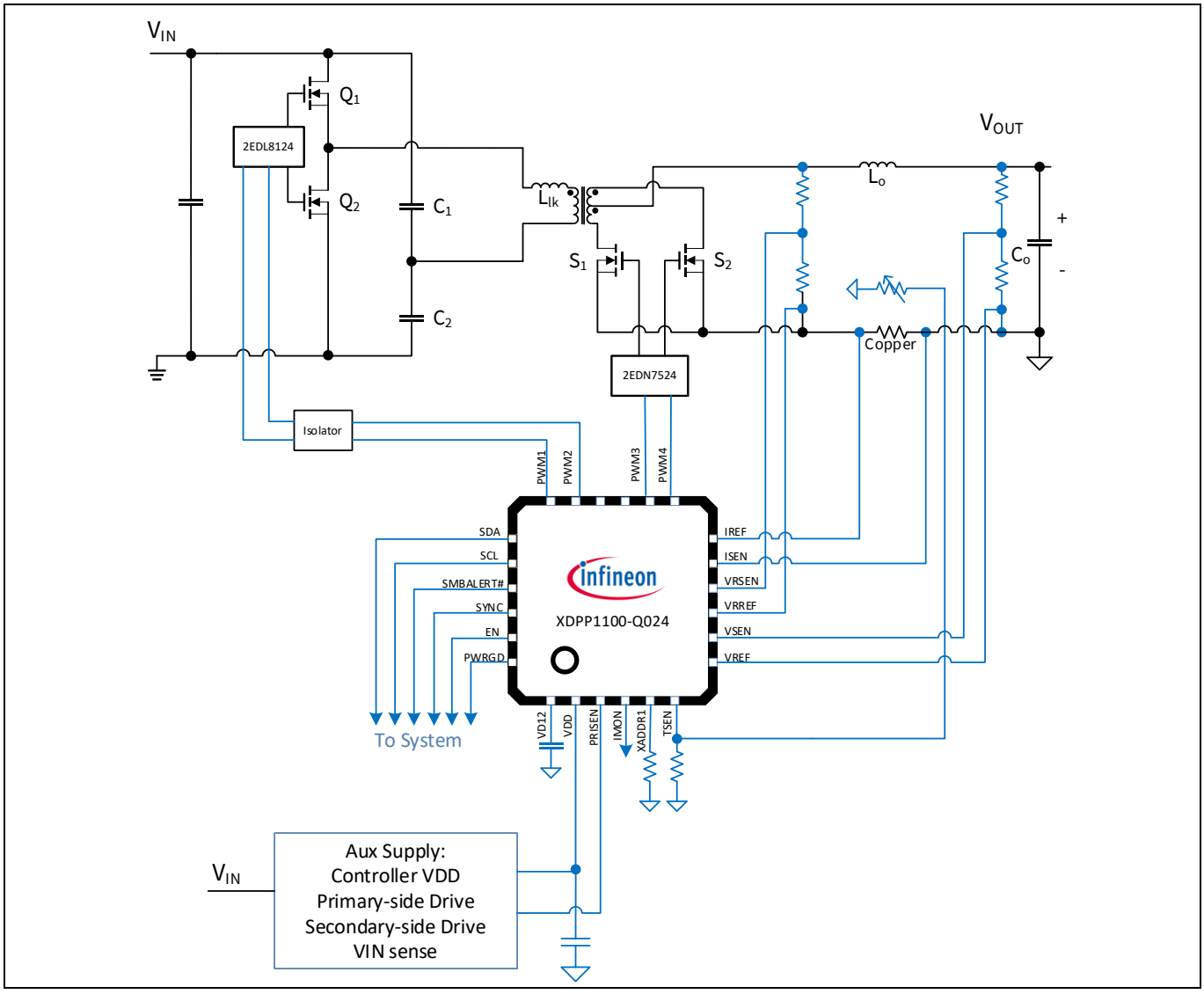

Figure 25 Half-bridge converter with center-tapped output windings

In this example the XDPP1100 controls a half-bridge using voltage mode control. The controller is on the secondary-side and senses primary input voltage via the rectified voltage from the secondary side of transformer. It also has the capability to sense primary voltage through the auxiliary power supply via PRISEN pin, which could get V_{IN} information when the main converter is in the off state. The primary current is estimated based on the measured secondary current, input and output voltage.

6.3 Active clamp forward converter

Another example of voltage mode control is active clamp forward (ACF) as shown in Figure 26. The primary clamp FET is a PMOS for easy gate driving. The controller is on the secondary-side and is sensing the rectified voltage, the output voltage, and the output current. The output current is sensed through PCB copper trace to minimize component count. A NTC thermistor should be placed very close to the current sense copper trace for temperature compensation.

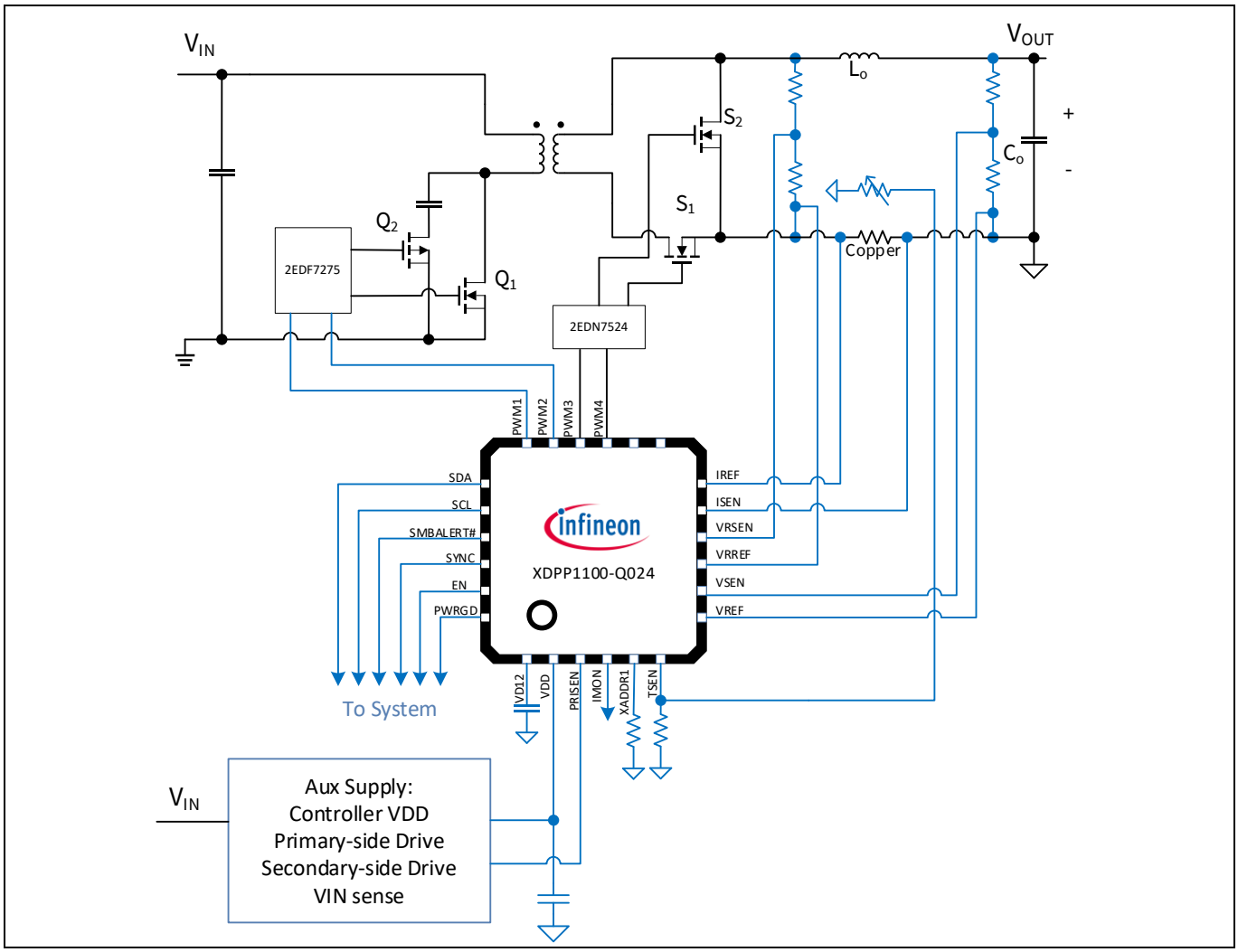

Figure 26 Active Clamp Forward converter

6.4 Interleaved Active Clamp Forward

The XDPP1100-Q040 supports interleaved topology. An example of interleaved ACF (IACF) is shown in Figure 27.

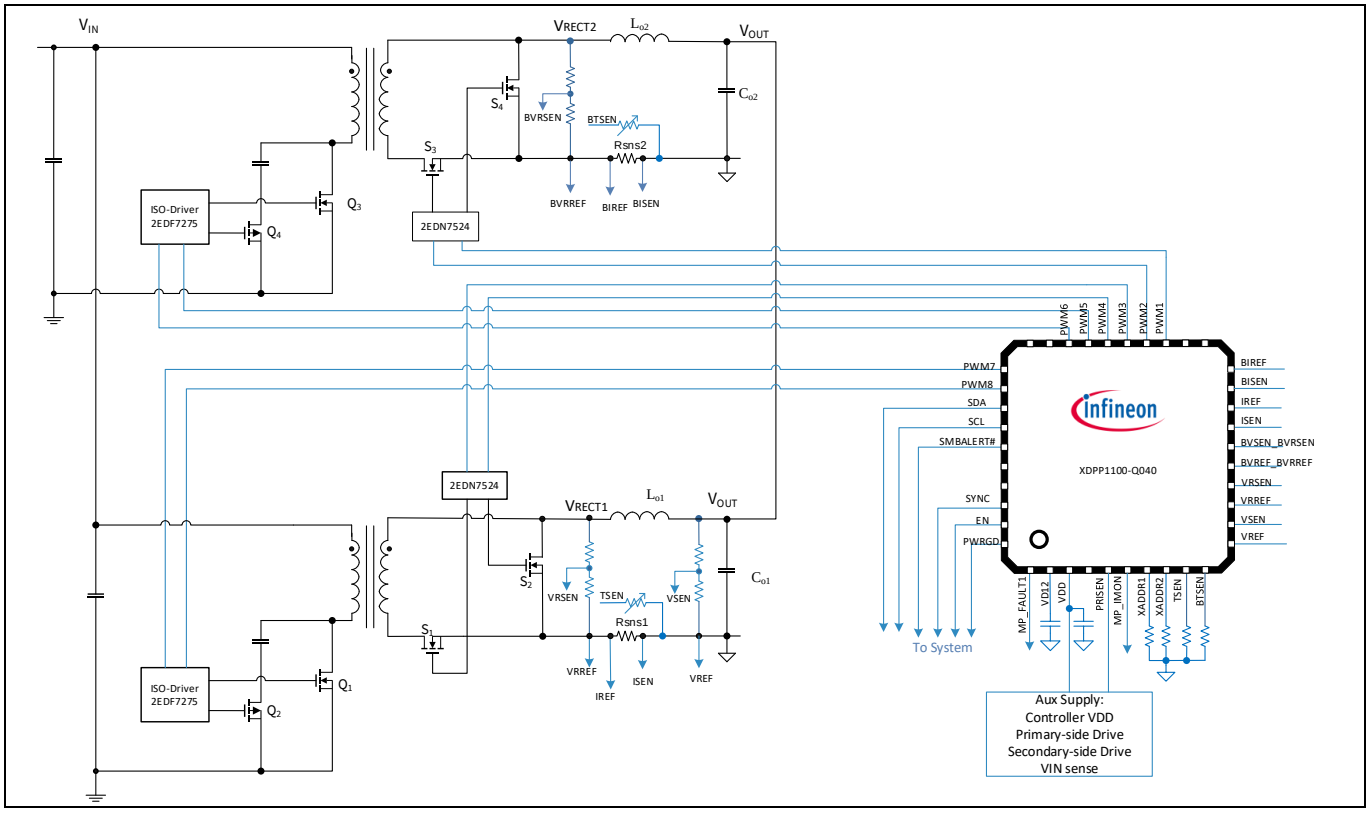

Figure 27 Interleaved –ACF converter

The two power supply stages, fed from the same input source, operate in parallel with their output inductors connected to a common capacitor bank. The phase shift between the interleaved phases is 180° for ripple cancellation. The output current in both phases are sensed, the converter could calculate total output current and balance the current in each phase.

6.5 Dual-Loop converter

The XDPP1100 supports up to two independent loops producing independent output voltages. As an example, a PWM-full-bridge with center-tapped rectification can implement a 12 V output, while an ACF can implement a 3.3 V output. Another option includes a series connection of the converter stages to provide pre- or post-regulation for the main converter.

Figure 28 is an example of dual half-bridge converters for two independent outputs. The input voltage can be sensed at VRSEN or PRISEN pins. The two loops could config the input voltage source independently. As the VRSEN is connected to the rectifier voltage of the first loop (V_{O1}), the second loop (V_{O2}) should choose PRISEN as the input voltage source, or choose VRSEN for input voltage source but only turns on when loop1 is in regulation.

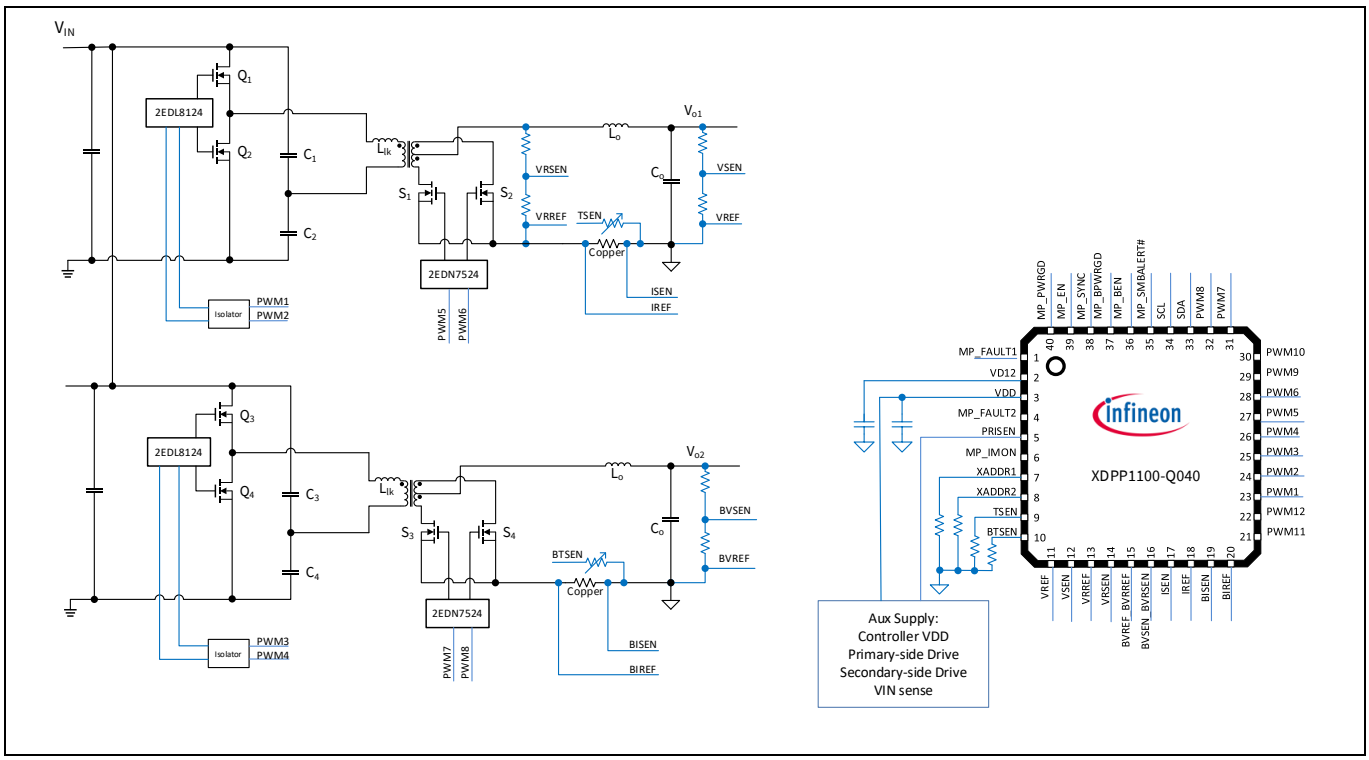

Figure 28 Dual Half-Bridge converters

6.6 Non-isolated converter

The XDPP1100 supports non-isolated DC/DC topologies such as Buck, Boost, and inverted Buck-Boost. Figure 29 is the typical connection of a Buck converter. Figure 30 is the examples of inverted Buck-Boost. For inverted Buck-Boost, the input voltage is negative reference to output ground.

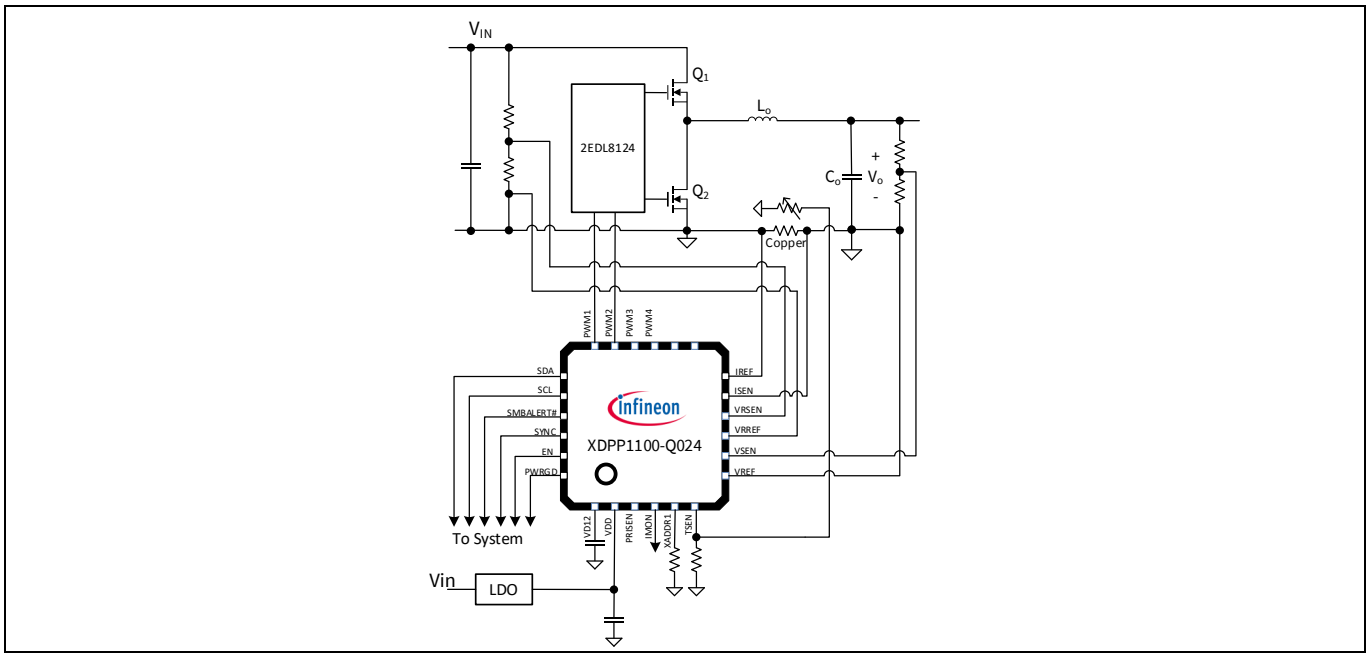

Figure 29 Buck converter

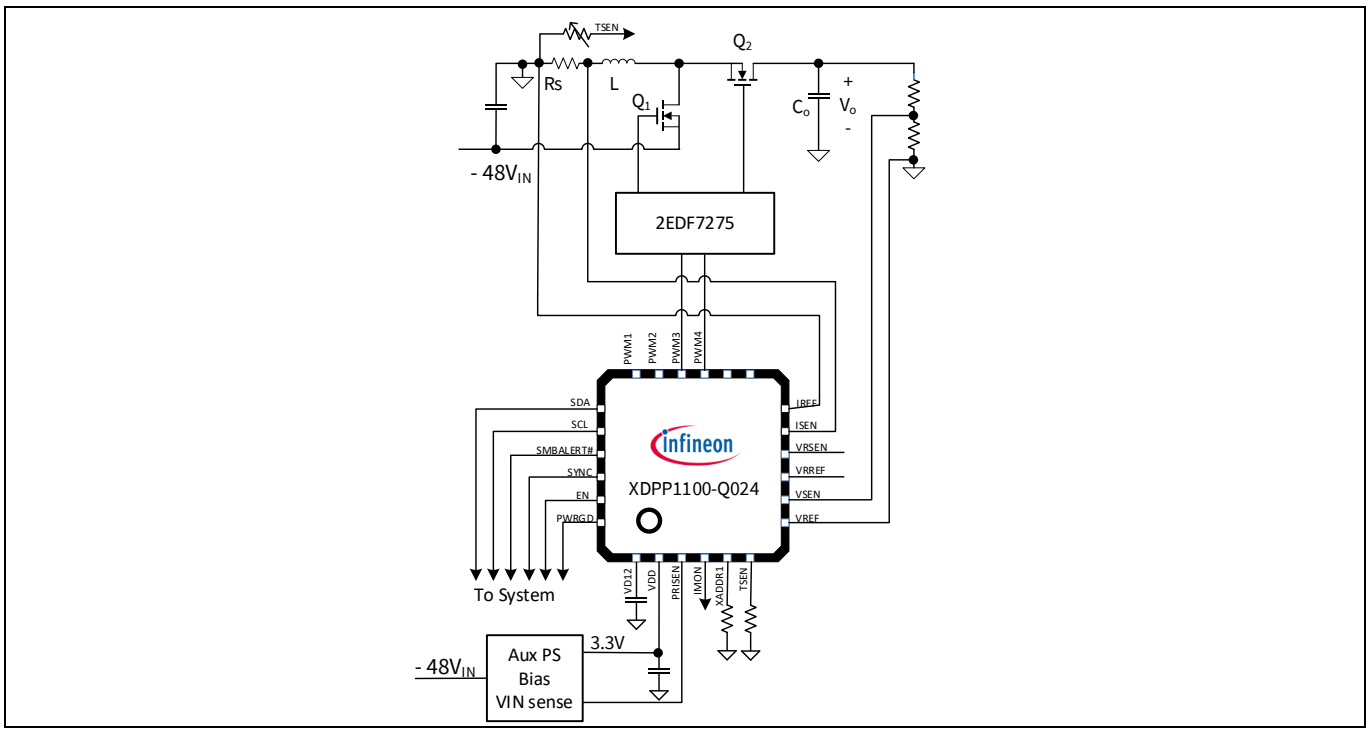

Figure 30 Inverted Buck-Boost converter

6.7 Layout Guidelines

In order to optimize voltage regulator performance, it is important to minimize the effects of printed circuit board parasitic impedances on the digital controller. The following layout techniques highlight important practices which should be incorporated in the layout process to optimize the heat-dissipating capabilities of the printed circuit board.

6.7.1 Component placement

Within the allotted implementation area, orient the switching components first. The switching components are the most critical because they carry large amounts of energy and tend to generate high levels of noise. Switching component placement should take into account power dissipation. Align the output inductors and MOSFETs such that space between the components is minimized.

Critical small signal components including the VDD and VD12 decoupling capacitors, ISEN resistors, TSEN capacitors, and voltage feedback RC filters should be placed near the controller.

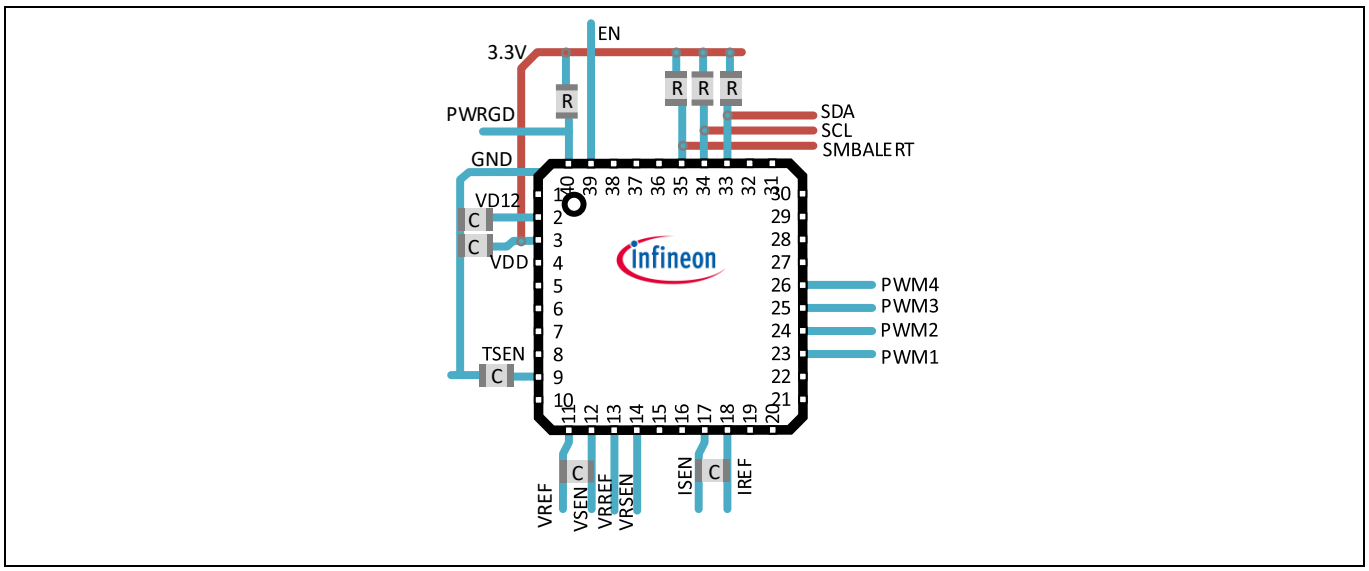

Figure 31 Decoupling cap placement and routing

6.7.2 Routing

For each voltage sense and current sense inputs, i.e. VSEN/VREF, ISEN/IREF, route the signal and its reference in differential pairs (Kelvin connection).

Avoid route the VRSEN/VRREF, BVRSEN/BVRREF near any switching nodes, especially in dual-loop or two-phase applications. Unlike output voltage sensing, VRSEN measures pulse signal thus it couldn't use filter cap for noise immunity. Keep the trace shielded by ground plane is recommended.

6.7.3 Sense output current by copper trace

The high resolution of IADC allows the XDPP1100 sense output current through very small PCB copper shunt, saving power loss and cost of precision sense resistor and Op-Amp. Use the following equation to calculate copper trace resistance.

$$R_{copper} = \rho \cdot \frac{L}{T \cdot W} \cdot (1 + tc \cdot (temp - 25))$$

ρ: resistivity of copper, $17 \cdot 10^{-6}\ \Omega\ mm$

L: Length of the copper trace

W: Width of the copper trace

T: Thickness of the copper trace

tc: temperature coefficient, $3.9 \cdot 10^{-3}\ /^{\circ}C$

temp: trace temperature, unit $^{\circ}C$

The thickness of copper trace is usually rated in ounces and represents the thickness of 1 ounce of copper rolled out to an area of 1 square of foot. 1 oz. copper has a thickness of 1.4 mils or 0.0356 mm. Here is a design example of copper shunt: 130 mil x 100 mil (L x W), top layer, 4 Oz copper, trace resistance is 0.158 mΩ.

It is recommended to layout the copper trace shunt in the first mid layer, so that the XDPP1100 controller could be placed right on top of the shunt trace for the shortest routing distance. Also put a ground shielding layer next to the copper sense layer to reduce stray inductance for better current sense accuracy.

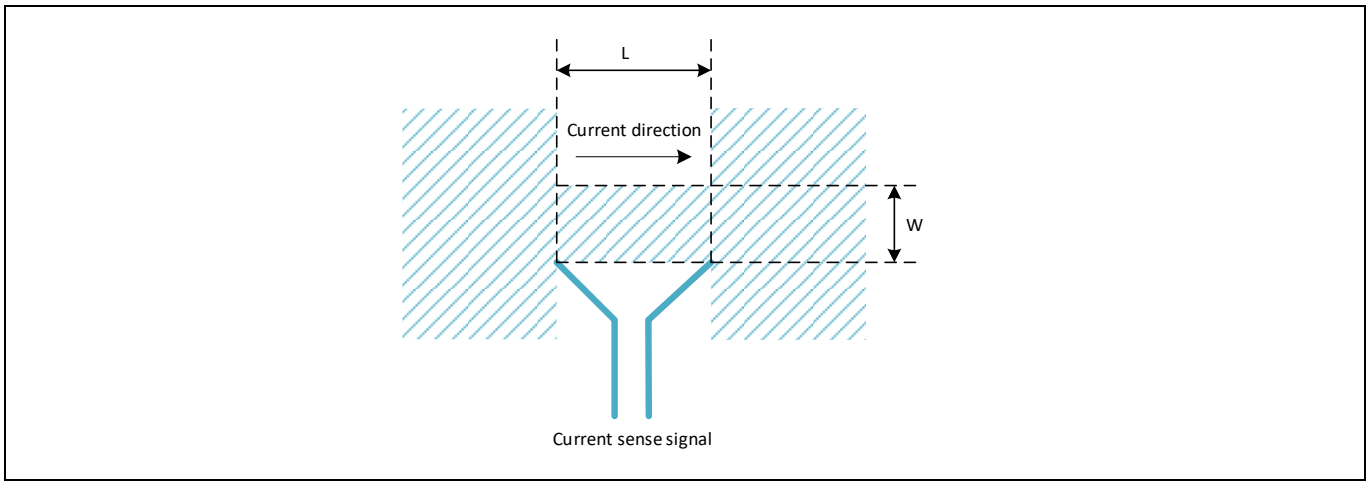

Figure 32 Current sense by copper trace

7 Package Information

7.1 XDPP1100-Q024 QFN 4x4 – 24pin

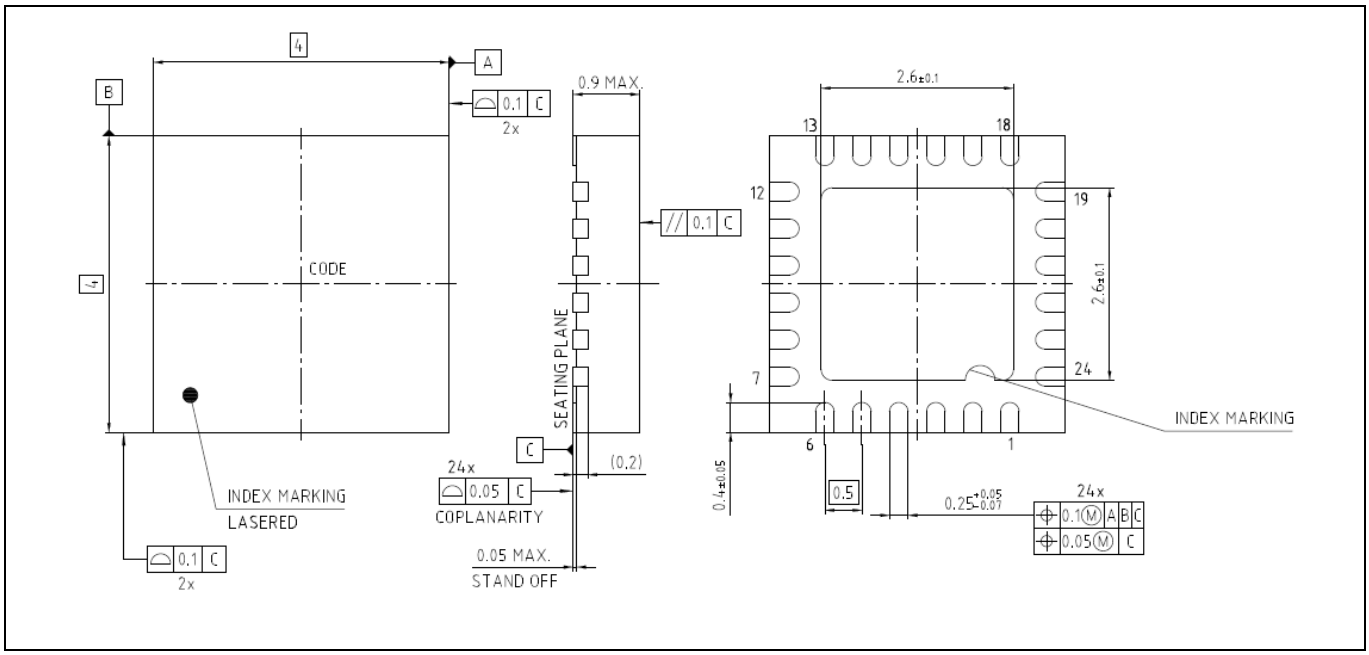

Figure 33 PG-VQFN-24-20

7.2 XDPP1100-Q040 QFN 6x6 – 40pin

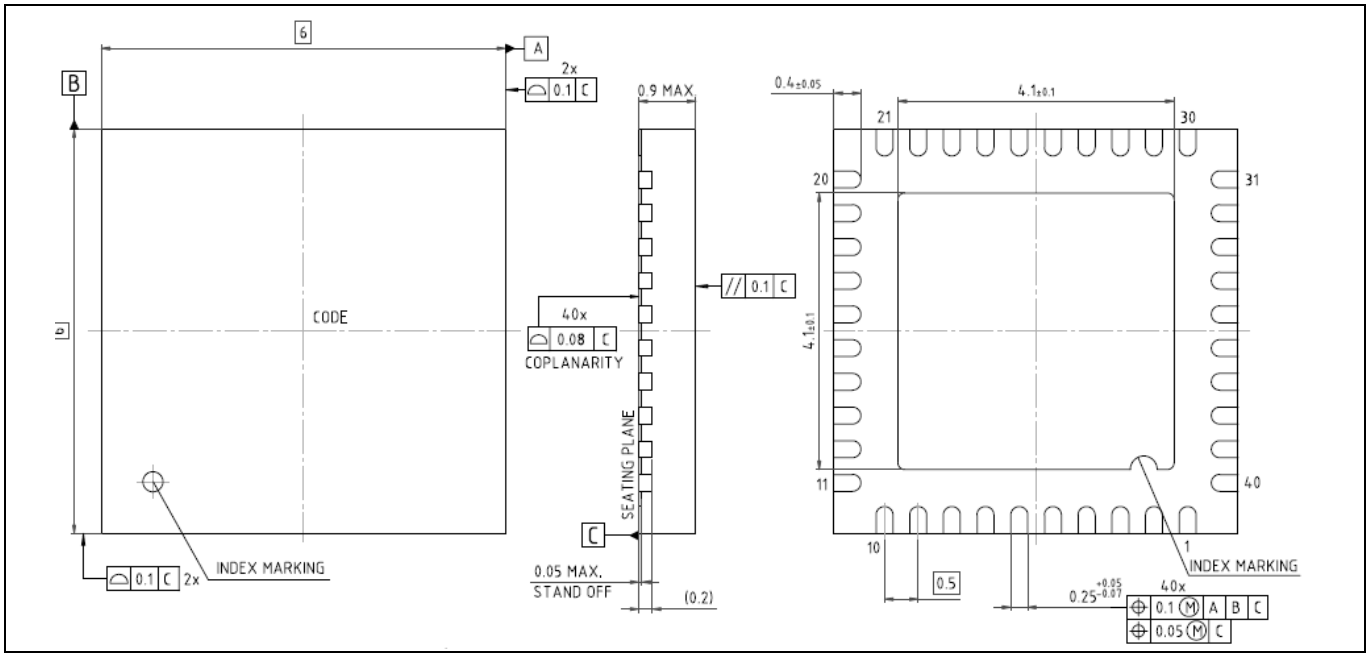

Figure 34 PG-VQFN-40-19

7.3 Part Marking

The part marking shows in Figure 35.

XDPP1100-Q024

XDPP1100-Q040

Figure 35 Package Marking

Examples of Lot number and Date code:

Lot number: 1YUS1ANNB03

Date code: H2018B03

The B03 at the end of date code is the last 3 digits of the lot number.

Revision history

Document version	Date of release	Description of changes
Revision 2.0	2020-11-20	Final data sheet
Revision 2.1	2021-07-28	Update SDA, SCL, SMBALERT V_{IH_MIN} threshold, from 2.3 V to 2.1 V (3.3 V mode), from 1.4 V to 1.35 V (1.8 V mode). Add GPIO spec GPIO Inputs/Outputs of PWRGD, BPWRGD, PWM6, PWM11 (Table 19) Update GPIO spec (Table 18), V_{IH_MIN} threshold, from 2.3 V to 2.1 V

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