Document Number: A2T21H450W19S
Rev. 0, 9/2016

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 89 W asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 2110 to 2200 MHz.

2100 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 30 Vdc, I_{DQA} = 800 mA, V_{GSB} = 0.7 Vdc, P_{out} = 89 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

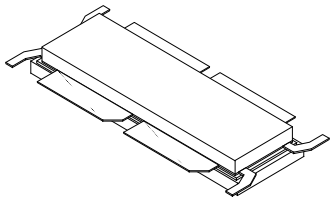
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
2110 MHz	15.7	46.1	8.0	–31.4
2145 MHz	15.7	46.2	8.0	–33.9
2180 MHz	15.7	45.9	7.8	–36.1
2200 MHz	15.6	45.4	7.8	–35.6

Features

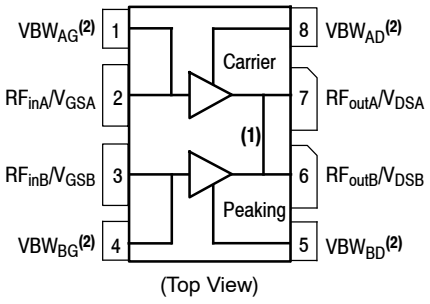
- Advanced High Performance In-Package Doherty
- Designed for Wide Instantaneous Bandwidth Applications
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Able to Withstand Extremely High Output VSWR and Broadband Operating Conditions
- Designed for Digital Predistortion Error Correction Systems

A2T21H450W19SR6

2110–2200 MHz, 89 W AVG., 30 V AIRFAST RF POWER LDMOS TRANSISTOR



NI-1230S-4S4S



(Top View)

Figure 1. Pin Connections

1. Pin connections 6 and 7 are DC coupled and RF independent.
2. Device cannot operate with V_{DD} current supplied through pins 1, 4, 5 and 8.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +125	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C
CW Operation @ T_C = 25°C Derate above 25°C	CW	236 1.3	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 74°C, 89 W Avg., W-CDMA, 30 Vdc, I_{DQA} = 800 mA, V_{GSB} = 0.7 Vdc, 2145 MHz	$R_{\theta JC}$	0.26	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (4)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	5	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics - Side A, Carrier					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 200 μAdc)	$V_{GS(th)}$	1.2	1.8	2.1	Vdc
Gate Quiescent Voltage (V_{DD} = 30 Vdc, I_D = 800 mAdc, Measured in Functional Test)	$V_{GSA(Q)}$	2.1	2.5	2.9	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	0.05	0.17	0.3	Vdc
On Characteristics - Side B, Peaking					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 300 μAdc)	$V_{GS(th)}$	0.8	1.3	1.6	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 3 Adc)	$V_{DS(on)}$	0.05	0.15	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.nxp.com/RF/calculators.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.
4. Side A and Side B are tied together for these measurements.

(continued)

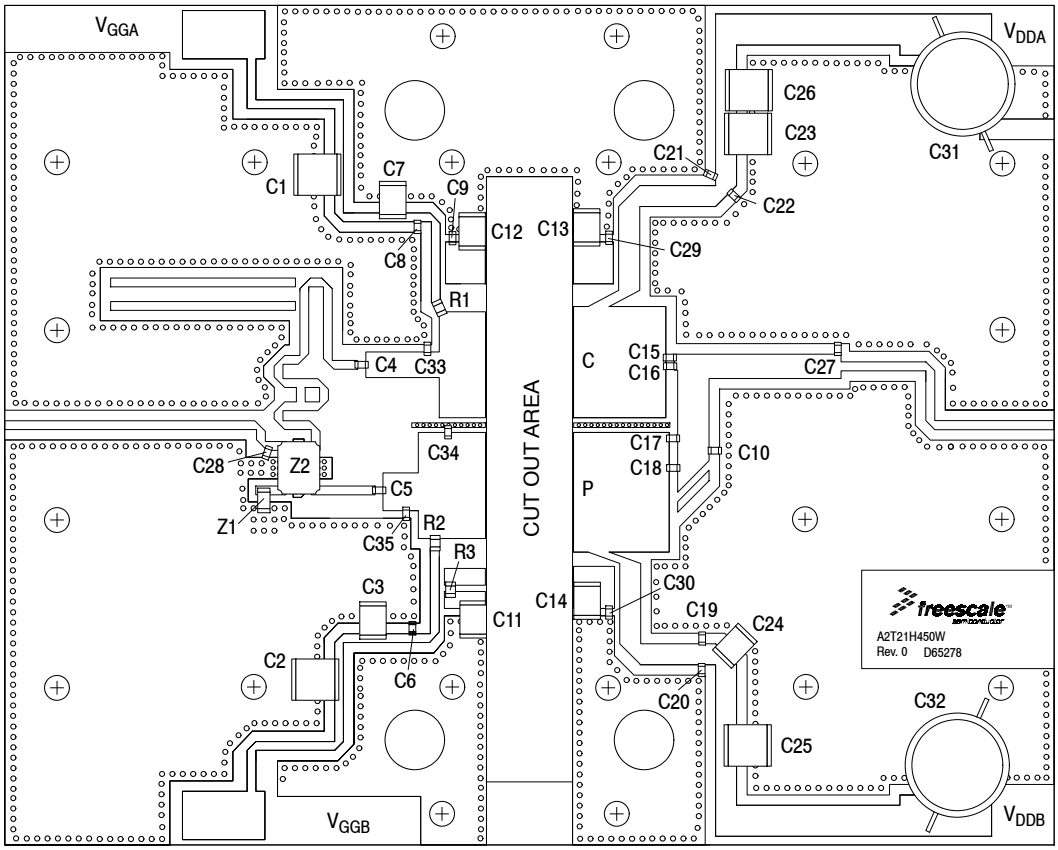
Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1,2,3) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 30 Vdc, I_{DQA} = 800 mA, V_{GSB} = 0.7 Vdc, P_{out} = 89 W Avg., f = 2110 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	14.5	15.7	17.5	dB
Drain Efficiency	η_D	43.0	46.1	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	7.3	8.0	—	dB
Adjacent Channel Power Ratio	ACPR	—	–31.4	–29.5	dBc
Load Mismatch (3) (In Freescale Doherty Test Fixture, 50 ohm system) I_{DQA} = 800 mA, V_{GSB} = 0.7 Vdc, f = 2145 MHz, 12 μsec(on), 10% Duty Cycle					
VSWR 10:1 at 32 Vdc, 560 W Pulsed CW Output Power (3 dB Input Overdrive from 513 W Pulsed CW Rated Power)	No Device Degradation				
Typical Performance (3) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 30 Vdc, I_{DQA} = 800 mA, V_{GSB} = 0.7 Vdc, 2110–2180 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	390 (4)	—	W
P_{out} @ 3 dB Compression Point (5)	P3dB	—	525	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2110–2180 MHz bandwidth)	Φ	—	–26	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	150	—	MHz
Gain Flatness in 70 MHz Bandwidth @ P_{out} = 89 W Avg.	G_F	—	0.15	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.011	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C) (4)	ΔP1dB	—	0.006	—	dB/°C

Table 5. Ordering Information

Device	Tape and Reel Information	Package
A2T21H450W19SR6	R6 Suffix = 150 Units, 56 mm Tape Width, 13-inch Reel	NI-1230S-4S4S

1. V_{DDA} and V_{DDB} must be tied together and powered by a single DC power supply.
2. Part internally matched both on input and output.
3. Measurements made with device in an asymmetrical Doherty configuration.
4. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.
5. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.



Note: V_{DDA} and V_{DDB} must be tied together and powered by a single DC power supply.

Figure 2. A2T21H450W19SR6 Test Circuit Component Layout

Table 6. A2T21H450W19SR6 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C23, C25, C26	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C3, C7, C11, C12, C13, C14, C24	4.7 μF Chip Capacitors	C4532X7S2A475M230KB	TDK
C4, C5, C6, C8, C9, C19, C20, C21, C22, C29, C30	10 pF Chip Capacitors	ATC600S100JT250XT	ATC
C10, C28	0.5 pF Chip Capacitors	ATC600S0R5BT250XT	ATC
C15, C16	3 pF Chip Capacitors	ATC600S3R0BT250XT	ATC
C17, C18	8.2 pF Chip Capacitors	ATC600S8R2BT250XT	ATC
C27	0.2 pF Chip Capacitor	ATC600S0R2BT250XT	ATC
C31, C32	220 μF, 100 V Electrolytic Capacitors	EEVFK2A221M	Panasonic-ECG
C33, C35	0.6 pF Chip Capacitors	ATC600S0R6BT250XT	ATC
C34	1.1 pF Chip Capacitor	ATC600S1R1BT250XT	ATC
R1, R2	3.3 Ω, 1/8 W Chip Resistors	WCR0805-3R3F	Welwyn
R3	10 Ω, 1/8 W Chip Resistor	WCR0805-10RF	Welwyn
Z1	50 Ω, 10 W Surface Mount Terminator	C10A50Z4	Anaren
Z2	2000–2300 MHz Band, 90°, 5 dB Directional Coupler	X3C21P1-05S	Anaren
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D65278	MTL

TYPICAL CHARACTERISTICS — 2110–2180 MHz

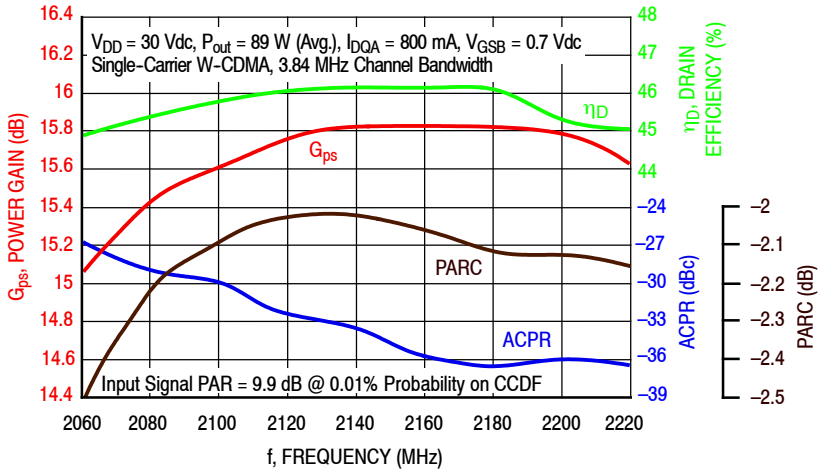


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 89 Watts Avg.

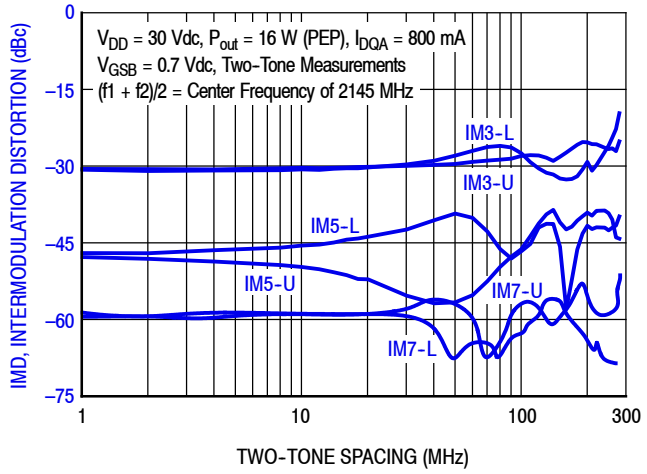


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

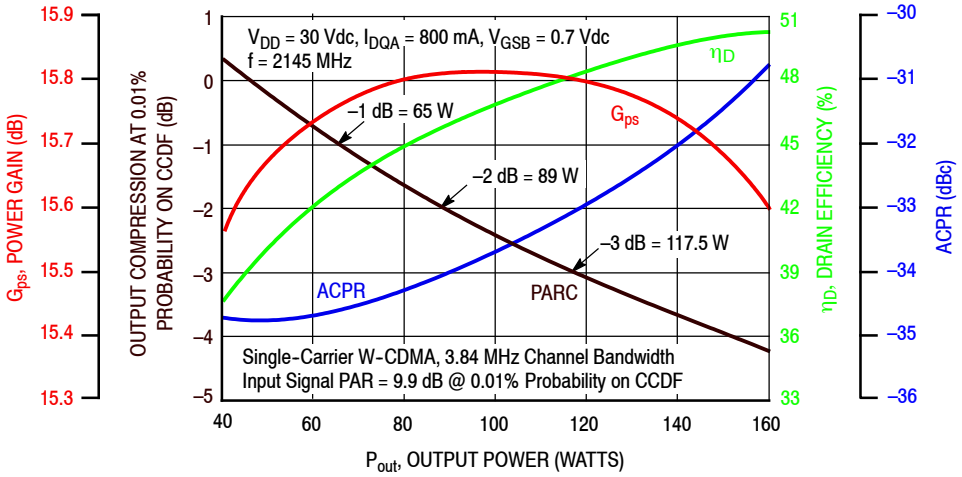


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 2110–2180 MHz

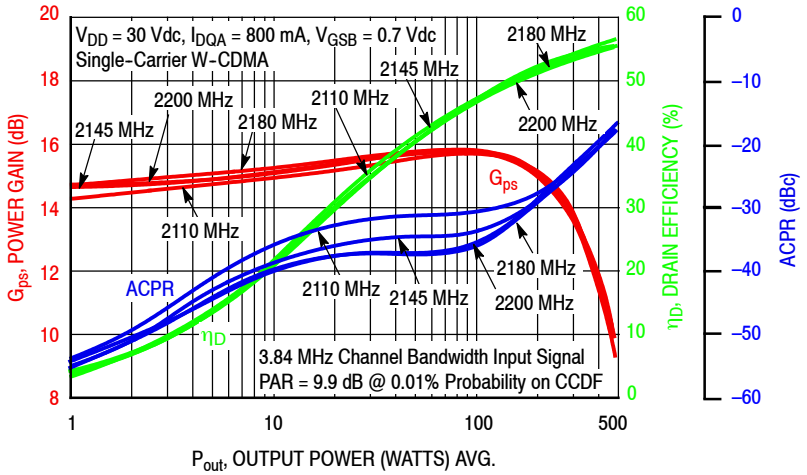


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

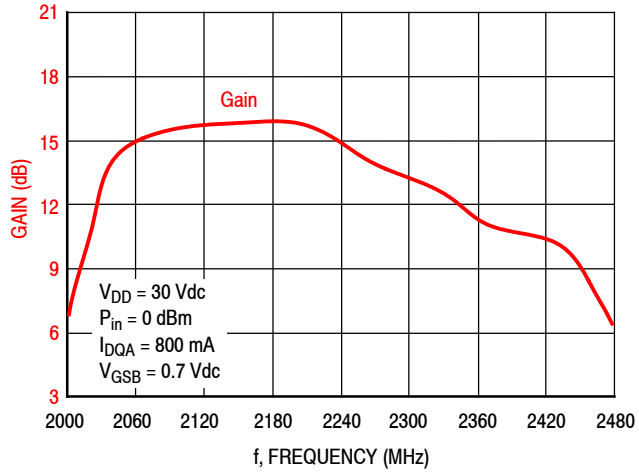


Figure 7. Broadband Frequency Response

Table 7. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 30 Vdc, I_{DQA} = 800 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	1.39 – j6.73	1.34 + j6.50	1.16 – j4.54	16.8	53.9	243	58.6	–10
2140	1.37 – j6.83	1.50 + j6.72	1.12 – j4.39	16.9	53.8	241	58.1	–11
2170	1.51 – j7.19	1.74 + j7.00	1.13 – j4.33	16.9	53.7	236	58.1	–12

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	1.39 – j6.73	1.24 + j6.66	1.12 – j4.64	14.6	54.6	288	59.4	–15
2140	1.37 – j6.83	1.41 + j6.91	1.11 – j4.55	14.7	54.5	283	58.8	–16
2170	1.51 – j7.19	1.65 + j7.21	1.11 – j4.49	14.7	54.4	277	58.4	–16

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 8. Carrier Side Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 30 Vdc, I_{DQA} = 800 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	1.39 – j6.73	1.28 + j6.62	2.70 – j3.63	19.4	51.9	155	70.8	–18
2140	1.37 – j6.83	1.43 + j6.86	2.64 – j3.15	19.7	51.4	139	70.5	–20
2170	1.51 – j7.19	1.67 + j7.16	2.53 – j2.96	19.7	51.3	134	69.7	–21

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	1.39 – j6.73	1.19 + j6.71	2.34 – j4.10	16.9	53.2	209	70.3	–21
2140	1.37 – j6.83	1.36 + j6.97	2.37 – j3.82	17.2	52.9	195	69.5	–23
2170	1.51 – j7.19	1.60 + j7.28	2.23 – j3.76	17.0	53.0	199	68.6	–23

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

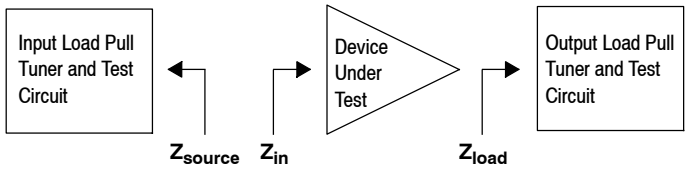


Table 9. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 30 Vdc, V_{GSB} = 0.7 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	0.91 – j5.28	1.01 + j5.04	2.20 – j4.87	14.7	56.2	413	55.6	–30
2140	1.15 – j5.62	1.16 + j5.29	2.33 – j4.74	14.8	56.1	409	56.0	–31
2170	1.45 – j5.72	1.42 + j5.60	2.34 – j4.65	15.0	56.0	402	55.5	–30

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	0.91 – j5.28	1.05 + j5.19	2.32 – j5.14	12.5	56.9	487	58.4	–38
2140	1.15 – j5.62	1.23 + j5.47	2.41 – j5.02	12.6	56.8	481	58.0	–38
2170	1.45 – j5.72	1.52 + j5.79	2.46 – j4.90	12.8	56.7	472	57.4	–36

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

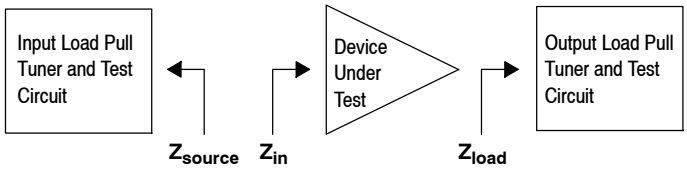
Table 10. Peaking Side Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 30 Vdc, V_{GSB} = 0.7 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	0.91 – j5.28	0.95 + j5.01	4.20 – j2.40	15.7	54.4	277	65.5	–37
2140	1.15 – j5.62	1.09 + j5.26	3.55 – j2.11	15.8	54.4	274	64.9	–37
2170	1.45 – j5.72	1.31 + j5.54	3.09 – j2.00	16.0	54.3	271	65.4	–37

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	0.91 – j5.28	1.01 + j5.17	4.09 – j3.52	13.6	55.7	371	63.3	–43
2140	1.15 – j5.62	1.17 + j5.44	3.96 – j2.72	13.6	55.4	343	62.8	–44
2170	1.45 – j5.72	1.43 + j5.76	3.52 – j2.02	13.9	54.9	312	63.4	–44

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 2140 MHz

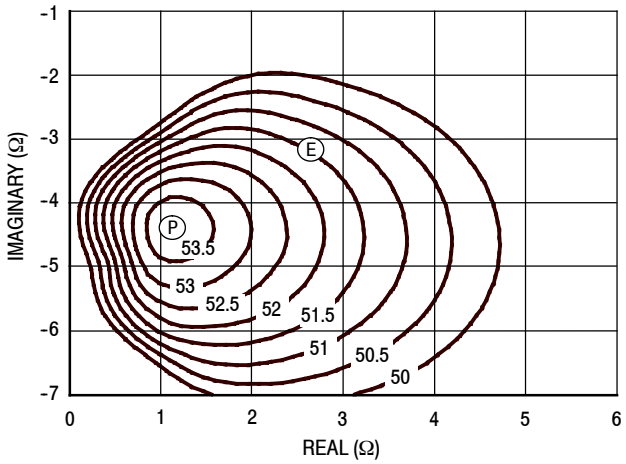


Figure 8. P1dB Load Pull Output Power Contours (dBm)

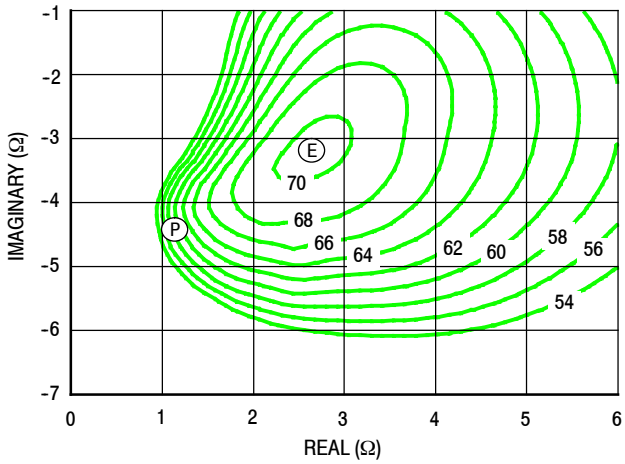


Figure 9. P1dB Load Pull Efficiency Contours (%)

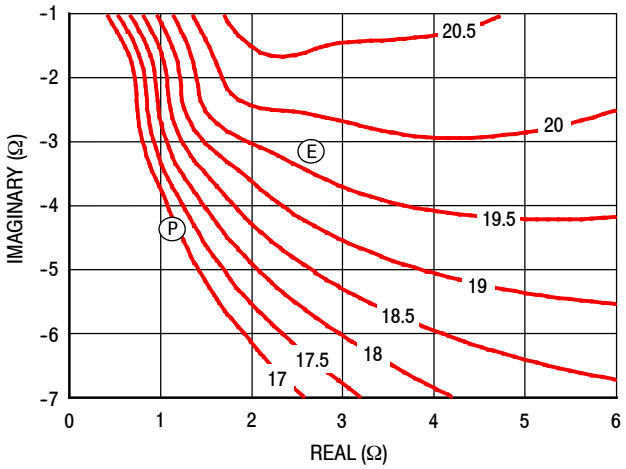


Figure 10. P1dB Load Pull Gain Contours (dB)

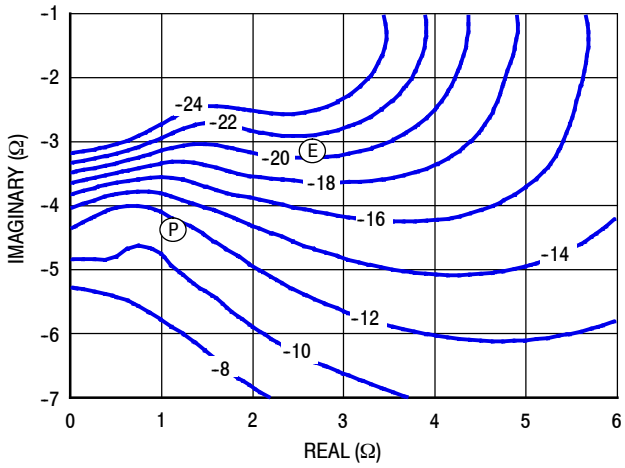


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 2140 MHz

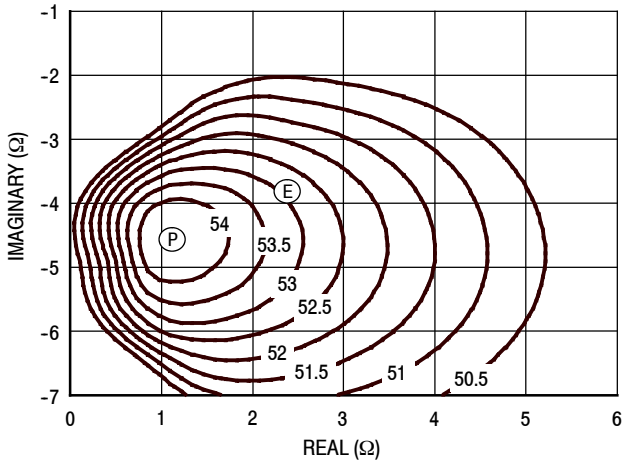


Figure 12. P3dB Load Pull Output Power Contours (dBm)

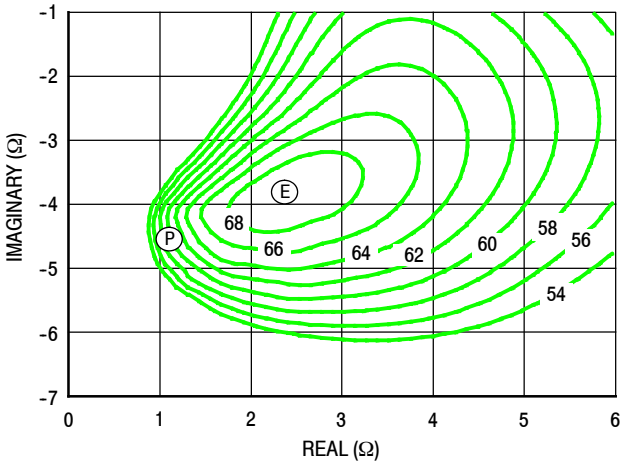


Figure 13. P3dB Load Pull Efficiency Contours (%)

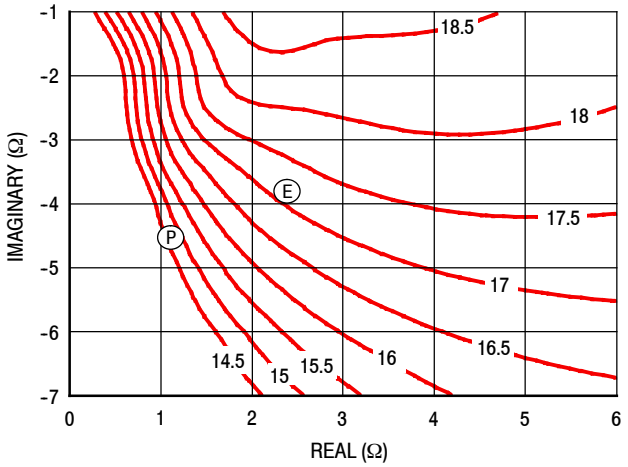


Figure 14. P3dB Load Pull Gain Contours (dB)

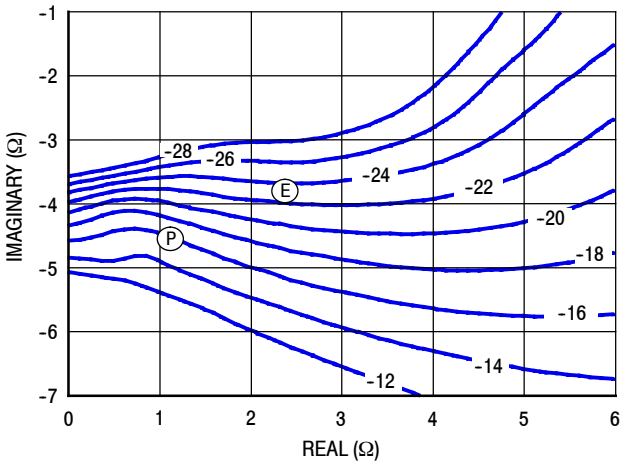


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P1dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 2140 MHz

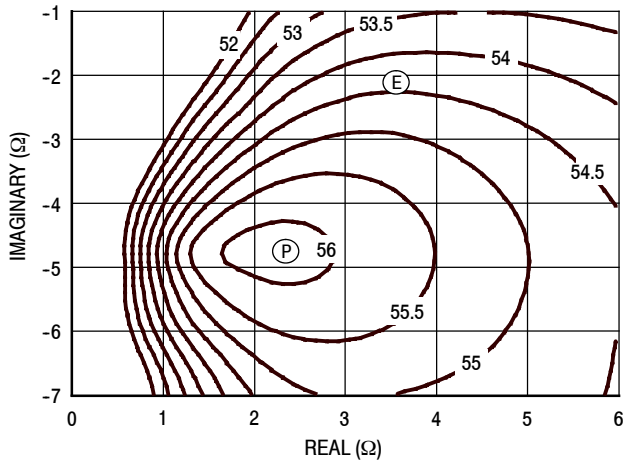


Figure 16. P1dB Load Pull Output Power Contours (dBm)

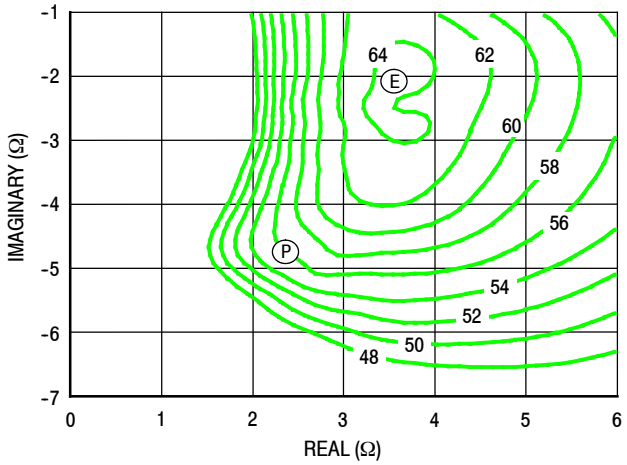


Figure 17. P1dB Load Pull Efficiency Contours (%)

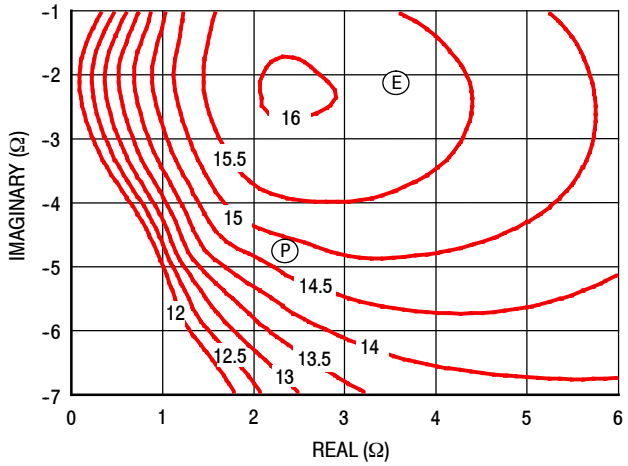


Figure 18. P1dB Load Pull Gain Contours (dB)

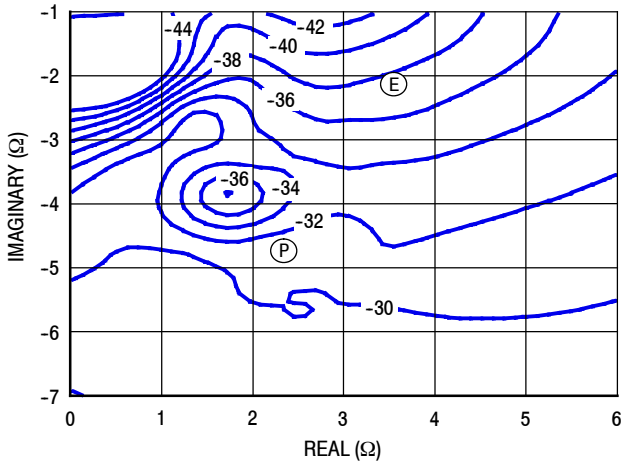


Figure 19. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 2140 MHz

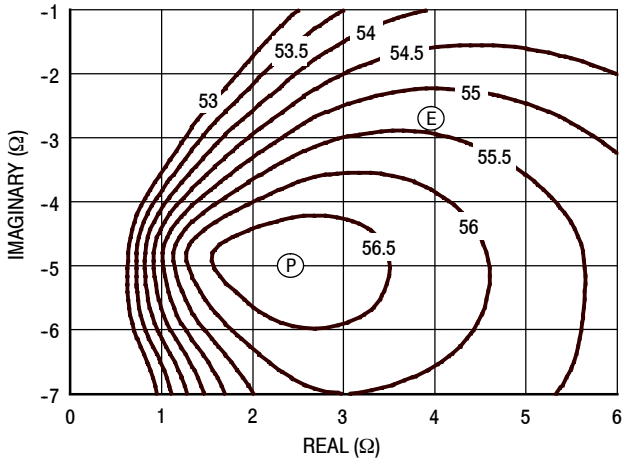


Figure 20. P3dB Load Pull Output Power Contours (dBm)

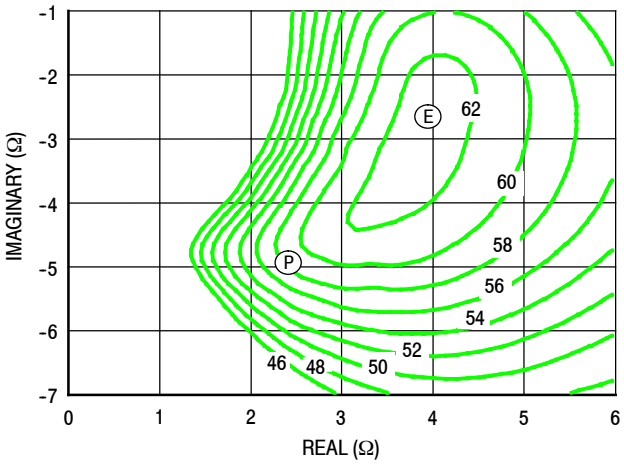


Figure 21. P3dB Load Pull Efficiency Contours (%)

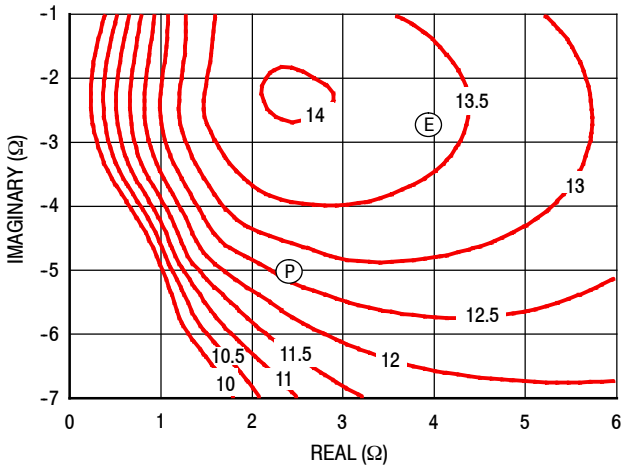


Figure 22. P3dB Load Pull Gain Contours (dB)

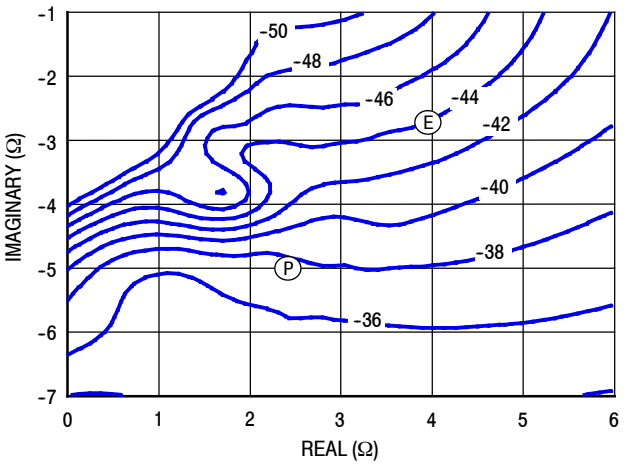


Figure 23. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

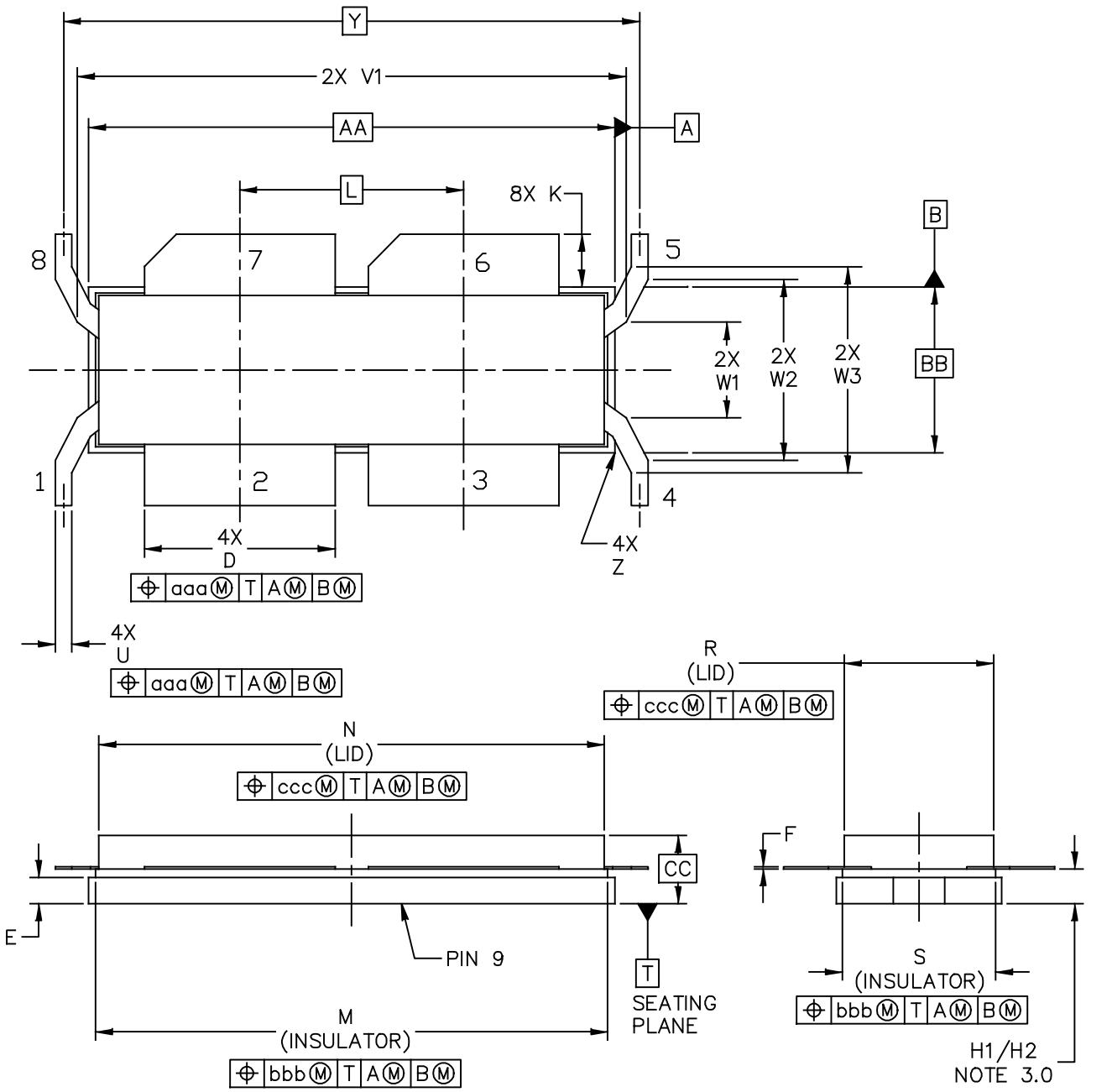
Gain

Drain Efficiency

Linearity

Output Power

PACKAGE DIMENSIONS



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	SOT1795−1	31 MAY 2016

NOTES:

1.0 INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

2.0 CONTROLLING DIMENSION: INCH

3.0 DIMENSION H1 AND H2 ARE MEASURED .030 (0.762 MM) AWAY FROM FLANGE TO CLEAR EPOXY FLOW OUT PARALLEL TO DATUM B. H1 APPLIES TO PINS 2,3,6,7. H2 APPLIES TO PINS 1,4,5,8.

4.0 –DELETED–

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	1.265	1.275	32.13	32.39	N	1.218	1.242	30.94	31.55
BB	.397	.403	10.08	10.24	R	.365	.375	9.27	9.53
CC	.150	.200	3.81	5.08	S	.365	.375	9.27	9.53
D	.455	.465	11.56	11.81	U	.035	.045	0.89	1.14
E	.062	.066	1.57	1.68	V1	1.320	1.330	33.53	33.78
F	.004	.007	0.10	0.18	T3	DELETED		DELETED	
H1	.082	.090	2.08	2.29	W1	.225	.235	5.72	5.97
H2	.078	.094	1.98	2.39	W2	.431	.441	10.95	10.20
K	.117	.137	2.97	3.48	W3	.491	.501	12.47	12.73
L	.540 BSC		13.72 BSC		Y	1.390 BSC		35.31 BSC	
M	1.219	1.241	30.96	31.52	Z	---	R.040	---	R1.02
					aaa	.005		0.13	
					bbb	.010		0.25	
					ccc	.020		0.51	

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SOT1795–1 31 MAY 2016

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1908: Solder Reflow Attach Method for High Power RF Devices in Air Cavity Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Sept. 2016	• Initial release of data sheet

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