PN7160_PN7161

Near Field Communication (NFC) controller

Rev. 3.2 — 30 September 2021

Product data sheet
COMPANY PUBLIC

1 Introduction

This data sheet describes the PN7160 and PN7161 NFC controllers with NCI interface and integrated firmware.

The PN7161 support all features of PN7160 plus "Enhanced Contactless Polling" (ECP) by Apple (see Ref. [12]). Please note, that the ECP feature is available after formal authorization only.

In the following document PN7160 refers to PN7160 and PN7161, otherwise stated.

This data sheet requires additional documents for functional chip description and design in. Refer to the references listed in this document for full list of documentation provided by NXP.

2 General description

PN7160 is an NFC controller designed for integration in mobile devices and devices compliant with NFC standards (NFC Forum, NCI).

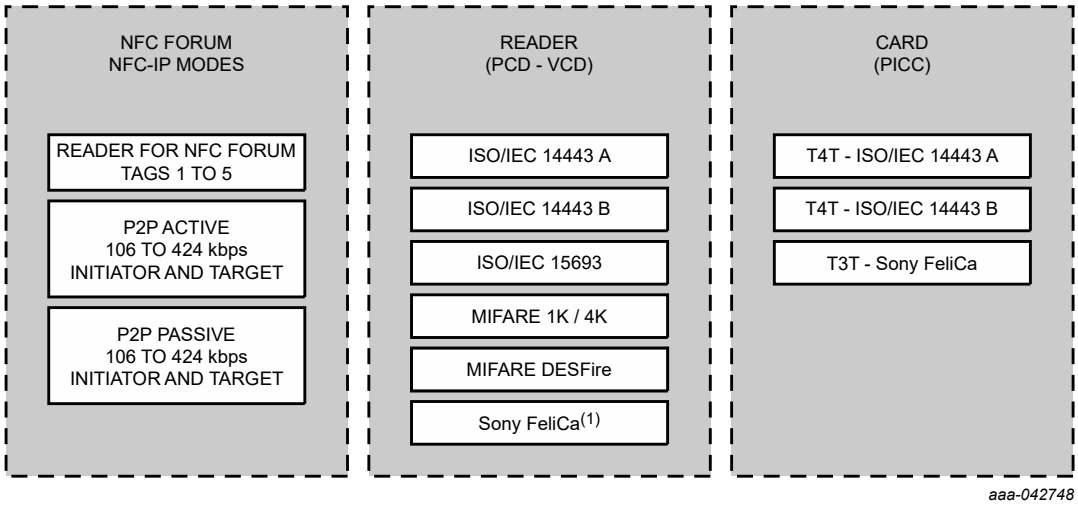
PN7160 is designed based on experience from previous NXP NFC device generation to ease the integration of NFC technology in mobile devices by providing:

- A low PCB footprint and a reduced external Bill of Material
- An optimized architecture for low-power consumption in different modes (Standby, low-power polling loop)
- A highly efficient integrated power management unit allowing direct supply from an extended battery supply range (2.8 V to 5.5 V).
- Support of an external DC-to-DC like NXP PCA941xA (with x = 0, 1 and 2), to provide more output power.

PN7160 embeds a new generation RF contactless front-end, supporting various transmission modes according to NFCIP-1 and NFCIP-2, ISO/IEC14443, ISO/IEC 15693, MIFARE and FeliCa specifications. This new contactless front-end design brings a major performance step-up with on one hand a higher sensitivity and on the other hand the capability to work in active load modulation communication enabling the support of small antenna form factor. It also allows to provide a higher output power by supplying the transmitter output stage from 2.7 V to 5.25 V.

- Enhanced Dynamic LMA (DLMA) to optimize and to enhance load modulation amplitude depending on external field strength. It allows higher range communication distance in card mode.
- Independent LMA phase adjustment by step of 5° for type A, B and F
- Dynamic power control which allows to make use of the maximum power in reader mode without exceeding the maximum power allowed by the standard in 0 distance.
- Card mode receiver sensitivity of 20 $mV_{(p-p)}$
- Support of single ended receiver
- 1.3 W output transmitter power

Supported transmission modes are listed in Figure 1. For contactless card functionality, the PN7160 can act autonomously if previously configured by the host in such a manner. PICC functionality can be supported without host being turned on.



1. According to ISO/IEC 18092 (Ecma 340) standard.

Figure 1. PN7160 transmission modes

3 Features and benefits

- Highly integrated demodulator and decoder
- Buffered output drivers to connect an antenna with minimum number of external components
- Integrated RF level detector
- Integrated Polling Loop for automatic device discovery
- RF protocols supported
  - ISO/IEC 14443A, ISO/IEC 14443B PICC mode
  - ISO/IEC 14443A, ISO/IEC 14443B PCD mode designed according to NFC Forum digital protocol T4T platform and ISO-DEP (see Ref. [1])
  - FeliCa PCD mode
  - MIFARE PCD encryption mechanism (MIFARE 1K/4K)
  - NFC Forum tags T1T, T2T, T3T, T4T and T5T (see Ref. [1])
  - NFCIP-1, NFCIP-2 protocol (see Ref. [8] and Ref. [10])
  - NFC Forum certification for P2P, reader and card mode (see Ref. [1])
  - FeliCa PICC mode
  - ISO/IEC 15693/ICODE VCD mode (see Ref. [9])
  - NFC Forum-compliant embedded T4T for NDEF short record
  - Support for "Enhanced Contactless Polling" by Apple (see Ref. [12]) (PN7161 only)
- Supported host interfaces
  - NCI protocol interface according to NFC Forum standardization (see Ref. [2])
  - I^2C-bus High-speed mode (see Ref. [3])
  - SPI-bus (see Ref. [4])
- Flexible clock supply concept to facilitate PN7160 integration
  - Internal oscillator for 27.12 MHz crystal connection
  - Integrated PLL unit to make use of device reference clock and facilitate PN7160 integration
- Integrated power management unit
  - Direct connection to a battery (2.5 V to 5.5 V voltage supply range)
  - Support different low-power states configuration: Hard Power-Down state and Standby state activated by firmware
  - Autonomous mode when host is shut down
- Automatic wake-up via RF field, internal timer and host interfaces
- Integrated non-volatile memory to store data and executable code for customization
  - Anti tearing support to recover from tearing events
- Standards compliance
  - NFC Forum Device Requirements (see Ref. [1])
  - NCI 2.0

4 Applications

- Mobile devices
- Portable equipment (personal digital assistants, tablet, notebook, wearable)
- Consumer devices
- Smart home gateways

5 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	Card Emulation and Passive Target; V_{SS} = 0 V	[1]	2.5	-	5.5	V
		Reader, Active Initiator and Active Target; V_{SS} = 0 V	[1]	2.8	-	5.5	V
$V_{DD(UP)}$	$V_{DD(UP)}$ input supply voltage	Reader, Active Initiator and Active Target; V_{SS} = 0 V	[1]	2.8	-	5.8	V
		All other cases except Hard Power Down state; V_{SS} = 0 V	[1] [2]	2.5	-	5.8	V
$V_{DD(PAD)}$	$V_{DD(PAD)}$ supply voltage	supply voltage for host interface; V_{SS} = 0 V	[1]	1.65	1.8	1.95	V
				3.0	3.3	3.6	V
I_{BAT}	battery supply current	in Hard Power Down state; V_{BAT} = 3.6 V; T = 25 °C	[3]	-	10.5	16	µA
		in Standby state; V_{BAT} = 3.6 V					
		enhanced RF detector		-	32	52	µA
		low sensitivity RF detector		-	21	36	µA
		in low-power polling loop; V_{BAT} = 3.6 V; T = 25 °C; loop time = 500 ms		-	100	-	µA
		continuous total current consumption in PCD mode at V_{BAT} = 3.6 V	[4]	-	-	290	mA
$I_{th(Ilim)}$	current limit threshold	current limiter on transmitter	[4]	270	300	330	mA
P_{tot}	total power dissipation	PCD mode at typical $V_{DD(TX)}$ = 5.25 V, $V_{DD(UP)}$ = 5.8 V and V_{BAT} = 3.6 V; includes power from V_{BAT} and $V_{DD(UP)}$		-	-	620	mW
T_{amb}	ambient temperature	JEDEC PCB-0.5		-25	-	+85	°C

[1] V_{SS} represents $V_{SS(PAD)}$ and $V_{SS(TX)}$.
[2] When $V_{DD(UP)}$ is below 2.8 V the TXLDO can be in follower mode (see Section 10.4.3), there will be no more $V_{DD(UP)}$ noise rejection. Any noise below 848 kbit/s will affect the performance.
[3] External clock on NFC_CLK_XTAL1 must be LOW.
[4] This is considering an antenna tuned to sink maximum 250 mA continuous current from the transmitter. The antenna shall be tuned to never exceed this 250 mA maximum current.

6 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PN7160xyzz/C100 [1] [2] [3]	VFBGA64	plastic very thin fine-pitch ball grid array package; 64 balls	SOT1860-1
	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals	SOT618-1
PN7161xyzz/C100 [1] [2] [3]	VFBGA64	plastic very thin fine-pitch ball grid array package; 64 balls	SOT1860-1
	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals	SOT618-1

[1] x: A = I^2C-bus interface; B = SPI-bus interface.
[2] y: correspond to firmware variant.
[3] zz: correspond to package variant. HN = HVQFN40 package; EV = VFBGA64 package.

7 Marking

7.1 Marking VFBGA64

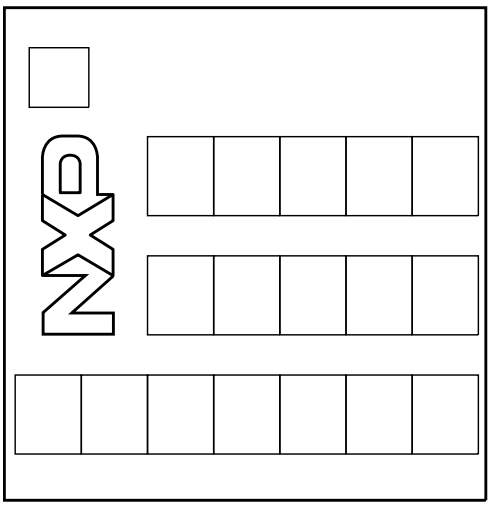


Figure 2. PN7160 package marking (top view)

Table 3. Marking code

Line number	Marking code
Line 1	product version identification
Line 2	diffusion batch sequence number + assembly lot ID
Line 3	manufacturing code including: • diffusion center code: – S: Power chip (PTCT) • assembly center code: – S: ATKH • RoHS compliancy indicator: – D: Dark Green; fully compliant RoHS and no halogen and antimony • manufacturing year and week, 3 digits: – Y: year – WW: week code • product life cycle status code: – X: means not qualified product – nothing means released product

7.2 Marking HVQFN40

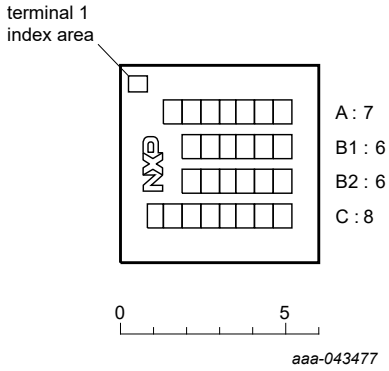


Figure 3. PN7160 Package marking HVQFN40 (top view)

Table 4. Marking codes

Type number	Marking code
Line A	7 characters used: product version identification
Line B1 + Line B2	Diffusion Bath ID (9 digits) + space + assembly ID number (2 digits)
Line C	8 characters used: manufacturing code including: • diffusion center code: – S: Power chip (PTCT) • assembly center code: – S: ATKH • RoHS compliancy indicator: – D: Dark Green; fully compliant RoHS and no halogen and antimony • manufacturing year and week, 3 digits: – YY: year – WW: week code • product life cycle status code: – X: means not qualified product – nothing means released product

8 Block diagram

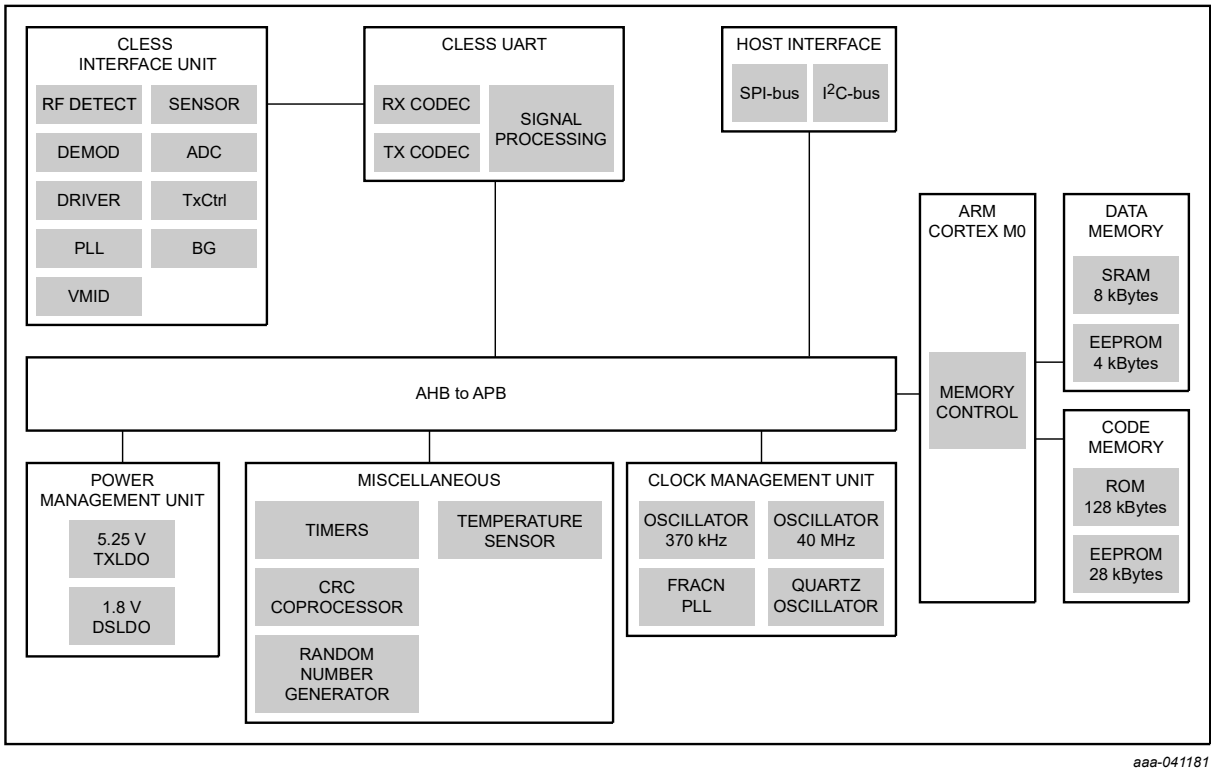


Figure 4. PN7160 block diagram

9 Pinning information

9.1 Pinning

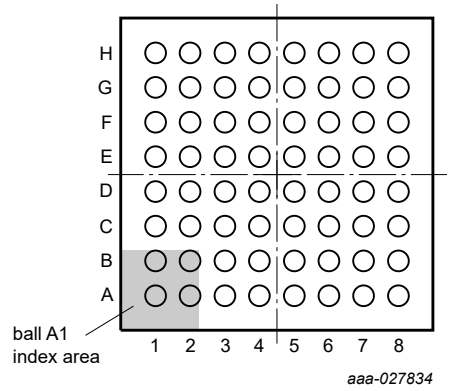


Figure 5. PN7160 pinning VFBGA64 (bottom view)

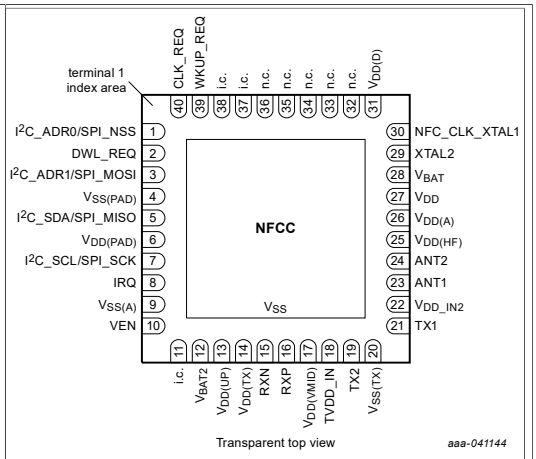


Figure 6. PN7160 pinning HVQFN40

Table 5. PN7160 pin description

Symbol	Pin HVQFN40	Pin VFBGA64	Type[1]	Refer	Description
I^2C_ADR0/SPI_NSS	1	C3	I/O	$V_{DD(PAD)}$	Host interface pin 1
DWL_REQ	2	D3	I	$V_{DD(PAD)}$	Firmware download control pin
I^2C_ADR1/SPI_MOSI	3	D1	I/O	$V_{DD(PAD)}$	Host interface pin 2
$V_{SS(PAD)}$	4	C1	G	n/a	Pad ground. Must be connected to ground.
I^2C_SDA/SPI_MISO	5	E1	I/O	$V_{DD(PAD)}$	Host interface pin 3
$V_{DD(PAD)}$	6	D2	P	n/a	Pad supply voltage
I^2C_SCL/SPI_SCK	7	E2	I/O	$V_{DD(PAD)}$	Host interface pin 4
IRQ	8	E3	O	$V_{DD(PAD)}$	Interrupt request output
$V_{SS(A)}$	9	G3	G	n/a	Analog ground supply voltage
VEN	10	H1	I	V_{BAT}	Reset pin. Set the device in Hard Power Down.
i.c.	11	-	-	-	Internally Connected. To be left open.
V_{BAT2}	12	-	P	n/a	Battery supply voltage. Must be connected to V_{BAT}. VFBGA package: internally connected.
$V_{DD(UP)}$	13	H3	P	n/a	TXLDO input supply voltage
$V_{DD(TX)}$	14	G7	P	n/a	Transmitter supply voltage
RXN	15	H6	I	$V_{DD(A)}$	Negative receiver input
RXP	16	H5	I	$V_{DD(A)}$	Positive receiver input
$V_{DD(VMID)}$	17	H4	P	n/a	Receiver reference input supply voltage
TVDD_IN	18	-	P	n/a	Must be connected to $V_{DD(TX)}$ and TVDD_IN2. VFBGA package: internally connected.
TX2	19	H7	O	$V_{DD(TX)}$	Antenna driver output
$V_{SS(TX)}$	20	H8	G	n/a	Contactless transmitter ground. Must be connected to ground.

Table 5. PN7160 pin description*...continued*

Symbol	Pin HVQFN40	Pin VFBGA64	Type[1]	Refer	Description
TX1	21	G8	O	$V_{DD(TX)}$	Antenna driver output
TVDD_IN2	22	-	P		Must be connected to $V_{DD(TX)}$ and TVDD_IN. VFBGA package: internally connected.
ANT1	23	F7	P	n/a	Antenna connection for wake-up
ANT2	24	E7	P	n/a	Antenna connection for wake-up
$V_{DD(HF)}$	25	D6	P	n/a	Monitor rectifier output voltage
$V_{DD(A)}$	26	D7	P	n/a	Analog supply voltage. Connect to $V_{DD(D)}$.
V_{DD}	27	-			Must be connected to AVDD and DVDD. VFBGA package: internally connected.
V_{BAT}	28	E8	P	n/a	Battery supply voltage. Must be connected to V_{BAT2}.
XTAL2	29	D8	O	$V_{DD(D)}$	Oscillator output
NFC_CLK_XTAL1	30	C8	I	$V_{DD(D)}$	PLL input
$V_{DD(D)}$	31	C7	P	n/a	Digital supply voltage for decoupling. Must be connected to V_{DD} and $V_{DD(A)}$.
n.c.	32	-			
n.c.	33	-			
n.c.	34	-			
n.c.	35	-			
n.c.	36	-			
i.c.	37	A2			To be left open.
i.c.	38	B2			To be left open.
WKUP_REQ	39	A1	I	$V_{DD(PAD)}$	Wake-up request when in standby
CLK_REQ	40	B1	O	$V_{DD(PAD)}$	Clock request pin
V_{SS}	Center Pad	-	G	n/a	Pad ground. Must be connected to ground.
i.c.	-	A3			To be left open.
i.c.	-	A4			Must be connected to ground.
i.c.	-	A5			To be left open.
i.c.	-	A6			To be left open.
i.c.	-	A7			Must be connected to ground.
i.c.	-	A8			To be left open.
i.c.	-	B3			To be left open.
n.c.	-	B4			To be left open.
n.c.	-	B5			To be left open.
i.c.	-	B6			To be left open.
i.c.	-	B7			To be left open.
i.c.	-	B8			To be left open.
i.c.	-	C2			To be left open.
n.c.	-	C4			To be left open.
n.c.	-	C5			To be left open.
$V_{SS(D)}$	-	C6	G	n/a	Digital ground supply voltage. Must be connected to ground.
n.c.	-	D4			To be left open.
n.c.	-	D5			To be left open.

Table 5. PN7160 pin description*...continued*

Symbol	Pin HVQFN40	Pin VFBGA64	Type[1]	Refer	Description
n.c.	-	E4			To be left open.
n.c.	-	E5			To be left open.
n.c.	-	E6			To be left open.
i.c.	-	F1			To be left open.
i.c.	-	F2			To be left open.
i.c.	-	F3			To be left open.
n.c.	-	F4			To be left open.
n.c.	-	F5			To be left open.
n.c.	-	F6			To be left open.
TX_PWR_REQ	-	F8	O	$V_{DD(D)}$	External TX power supply request on $V_{DD(D)}$
i.c.	-	G1			Must be connected to ground.
i.c.	-	G2			To be left open.
n.c.	-	G4			To be left open.
$V_{SS(A)}$	-	G5	G	n/a	Analog ground supply voltage
$V_{SS(A)}$	-	G6	G	n/a	Analog ground supply voltage
i.c.	-	H2			To be left open.

[1] P = power supply; G = ground; I = input; O = output; I/O = input/output

10 Functional description

PN7160 can be connected on a host controller through different physical interfaces (I^2C-bus and SPI-bus). The logical interface towards the host controller is NCI-compliant Ref. [2] with additional command set for NXP-specific product features. This IC is fully user controllable by the firmware interface described in Ref. [5].

Moreover, PN7160 provides flexible and integrated power management unit in order to preserve energy supporting Power Off mode.

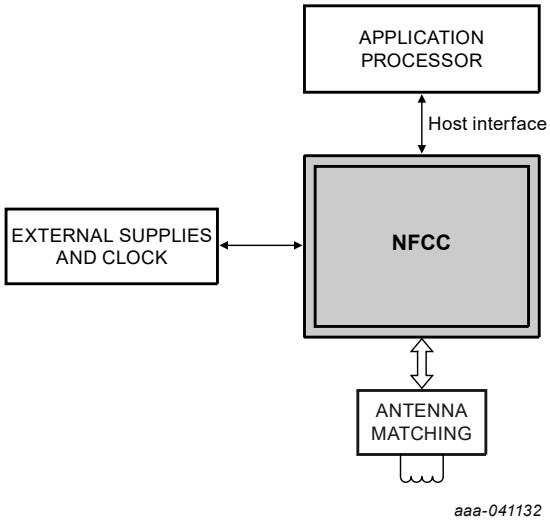


Figure 7. PN7160 connection in mobile system

10.1 System modes

10.1.1 System power modes

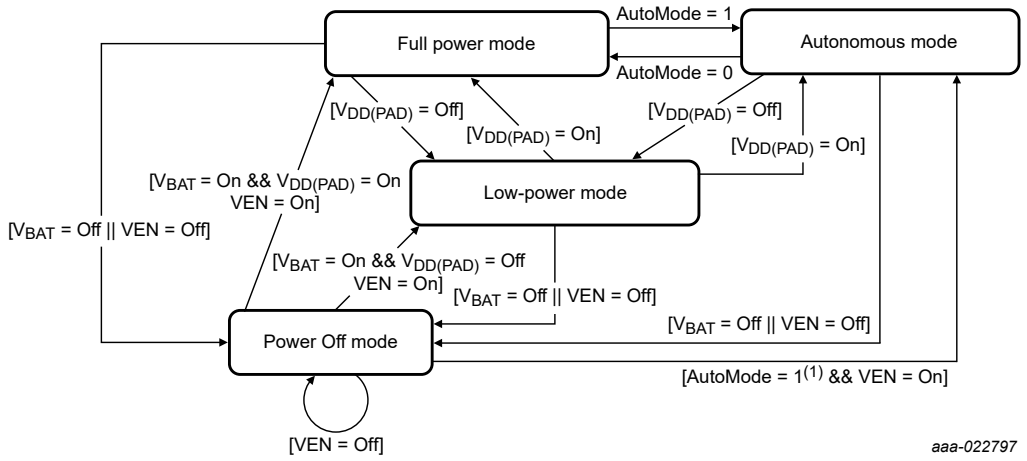
4 power modes are specified: Full power mode, Autonomous mode, Low-power mode and Power Off mode.

Table 6. System power modes description

System power mode	Description
Full power mode	The battery supply (V_{BAT}) as well as the pad supply ($V_{DD(PAD)}$) are available
Autonomous mode	The battery supply (V_{BAT}) as well as the pad supply ($V_{DD(PAD)}$) are available. Via a SW command the host sets the NFC controller in autonomous mode (AutoMode bit is set). In that power mode, the NFC controller will not send any command or signal over $V_{DD(PAD)}$ connected pins. In case of reset via VEN pin the AutoMode bit value is kept unchanged. This mode is useful to present an NDEF message in Card Emulation mode although the main system is shut down.
Low-power mode	The battery supply (V_{BAT}) is available but the pad supply ($V_{DD(PAD)}$) is not available. No host communication is available.

Table 6. System power modes description...*continued*

System power mode	Description
Power Off mode	The system is not supplied from any source or the system is kept Hard Power Down (HPD)



1. When V_{BAT} goes OFF, AutoMode = 0.

Figure 8. System power mode diagram

Table 7 summarizes the system power mode of the PN7160 depending on the status of the external supplies available in the system:

Table 7. System power modes configuration

V_{BAT}	$V_{DD(PAD)}$	VEN	AutoMode bit	Power mode
Off	X	X	X	Power Off mode
On	X	Off	X	Power Off mode
On	On	On	0	Full power mode
On	On	On	1	Autonomous mode
On	Off	On	X	Low-power mode

Depending on power modes, some application states are limited:

Table 8. System power modes description

System power mode	Allowed communication modes
Power Off mode	not applicable
Low-power mode Autonomous mode	Card Emulation only
Full power mode	Reader/Writer, Card Emulation, P2P modes

10.1.2 PN7160 power states

Next to system power modes defined by the status of the power supplies, the power states include the logical status of the system. Thus extend the power modes.

3 power states are specified: Hard Power Down (HPD), Standby, Active.

Table 9. PN7160 power states

Power state name	Description
Hard Power Down	The PN7160 is supplied by V_{BAT} within its operating range and PN7160 is kept in Hard Power Down (VEN voltage is kept low by host or SW programming) to have the minimum power consumption. The system mode is in Power Off.
Standby	The PN7160 is supplied by V_{BAT} within its operating range, VEN voltage is high (by host or SW programming) and minimum part of PN7160 is kept supplied to enable configured wake-up sources which allow to switch to Active state; RF field, Host interface (if $V_{DD(PAD)}$ is high). The system mode is Low-power mode or Full power mode.
Active	The PN7160 is supplied by V_{BAT} within its operating range, VEN voltage is high (by host or SW programming), $V_{DD(PAD)}$ is high and the PN7160 internal blocks are supplied. 3 sub-modes are defined: Idle, Listener and Poller. The system mode is Full power mode.

At application level, the PN7160 will continuously switch between different states to optimize the current consumption (polling loop mode). Refer to Table 1 for targeted current consumption in here described states.

The PN7160 is designed to allow the host controller to have full control over its functional states.

10.1.2.1 Hard Power Down (HPD) state

The Hard Power Down state is entered when $V_{DD(PAD)}$ and V_{BAT} are high by setting VEN voltage < 0.4 V. As these signals are under host control, the PN7160 has no influence on entering or exiting this state.

10.1.2.2 Standby state

Active state is PN7160's default state after boot sequence in order to allow a quick configuration of PN7160. It is recommended to change the default state to Standby state after first boot in order to save power. PN7160 can switch to Standby state autonomously (if configured by host). This state is independent of the $V_{DD(PAD)}$ value.

In this state, PN7160 most blocks including CPU are disconnected from power supply. Number of wake-up sources exist to put PN7160 into Active state (all host-related wake-up events imply that $V_{DD(PAD)}$ is available):

- Host interface wake-up event (I^2C-bus, SPI-bus)
- Host interface wake-up via WKUP_REQ pin
- Antenna RF level detector
- Internal timer event when using polling loop (370 kHz Low-power oscillator is enabled)

If wake-up event occurs, PN7160 will switch to Active state. Any further operation depends on software configuration and/or wake-up source.

10.1.2.3 Active state

Within the Active state, the system is acting as an NFC device. The device can be in 3 different power states: Idle, Listener and Poller.

Table 10. Functional modes in active state

Functional modes	Description
Idle	the PN7160 is active and host interface communication is on going. The RF interface is not activated. If Standby state is de-activated PN7160 stays in Idle mode even when no host communication.
Listener	the PN7160 is active and is listening to external device. The RF interface is activated.
Poller	the PN7160 is active and is in Poller mode. It polls external device. The RF interface is activated.

Poller mode

In this mode, PN7160 is acting as Reader/Writer or NFC Initiator, searching for or communicating with passive tags or NFC target. Once RF communication has ended, PN7160 will switch to Idle mode or Standby state to save energy. Poller mode shall be used with 2.8 V < V_{BAT} < 5.5 V and VEN voltage > 1.1 V. Poller mode shall not be used with V_{BAT} < 2.8 V. $V_{DD(PAD)}$ is within its operational range (see Table 1).

Listener mode

In this mode, PN7160 is acting as a card or as an NFC Target. Listener mode shall be used with 2.8 V < V_{BAT} < 5.5 V and VEN voltage > 1.1 V. Once RF communication has ended, PN7160 will switch to Idle mode or Standby state to save energy.

10.1.2.4 Polling loop

The polling loop will sequentially set PN7160 in different power states (Active or Standby). All RF technologies supported by PN7160 can be independently enabled within this polling loop.

There are 2 main phases in the polling loop:

- Listening phase. The PN7160 can be in Standby power state or Idle mode (called pause in Figure 9; no communication is on-going) or Listener mode (called Emulation in Figure 9; card / target communication is started)
- Polling phase. The PN7160 is in Poller mode

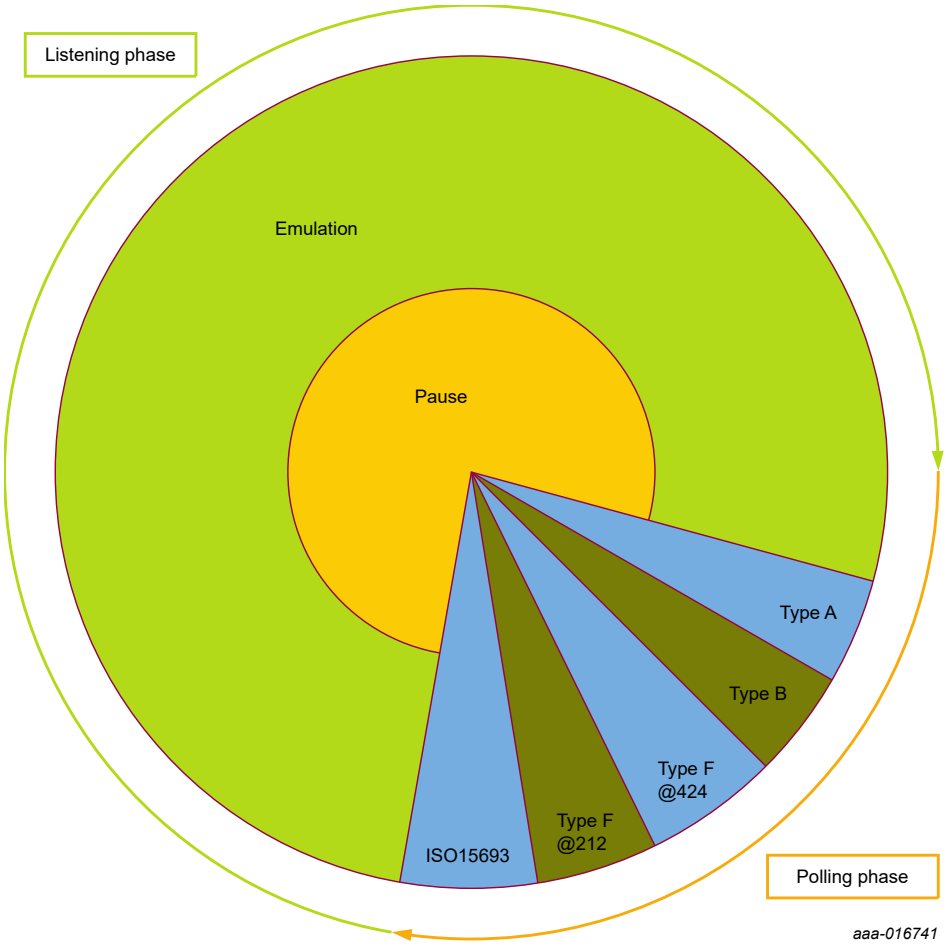


Figure 9. Polling loop: all phases enabled

In Listening phase when no RF field PN7160 is in Standby state if enabled (otherwise it is Idle mode) and is in Listener mode (Emulation) when RF field is detected. When in Polling phase, PN7160 goes to Poller mode.

To further decrease the power consumption when running the polling loop, PN7160 features a low-power RF polling. When PN7160 is in Polling phase instead of sending regularly RF command PN7160 senses with a short RF field duration if there is any NFC Target or card/tag present. If yes, then it goes back to standard polling loop. With 500 ms (configurable duration, see Ref. [5]) listening phase duration, the average power consumption is around 100 µA depending on RF matching conditions.

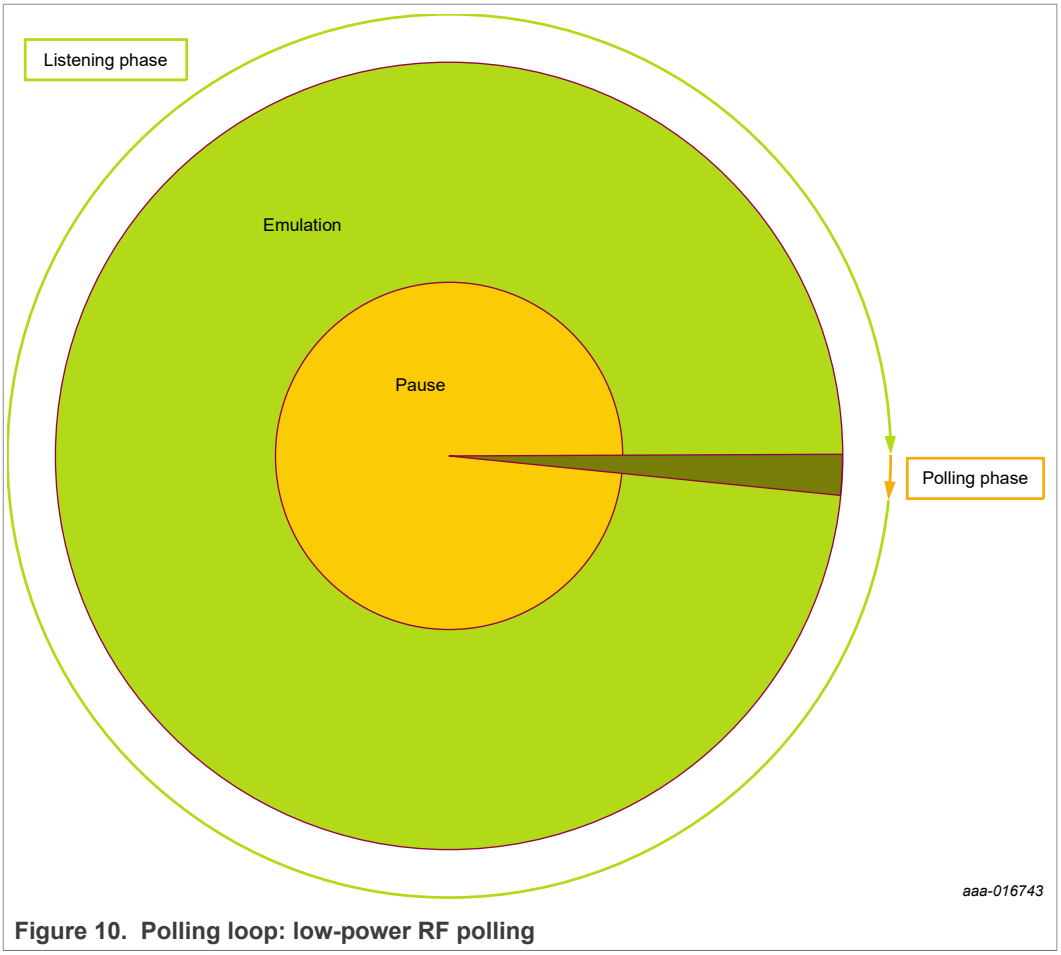


Figure 10. Polling loop: low-power RF polling

Detailed description of polling loop configuration options is given in Ref. [5].

10.2 Host interfaces

PN7160 provides the support of the following host interfaces:

- I^2C-bus Slave Interface, up to 3.4 MBaud
- SPI-bus Slave Interface, up to 7 MBaud

Only one host interface can be active at a time, as the pins are shared for all interfaces.

The selection between interfaces is fused during IC manufacturing so that different ordering numbers for the I^2C-bus and SPI-bus version are in place.

The host interfaces are woken-up in the following way:

- wake-up with WKUP_REQ input pin
- I^2C-bus: wake-up on I^2C-bus address
- SPI-bus: transition of NSS serial
- data received on RX line

To enable and ensure data flow control between PN7160 and host controller, additionally a dedicated interrupt line IRQ is provided which Active state is programmable. See Ref. [5] for more information.

10.2.1 I²C-bus interface

The I²C-bus interface implements a slave I²C-bus interface with integrated shift register, shift timing generation and slave address recognition.

I²C-bus Standard mode (100 kHz SCL), Fast mode (400 kHz SCL) and High-speed mode (3.4 MHz SCL) are supported.

The main hardware characteristics of the I²C-bus module are:

- Support slave I²C-bus
- Standard, Fast and High-speed modes supported
- Wake-up of PN7160 on its address only
- Serial clock synchronization can be used by PN7160 as a handshake mechanism to suspend and resume serial transfer (clock stretching)

The I²C-bus interface module meets the I²C-bus specification Ref. [3] except General call, 10 bit addressing and Fast mode Plus (Fm+).

10.2.1.1 I²C-bus configuration

The I²C-bus interface shares four pins with SPI-bus interface also supported by PN7160. When I²C-bus is configured in EEPROM settings, functionality of the interface pins changes as described in Table 11.

Table 11. Functionality for I²C-bus interface

Pin name	Functionality
HIF1	I²C-bus address 0
HIF2	I²C-bus address 1
HIF3 [1]	I²C-bus data line
HIF4 [1]	I²C-bus clock line

[1] HIF3 and HIF4 are not fail-safe and $V_{DD(pad)}$ shall always be available when using the SCL and SDA lines connected to these pins.

PN7160 supports 7-bit addressing mode. Selection of the I²C-bus address is done by 2-pin configurations on top of a fixed binary header: 0, 1, 0, 1, 0, HIF2, HIF1, R/W.

Table 12. I²C-bus interface addressing

HIF2	HIF1	I²C-bus address (R/W = 0, write)	I²C-bus address (R/W = 1, read)
0	0	0x50	0x51
0	1	0x52	0x53
1	0	0x54	0x55
1	1	0x56	0x57

10.2.2 Serial Peripheral Interface bus (SPI-bus)

10.2.2.1 Features

- Synchronous, Serial, Full-Duplex communication, 7 MHz maximum
- Slave mode

- Programmable clock polarity and phase

10.2.2.2 SPI-bus configuration options

In order to select SPI-bus interface for host communication, some EEPROM settings are programmed during production.

Four versions can be configured depending on CPOL/CPHA EEPROM setting.

The selection between interfaces is fused during IC manufacturing so that different ordering numbers for the SPI-bus version.

Table 13. SPI-bus configuration

Connection
CPHA switch: Clock PHAse: defines the sampling edge of MOSI data • CPHA = 1: data are sampled on MOSI on the even clock edges of SCK after NSS goes low • CPHA = 0: data are sampled on MOSI on the odd clock edges of SCK after NSS goes low
CPOL switch: Clock POLarity • IFSEL1 = 0: the clock is idle low and the first valid edge of SCK will be a rising one • IFSEL1 = 1: the clock is idle high and the first valid edge of SCK will be a falling one

The SPI-bus interface shares 4 pins with I^2C-bus interface also supported by PN7160. When SPI-bus is configured in EEPROM settings, functionality of interface pins changes to one described in Table 14.

Table 14. Functionality for SPI-bus interface

Pin name	Functionality
HIF1	NSS (Not Slave Select)
HIF2	MOSI (Master Out Slave In)
HIF3	MISO (Master In Slave Out)
HIF4	SCK (Serial Clock)

10.2.2.3 SPI-bus functional description

When a master device transmits data to PN7160 (slave device) via the MOSI line, PN7160 responds by sending data to the master device via the masters MISO line. This implies full-duplex transmission with both data out and data in synchronized with the same clock signal.

PN7160 starts sampling when receiving a logic low at pin NSS and the clock at input pin SCK. Thus, PN7160 is synchronized with the master. Data from the master is received serially at the slave MOSI line and loads the 8-bit shift register. After the 8-bit shift register is loaded, its data is transferred to the read buffer. During a write cycle, data is written into the shift register, then PN7160 waits for a clock train from the master to shift the data out on the slaves MISO line.

- Master In Slave Out (MISO)
  The MISO line is configured as an input in a master device and as an output in a slave device. It is used to transfer data from the slave to the master, with the most significant bit sent first. The MISO line of a slave device should be placed in the high impedance state if the slave is not selected.

- Master Out Slave In (MOSI)
  The MOSI line is configured as an output in a master device and as an input in a slave device. It is used to transfer data from the master to a slave, with the Most Significant Bit (MSB) sent first.
- Serial Clock (SCK)
  The serial clock is used to synchronize data movement both in and out of the device through its MOSI and MISO lines. The master and slave devices are capable of exchanging a byte of information during a sequence of eight clock cycles. Since the master device generates SCK, this line becomes an input on a slave device and an output at the master device.
- Not Slave Select (NSS)
  The slave select input line is used to select a slave device. It has to be low prior to data transactions and must stay low of the duration of the transaction. The NSS line on master side must be tied high.

Both master and slave devices must operate with the same timing. The master device always places data on the MOSI line a half cycle before the clock edge SCK, in order for the slave device to latch the data.

For more information about the SPI-bus functionality, see Ref. [4].

10.3 PN7160 clock concept

There are 4 different clock sources in PN7160:

- 27.12 MHz clock coming either/or from:
  - Internal oscillator for 27.12 MHz crystal connection on NFC_CLK_XTAL1 and XTAL2 pins
  - External reference clock on pin NFC_CLK_XTAL1. It is internally forwarded to an integrated PLL which includes a 1 GHz VCO.
- 13.56 MHz RF clock recovered from RF field
- Low-power oscillator 40 MHz
- Low-power oscillator 370 kHz

10.3.1 27.12 MHz quartz oscillator

When enabled, the 27.12 MHz quartz oscillator applied to PN7160 is the time reference for the RF front end when PN7160 is behaving in Reader mode or NFCIP-1 Initiator.

Therefore stability of the clock frequency is an important factor for reliable operation. It is recommended to adopt the circuit shown in Figure 11.

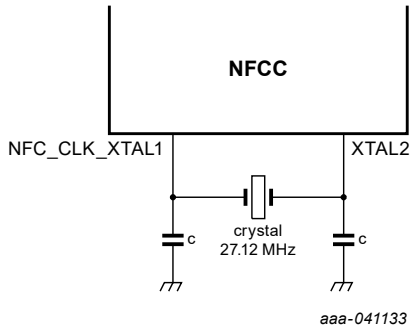


Figure 11. 27.12 MHz crystal oscillator connection

Table 15 describes the levels of accuracy and stability required on the crystal.

Table 15. Crystal requirements

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{xtal}	crystal frequency	ISO/IEC, FCC and FeliCa global compliancy		-	27.12	-	MHz
Δf_{xtal}	crystal frequency accuracy	full operating range	[1]	-50	-	+50	ppm
ESR	equivalent series resistance			-	50	100	Ω
C_L	load capacitance			-	10	-	pF
P_{xtal}	crystal power dissipation			-	-	100	µW

[1] This requirement is according to FCC regulations (± 100 ppm) and FeliCa global (± 50 ppm) requirements. To meet only ISO/IEC 14443 and ISO/IEC 18092, then ± 14 kHz apply which is equivalent to ± 516 ppm.

10.3.2 Integrated PLL to make use of external clock

When enabled, the PLL is designed to generate a low noise 27.12 MHz from an input clock 19.2 MHz, 26 MHz, 32 MHz, 38.4 MHz and 48 MHz.

The 27.12 MHz of the PLL is used as the time reference for the RF front end.

The input clock on NFC_CLK_XTAL1 shall comply with the.following phase noise requirements for the following input frequency: 19.2 MHz, 26 MHz, 32 MHz, 38.4 MHz and 48 MHz:

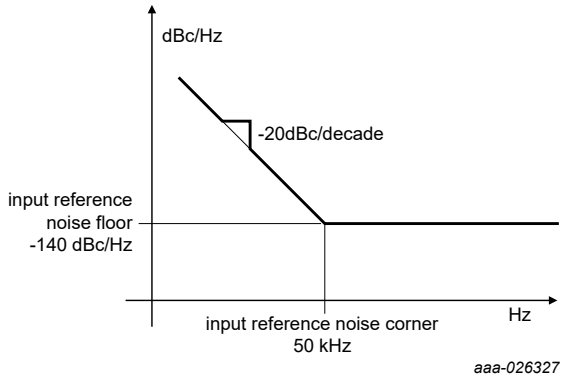


Figure 12. Input reference phase noise characteristics

This phase noise is equivalent to an RMS jitter of 6.23 ps from 10 Hz to 1 MHz. For configuration of input frequency, refer to Ref. [9]. There are 7 pre programmed and validated frequencies for the PLL: 19.2 MHz, 26 MHz, 32 MHz, 38.4 MHz and 48 MHz.

Table 16. PLL input requirements

Coupling: single-ended, AC coupling;

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{clk}	clock frequency	ISO/IEC, FCC and FeliCa global compliancy		-	19.2	-	MHz
				-	26	-	MHz
				-	32	-	MHz
				-	38.4	-	MHz

Table 16. PLL input requirements...*continued*

Coupling: single-ended, AC coupling;

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
				-	48	-	MHz
$f_{i(ref)acc}$	reference input frequency accuracy	full operating range; frequencies typical values: 19.2 MHz, 26 MHz, 32 MHz, 38.4 MHz and 48 MHz	[1]	-20	-	+20	ppm
φ_n	phase noise	input noise floor at 50 kHz		-140	-	-	dB/Hz
Sinusoidal shape							
$V_{i(p-p)}$	peak-to-peak input voltage			0.2	-	1.8	V
$V_{i(clk)}$	clock input voltage			0	-	1.8	V
Square shape							
$V_{i(clk)}$	clock input voltage		[2]	0	-	1.8	V

[1] This requirement is according to FCC regulations (± 100 ppm) and FeliCa global (± 50 ppm) requirements. To meet only ISO/IEC 14443 and ISO/IEC 18092, then ± 7 kHz apply which is equivalent to ± 516 ppm.

[2] Overshoot and undershoot shall not exceed 10%.

For detailed description of clock request mechanisms, refer to Ref. [5] and Ref. [6].

10.3.3 Low-power 40 MHz ± 2.5 % oscillator

Low-power 40 MHz ± 2.5 % oscillator is used as system clock of the system.

Output clock 40 MHz is used by default to clock the system.

10.3.4 Low-power 370 kHz oscillator

A Low Frequency Oscillator (LFO) is implemented to drive a counter (WUC) waking-up PN7160 from Standby state. This allows implementation of low-power reader polling loop at application level.

Moreover, this 370 kHz is used as the reference clock for write access to EEPROM memory.

10.4 Power concept

10.4.1 PMU functional description

The Power Management Unit of PN7160 generates internal supplies required by PN7160 out of V_{BAT} and $V_{DD(UP)}$ input supply voltages:

- V_{DDA}: analog output supply voltage. It must be connected to V_{DDD}.
- V_{DDD}: digital input supply voltage. It is internally connected to the output of the DSLDO V_{DD}.
- $V_{DD(TX)}$: output supply voltage for the transmitter. It is internally connected to the transmitter input supply voltage

The Figure 13 describes the main blocks available in PMU:

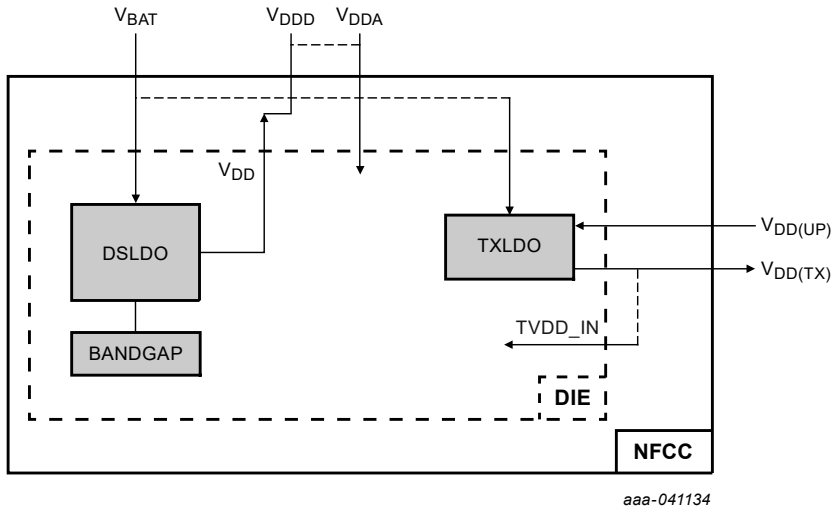


Figure 13. PMU functional diagram

10.4.2 DSLDO: Dual Supply LDO

The input pin of the DSLDO regulator is V_{BAT}.

The output of this regulator (V_{DD}) is internally connected to supply the internal digital blocks which are on V_{DDD}.

It must be externally de-coupled and V_{DDD} must be connected to V_{DDA}.

10.4.3 TXLDO

Transmitter voltage is generated by internal LDO ($V_{DD(TX)}$).

This TXLDO allows a maximum continuous current load up to 250 mA in order to support ISO/IEC 14443 and NFC Forum standard compliant operations.

The Low Drop Out regulator has been designed to reject the noise which could interfere with the RF communication.

Table 17. TXLDO

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DD(TXLDO)(drop)}$	drop TXLDO supply voltage	$V_{DD(UP)}$ = 5.3 V; Transmitter current = 250 mA		-	-	0.3	V

The regulator has been designed to work in 2 modes:

10.4.3.1 Configuration 1: the battery voltage is directly used to generate the RF field

The input supply of the regulator is directly the V_{BAT} voltage which is connected to $V_{DD(UP)}$ the input of the TXLDO.

The output is called $V_{DD(TX)}$.

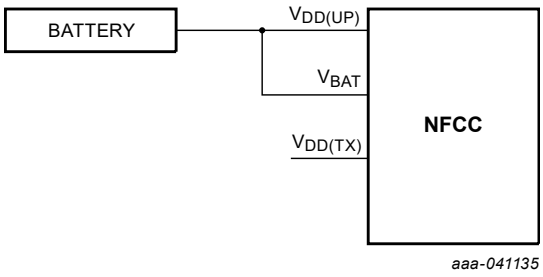


Figure 14. $V_{DD(UP)} = V_{BAT}$

V_{BAT} acceptable range depends on communication modes to be covered (see Table 29)

The $V_{DD(TX)}$ value is programmable and shall be chosen according to the minimum targeted VBAT value for which reader and card modes shall work: VTHRESHOLD.

The TXLDO output voltage is then given by:

$$V_{BAT} \geq V_{THRESHOLD} + V_{DD(TXLDO)(drop)} \Rightarrow V_{DD(TX)} = V_{THRESHOLD}$$

$$V_{THRESHOLD} \geq V_{BAT} - V_{DD(TXLDO)(drop)} \geq 2.8V \Rightarrow V_{DD(TX)} = V_{BAT} - V_{DD(TXLDO)(drop)}$$

Figure 15 shows $V_{DD(TX)}$ offset disabled behavior for both cases of $V_{DD(TX)}$ programmed for 3.0 V, 3.3 V or 3.6 V.

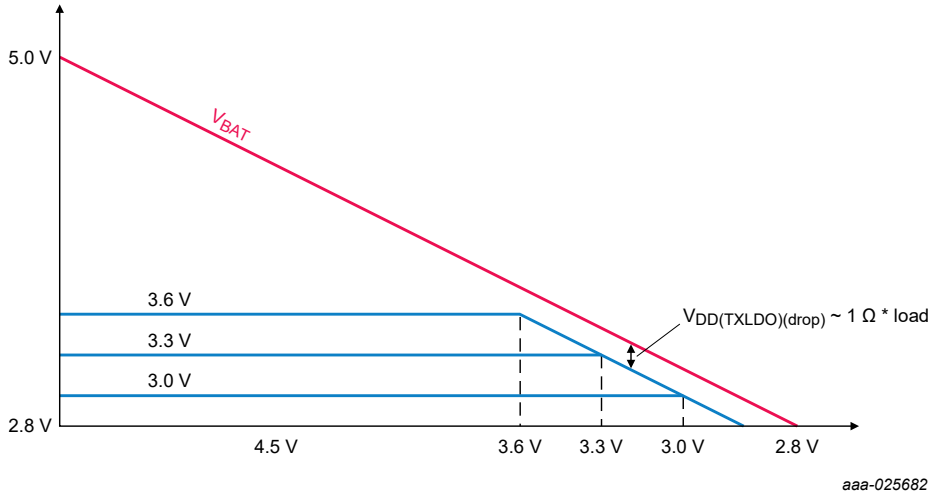


Figure 15. $V_{DD(TX)}$ behavior when supplied from V_{BAT}

In Standby state, whatever $V_{THRESHOLD}$ value is configured, $V_{DD(TX)}$ is regulated at 2.5 V.

Figure 16 shows the case where the PN7160 is in standby state.

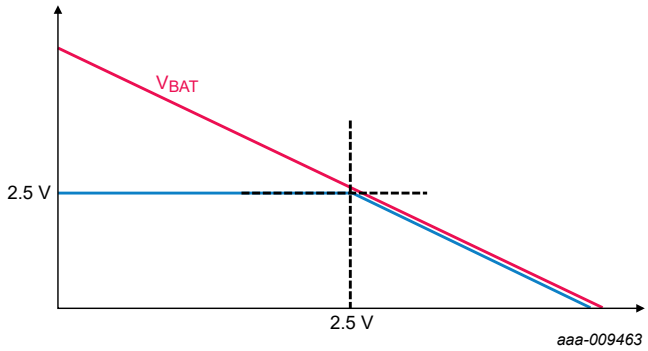


Figure 16. $V_{DD(TX)}$ behavior when PN7160 is in Standby state

10.4.3.2 Configuration 2: an extra external voltage is used to generate the RF field

TXLDO has also the possibility to generate $V_{DD(TX)}$ up to 5.25 V in case the supply of this regulator is an external supply.

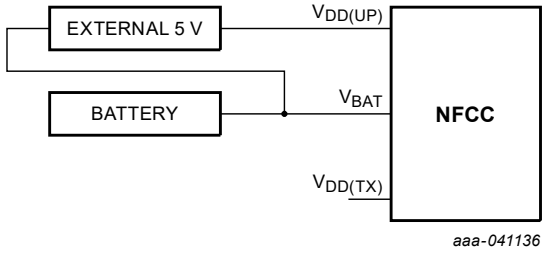


Figure 17. $V_{DD(UP)}$ up to 5.8 V, V_{BAT} up to 5.5 V

Minimum $V_{DD(UP)}$ and V_{BAT} acceptable values depend on communication modes to be covered (see Table 29)

The TXLDO output voltage is then given by:

$$V_{DD(UP)} \geq V_{THRESHOLD} + V_{DD(TXLDO)(drop)} \Rightarrow V_{DD(TX)} = V_{THRESHOLD}$$

$$V_{THRESHOLD} \geq V_{DD(UP)} - V_{DD(TXLDO)(drop)} \geq 2.8V \Rightarrow V_{DD(TX)} = V_{DD(UP)} - V_{DD(TXLDO)(drop)}$$

Figure 18 shows the behavior of $V_{DD(TX)}$ depending on $V_{DD(UP)}$ value.

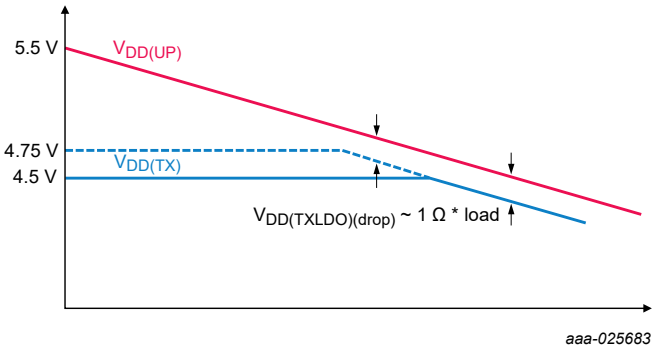


Figure 18. $V_{DD(TX)}$ behavior when PN7160 is supply using external supply on $V_{DD(UP)}$

In Standby state, whatever $V_{THRESHOLD}$ is configured, $V_{DD(TX)}$ is regulated at 2.5 V as illustrated by Figure 16.

10.4.3.3 TXLDO limiter

The TXLDO includes a current limiter to avoid too high current within TX1 and TX2.

The current limiter block compares an image of the TXLDO output current to a reference, when the reference is reached the output current gets limited.

The limiting current is 300 mA ± 30 mA, above the specified maximum current allowed for RF operation (250 mA).

10.4.3.4 TXLDO: configuration

Table 18. Configurations using TXLDO

PN7160 power state	TXLDO config.	Mode	$V_{DD(TX)}$
Active mode	configuration 1	Full-power	2.7 V/3 V/3.3 V/3.6 V [1]
	configuration 2	Full-power	2.7 V/3 V/3.3 V/3.6 V/3.9 V/4.2 V/4.5 V/4.7 V/4.75 V/5 V/5.25 V [1]
Standby	configuration 1 and configuration 2	Low-power	2.5 V
Hard-Power down	configuration 1 and configuration 2	Power-off	High impedance

[1] For proper operation, the $V_{DD(TX)}$ voltage value set shall be below the $V_{DD(UP)}$ - 0.3 V value. The maximum $V_{DD(UP)}$ value is 5.8 V in configuration 2. In configuration 1 the voltage is given by the battery then the higher voltages might not be usable.

When using an external DC-to-DC with pass-through functionality, the signal TX_PWR_REQ is used for control purpose. The DC-to-DC will be in pass-through mode except when high transmitter power is required (by default when RF emission or RF field present).

Note: the signal TX_PWR_REQ is not available on the HVQFN package variant.

10.4.4 Very low-power RF field detector

A very specific use case is the RF field detection when the NFCC is in Power Off mode. In this scenario, the NFCC should detect the presence of an external magnetic field and notify the host system about its presence.

Figure 19 shows the internal rectifier circuit. The circuit is built up by the input switches SW1 and SW2 which can disconnect the rectifier from the antenna by creating a short to ground. The rectifier itself is followed by a limiter.

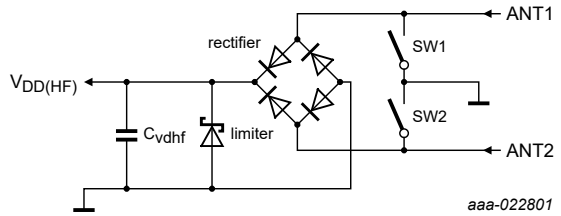


Figure 19. Internal rectifier circuit

10.5 Reset and download concept

10.5.1 Resetting PN7160

To enter reset, the V_{EN} voltage shall be set to low (this is also the Hard Power Down state):

Reset means resetting the embedded FW execution and the registers values to their default values. Parts of these default values are defined from EEPROM data loaded values, others are hardware defined. See Ref. [5] to know which ones are accessible to tune PN7160 to the application environment.

To get out of reset:

- Pulling VEN voltage high with V_{BAT} within its operating range

Figure 20 shows reset done via VEN pin.

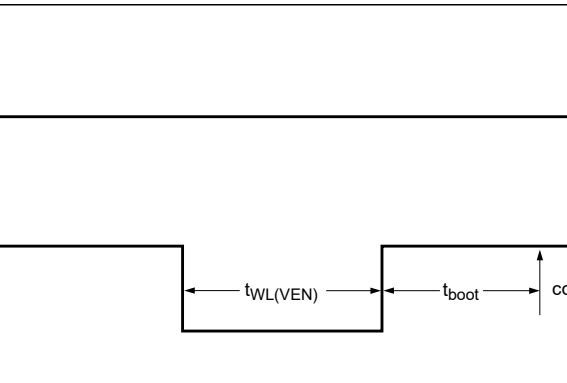


Figure 20. Resetting PN7160 via VEN pin

See Section 14.2.1 for the timings values.

10.5.2 Power-up sequences

PN7160 allows V_{BAT} and $V_{DD(PAD)}$ to be set up independently, therefore different power-up sequences have to be considered.

In all cases, host communication with PN7160 will only be possible after one defined amount of time from the different supply sequence setup and VEN reset pin.

10.5.2.1 V_{BAT} is set up before $V_{DD(PAD)}$

This is at least the case when V_{BAT} pin is directly connected to the battery and when PN7160 V_{BAT} is always supplied as soon the system is supplied.

As VEN pin is referred to V_{BAT} pin, V_{EN} shall go high after V_{BAT} has been set.

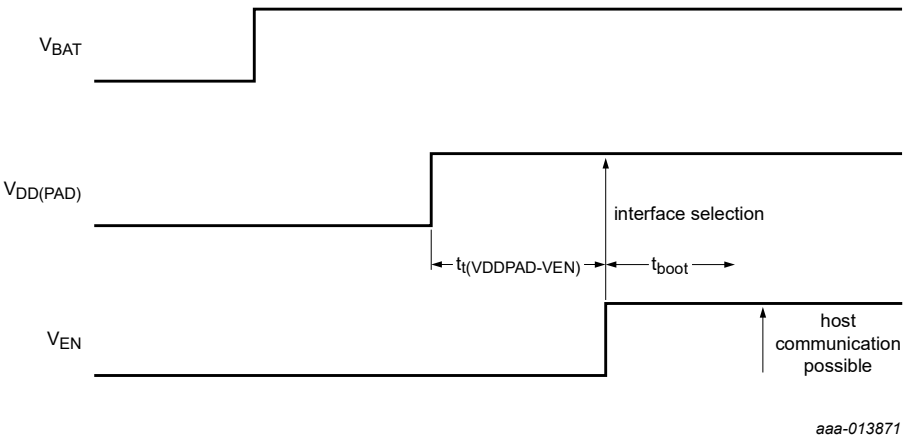


Figure 21. V_{BAT} is set up before $V_{DD(PAD)}$

See Section 14.2.1 and Section 14.2.2 for the timings values.

10.5.2.2 $V_{DD(PAD)}$ and V_{BAT} are set up at the same time

This is the case, when V_{BAT} pin is connected to a PMU/regulator which also supply $V_{DD(PAD)}$.

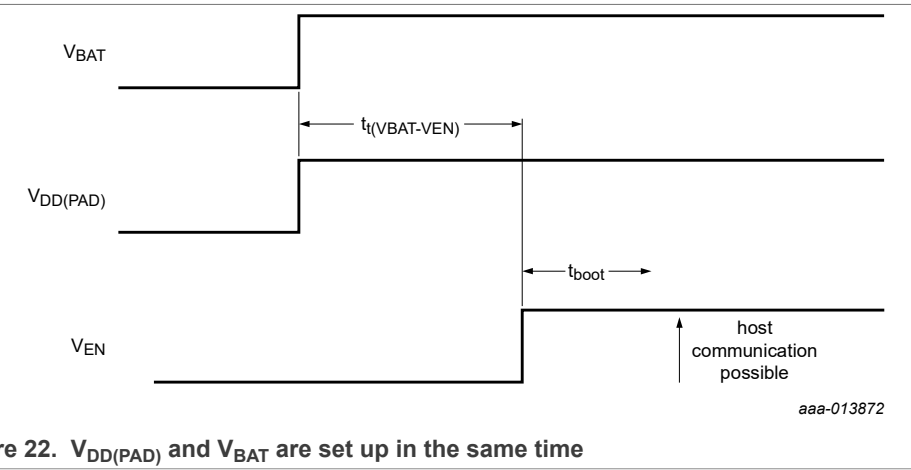


Figure 22. $V_{DD(PAD)}$ and V_{BAT} are set up in the same time

See Section 14.2.1 and Section 14.2.2 for the timings values.

10.5.2.3 PN7160 has been enabled before $V_{DD(PAD)}$ is set up or before $V_{DD(PAD)}$ has been cut-off

This can be the case when V_{BAT} pin is directly connected to the battery and when $V_{DD(PAD)}$ is generated from a PMU. When the battery voltage is too low, then the PMU might no more be able to generate $V_{DD(PAD)}$. When the device gets charged again, then $V_{DD(PAD)}$ is set up again.

As the pins to select the interface are biased from $V_{DD(PAD)}$, when $V_{DD(PAD)}$ disappears the pins might not be correctly biased internally and the information might be lost. Therefore it is required to make the IC boot after $V_{DD(PAD)}$ is set up again.

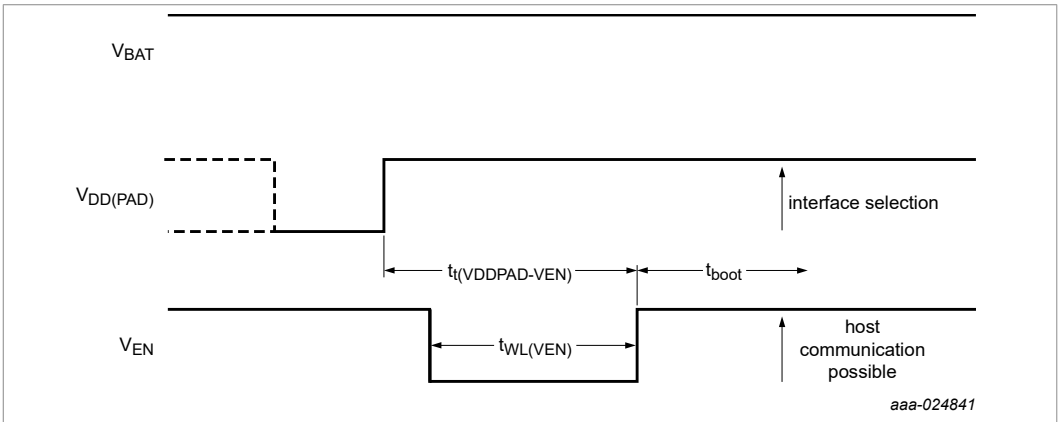


Figure 23. $V_{DD(PAD)}$ is set up or cut-off after PN7160 has been enabled

See Section 14.2.1 and Section 14.2.2 for the timings values.

10.5.3 Power-down sequences

During power-down sequence, V_{EN} shall always be set low before $V_{DD(PAD)}$ is shut down.

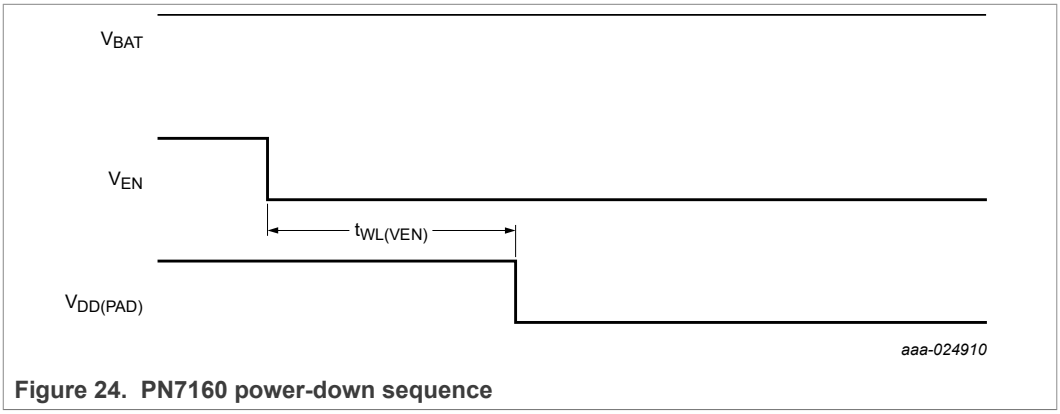


Figure 24. PN7160 power-down sequence

See Section 14.2.1 for the timings values.

10.5.4 Download mode

PN7160 offers the possibility to download EEPROM with upgrades using the host interface commands, see Ref. [5] for more details.

To enter this mode, the pin DWL_REQ shall be pulled to $V_{DD(PAD)}$ before reset via VEN pin is done.

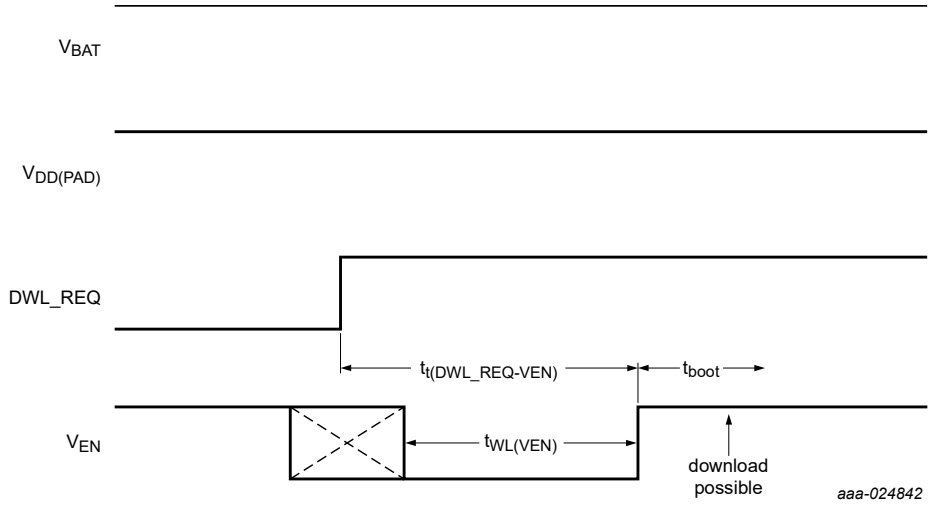


Figure 25. PN7160 download mode sequence

See Section 14.2.1 and Section 14.2.4 for the timings values.

10.6 Contactless Interface Unit

PN7160 supports various communication modes at different transfer speeds and modulation schemes. The following chapters give more detailed overview of selected communication modes.

Remark: all indicated modulation index and modes in this chapter are system parameters. This means that beside the IC settings a suitable antenna tuning is required to achieve the optimum performance.

10.6.1 Reader/Writer communication modes

Generally 5 Reader/Writer communication modes are supported:

- PCD Reader/Writer for ISO/IEC 14443A/MIFARE (NFC Forum Types 2 and 4 Tags)
- PCD Reader/Writer for NFC Forum Type 1 Tag
- PCD Reader/Writer for NFC Forum Type 3 Tag
- PCD Reader/Writer for ISO/IEC 14443B (NFC Forum Type 4 Tag)
- VCD Reader/Writer for NFC Forum Type 5 Tag

10.6.1.1 R/W mode for NFC Forum Type 1 and 2 Tags and Type 4 Tag type A

The R/W mode for NFC Forum Type 1 Tag (T1T), Type 2 Tag (T2T) and Type 4 Tag type A (T4T) is the general reader to card communication scheme according to the ISO/IEC 14443A specification.

Figure 26 describes the communication on a physical level, the communication table describes the physical parameters (the numbers take the antenna effect on modulation depth for higher data rates).

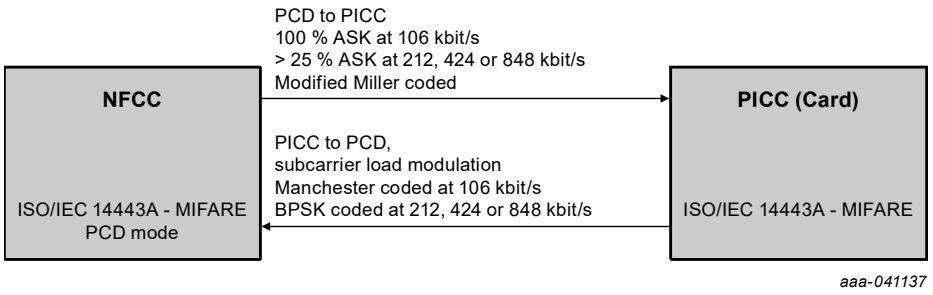


Figure 26. R/W mode for NFC Forum T1T, T2T and T4T type A communication diagram

Table 19. Communication overview for NFC Forum T1T, T2T and T4T type A R/W mode

Communication direction		**ISO/IEC 14443A/ MIFARE/ NFC Forum T2T and T4T**	**ISO/IEC 14443A higher transfer speeds**		
	Transfer speed	**106 kbit/s**	**212 kbit/s**	**424 kbit/s**	**848 kbit/s**
	Bit length	**(128/13.56) µs**	**(64/13.56) µs**	**(32/13.56) µs**	**(16/13.56) µs**
PN7160 → PICC					
(data sent by PN7160 to a card)	modulation on PN7160 side	100 % ASK	> 25 % ASK	> 25 % ASK	> 25 % ASK
	bit coding	Modified Miller	Modified Miller	Modified Miller	Modified Miller
PICC → PN7160					
(data received by PN7160 from a card)	modulation on PICC side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	bit coding	Manchester	BPSK	BPSK	BPSK

The contactless coprocessor and the on-chip CPU of PN7160 handle the complete ISO/IEC 14443A/MIFARE RF-protocol, nevertheless a dedicated external host has to handle the application layer communication.

10.6.1.2 R/W mode for NFC Forum Type 3 Tag, FeliCa communication mode

The R/W mode for NFC Forum Type 3 Tag (T3T) is the general Reader/Writer to card communication scheme according to the FeliCa specification. Figure 27 describes the communication on a physical level, the communication overview describes the physical parameters.

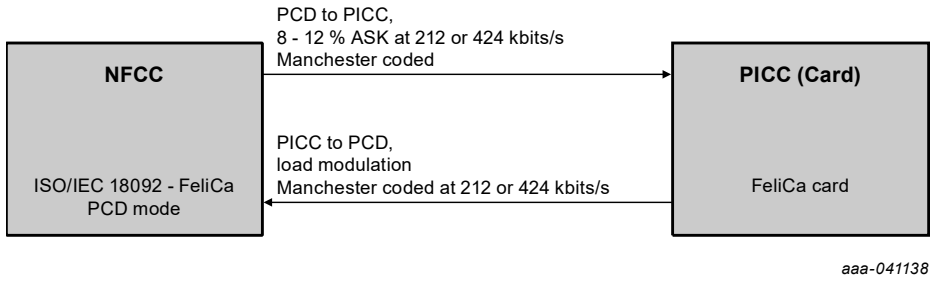


Figure 27. R/W mode for NFC Forum T3T communication diagram

Table 20. Communication overview for NFC Forum T3T R/W mode, FeliCa communication mode

Communication direction		FeliCa	FeliCa higher transfer speeds
	Transfer speed	212 kbit/s	424 kbit/s
	Bit length	(64/13.56) µs	(32/13.56) µs
PN7160 → PICC			
(data sent by PN7160 to a card)	modulation on PN7160 side	8 % - 12 % ASK	8 % - 12 % ASK
	bit coding	Manchester	Manchester
PICC → PN7160			
(data received by PN7160 from a card)	modulation on PICC side	load modulation	load modulation
	subcarrier frequency	no subcarrier	no subcarrier
	bit coding	Manchester	Manchester

The contactless coprocessor of PN7160 and the on-chip CPU handle the FeliCa protocol. Nevertheless a dedicated external host has to handle the application layer communication.

10.6.1.3 R/W mode for NFC Forum type 4 Tag (T4T) type B

The R/W mode for the NFC Forum Type 4 Tag of type B is the general reader to card communication scheme according to the ISO/IEC 14443B specification.Figure 28 describes the communication on a physical level, the communication table describes the physical parameters.

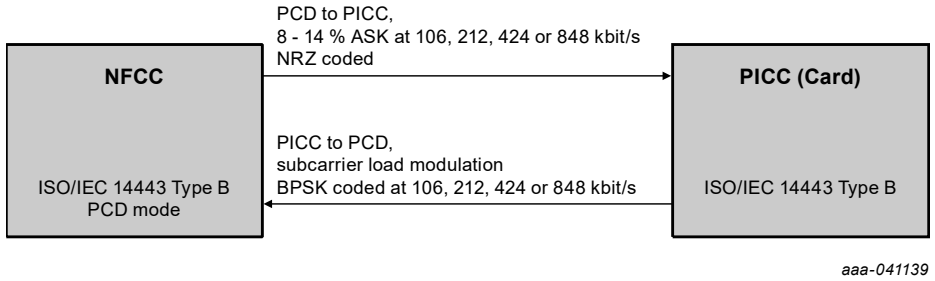


Figure 28. R/W mode for NFC forumT4T type B communication diagram

Table 21. Communication overview for NFC Forum T4T type B R/W mode

Communication direction		ISO/IEC 14443B	ISO/IEC 14443B higher transfer speeds		
	Transfer speed	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s
	Bit length	(128/13.56) µs	(64/13.56) µs	(32/13.56) µs	(16/13.56) µs
PN7160 → PICC					
(data sent by PN7160 to a card)	modulation on PN7160 side	8 % - 14 % ASK	8 % - 14 % ASK	8 % - 14 % ASK	8 % - 14 % ASK
	bit coding	NRZ	NRZ	NRZ	NRZ
PICC → PN7160					
(data received by PN7160 from a card)	modulation on PICC side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	bit coding	BPSK	BPSK	BPSK	BPSK

The contactless coprocessor and the on-chip CPU of PN7160 handles the complete ISO/IEC 14443B RF-protocol, nevertheless a dedicated external host has to handle the application layer communication.

10.6.1.4 R/W mode for NFC Forum Type 5 Tag

The R/W mode for NFC Forum Type 5 Tag (T5T) is the general reader to card communication scheme according to the ISO/IEC 15693 specification. PN7160 communicates with VICC (Type 5 Tag) using only 26.48 kbit/s with single subcarrier.

PN7160 supports the commands as defined by the ETSI HCI (see Ref. [11]) and on top offers the inventory of the tags (anti-collision sequence) on its own.

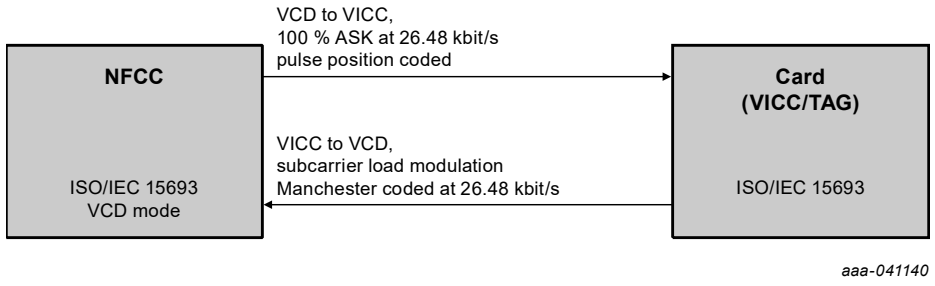


Figure 29. R/W mode for NFC Forum T5T communication diagram

Figure 29 shows the communication schemes used.

The following communication scheme is possible.

Table 22. Communication overview for NFC Forum T5T R/W mode

Communication direction		
PN7160 → VICC		
(data sent by PN7160 to a tag)	transfer speed	26.48 kbit/s
	bit length	(512/13.56) µs
	modulation on PN7160 side	100 % ASK

Table 22. Communication overview for NFC Forum T5T R/W mode*...continued*

Communication direction		
	bit coding	pulse position modulation 1 out of 4 mode
VICC → PN7160		
(data received by PN7160 from a tag)	transfer speed	26.48 kbit/s
	bit length	(512/13.56) µs
	modulation on VICC side	subcarrier load modulation
	subcarrier frequency	single subcarrier
	bit coding	Manchester

10.6.2 ISO/IEC 18092, Ecma 340 NFCIP-1 communication modes

An NFCIP-1 communication takes place between 2 devices:

- NFC Initiator: generates RF field at 13.56 MHz and starts the NFCIP-1 communication.
- NFC Target: responds to NFC Initiator command either in a load modulation scheme in Passive communication mode or using a self-generated and self-modulated RF field for Active communication mode.

The NFCIP-1 communication differentiates between Active and Passive communication modes.

- Active communication mode means both the NFC Initiator and the NFC Target are using their own RF field to transmit data
- Passive communication mode means that the NFC Target answers to an NFC Initiator command in a load modulation scheme. The NFC Initiator is active in terms of generating the RF field.

PN7160 supports the Active Initiator, Active Target, Passive Initiator and Passive Target communication modes at the transfer speeds 106 kbit/s, 212 kbit/s and 424 kbit/s as defined in the NFCIP-1 standard.

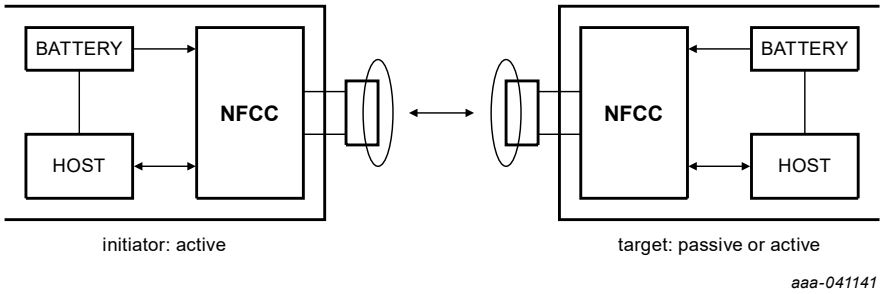


Figure 30. NFCIP-1 communication mode

The contactless coprocessor of PN7160 and the on-chip CPU handle NFCIP-1 protocol, for all communication modes and data rates, for both NFC Initiator and NFC Target.

Nevertheless a dedicated external host has to handle the application layer communication.

10.6.2.1 Active communication mode

Active communication mode means both the NFC Initiator and the NFC Target are using their own RF field to transmit data.

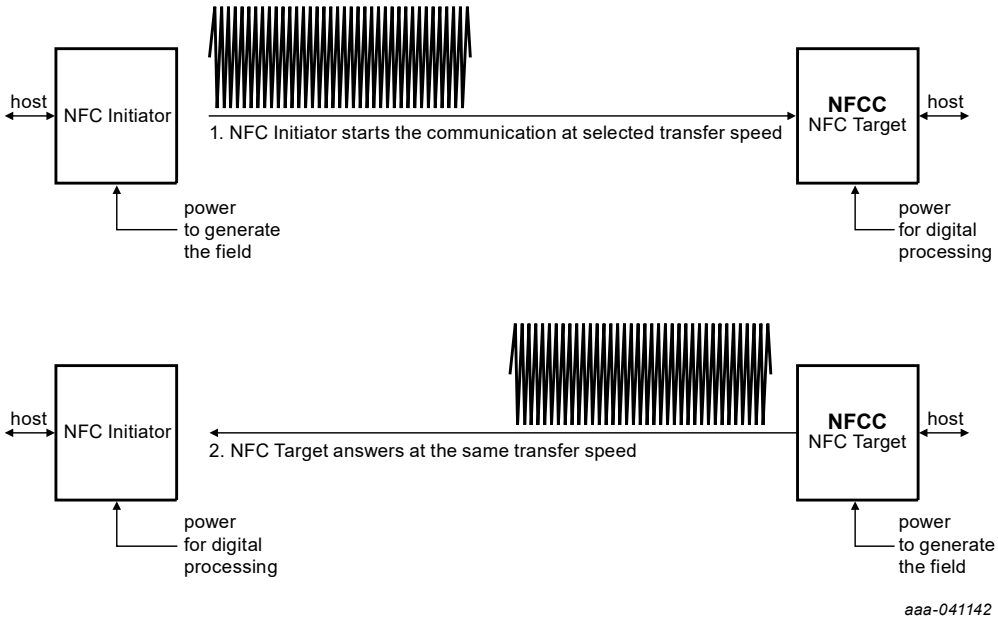


Figure 31. Active communication mode

Table 23 gives an overview of the Active communication modes:

Table 23. Overview for Active communication mode

Communication direction		ISO/IEC 18092, Ecma 340, NFCIP-1		
	Baud rate	106 kbit/s	212 kbit/s	424 kbit/s
	Bit length	(128/13.56) µs	(64/13.56) µs	(32/13.56) µs
NFC Initiator to NFC Target				
	modulation	100 % ASK	8 % - 30 % ASK [1]	8 % - 30 % ASK [1]
	bit coding	Modified Miller	Manchester	Manchester
NFC Target to NFC Initiator				
	modulation	100 % ASK	8 % - 30 % ASK [1]	8 % - 30 % ASK [1]
	bit coding	Miller	Manchester	Manchester

[1] This modulation index range is according to NFCIP-1 standard. It might be that some NFC Forum type 3 cards does not withstand the full range as based on FeliCa range which is narrow (8 % to 14 % ASK). To adjust the index, see [7].

10.6.2.2 Passive communication mode

Passive communication mode means that the NFC Target answers to an NFC Initiator command in a load modulation scheme.

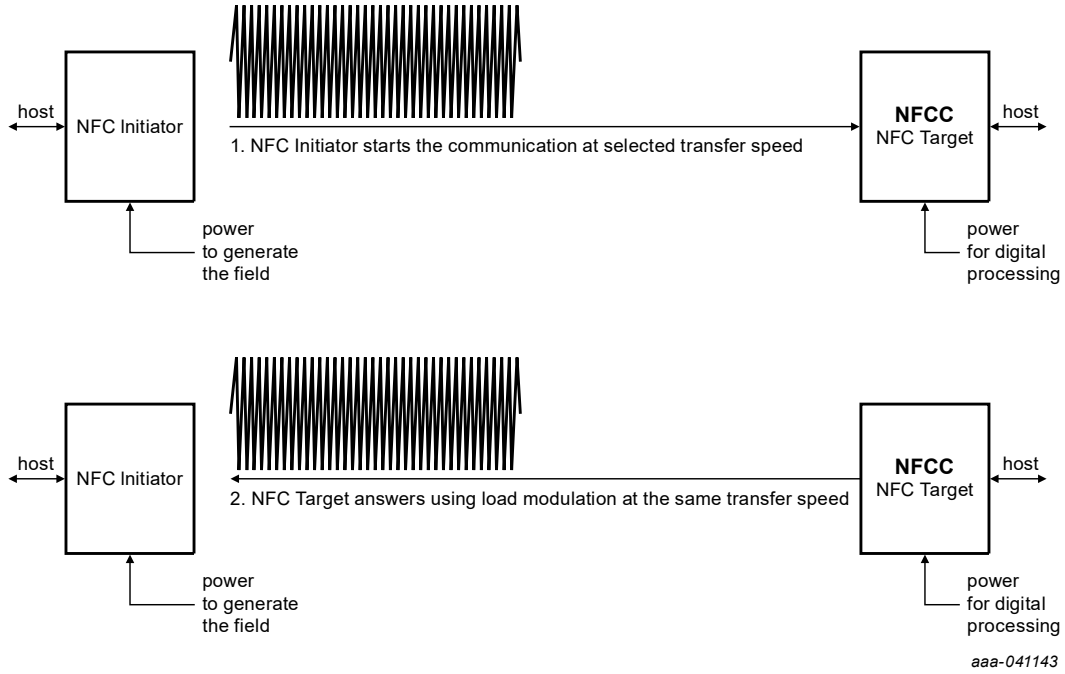


Figure 32. Passive communication mode

Table 24 gives an overview of the Passive communication modes:

Table 24. Overview for Passive communication mode

Communication direction		ISO/IEC 18092, Ecma 340, NFCIP-1		
	Baud rate	**106 kbit/s**	**212 kbit/s**	**424 kbit/s**
	Bit length	**(128/13.56) µs**	**(64/13.56) µs**	**(32/13.56) µs**
NFC Initiator to NFC Target				
	modulation	100 % ASK	8 % - 30 % ASK [1]	8 % - 30 % ASK [1]
	bit coding	Modified Miller	Manchester	Manchester
NFC Target to NFC Initiator				
	modulation	subcarrier load modulation	load modulation	load modulation
	subcarrier frequency	13.56 MHz/16	no subcarrier	no subcarrier
	bit coding	Manchester	Manchester	Manchester

[1] This modulation index range is according to NFCIP-1 standard. It might be that some NFC Forum type 3 cards does not withstand the full range as based on FeliCa range which is narrow (8 % to 14 % ASK). To adjust the index, see Ref. [7].

10.6.2.3 NFCIP-1 framing and coding

The NFCIP-1 framing and coding in Active and Passive communication modes are defined in the NFCIP-1 standard: ISO/IEC 18092 or Ecma 340.

10.6.2.4 NFCIP-1 protocol support

The NFCIP-1 protocol is not completely described in this document. For detailed explanation of the protocol, refer to the ISO/IEC 18092 or Ecma 340 NFCIP-1 standard. However the datalink layer is according to the following policy:

- Transaction includes initialization, anti-collision methods and data transfer. This sequence must not be interrupted by another transaction.
- PSL shall be used to change the speed between the target selection and the data transfer, but the speed should not be changed during a data transfer.

10.6.3 Card mode

PN7160 can be addressed as an NFC Forum T3T, NFC Forum T4T, ISO/IEC 14443A, MIFARE, ISO/IEC 14443B cards. This means that PN7160 can generate an answer in a load modulation scheme according to the ISO/IEC 14443A, ISO/IEC 14443B and Sony FeliCa interface description.

Remark: PN7160 does not support a complete card protocol. This has to be handled by the host controller.

Table 25, Table 26 and Table 27 describe the physical parameters.

10.6.3.1 NFC Forum T4T, ISO/IEC 14443A

Table 25. Overview for NFC Forum T4T, ISO/IEC 14443A card mode

Communication direction		ISO/IEC 14443A	ISO/IEC 14443A higher transfer speeds	
	Transfer speed	106 kbit/s	212 kbit/s	424 kbit/s
	Bit length	(128/13.56) µs	(64/13.56) µs	(32/13.56) µs
PCD → PN7160				
(data received by PN7160 from a card)	modulation on PCD side	100 % ASK	> 25 % ASK	> 25 % ASK
	bit coding	Modified Miller	Modified Miller	Modified Miller
PN7160 → PCD				
(data sent by PN7160 to a card)	modulation on PN7160 side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	bit coding	Manchester	BPSK	BPSK

10.6.3.2 NFC Forum T4T, ISO/IEC 14443B card mode

Table 26. Overview for NFC Forum T4T, ISO/IEC 14443B card mode

Communication direction		ISO/IEC 14443B	ISO/IEC 14443B higher transfer speeds	
	Transfer speed	106 kbit/s	212 kbit/s	424 kbit/s
	Bit length	(128/13.56) µs	(64/13.56) µs	(32/13.56) µs
PCD → PN7160				
(data received by PN7160 from a Reader)	modulation on PCD side	8 % - 14 % ASK	8 % - 14 % ASK	8 % - 14 % ASK

Table 26. Overview for NFC Forum T4T, ISO/IEC 14443B card mode*...continued*

Communication direction		ISO/IEC 14443B	ISO/IEC 14443B higher transfer speeds	
	Transfer speed	**106 kbit/s**	**212 kbit/s**	**424 kbit/s**
	Bit length	**(128/13.56) µs**	**(64/13.56) µs**	**(32/13.56) µs**
	bit coding	NRZ	NRZ	NRZ
PN7160 → PCD				
(data sent by PN7160 to a Reader)	modulation on PN7160 side	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	bit coding	BPSK	BPSK	BPSK

10.6.3.3 NFC Forum T3T, Sony FeliCa card mode

Table 27. Overview for NFC Forum T3T, Sony FeliCa card mode

Communication direction		FeliCa	FeliCa higher transfer speeds
	Transfer speed	**212 kbit/s**	**424 kbit/s**
	Bit length	**(64/13.56) µs**	**(32/13.56) µs**
PCD → PN7160			
(data received from a reader by the PN7160)	modulation on PN7160 side	8 % - 12 % ASK	8 % - 12 % ASK
	bit coding	Manchester	Manchester
PN7160 → PCD			
(data sent by PN7160 to a reader)	modulation on PICC side	load modulation	load modulation
	subcarrier frequency	no subcarrier	no subcarrier
	bit coding	Manchester	Manchester

10.6.4 Frequency interoperability

When in communication, PN7160 is generating some RF frequencies. PN7160 is also sensitive to some RF signals as it is looking from data in the field.

In order to avoid interference with others RF communication, it is required to tune the antenna and design the board according to Ref.[6].

Although ISO/IEC 14443 and ISO/IEC 18092/Ecma 340 allows an RF frequency of 13.56 MHz ± 7 kHz, FCC regulation does not allow this wide spread and limits the dispersion to ± 100 ppm, which is in line with PN7160 capability, see Table 15 and Table 16.

11 Limiting values

Table 28. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(PAD)}$	$V_{DD(PAD)}$ supply voltage	supply voltage for host interface		-	4.2	V
$V_{DD(UP)}$	$V_{DD(UP)}$ supply voltage	supply voltage for host interface		-	7	V
V_{BAT}	battery supply voltage			-	6	V
V_{ESD}	electrostatic discharge voltage	HBM; 1500 Ω, 100 pF; EIA/JESD22-A114-D		-	2	kV
		CDM; field induced model; EIA/JESC22-C101-C		-	1	kV
T_{stg}	storage temperature			-40	+150	°C
P_{tot}	total power dissipation	all modes	[1]	-	620	mW
$V_{RXN(i)}$	RXN input voltage			0	2.5	V
$V_{RXP(i)}$	RXP input voltage			0	2.5	V

[1] The design of the solution shall be done so that for the different use cases targeted the power to be dissipated from the field or generated by PN7160 does not exceed this value.

12 Recommended operating conditions

Table 29. Operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb}	ambient temperature	JEDEC PCB-0.5		-25	-	+85	°C
V_{BAT}	battery supply voltage	Card Emulation and Passive Target; V_{SS} = 0 V	[1]	2.5	-	5.5	V
		Reader, Active Initiator and Active Target; V_{SS} = 0 V	[1]	2.8	-	5.5	V
$V_{DD(UP)}$	$V_{DD(UP)}$ input supply voltage	Reader, Active Initiator and Active Target; V_{SS} = 0 V	[1]	2.8	-	5.8	V
		All other cases except HPD state; V_{SS} = 0 V	[1] [2]	2.5	-	5.8	V
$V_{DD(PAD)}$	$V_{DD(PAD)}$ supply voltage	supply voltage for host interface; V_{SS} = 0 V	[1]	1.65	1.8	1.95	V
				3.0	3.3	3.6	V
P_{tot}	total power dissipation	PCD mode at typical $V_{DD(TX)}$ = 5.25 V, $V_{DD(UP)}$ = 5.8 V and V_{BAT} = 3.6 V; includes power from V_{BAT} and $V_{DD(UP)}$		-	-	620	mW
I_{BAT}	battery supply current	in Hard Power Down state; V_{BAT} = 3.6 V; T = 25 °C	[3]	-	10.5	16	µA
		in Standby state; V_{BAT} = 3.6 V					
		enhanced RF detector		-	31	52	µA
		low sensitivity RF detector		-	21	36	µA
		in low-power polling loop; V_{BAT} = 3.6 V; T = 25 °C; loop time = 500 ms		-	100	-	µA
		continuous total current consumption in PCD mode at V_{BAT} = 3.6 V	[4]	-	-	290	mA
$I_{th(Ilim)}$	current limit threshold	current limiter on transmitter	[4]	270	300	330	mA

[1] V_{SS} represents $V_{SS(PAD)}$ and $V_{SS(TX)}$.
[2] When $V_{DD(UP)}$ is below 2.8 V the TXLDO can be in follower mode (see Section 10.4.3), there will be no more $V_{DD(UP)}$ noise rejection. Any noise below 848 kbit/s will affect the performance.
[3] External clock on NFC_CLK_XTAL1 must be LOW.
[4] This is considering an antenna tuned to sink maximum 250 mA continuous current from the transmitter. The antenna shall be tuned to never exceed this 250 mA maximum current.

13 Thermal characteristics

Table 30. Thermal characteristics VFBGA64 package

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air with exposed pad soldered on a 4 layer JEDEC PCB	52.0	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	-	10.0	K/W

Table 31. Thermal characteristics HVQFN40 package

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air with exposed pad soldered on a 4 layer JEDEC PCB	28.0	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	-	13.2	K/W

Table 32. Junction Temperature

Symbol	Parameter	Conditions	Max	Unit
T_{j_max}	maximum junction temperature	-	125	°C

Table 33. Thermal Shutdown Temperature

Symbol	Parameter	Conditions	Typ	Unit
$T_{shutdown}$	shutdown of chip due to high temperature detected by temp sensor	-	125	°C

14 Characteristics

14.1 Current consumption characteristics

Table 34. Current consumption characteristics for operating ambient temperature range

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{BAT}	battery supply current	in Hard Power Down state; V_{BAT} = 3.6 V; VEN voltage = 0 V		-	10	24	µA
		in Standby state; V_{BAT} = 3.6 V;	[1]	-	20	35	µA
		in Idle and Target Active power states; V_{BAT} = 3.6 V		-	4.55	-	mA
		in Initiator Active power state; V_{BAT} = 3.6 V; RF on	[2]	-	240	-	mA

[1] Refer to Section 10.1.2 for the description of the power modes.
[2] For transmitter current tuned at 210 mA unloaded.

14.2 Functional block electrical characteristics

14.2.1 Reset via VEN

Table 35. Reset timing

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{WL(VEN)}$	pulse width VEN LOW	to reset		10	-	-	µs
t_{boot}	boot time			-	-	2.5	ms

14.2.2 Power-up timings

Table 36. Power-up timings

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{t(VBAT-VEN)}$	transition time from pin V_{BAT} to pin VEN	V_{BAT}, VEN voltages = HIGH		0	-	-	ms
$t_{t(VDDPAD-VEN)}$	transition time from pin $V_{DD(PAD)}$ to pin VEN	$V_{DD(PAD)}$, VEN voltages = HIGH		0	-	-	ms
$t_{t(VBAT-VDDPAD)}$	transition time from pin V_{BAT} to pin $V_{DD(PAD)}$	V_{BAT}, $V_{DD(PAD)}$ = HIGH		0	-	-	ms

14.2.3 Power-down timings

Table 37. Power-down timings

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{WL(VBAT)}$	pulse width V_{BAT} LOW			20	-	-	ms
t_d	delay time			0	-	-	ms

14.2.4 Download mode timings

Table 38. Download mode timings

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{t(DWL\_REQ-VEN)}$	transition time from pin DWL_REQ to pin VEN	DWL_REQ, VEN voltages = HIGH		0	0.5	-	ms

14.2.5 I²C-bus timings

Here below are timings and frequency specifications.

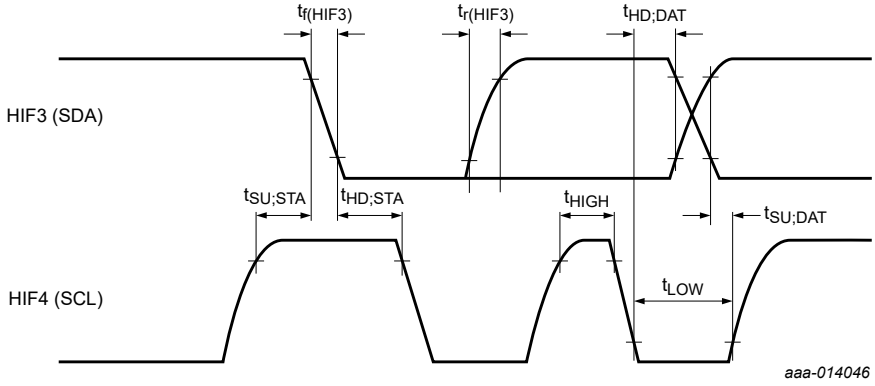


Figure 33. I²C-bus timings

Table 39. High-speed mode I²C-bus timings specification

Symbol	Parameter	Conditions		Min	Max	Unit
$f_{clk(HIF4)}$	clock frequency on pin HIF4	I²C-bus SCL; C_b < 100 pF		0	3.4	MHz
$t_{SU;STA}$	set-up time for a repeated START condition	C_b < 100 pF		160	-	ns
$t_{HD;STA}$	hold time (repeated) START condition	C_b < 100 pF		160	-	ns
t_{LOW}	LOW period of the SCL clock	C_b < 100 pF		160	-	ns
t_{HIGH}	HIGH period of the SCL clock	C_b < 100 pF		60	-	ns
$t_{SU;DAT}$	data set-up time	C_b < 100 pF		10	-	ns
$t_{HD;DAT}$	data hold time	C_b < 100 pF		0	-	ns
$t_{r(HIF3)}$	rise time on pin HIF3	I²C-bus SDA; C_b < 100 pF		10	80	ns
$t_{f(HIF3)}$	fall time on pin HIF3	I²C-bus SDA; C_b < 100 pF		10	80	ns
V_{hys}	hysteresis voltage	Schmitt trigger inputs; C_b < 100 pF		$0.1V_{DD(PAD)}$	-	V

Table 40. Fast mode I^2C-bus timings specification

Symbol	Parameter	Conditions		Min	Max	Unit
$f_{clk(HIF4)}$	clock frequency on pin HIF4	I^2C-bus SCL; C_b < 400 pF		0	400	kHz
$t_{SU;STA}$	set-up time for a repeated START condition	C_b < 400 pF		600	-	ns
$t_{HD;STA}$	hold time (repeated) START condition	C_b < 400 pF		600	-	ns
t_{LOW}	LOW period of the SCL clock	C_b < 400 pF		1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock	C_b < 400 pF		600	-	ns
$t_{SU;DAT}$	data set-up time	C_b < 400 pF		100	-	ns
$t_{HD;DAT}$	data hold time	C_b < 400 pF		0	900	ns
V_{hys}	hysteresis voltage	Schmitt trigger inputs; C_b < 400 pF		$0.1V_{DD(PAD)}$	-	V

14.2.6 SPI-bus timings

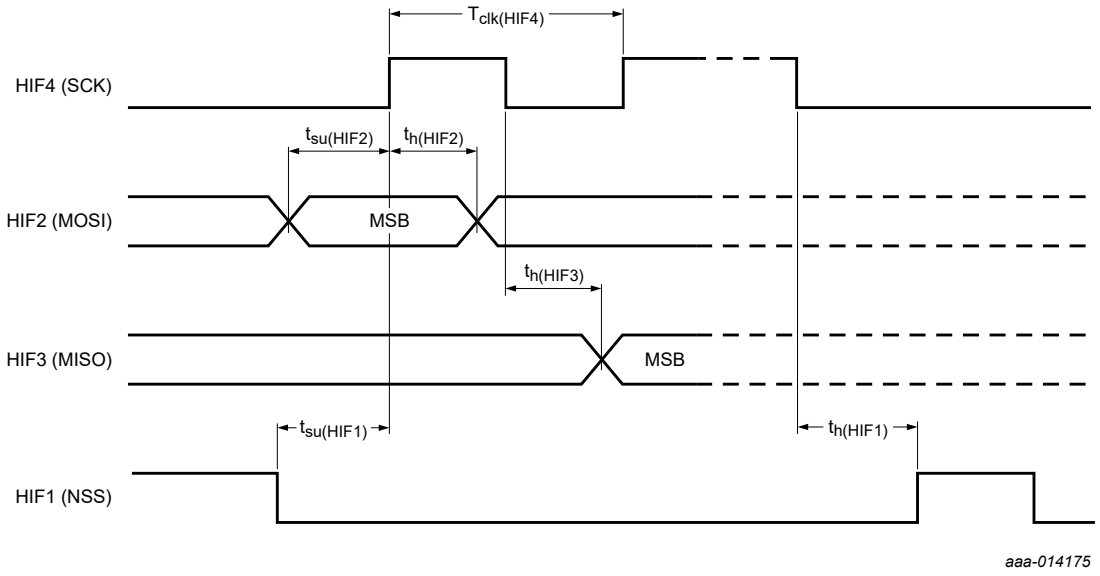


Figure 34. SPI-bus timing diagram

Table 41. SPI-bus timings specification

Symbol	Parameter	Conditions		Min	Max	Unit
$T_{clk(HIF4)}$	clock period on pin HIF4	SPI SCK		142	-	ns
$t_{su(HIF2)}$	HIF2 set-up time	SPI MOSI	[1]	35	-	ns
$t_{h(HIF2)}$	HIF2 hold time	SPI MOSI	[1]	35	-	ns
$t_{h(HIF3)}$	HIF3 hold time	SPI MISO	[2]	-	37	ns
$t_{h(HIF1)}$	HIF1 hold time	SPI NSS	[1]	37	-	ns
$t_{su(HIF1)}$	HIF1 set-up time	SPI NSS	[1]	142	-	ns

[1] Controlled by host.
[2] Controlled by PN7160.

14.2.7 Active load modulation phase

Table 42. Active load modulation phase error

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
E_{φ}	phase error	ALM phase error from RXP input to clock recovery output 50 mV < V_{RX} < 500 mV		- 5	-	+ 5	°

14.3 Pin characteristics

14.3.1 NFC_CLK_XTAL1 and XTAL2 pins characteristics

Table 43. Input clock characteristics on NFC_CLK_XTAL1 when using PLL

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{i(p-p)}$	peak-to-peak input voltage			0.2	-	1.8	V
δ	duty cycle			35	-	65	%

Table 44. Pin characteristics for NFC_CLK_XTAL1 when PLL input

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{IH}	HIGH-level input current	$V_I = V_{DDD}$		-1	-	+1	µA
I_{IL}	LOW-level input current	V_I = 0 V		-1	-	+1	µA
V_i	input voltage			-	-	V_{DDD}	V
$V_{i(clk)(p-p)}$	peak-to-peak clock input voltage			200	-	-	mV
C_i	input capacitance	all power modes		-	2	-	pF

Table 45. Pin characteristics for 27.12 MHz crystal oscillator

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$C_{i(NFC\_CLK\_XTAL1)}$	NFC_CLK_XTAL1 input capacitance	V_{DDD} = 1.8 V		-	2	-	pF
$C_{i(XTAL2)}$	XTAL2 input capacitance			-	2	-	pF

Table 46. PLL accuracy

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{o(acc)}$	output frequency accuracy	deviation added to NFC_CLK_XTAL1 frequency on RF frequency generated; worst case whatever input frequency		-30	-	+30	ppm

14.3.2 VEN input pin characteristics

Table 47. VEN input pin characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage			1.1	-	V_{BAT}	V
V_{IL}	LOW-level input voltage			0	-	0.4	V
I_{IH}	HIGH-level input current	VEN voltage = V_{BAT}		-1	-	+1	µA
I_{IL}	LOW-level input current	VEN voltage = 0 V		-1	-	+1	µA
C_i	input capacitance			-	5	-	pF

14.3.3 Output pin characteristics for IRQ, CLK_REQ

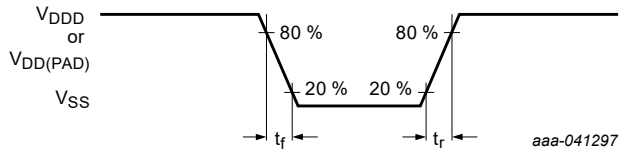


Figure 35. Output timing measurement condition

Table 48. Output pin characteristics for IRQ, CLK_REQ

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} < 3 mA		$V_{DD(PAD)}$ - 0.4	-	$V_{DD(PAD)}$	V
V_{OL}	LOW-level output voltage	I_{OL} < 3 mA		0	-	0.4	V
C_L	load capacitance			-	-	20	pF
t_f	fall time	C_L = 12 pF max	[1]	2	-	10	ns
t_r	rise time	C_L = 12 pF max	[1]	2	-	10	ns
R_{pd}	pull-down resistance	for IRQ and CLK_REQ	[2]	0.35	-	0.85	MΩ
		for IRQ and CLK_REQ	[3] [4]	55	-	120	kΩ

[1] See Figure 35.
[2] Pull-down resistance is activated in HPD state.
[3] Pull-down resistance can be activated by firmware in Standby state.
[4] Pull-down resistance can be activated by firmware in Active state.

14.3.4 Output pin characteristics for TX_PWR_REQ

Table 49. Output pin characteristics for TX_PWR_REQ

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} < 3 mA	[1]	V_{DDD} - 0.4	-	V_{DDD}	V
V_{OL}	LOW-level output voltage	I_{OL} < 3 mA	[1]	0	-	0.4	V

Table 49. Output pin characteristics for TX_PWR_REQ...*continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_L	load capacitance			-	-	20	pF
t_f	fall time	C_L = 12 pF max	[2]	2	-	10	ns
t_r	rise time	C_L = 12 pF max	[2]	2	-	10	ns
R_{pd}	pull-down resistance		[3]	55	-	120	kΩ
R_{pu}	pull-up resistance		[4]	55	-	120	kΩ

[1] TX_PWR_REQ active driving is only possible when $V_{DD(PAD)}$ is present. When $V_{DD(PAD)}$ is not present, only pull-up or pull-down resistors can be enabled.
[2] See Figure 35.
[3] Unless disable by firmware, pull-down resistance is always activated.
[4] Can be enabled by firmware.

14.3.5 Input pin characteristics for DWL_REQ, WKUP_REQ

Table 50. Input pin characteristics for DWL_REQ, WKUP_REQ

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	typical 1.8 V interface supply voltage		$0.65V_{DD(PAD)}$	-	-	V
		typical 3.3 V interface supply voltage		2.0			V
V_{IL}	LOW-level input voltage	typical 1.8 V interface supply voltage		-	-	$0.35V_{DD(PAD)}$	V
		typical 3.3 V interface supply voltage				0.8	
I_{IH}	HIGH-level input current			-1	-	+1	µA
I_{IL}	LOW-level input current			-1	-	+1	µA
C_i	input capacitance			-	5	-	pF
R_{pd}	pull-down resistance	pull-down					
		DWL_REQ pin	[1]	0.35	-	0.85	MΩ
		WKUP_REQ pin	[1]	55	-	120	kΩ

[1] Activated in HPD state.

14.3.6 Input pin characteristics for RXN and RXP

Table 51. Input pin characteristics for RXN and RXP

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{RXN(i)}$	RXN input voltage			0	-	V_{DDA} - 0.05	V

Table 51. Input pin characteristics for RXN and RXP*...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{RXP(i)}$	RXP input voltage			0	-	V_{DDA} - 0.05	V
$C_{i(RXN)}$	RXN input capacitance			-	6	-	pF
$C_{i(RXP)}$	RXP input capacitance			-	6	-	pF
$Z_{i(RXN-VDDMID)}$	input impedance between RXN and $V_{DD(MID)}$	Reader, card and P2P modes		0	-	15	kΩ
$Z_{i(RXP-VDDMID)}$	input impedance between RXP and $V_{DD(MID)}$	Reader, card and P2P modes		0	-	15	kΩ
$V_{i(dyn)(RXN)}$	RXN minimum dynamic input voltage	Miller coded					
		106 kbit/s		-	-	20	mV(p-p)
		212 kbit/s to 424 kbit/s		-	-	20	mV(p-p)
$V_{i(dyn)(RXP)}$	RXP minimum dynamic input voltage	Miller coded					
		106 kbit/s		-	-	20	mV(p-p)
		212 kbit/s to 424 kbit/s		-	-	20	mV(p-p)
$V_{i(dyn)(RXN)}$	RXN minimum dynamic input voltage	Manchester, NRZ or BPSK coded; 106 kbit/s to 848 kbit/s		-	-	20	mV(p-p)
$V_{i(dyn)(RXP)}$	RXP minimum dynamic input voltage	Manchester, NRZ or BPSK coded; 106 kbit/s to 848 kbit/s		-	-	20	mV(p-p)
$V_{i(dyn)(RXN)}$	RXN maximum dynamic input voltage	All data coding; 106 kbit/s to 848 kbit/s		-	-	V_{DDA} - 0.05	V(p-p)
$V_{i(dyn)(RXP)}$	RXP maximum dynamic input voltage	All data coding; 106 kbit/s to 848 kbit/s		-	-	V_{DDA} - 0.05	V(p-p)
$V_{i(RF)}$	RF input voltage for RF level detector	RF input voltage detected for 9 mV threshold		5.5	9	15	mV(p-p)
	RF input voltage for NFC level detector	RF input voltage detected for 15 mV threshold		8	15	23	mV(p-p)

14.3.7 ANT1 and ANT2 pin characteristics

Table 52. Electrical characteristics of ANT1 and ANT2

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_I	input resistance	switches closed; for pins ANTX	[1]	-	10	17	Ω
I_I	input current	for pins ANTX	[1]	-50	-	+50	mA

[1] With X = 1 or 2.

14.3.8 $V_{DD(HF)}$ and V_{DDD} pins characteristics

Table 53. Electrical characteristics of $V_{DD(HF)}$ and V_{DDD}

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DD(HF)}$	$V_{DD(HF)}$ supply voltage	I_{ANTX} = 5 mA	[1]	-	2.7	-	V
V_{DDD}	V_{DDD} supply voltage 1.8 V	V_{SS} = 0 V		1.7	1.8	1.95	V
	V_{DDD} supply voltage 3.3 V			3.0	3.3	3.6	V

[1] With X = 1 or 2.

14.3.9 Output pin characteristics for TX1 and TX2

Table 54. Output pin characteristics for TX1 and TX2

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_{DD(TX)}$ = 3.3 V and I_{OH} = 30 mA; PMOS driver fully on		$V_{DD(TX)}$ - 150	-	-	mV
V_{OL}	LOW-level output voltage	$V_{DD(TX)}$ = 3.3 V and I_{OL} = 30 mA; NMOS driver fully on		-	-	200	mV

Table 55. Output resistance for TX1 and TX2

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_{OL}	LOW-level output resistance	$V_{DD(TX)}$ - 100 mV; CWGsN = 01h		-	-	80	Ω
		$V_{DD(TX)}$ - 100 mV; CWGsN = 0Fh		-	0.9	-	Ω
R_{OH}	HIGH-level output resistance	$V_{DD(TX)}$ = 5 V; $V_{(TXn)}$ = $V_{DD(TX)}$ - 100 mV	[1]	0.65	0.9	1.4	Ω

[1] With n = 1 or 2.

14.3.10 Input pin characteristics for HIF1 (used as SPI-bus NSS, used as I^2C-bus address 0), HIF2 (used as SPI-bus MOSI, used as I^2C-bus address 1), HIF4 (used as SPI-bus SCK)

Table 56. Input pin characteristics for HIF1 (used as SPI-bus NSS, used as I^2C-bus address 0), HIF2 (used as SPI-bus MOSI, used as I^2C-bus address 1), HIF4 (used as SPI-bus SCK)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage			0.65$V_{DD(PAD)}$	-	$V_{DD(PAD)}$	V
V_{IL}	LOW-level input voltage			0	-	0.35$V_{DD(PAD)}$	V
I_{IH}	HIGH-level input current	V_I = $V_{DD(PAD)}$		-1	-	+1	µA

Table 56. Input pin characteristics for HIF1 (used as SPI-bus NSS, used as I^2C-bus address 0), HIF2 (used as SPI-bus MOSI, used as I^2C-bus address 1), HIF4 (used as SPI-bus SCK)*...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{IL}	LOW-level input current	V_I = 0 V		-1	-	+1	µA
C_i	input capacitance			-	5	-	pF
R_{pu}	pull-up resistance	HIF1 used as I^2C-bus address 0; HIF2 used as I^2C-bus address 1	[1]	55	-	120	kΩ

[1] Unless disable by firmware, extra pull-up resistance is always activated.

14.3.11 Pin characteristics for HIF3 (used as I^2C-bus SDA) and HIF4 (used as I^2C-bus SCL)

Table 57. Pin characteristics for HIF3 (used as I^2C-bus SDA) and HIF4 (used as I^2C-bus SCL)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	I_{OL} < 3 mA	[1]	0	-	0.4	V
C_L	load capacitance			-	-	10	pF
t_f	fall time	C_L = 100 pF; Rpull-up = 2 kΩ; Standard and Fast mode	[1]	30	-	250	ns
		C_L = 100 pF; Rpull-up = 1 kΩ; High-speed mode	[1]	80	-	110	ns
t_r	rise time	C_L = 100 pF; Rpull-up = 2 kΩ; Standard and Fast mode	[1]	30	-	250	ns
		C_L = 100 pF; Rpull-up = 1 kΩ; High-speed mode	[1]	10	-	100	ns
V_{IH}	HIGH-level input voltage			$0.7V_{DD(PAD)}$	-	$V_{DD(PAD)}$	V
V_{IL}	LOW-level input voltage			0	-	$0.3V_{DD(PAD)}$	V
I_{IH}	HIGH-level input current	$V_I = V_{DD(PAD)}$; high impedance		-1	-	+1	µA
I_{IL}	LOW-level input current	V_I = 0 V; high impedance		-1	-	+1	µA
C_i	input capacitance			-	5	-	pF

[1] Only for pin HIF3 (I^2C-bus SDA), HIF4 (I^2C-bus SCL) is only used as input.

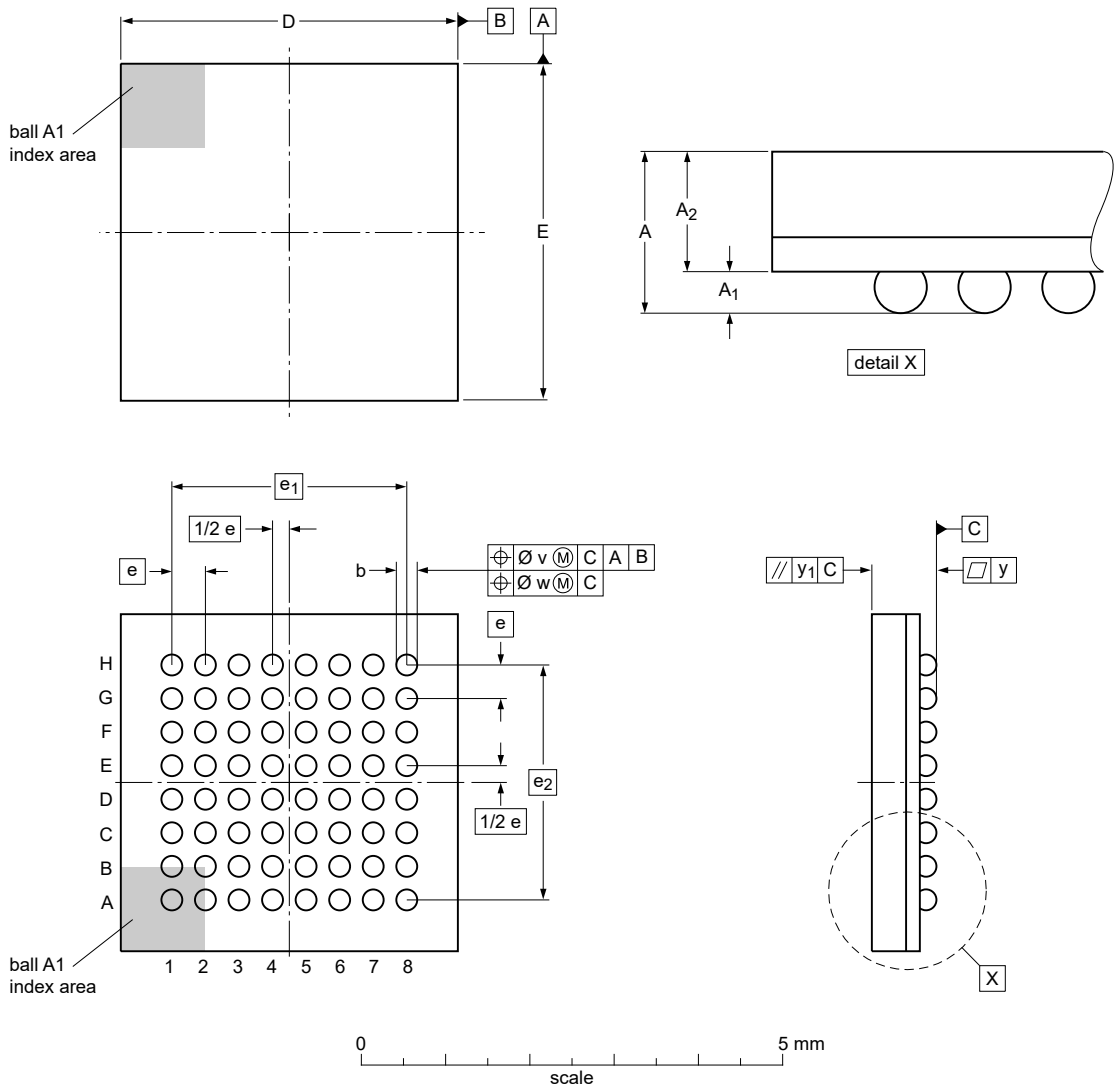
14.3.12 Pin characteristics for HIF3 (used as SPI-bus MISO)

Table 58. Pin characteristics for HIF3 (used as SPI-bus MISO)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} < 4 mA		$V_{DD(PAD)}$ - 0.4	-	$V_{DD(PAD)}$	V
V_{OL}	LOW-level output voltage	I_{OL} < 4 mA		0	-	0.4	V
C_L	load capacitance			-	-	20	pF
t_f	fall time	C_L = 12 pF max					
		high speed		1	-	3	ns
		slow speed		3	-	10	ns
t_r	rise time	C_L = 12 pF max					
		high speed		1	-	3	ns
		slow speed		3	-	10	ns

15 Package outline VFBGA64

VFBGA64: plastic very thin fine-pitch ball grid array package; 64 balls **SOT1860-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
	max	0.90	0.25	0.65	0.30	4.1	4.1							
mm	nom	0.80	0.20	0.60	0.25	4.0	4.0	0.4	2.8	2.8	0.15	0.05	0.08	0.1
	min	0.70	0.15	0.55	0.20	3.9	3.9							

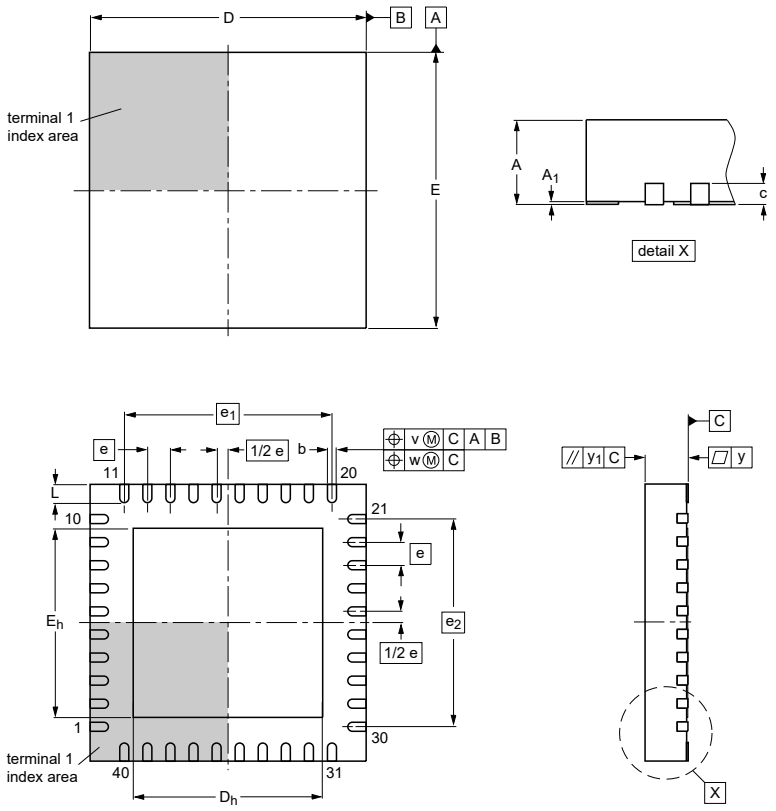
sot1860-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
sot1860-1		- - -				~~16-02-05~~ 16-03-31

Figure 36. Package outline

16 Package outline HVQFN40

HVQFN40: plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm **SOT618-1**



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
	max	1.00	0.05	0.30	0.2	6.1	4.25	6.1	4.25	0.5	4.5	4.5	0.5	0.1	0.05	0.05	0.1
mm	nom	0.85	0.02	0.21		6.0	4.10	6.0	4.10				0.4				
	min	0.80	0.00	0.18		5.9	3.95	5.9	3.95				0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot618-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT618-1		MO-220				~~02-10-22~~ 13-11-05

Figure 37. Package outline, HVQFN40, SOT618-1, MSL3

17 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 38) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 59 and Table 60

Table 59. SnPb eutectic process (from J-STD-020C)

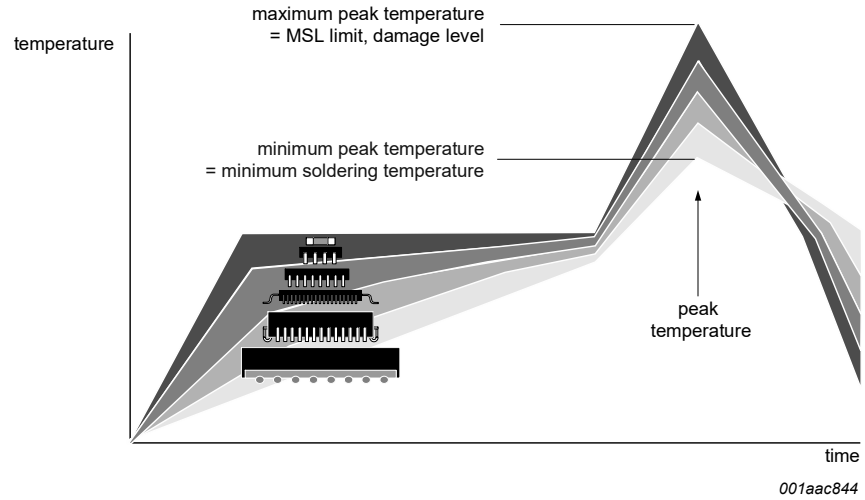
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 60. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2 000	> 2 000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 38.



MSL: Moisture Sensitivity Level

Figure 38. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

18 Abbreviations

Table 61. Abbreviations

Acronym	Description
ASK	Amplitude Shift keying
ASK modulation index	The ASK modulation index is defined as the voltage ratio (Vmax - Vmin)/ (Vmax + Vmin) × 100%
Automatic device discovery	Detect and recognize any NFC peer devices (NFC Initiator or NFC Target) like: NFC Initiator or NFC Target, ISO/IEC 14443-3, -4 Type A&B PICC, MIFARE Classic and MIFARE Ultralight PICC, ISO/IEC 15693 VICC
BPSK	Bit Phase Shift Keying
Card Emulation	The IC is capable of handling a PICC emulation on the RF interface including part of the protocol management. The application handling is done by the host controller
DEP	Data Exchange Protocol
DSLDO	Dual Supplied LDO
FW	FirmWare
HPD	Hard Power Down
LDO	Low Drop Out
LFO	Low Frequency Oscillator
MISO	Master In Slave Out (for SPI-bus interface)
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MOSI	Master Out Slave In (for SPI-bus interface)
MSL	Moisture Sensitivity Level
NCI	NFC Controller Interface
NFC	Near Field Communication
NFCC	NFC Controller, PN7160 in this data sheet
NFC Initiator	Initiator as defined in ISO/IEC 18092 or Ecma 340: NFCIP-1 communication
NFCIP	NFC Interface and Protocol
NFC Target	Target as defined in ISO/IEC 18092 or Ecma 340: NFCIP-1 communication
NRZ	Non Return to Zero
NSS	Not Slave Select (for SPI-bus interface)
P2P	Peer to Peer
PCD	Proximity Coupling Device. Definition for a Card reader/writer device according to the ISO/IEC 14443 specification or MIFARE
PCD -> PICC	Communication flow between a PCD and a PICC according to the ISO/IEC 14443 specification or MIFARE
PICC	Proximity Interface Coupling Card. Definition for a contactless Smart Card according to the ISO/IEC 14443 specification or MIFARE
PICC-> PCD	Communication flow between a PICC and a PCD according to the ISO/IEC 14443 specification or MIFARE
PMOS	P-channel MOSFET

Table 61. Abbreviations...*continued*

Acronym	Description
PMU	Power Management Unit
PSL	Parameter SeLection
SCK	Serial Clock (for SPI interface)
SPI-bus	Serial Peripheral Interface bus
TXLDO	Transmitter LDO
UM	User Manual
VCD	Vicinity Coupling Device. Definition for a reader/writer device according to the ISO/IEC 15693 specification
VCO	Voltage Controlled Oscillator
VICC	Vicinity Integrated Circuit Card
WUC	Wake-up Counter

19 References

[1] NFC Forum Device Requirements V2.0
[2] NFC Controller Interface (NCI) Technical Specification V2.0
[3] I^2C Specification I^2C Specification, UM10204 rev4 (13/02/2012)
[4] SPI Motorola de-facto standard described in Motorola 68HC11 data sheet
[5] UM11490 PN7160 User Manual
[6] AN12988 PN7160 hardware design guide
[7] AN13219 PN7160 antenna design and matching guide
[8] ISO/IEC 18092 (NFCIP-1) edition, 15/03/2013. This is similar to Ecma 340.
[9] ISO/IEC15693 part 2: 2nd edition (15/12/2006), part 3: 1st edition (01/04/2001)
[10] ISO/IEC 21481 (NFCIP-2) edition, 01/07/2012. This is similar to Ecma 352.
[11] ETSI HCI TS 102 622; UICC - Contactless Front-end (CLF) Interface; Host Controller Interface (HCI) (Release 12)
[12] Apple Enhanced Contactless Polling Specification: Version 1.1.

20 Revision history

Table 62. Revision history

Document ID	Release date	Data sheet status	Supersedes
PN7160_PN7161 v.3.2	20210930	Product data sheet	PN7160_PN7161 v.3.1
Modifications:	• Clarified pin naming TVDD vs $V_{DD(TX)}$		
PN7160_PN7161 v.3.1	20210913	Product data sheet	PN7160_PN7161 v.3.0
Modifications:	• Security status changed into "Company public"		
PN7160_PN7161 v.3.0	20210819	Product data sheet	PN7160_PN7161 v.2.0
Modifications:	• Data sheet status changed into "Product data sheet" • Security status changed into "Company restricted"		
PN7160_PN7161 v.2.0	20210709	Preliminary data sheet	PN7160 v.1.0
Modifications:	• PN7161 included • Section 13: updated • Some figures updated		
PN7160 v.1.0	20210308	Objective data sheet	-
	• Initial version		

21 Legal information

21.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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