Notification about the transfer of the semiconductor business

The semiconductor business of Panasonic Corporation was transferred on September 1, 2020 to Nuvoton Technology Corporation (hereinafter referred to as "Nuvoton"). Accordingly, Panasonic Semiconductor Solutions Co., Ltd. became under the umbrella of the Nuvoton Group, with the new name of Nuvoton Technology Corporation Japan (hereinafter referred to as "NTCJ").

In accordance with this transfer, semiconductor products will be handled as NTCJ-made products after September 1, 2020. However, such products will be continuously sold through Panasonic Corporation.

Publisher of this Document is NTCJ.

If you would find description "Panasonic" or "Panasonic semiconductor solutions", please replace it with NTCJ.

Except below description page
 "Request for your special attention and precautions in using the technical information and semiconductors described in this book"

Nuvoton Technology Corporation Japan

Panasonic FG6543010R

FG6543010R

Silicon N-channel MOSFET(FET1)

Silicon P-channel MOSFET(FET2)

For switching

■ Features

- Low drive voltage: 2.5 V drive
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL:Level 1 compliant)
- Marking Symbol:V7
- Basic Part Number

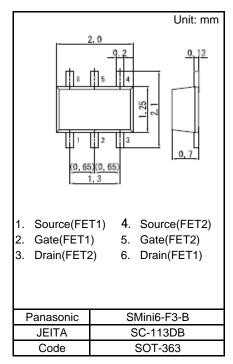
FJ330301 + FK330301 (Individual)

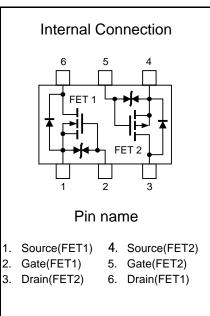
■ Packaging

FG6543010R Embossed type (Thermo-compression sealing): 3 000 pcs / reel (standard)

■ Absolute Maximum Ratings Ta = 25 °C

	Parameter	Symbol	Rating	Unit
FET1 (Nch.)	Drain-source Voltage	VDS	30	V
	Gate-source Voltage	VGS	± 12	V
	Drain Current	ID	100	mA
	Drain Current (Pulsed)	IDp	200	mA
FET2 (Pch.)	Drain-source Voltage	VDS	- 30	V
	Gate-source Voltage	VGS	± 12	V
	Drain Current	ID	- 100	mA
	Drain Current (Pulsed)	IDp	- 200	mA
Overall	Total Power Dissipation	PD	150	mW
	Channel Temperature	Tch	150	°C
	Storage Temperature	Tstg	- 55 to + 150	°C





Panasonic FG6543010R

■ Electrical Characteristics Ta = 25 $^{\circ}$ C \pm 3 $^{\circ}$ C FET1(Nch.)

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Drain-source Breakdown Voltage	VDSS	ID = 1 mA, VGS = 0 V	30			V
Zero Gate Voltage Drain Current	IDSS	VDS = 30 V, VGS = 0 V			1.0	μΑ
Gate-source Leakage Current	IGSS	VGS = ±10 V, VDS = 0 V			± 10	μΑ
Gate-source Threshold Voltage	Vth	ID = 1.0 μA, VDS = 3.0 V	0.5	1.0	1.5	V
Drain-source On-state Resistance	RDS(on)1	ID = 10 mA, VGS = 2.5 V		3	6	Ω
Dialii-Source Oil-State Resistance	RDS(on)2	ID = 10 mA, VGS = 4.0 V		2	3	
Forward transfer admittance	Yfs	ID = 10 mA, VDS = 3.0 V	20	55		mS
Input Capacitance	Ciss			12		
Output Capacitance	Coss	VDS = 3 V, $VGS = 0 V$, $f = 1 MHz$		7		pF
Reverse Transfer Capacitance	Crss			3		
Turn-on Time *1	ton	VDD = 3 V, VGS = 0 V to 3 V		100		ns
rum-on rime	ton	ID = 10 mA				
Turn-off Tme *1	toff	VDD = 3 V, VGS = 3 V to 0 V		100	nc.	nc
rum-on rme	ton	ID = 10 mA	100			ns

Note: Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

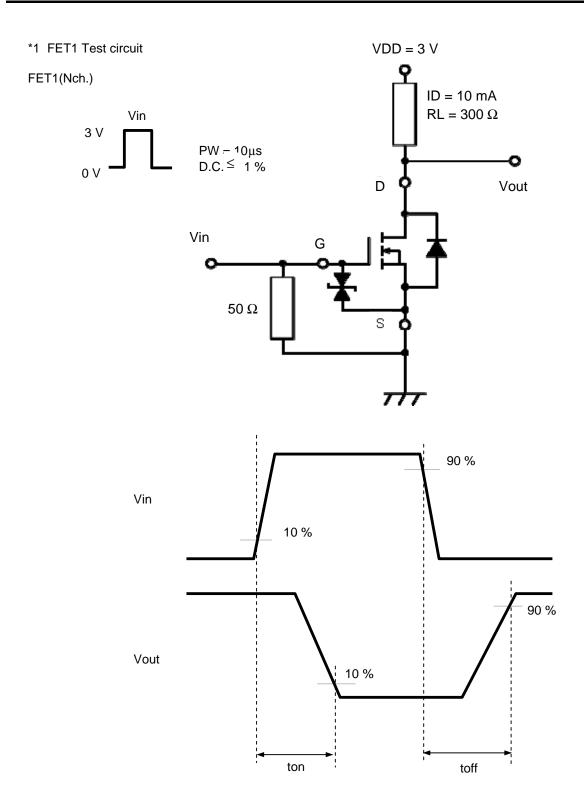
■ Electrical Characteristics $Ta = 25 \, ^{\circ}C \pm 3 \, ^{\circ}C$ FET2(Pch.)

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Drain-source Breakdown Voltage	VDSS	ID = -1 mA, VGS = 0 V	-30			V
Zero Gate Voltage Drain Current	IDSS	VDS = -30 V, VGS = 0 V			-1.0	μΑ
Gate-source Leakage Current	IGSS	VGS = ±10 V, VDS = 0 V			±10	μΑ
Gate-source Threshold Voltage	Vth	ID = -1.0 μA, VDS = -3.0 V	-0.5	-1.0	-1.5	V
Drain-source On-state Resistance	RDS(on)	ID = -10 mA, VGS = -2.5 V		7	17	Ω
Diain-source On-state Resistance	KD3(0II)	ID = -10 mA, VGS = -4.0 V		4	7	22
Forward transfer admittance	Yfs	ID = -10 mA, VDS = -3.0 V	20	40		mS
Input Capacitance	Ciss			12		
Output Capacitance	Coss	VDS = -3 V, $VGS = 0 V$, $f = 1 MHz$		7		pF
Reverse Transfer Capacitance	Crss			3		
Turn-on Time *2	ton	VDD = -3 V, VGS = 0 V to -3 V,		100		ns
rum-on rime		ID = -10 mA		100		
Turn-off Tme *2	toff	VDD = -3 V, VGS = -3 V to 0 V,		100		ns
rum-on mie	ton	ID = -10 mA	100			113

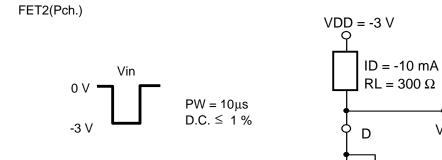
Note: Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

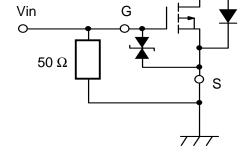
^{*1} See FET1 Test circuit.

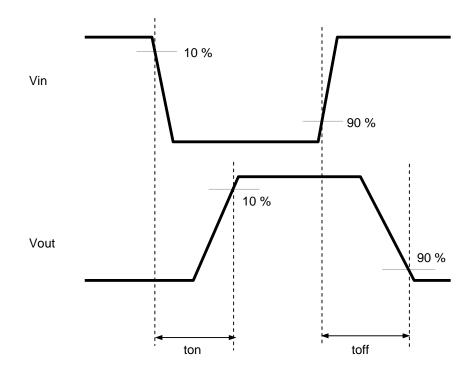
^{*2} See FET2 Test circuit.



*2 FET2 Test circuit





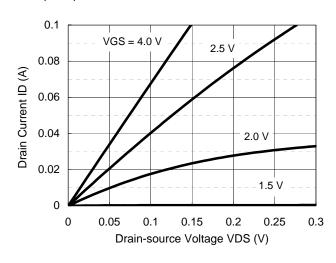


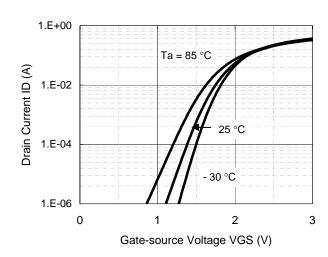
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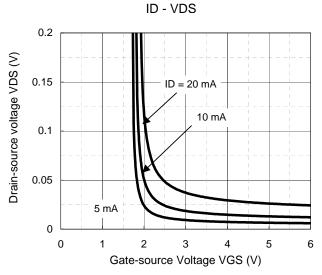
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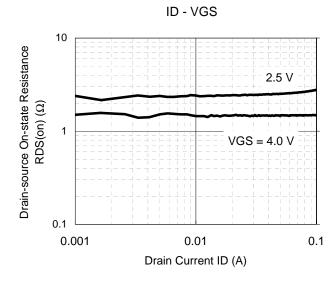
Vout

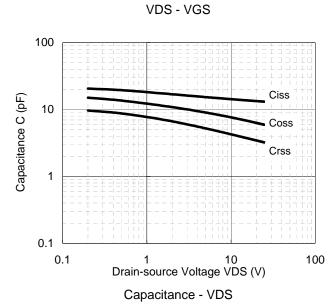
FET1(Nch.)





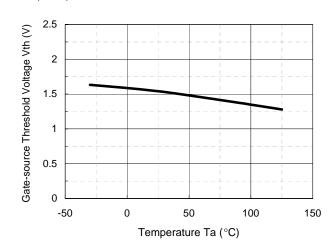


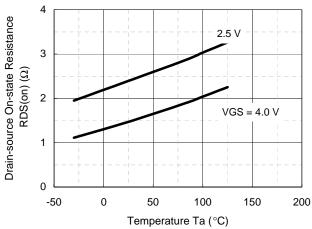


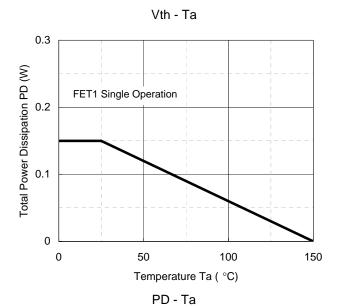


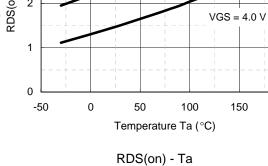
RDS(on) - ID

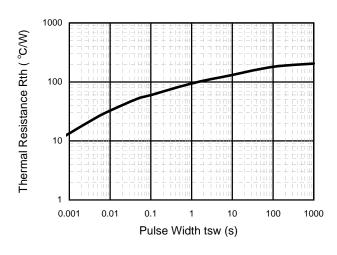
FET1(Nch.)



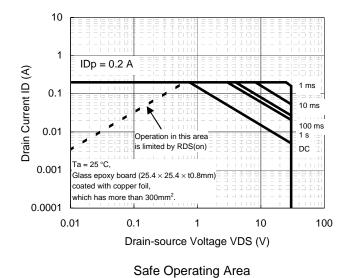








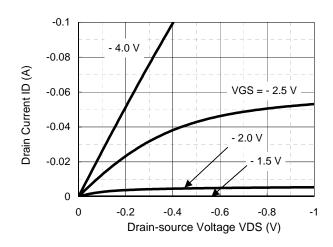
Rth -tsw

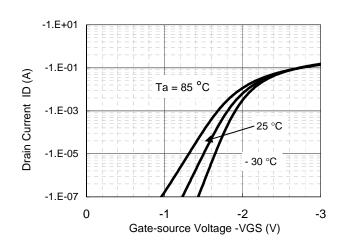


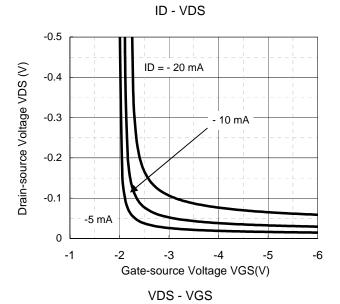
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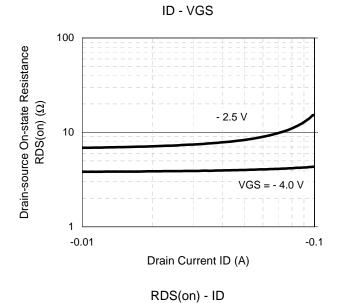
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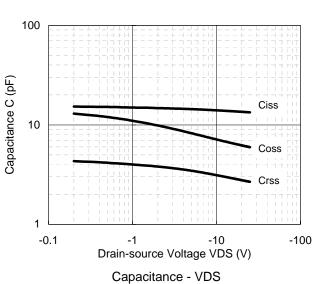
FET2(Pch.)



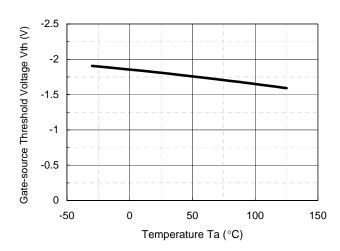


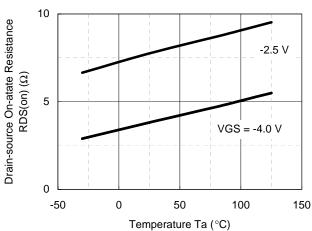


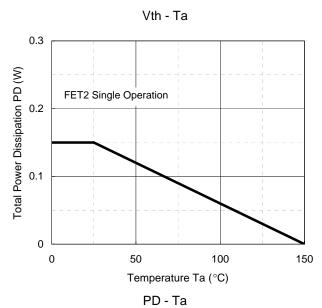


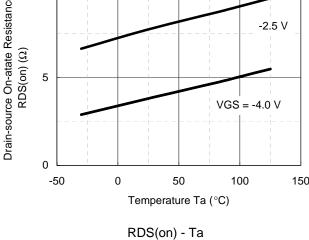


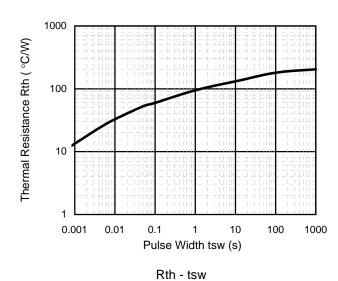
FET2(Pch.)

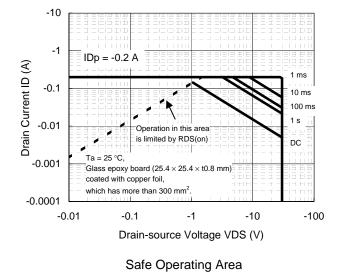






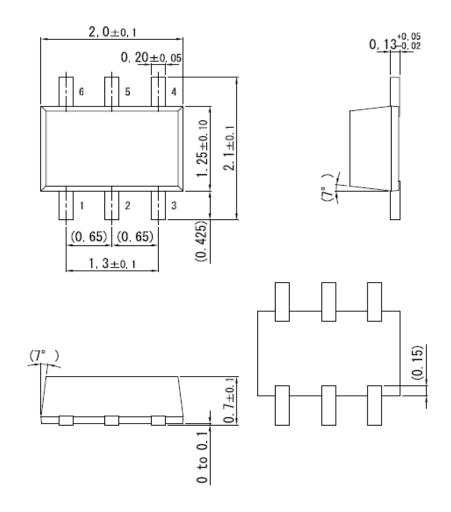




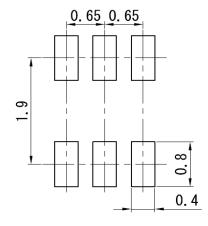


SMini6-F3-B





■ Land Pattern (Reference) (Unit: mm)



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