

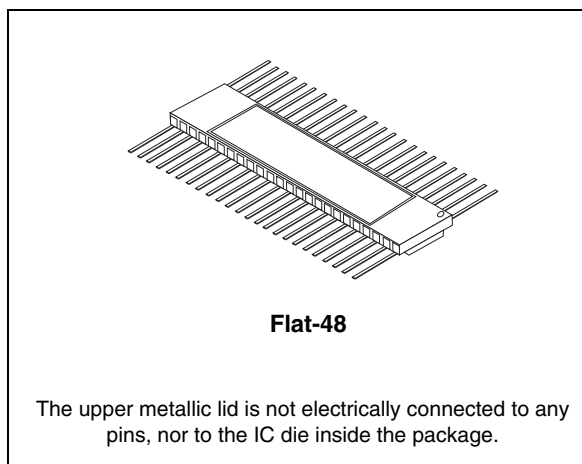


## 54VCXH162374

Rad hard low voltage CMOS 16-bit d-type flip-flop (3-state)  
with 3.6 V tolerant inputs and outputs

### Features

- 1.65 to 3.6 V inputs and outputs
- High speed:
  - $t_{PD} = 3.4$  ns (Max.) at  $V_{CC} = 3.0$  to 3.6 V
  - $t_{PD} = 4.8$  ns (Max.) at  $V_{CC} = 2.3$  to 2.7 V
- Symmetrical impedance outputs:
  - $|I_{OH}| = I_{OL} = 12$  mA (Min.) at  $V_{CC} = 3.0$  V
  - $|I_{OH}| = I_{OL} = 8$  mA (Min.) at  $V_{CC} = 2.3$  V
- Power down protection on inputs and outputs
- 26  $\Omega$  serie resistors in outputs
- Operating voltage range:
  - $V_{CC(Opr)} = 1.65$  V to 3.6 V
- Pin and function compatible with 54 series H162374
- Bus hold provided on both sides
- Cold spare function
- Latch-up performance exceeds 300 mA (JESD 17)
- ESD performance:
  - HBM > 2000 V (MIL STD 883 method 3015); MM > 200 V
- 300 KRad Mil1019.6 condition A, (RHA QML qualification extension undergone)
- No SEL, no SEU and no SET under 110 Mev/cm<sup>2</sup>/mg LET heavy ions irradiation
- QML qualified product
- Device fully compliant with DSCC SMD 5962-05212
- 100 mV typical input hysteresis



### Description

The 54VCXH162374 is a low voltage CMOS 16 bit d-type flip-flop with 3 state outputs non inverting fabricated with sub-micron silicon gate and five-layer metal wiring C<sup>2</sup>MOS technology. It is ideal for low power and very high speed 1.65 to 3.6 V applications; it can be interfaced to 3.6 V signal environment for both inputs and outputs. These 16 bit d-type flip-flops are controlled by two clock inputs (nCK) and two output enable inputs (nOE). On the positive transition of the (nCK), the nQ outputs will be set to the logic state that were setup at the nD inputs. While the (nOE) input is low, the 8 outputs (nQ) will be in a normal state (HIGH or LOW logic level) and while high level the outputs will be in a high impedance state. Any output control does not affect the internal operation of flip flops; that is, the old data can be retained or the new data can be entered even while the outputs are OFF.

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# 1 Logic symbols and I/O equivalent circuit

Figure 1. IEC logic symbols

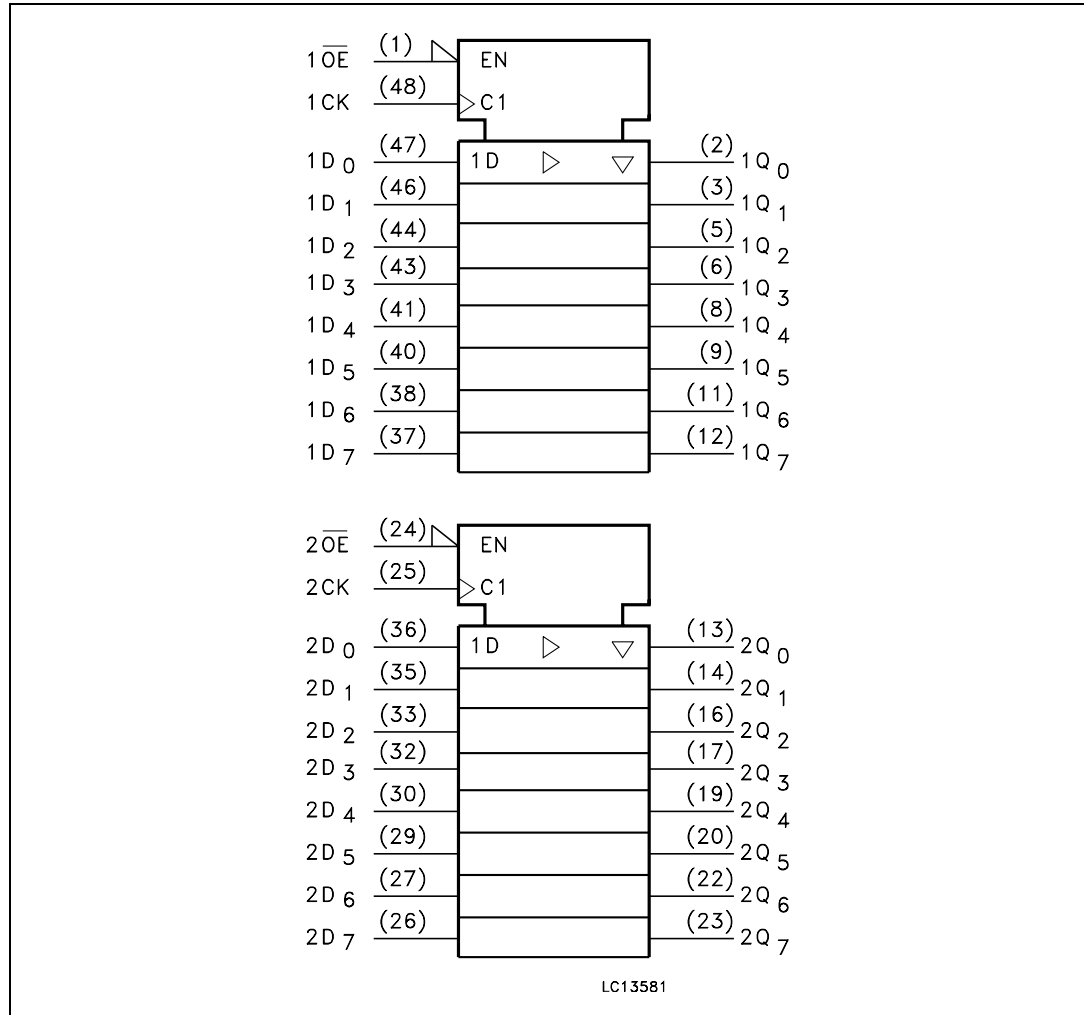
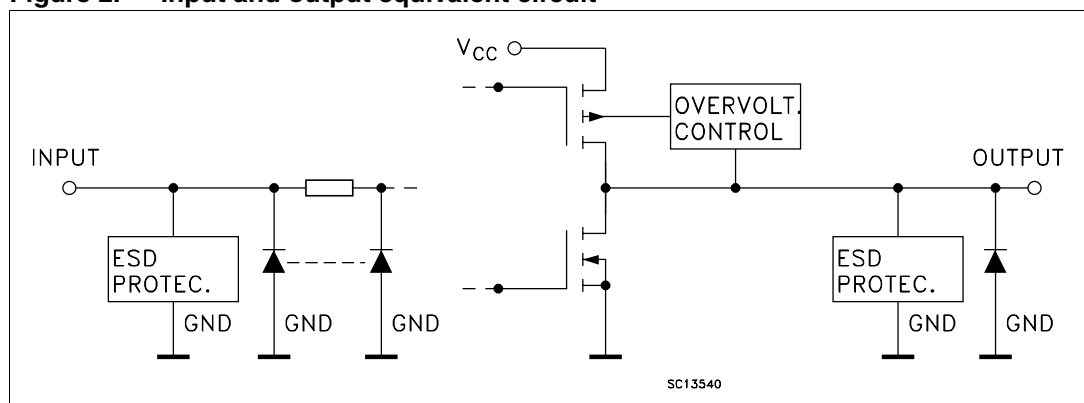


Figure 2. Input and output equivalent circuit

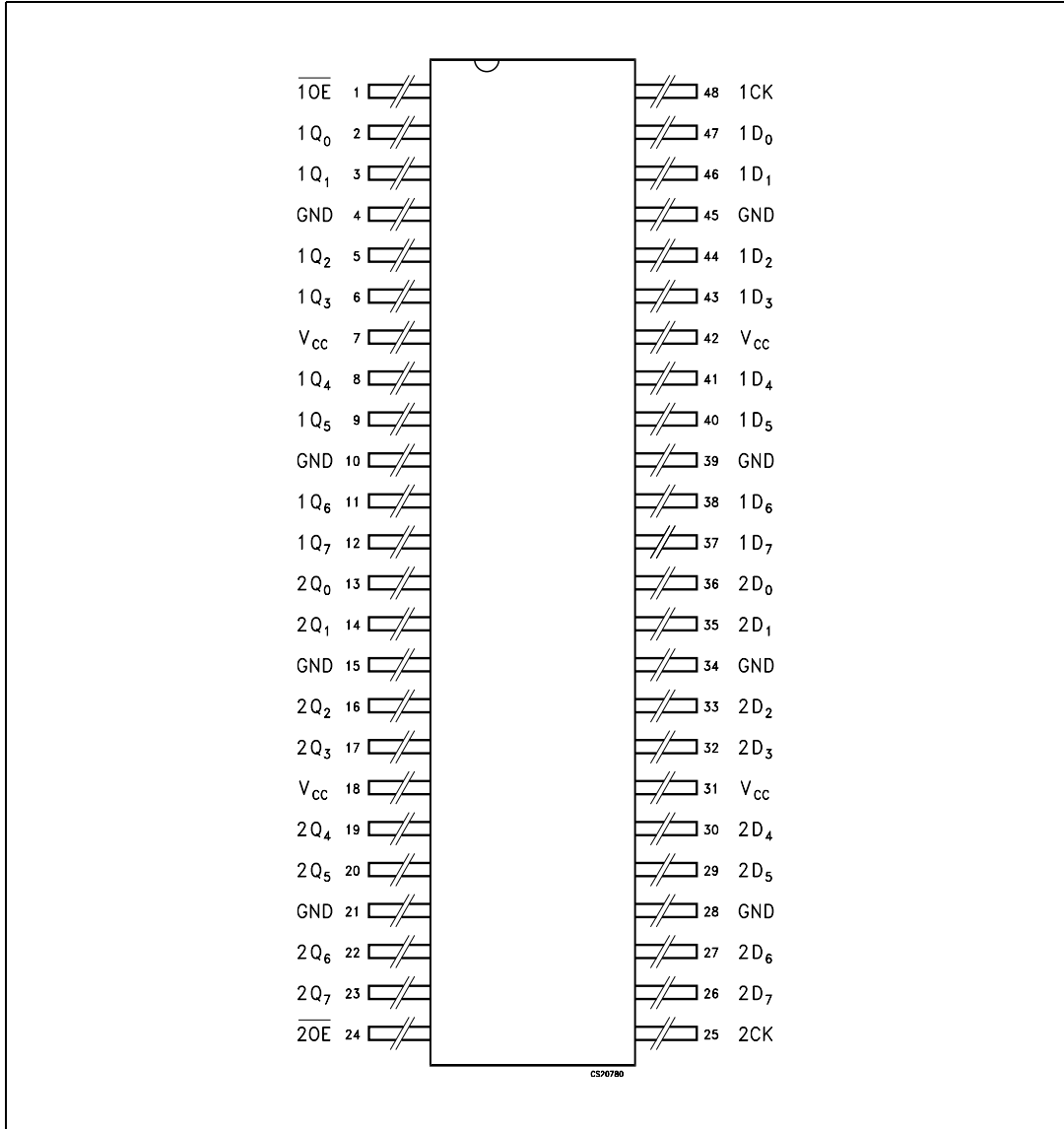




## 2 Pin settings

### 2.1 Pin connection

Figure 4. Pin connection (top through view)



## 2.2 Pin description

Table 1. Pin description

Pin n°	Symbol	Name and function
1	$1\overline{OE}$	3 state output enable input (Active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Q0 to 1Q7	3-state outputs
13, 14, 16, 17, 19, 20, 22, 23	2Q0 to 2Q7	3-state outputs
24	$2\overline{OE}$	3 state output enable input (Active LOW)
25	2CK	Clock input
36, 35, 33, 32, 30, 29, 27, 26	2D0 to 2D7	Data inputs
47, 46, 44, 43, 41, 40, 38, 37	1D0 to 1D7	Data inputs
48	1CK	Clock input
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0 V)
7, 18, 31, 42	V <sub>CC</sub>	Positive supply voltage

## 2.3 Truth table

Table 2. Truth table

Inputs			Output
OE	LE	D	Q
H	X	X	Z
L	$\overline{\text{L}}$	X	No change <sup>(1)</sup>
L	$\text{L}$	L	L
L	$\text{L}$	H	H

1. Q outputs are latched at the time when the LE input is taken low logic level.

Note: X = Do not care; Z = High impedance

### 3 Maximum rating

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage	-0.5 to +4.6	V
$V_I$	DC input voltage	-0.5 to +4.6	V
$V_O$	DC output voltage (OFF state)	-0.5 to +4.6	V
$V_O$	DC output voltage (high or low state) <sup>(1)</sup>	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC input diode current	- 50	mA
$I_{OK}$	DC output diode current <sup>(2)</sup>	- 50	mA
$I_O$	DC output current	$\pm 50$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or ground current per supply pin	$\pm 100$	mA
$P_D$	Power dissipation	400	mW
$T_{stg}$	Storage temperature	-65 to +150	°C
$T_L$	Lead temperature (10 sec)	260	°C

1.  $I_O$  absolute maximum rating must be observed

2.  $V_O < GND$ ,  $V_O > V_{CC}$

### 3.1 Recommended operating conditions

**Table 4. Recommended operating conditions**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage	1.8 to 3.6	V
$V_I$	Input voltage	-0.3 to 3.6	V
$V_O$	Output voltage (OFF state)	0 to 3.6	V
$V_O$	Output voltage (high or low state)	0 to $V_{CC}$	V
$I_{OH}$ , $I_{OL}$	High or low level output current ( $V_{CC} = 3.0$ to $3.6$ V)	$\pm 12$	mA
$I_{OH}$ , $I_{OL}$	High or low level output current ( $V_{CC} = 2.3$ to $2.7$ V)	$\pm 8$	mA
$T_{op}$	Operating temperature	-55 to 125	°C
dt/dv	Input rise and fall time <sup>(1)</sup>	0 to 10	ns/V

1.  $V_{IN}$  from 0.8 V to 2 V at  $V_{CC} = 3.0$  V

## 4 Electrical characteristics

2.7 V < V<sub>CC</sub> < 3.6 V unless otherwise specified

**Table 5. DC specifications**

Symbol	Parameter	Test condition		Value		Unit
		V <sub>CC</sub> (V)		-55 to 125°C		
				Min.	Max.	
V <sub>IH</sub>	High level input voltage	2.7 to 3.6		2.0		V
V <sub>IL</sub>	Low level input voltage				0.8	
V <sub>OH</sub>	High level output voltage	2.7 to 3.6	I <sub>O</sub> =-100 μA	V <sub>CC</sub> -0.2		V
		2.7	I <sub>O</sub> =-6 mA	2.2		
		3.0	I <sub>O</sub> =-8 mA	2.4		
			I <sub>O</sub> =-12 mA	2.2		
V <sub>OL</sub>	Low level output voltage	2.7 to 3.6	I <sub>O</sub> =100 μA		0.2	V
		2.7	I <sub>O</sub> =6 mA		0.4	
		3.0	I <sub>O</sub> =8 mA		0.55	
			I <sub>O</sub> =12 mA		0.8	
I <sub>I</sub>	Input leakage current	2.7 to 3.6	V <sub>I</sub> = 0 to 3.6 V		± 5	μA
I <sub>I(HOLD)</sub>	Input hold current	3.0	V <sub>I</sub> = 0.8 V	75		μA
			V <sub>I</sub> = 2 V	-75		
		3.6	V <sub>I</sub> = 0 to 3.6 V		± 500	
I <sub>off</sub>	Power off leakage current	0	V <sub>I</sub> or V <sub>O</sub> = 0 to 3.6 V		10	μA
I <sub>OZ</sub>	High impedance output leakage current	2.7 to 3.6	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = 0 to 3.6 V		± 10	μA
I <sub>CC</sub>	Quiescent supply current	2.7 to 3.6	V <sub>I</sub> = V <sub>CC</sub> or GND		20	μA
			V <sub>I</sub> or V <sub>O</sub> = V <sub>CC</sub> to 3.6 V		± 20	
ΔI <sub>CC</sub>	I <sub>CC</sub> incr. per Input	2.7 to 3.6	V <sub>IH</sub> = V <sub>CC</sub> - 0.6 V		750	μA



2.3 V <  $V_{CC}$  < 2.7 V unless otherwise specified

**Table 6. DC specifications**

Symbol	Parameter	Test condition		Value			Unit
		$V_{CC}$ (V)		-55 to 125°C			
				Min.	Max.		
$V_{IH}$	High level input voltage	2.3 to 2.7		1.6		V	
$V_{IL}$	Low level input voltage				0.7		
$V_{OH}$	High level output voltage	2.3 to 2.7	$I_O = -100 \mu A$	$V_{CC} - 0.2$		V	
		2.3	$I_O = -4 \text{ mA}$	2.0			
			$I_O = -6 \text{ mA}$	1.8			
			$I_O = -8 \text{ mA}$	1.7			
$V_{OL}$	Low level output voltage	2.3 to 2.7	$I_O = 100 \mu A$		0.2	V	
		2.3	$I_O = 6 \text{ mA}$		0.4		
			$I_O = 8 \text{ mA}$		0.6		
$I_I$	Input leakage current	2.3 to 2.7	$V_I = V_{CC}$ or GND		$\pm 5$	$\mu A$	
$I_{I(HOLD)}$	Input hold current	2.3	$V_I = 0.7 \text{ V}$	45		$\mu A$	
			$V_I = 1.7 \text{ V}$	-45			
$I_{off}$	Power Off leakage current	0	$V_I$ or $V_O = 0$ to 3.6 V		10	$\mu A$	
$I_{OZ}$	High impedance output leakage current	2.3 to 2.7	$V_I = V_{IH}$ or $V_{IL}$ $V_O = 0$ to 3.6 V		$\pm 10$	$\mu A$	
$I_{CC}$	Quixent	2.3 to 2.7	$V_I = V_{CC}$ or GND		20	$\mu A$	
			$V_I$ or $V_O = V_{CC}$ to 3.6 V		$\pm 20$		

$T_A = 25 \text{ }^\circ\text{C}$ , Input  $t_r = t_f = 2.0 \text{ ns}$ ,  $C_L = 30 \text{ pF}$ ,  $R_L = 500 \text{ } \Omega$

**Table 7. Dynamic switching characteristics**

Symbol	Parameter	Test condition		Value			Unit
		$V_{CC}$ (V)		$T_A = 25 \text{ }^\circ\text{C}$			
				Min.	Typ.	Max.	
$V_{OLV}$	Dynamic valley low voltage quiet output <sup>(1)</sup> <sup>(2)</sup>	2.5	$V_{IL} = 0 \text{ V}$ $V_{IH} = V_{CC}$	-	0.25	-	V
		3.3		-	0.35	-	
$V_{OHV}$	Dynamic valley high voltage quiet output <sup>(2)</sup> <sup>(3)</sup>	2.5	$V_{IL} = 0 \text{ V}$ $V_{IH} = V_{CC}$	-	-0.25	-	V
		3.3		-	-0.35	-	
$V_{OHV}$	Dynamic valley high voltage quiet output <sup>(2)</sup> <sup>(3)</sup>	2.5	$V_{IL} = 0 \text{ V}$ $V_{IH} = V_{CC}$	-	2.05	-	V
		3.3		-	2.65	-	

- Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the LOW state.
- Parameters guaranteed by design.
- Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the HIGH state.

$C_L = 30 \text{ pF}$ ,  $R_L = 500 \text{ } \Omega$ , Input  $t_r = t_f = 2.0 \text{ ns}$

**Table 8. AC electrical characteristics**

Symbol	Parameter	Test condition		Value		Unit
		$V_{CC}$ (V)		-55 to 125 °C		
				Min.	Max.	
$t_{PLH}$ $t_{PHL}$	Propagation delay time Dn to Qn	2.3 to 2.7		1.0	5.5	ns
		3.0 to 3.6		0.8	4.5	
$t_{PLH}$ $t_{PHL}$	Propagation delay time LE to Qn	2.3 to 2.7		1.0	6.2	ns
		3.0 to 3.6		0.8	4.5	
$t_{PZL}$ $t_{PZH}$	Output enable time	2.3 to 2.7		1.0	5.1	ns
		3.0 to 3.6		0.8	4.6	
$t_{PLZ}$ $t_{PHZ}$	Output disable time	2.3 to 2.7		1.0		ns
		3.0 to 3.6		1.0		
$t_s$	Setup time, HIGH or LOW level Dn to LE	2.3 to 2.7		1.5		ns
		3.0 to 3.6		1.5		
$t_h$	Hold time High or LOW level Dn to LE	2.3 to 2.7		1.5		ns
		3.0 to 3.6		1.5		
$t_w$	LE pulse width, HIGH	2.3 to 2.7		190		ns
		3.0 to 3.6		235		
$t_{OSLH}$ $t_{OSHL}$	Output to output skew time <sup>(1)</sup> <sup>(2)</sup>	2.3 to 2.7			0.5	ns
		3.0 to 3.6			0.5	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ( $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$ ,  $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$ )

2. Parameter guaranteed by design

**Table 9. Capacitive characteristics**

Symbol	Parameter	Test condition		Value			Unit
		$V_{CC}$ (V)		$T_A = 25 \text{ } ^\circ\text{C}$			
				Min.	Typ.	Max.	
$C_{IN}$	Input capacitance	2.5 or 3.3	$V_{IN} = 0$ or $V_{CC}$	-	6	-	pF
$C_{OUT}$	Output capacitance	2.5 or 3.3	$V_{IN} = 0$ or $V_{CC}$	-	7	-	pF
$C_{PD}$	Power dissipation capacitance <sup>(1)</sup>	2.5 or 3.3	$f_{IN} = 10\text{MHz}$ $V_{IN} = 0$ or $V_{CC}$	-	20	-	pF

1.  $C_{PD}$  is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/16$  (per circuit)

## 5 Test circuit

Figure 5. Test circuit

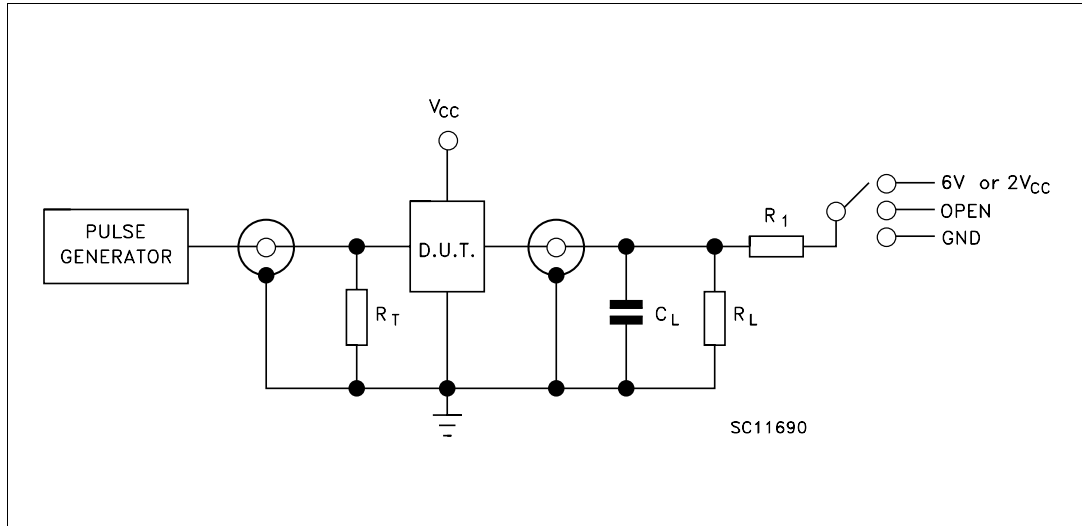


Table 10. Test circuit

Test	Switch
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$ ( $V_{CC} = 3.0$ to $3.6$ V)	6 V
$t_{PZL}$ , $t_{PLZ}$ ( $V_{CC} = 2.3$ to $2.7$ V)	$2 V_{CC}$
$t_{PZH}$ , $t_{PHZ}$	GND

$C_L = 30$  pF or equivalent (includes jig and probe capacitance)

$R_L = R_1 = 500 \Omega$  or equivalent

$R_T = Z_{OUT}$  of pulse generator (typically  $50 \Omega$ )

# 6 Waveforms

**Table 11. Waveform symbol value**

Symbol	V <sub>CC</sub>	
	3.0 to 3.6 V	2.3 to 2.7 V
V <sub>IH</sub>	2.7 V	V <sub>CC</sub>
V <sub>M</sub>	1.5 V	V <sub>CC</sub> /2
V <sub>X</sub>	V <sub>OL</sub> + 0.3 V	V <sub>OL</sub> + 0.15 V
V <sub>Y</sub>	V <sub>OH</sub> - 0.3 V	V <sub>OH</sub> - 0.15 V

**Figure 6. Waveform - nCK TO Qn propagation delays, nCK maximum frequency, Dn TO nCK setup and hold times (f = 1 MHz; 50% duty cycle)**

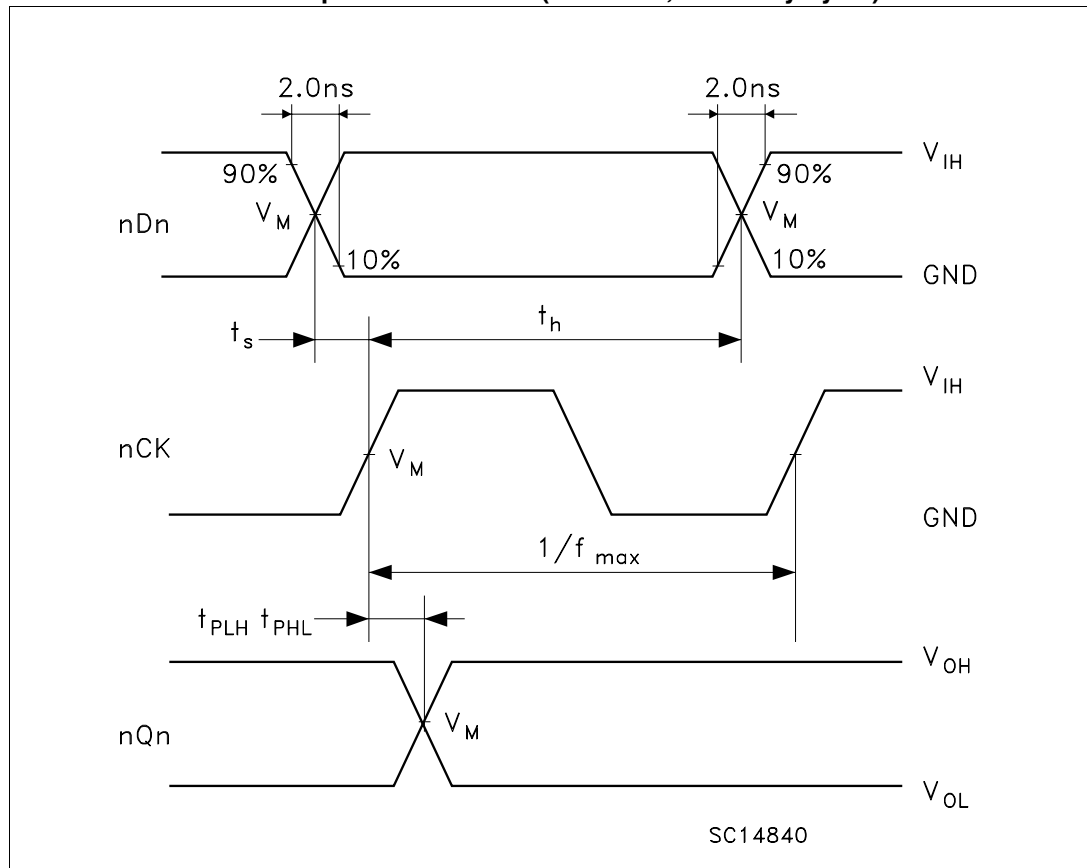


Figure 7. Waveform - output enable and disable time (f = 1 MHz; 50% duty cycle)

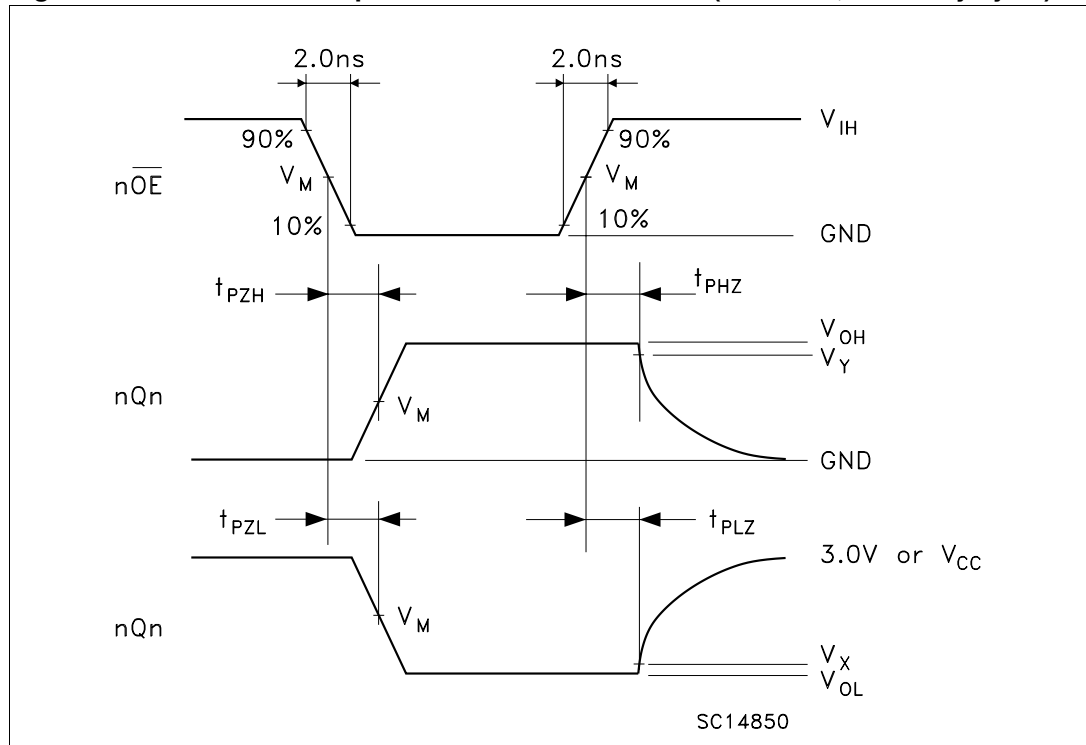
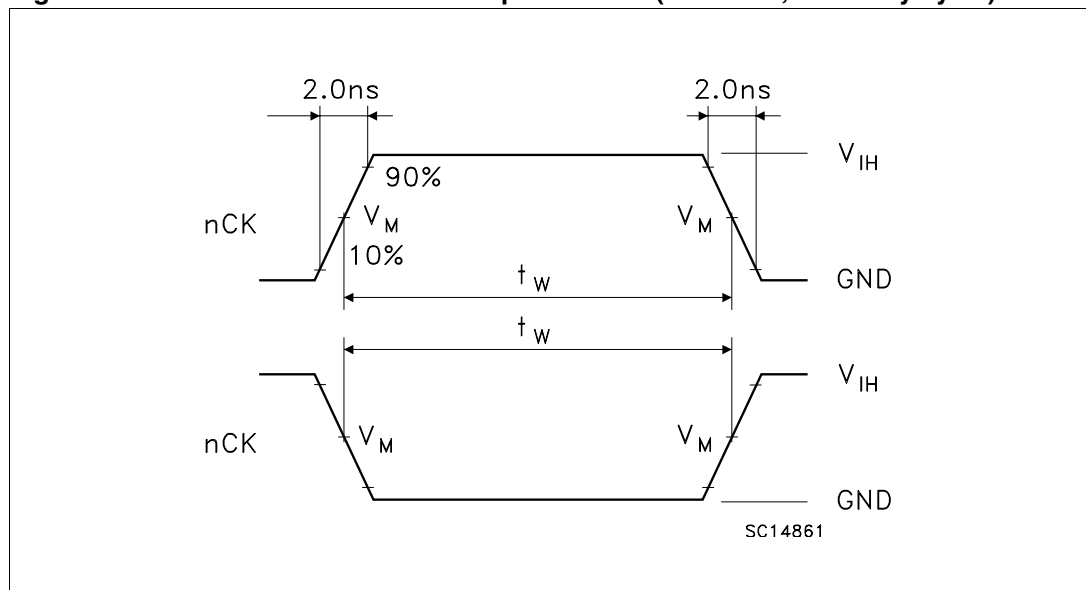


Figure 8. Waveform - nCK minimum pulse width (f = 1 MHz; 50% duty cycle)



## 7 Package mechanical data

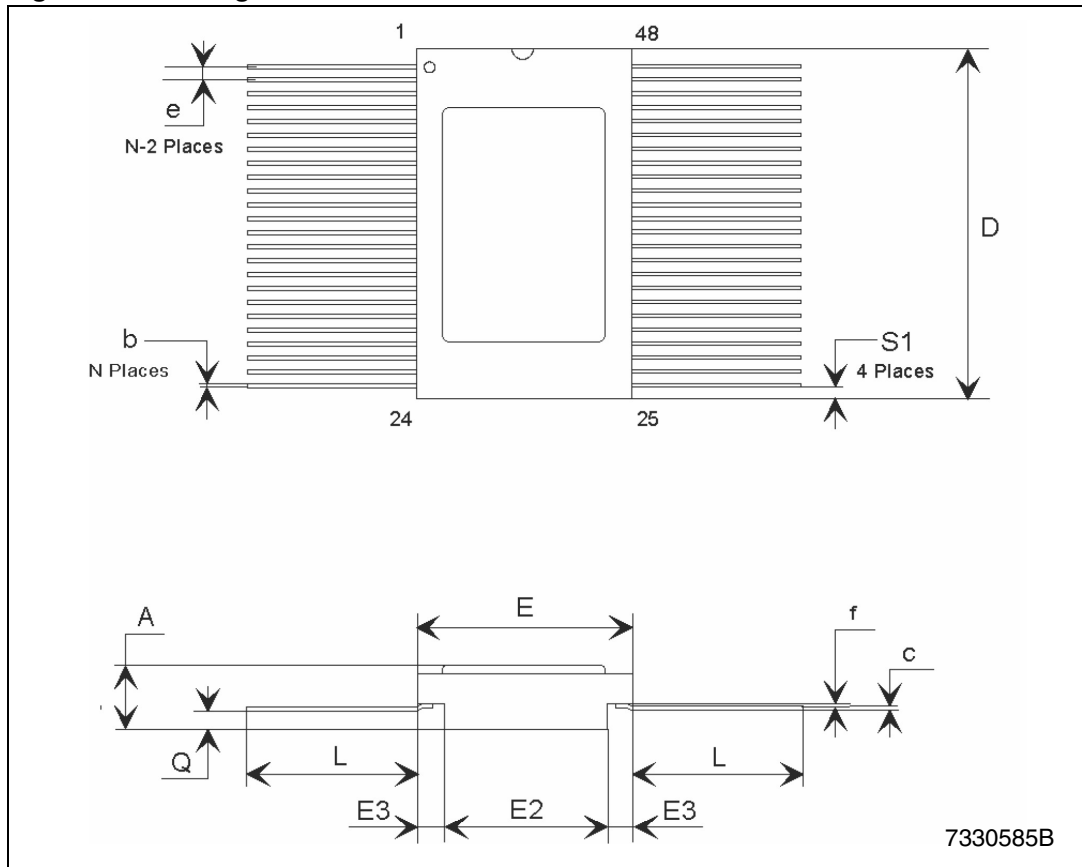
54VCXH162374 products are supplied into ceramic body / metal lid hermetic Flat 48-pin space package.

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

**Table 12. Flat-48 (MIL-STD-1835) mechanical data**

Dim.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.18	2.47	2.72	0.086	0.097	0.107
b	0.20	0.254	0.30	0.008	0.010	0.012
c	0.12	0.15	0.18	0.005	0.006	0.007
D	15.57	15.75	15.92	0.613	0.620	0.627
E	9.52	9.65	9.78	0.375	0.380	0.385
E2	6.22	6.35	6.48	0.245	0.250	0.255
E3	1.52	1.65	1.78	0.060	0.065	0.070
e		0.635			0.025	
f		0.20			0.008	
L	6.85	8.38	9.40	0.270	0.330	0.370
Q	0.66	0.79	0.92	0.026	0.031	0.036
S1	0.25	0.43	0.61	0.010	0.017	0.024

Figure 9. Package dimension



**Note:** The upper metallic lid is not electrically connected to any pins, nor to the IC die inside the package. Connecting unused pins or metal lid to ground or to the power supply will not affect the electrical characteristics.

## 8 Order codes

**Table 13. Ordering information**

Package	Min op. voltage	Lead finish	Radiation level	Flight models	Engineering model	Packing
				QML-V		
48-pin flat	1.8 V	Gold plated	300 krad	RHFXH162374K03V	RHRXH162374K1	Conductive strip pack



## 9 Revision history

**Table 14. Document revision history**

Date	Revision	Changes
09-Jul-2004	1	First release.
17-May-2005	2	SMD qualified.
19-Jun-2006	3	300 Krad bullet updated, new template, mechanical data updated
25-Jul-2007	4	Typo in <a href="#">Table 12 on page 14</a> .
17-Sep-2008	5	Updated cover page
23-Sep-2009	6	Updated <a href="#">Table 13 on page 16</a>
02-Aug-2011	7	Added <a href="#">Note: on page 15</a> and in the "Pin connections" diagram on the coverpage

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