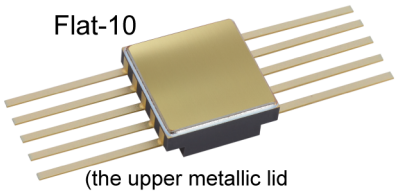
# RHRDAC121

Datasheet

## Rad-hard, 12-bit D/A converter




(the upper metallic lid
is electrically connected to pin 5)

## Features

- 12-bit architecture
- Ensured monotonicity
- Rail-to-rail voltage output
- Power-on-reset to zero volt output
- Internal voltage reference
- SYNC interrupt facility
- 2.3 V to 3.6 V power supply range
- Power-down function
- Guaranteed over -55 °C to +125 °C ambient temperature
- Hermetic package
- 100 krad(Si) TID
- SEL-free up to 120 MeV.cm²/mg
- SMD: on-going
- Mass: 0.42 g

## Application

- Satellite equipment
- Telemetry
- Housekeeping

| Product status link |
| --- |
| RHRDAC121 |

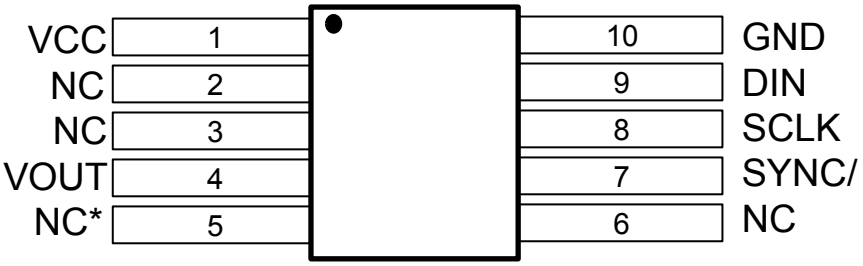
## Description

The RHRDAC121 is a 12-bit voltage-output digital-to-analog converter that can operate from 2.3 V to 3.6 V power supply drawing a very low current consumption, with an internal voltage referencing. The output features rail-to-rail swing and the three-wire serial interface operates at clock rates up to 20 MHz compatible with standard SPI.

The RHRDAC121 comes in a hermetic ceramic Flat10-lead, and it can operate from -55 °C to +125 °C ambient temperature.

# 1 Functional description

**Figure 1. Pin localization**




*pin 5 is internally connected to the metallic upper lid, pin5 can be NC or it can be connected to ground to sink electronic charges

**Figure 2. Block diagram**

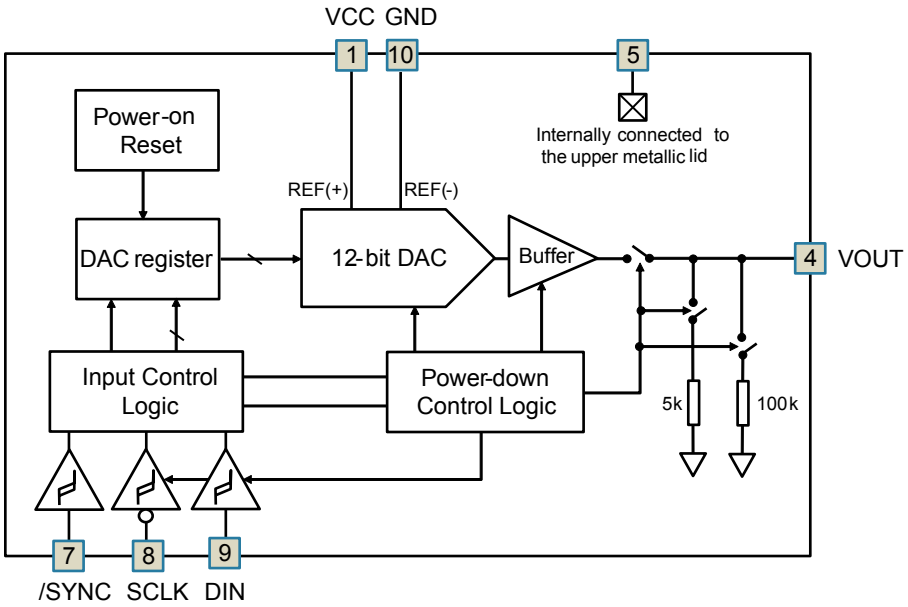


**Table 1. Pin description**

| # | Name | Type | Description |
|---|---|---|---|
| 1 | Vcc | Supply | Power supply and reference input; must be decoupled to GND |
| 2 | NC | - | No connected, not internally connected to die |
| 3 | NC | - | No connected, not internally connected to die |
| 4 | VOUT | Output | Analog output voltage |
| 5 | NC | - | No connected, not internally connected to die, internally connected to the upper lid |
| 6 | NC | - | No connected, not internally connected to die |
| 7 | SYNC/ | Input | Frame synchronization input for the data input. When this pin goes low, it enables the input shift register and data it is transferred on the falling edges of SCLK. The DAC is updated on the $16^{th}$ clock cycle unless SYNC/ is brought high before the $16^{th}$ clock, in which case the rising edge of SYNC acts as an interrupt and the write sequence is ignored by the DAC |
| 8 | SCLK | Input | Serial clock input; data is clocked into the input shift register on the falling edges of this pin |
| 9 | DIN | Input | Serial data input; data is clocked into the 16-bit shift register on the falling edges of SCLK after the fall of SYNC/ |
| 10 | GND | - | Ground reference for the whole circuitry |

# 2 Maximum ratings and operating conditions

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

**Table 2. Absolute maximum ratings**

| Symbol | Parameters | Value | Units |
|---|---|---|---|
| $V_{CC}$(1) | Maximum power supply between VCC and GND | -0.3 V to 4.8 V | V |
| $V_i$(2) | Max. voltage on any pin vs. GND | -0.3 V to VCC+0.3 V (and 4.8 V max.) | V |
| $T_{stg}$ | Maximum temperature storage | -65 to +150 | °C |
| $T_j$ | Maximum junction temperature | +150 | °C |
| $R_{thja}$ | Junction to ambient thermal resistance (Flat-10 package)(3) | 140 | °C/W |
| $R_{thjc}$ | Junction to case thermal resistance (Flat-10 package)(3) | 22 | °C/W |
| Ii | Max input current at any pin | ±10 | mA |
| ESD | HBM on all pins (human body model) | 4 k | V |
| | CDM on all pins (charged device model) | 1 k | V |

1. *All voltages, except differential I/O bus voltage, are with respect to the network ground terminal .*
2. *When the input voltage at any pin exceeds the power supplies (that is VIN < GND or VIN > VCC ), the current at that pin should be limited to 10 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two.*
3. *Short-circuits can cause excessive heating. Destructive dissipation can result from short-circuits on the amplifiers.*

**Table 3. Operating conditions**

| Symbol | Parameters | Min. | Max. | Units |
|---|---|---|---|---|
| Vcc | Supply voltage | 2.3 | 3.6 | V |
| Vi | Input voltage on any pin vs. GND | 0 | Vcc | V |
| SCLK | Clock frequency | 1 | 20 | MHz |
| | Maximum load capacity | | 1 | nF |
| Ta | Ambient temperature range | -55 | +125 | °C |

# 3 Radiations

**Total dose (MIL-STD-883 TM 1019):**

The products guaranteed in radiation within the RHA QML-V system fully comply with the MIL-STD-883 TM 1019 specification.

The RHRDAC121 is RHA QML-V, tested and characterized in full compliance with the

MIL-STD-883 specification, between 50 and 300 rad/s only (full CMOS technology).

All parameters provided in Table 5. Electrical characteristics in single-ended input apply to both pre- and post-irradiation, as follows:

- All tests are performed in accordance with MIL-PRF-38535 and test method 1019 of MIL-STD-883 for total ionizing dose (TID).
- The initial characterization is performed in qualification only on both biased and unbiased parts.
- Each wafer lot is tested at high dose rate only, in the worst bias case condition, based on the results obtained during the initial qualification.

**Heavy ions:**

The behavior of the product when submitted to heavy ions is not tested in production. Heavy-ion trials are performed on qualification lots only.

**Table 4. Radiations**

| Type | Characteristics | Value | Unit |
|---|---|---|---|
| TID (1) | High-dose rate (50 - 300 rad/s) up to: | 100 | krad |
| Heavy-ions | SEL(2) immune up to :<br>(with a particle angle of 60° at 125 °C and a fluence of 1 x $10^7$ ions/cm2 (10 Million of particles per cm²)) | 120 | MeV.cm²/mg |
| | SEL immune up to:<br>(with a particle angle of 0° at 125 °C and a fluence of 1 x $10^7$ ions/cm2 (10 million of particles per cm²)) | 60 | |

1. *A total ionizing dose (TID) of 100 krad(Si) is equivalent to 1000 Gy(Si), (1 gray = 100 rad).*
2. *SEL: single event latch-up.*

# 4 Electrical characteristics

Vcc = +3.3 V, GND = 0 V, $f_{SCLK}$ = 20 MHz, $C_L$ = 200 pF, typ. values at +25 °C, min./max. values at -55 °C/125 °C, unless otherwise specified.

**Table 5. Electrical characteristics in single-ended input**

| Symbol | Parameters | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | |
| | Resolution with no missing codes | From -55 °C to +125 °C | | 12 | | Bits |
| INL | Integral non-linearity (end point method) | Over codes 48 to 4047 | -4 | | 4 | LSB |
| DNL | Differential non-linearity | DNL max., Vcc from 2.3 V to 3.6 V | | | 0.7 | LSB |
| | | DNL min., Vcc from 2.3 V to 3.6 V | -0.7 | | | LSB |
| VOFF | Offset error | Iout=0 | | | 10 | mV |
| FSE | Full scale error | Iout=0 | | | -1 | %FSR |
| GE | Gain error | All ones loaded to DAC register | -1 | | +1 | %FSR |
| ZCED | Zero code error drift | | | -20 | | µV/°C |
| TGE | Gain error tempCo | | | -0.7 | | ppm/°C |
| **Output characteristics** | | | | | | |
| $IPD_{sink}$ | $I_{sink}$ on Vout pin in power-down mode(1) | All PD mode | | | 1 | mA |
| ZCO | Zero code output | Iout = 10 µA | | 1 | 5 | mV |
| | | Iout = 100 µA | | 4.5 | 9 | mV |
| FSO | Full scale output | Iout = 10 µA | 3.290 | 3.298 | | V |
| | | Iout = 100 µA | 3.285 | 3.288 | | V |
| | DC output impedance | | | 0.1 | 16 | Ohm |
| **Logic input** | | | | | | |
| $I_{in}$ | Input current | | -200 | | +200 | nA |
| $V_{IL}$ | Input low voltage | From -55 °C to +125 °C Vcc = 3.6 V | | | 0.7 | V |
| | | From -55 °C to +125 °C Vcc = 2.3 V | | | 0.7 | V |
| $V_{IH}$ | Input high voltage | From -55 °C to +125 °C Vcc = 3.6 V | 2 | | | V |
| | | From -55 °C to +125 °C Vcc = 2.3 V | 1.7 | | | V |
| $C_{in}$ | Input capacitance | | | | 3 | pF |

| Symbol | Parameters | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Consumption** | | | | | | |
| $I_{CC}$ | Supply current (output unloaded) | Normal mode, $V_{cc}$=3.6 V, $f_{SCLK}$=20 MHz | | 165 | 180 | µA |
| | | Normal mode, $V_{cc}$=3.6 V, $f_{SCLK}$=10 MHz | | 145 | 160 | |
| | | Normal mode, $V_{cc}$=3.6 V, $f_{SCLK}$=0 | | 110 | 140 | |
| | | All PD modes, $V_{cc}$=3.6 V, $f_{SCLK}$=20 MHz | | 60 | 80 | |
| | | All PD modes, $V_{cc}$=3.6 V, $f_{SCLK}$=10 MHz | | 38 | 50 | |
| | | All PD modes, $V_{cc}$=3.6 V, $f_{SCLK}$=0 | | 0.5 | 1 | |
| $t_s$ | Output voltage settling time | FF0 to 00F code, no load CL = 200 pF | | 3.8 | 13 | µs |
| | | FF0 to 00F code, CL = 500 pF | | 4 | 13 | |
| | | 00Fh to FF0h code, CL = 200 pF | | 3.2 | 13 | |
| | | 00Fh to FF0h code, CL = 500 pF | | 4 | 13 | |
| SR | Output slew rate | | | 0.8 | | V/µs |
| | Glitch impulse | Code change from 800h to 7FFh | | 12 | | nV/s |
| | Digital feedthrough | | | 0.5 | | |
| $T_{wu}$ | Wake-up time | Vcc = 3.6 V | | 3.5 | 6 | µs |
| | | Vcc = 2.3V | | 4 | 7 | |
| $1/f_{SCLK}$ | Clock cycle time | | 50 | | | ns |
| $t_H$ | Clock high time | | 20 | | | ns |
| $t_L$ | Clock low time | | 20 | | | ns |
| $t_{SUCL}$ | Set-up time SYNC/ to SCLK rising edge | | 0 | | | ns |
| $t_{SUD}$ | Data set-up time | | 6 | | | ns |
| $t_{DHD}$ | Data hold time | | 4.5 | | | ns |
| $t_{CS}$ | Clock fall to rise of SYNC/ | Vcc=3.6 V | 13 | | | ns |
| | | Vcc=2.3 V | 17 | | | ns |
| $t_{SYNC}$ | SYNC/ high time | Vcc=3.6 V | 36 | | | ns |
| | | Vcc=2.3 V | 35 | | | ns |

1. *Guaranteed by design and characterization.*

**Figure 3. Serial interface**

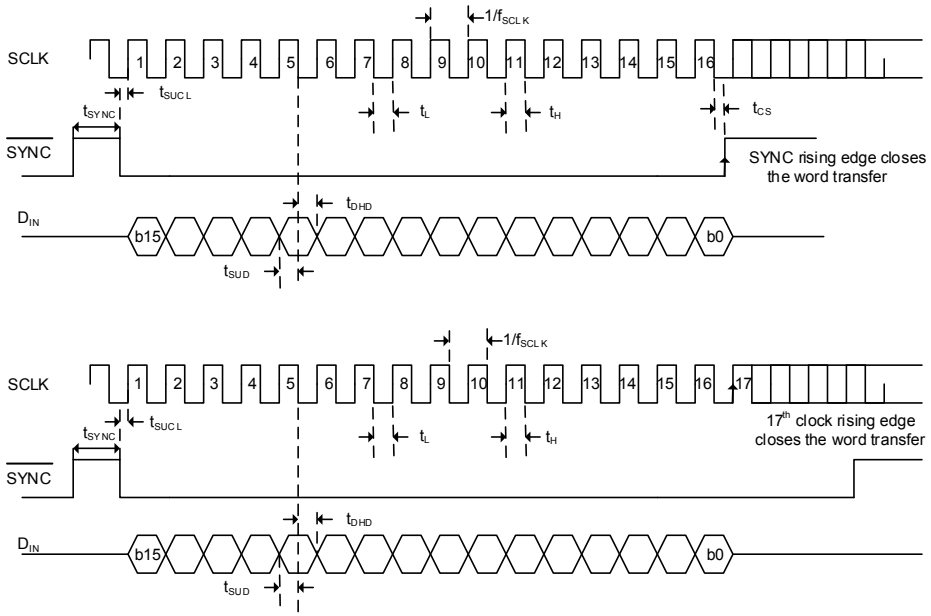
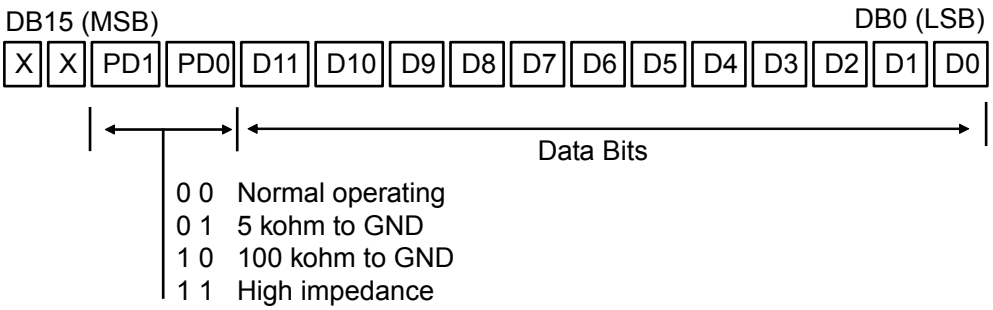



**Figure 4. Input register**



## 4.1 Typical characteristics

**Figure 5. INL vs. Vcc (temp.=25 °C)**

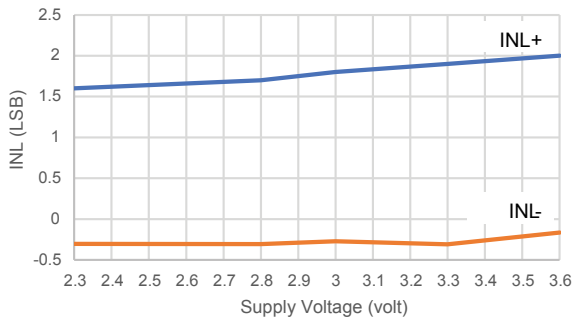



**Figure 6. DNL vs. Vcc (temp.=25 °C)**

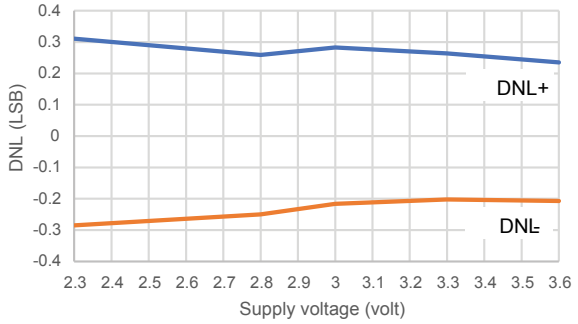



**Figure 7. INL vs. Vcc on full temp. range**

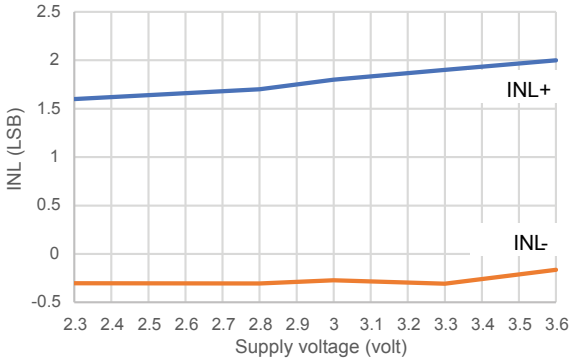



**Figure 8. DNL vs. Vcc on full temp. range**

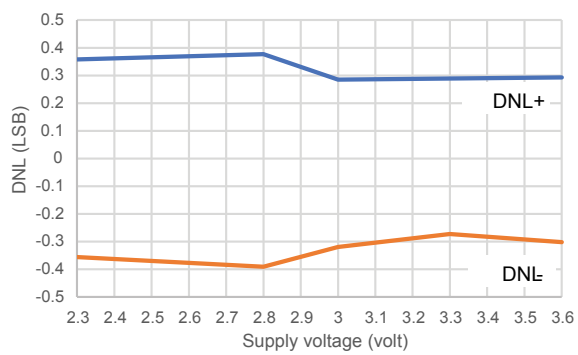



**Figure 9. INL vs. temp. (Vcc=3.3V)**

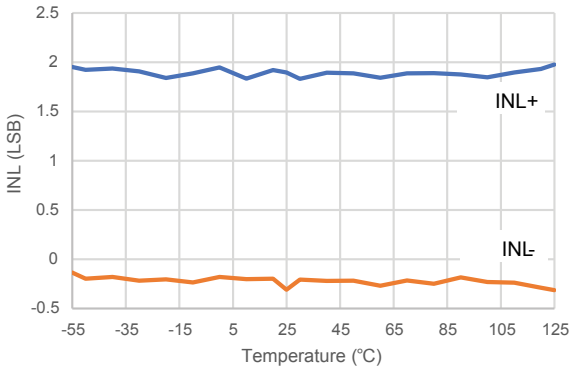



**Figure 10. DNL vs. temp. (Vcc=3.3V)**

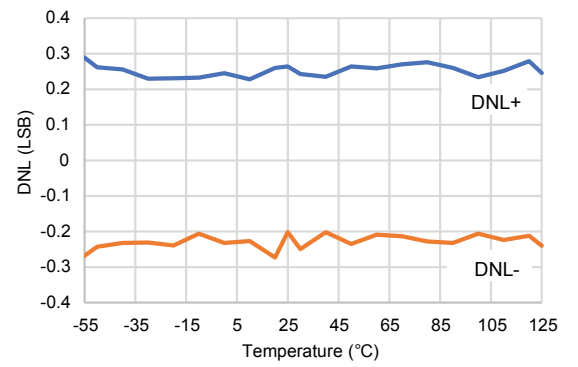


Figure 11. INL vs. clock frequency (temp.=25 °C)

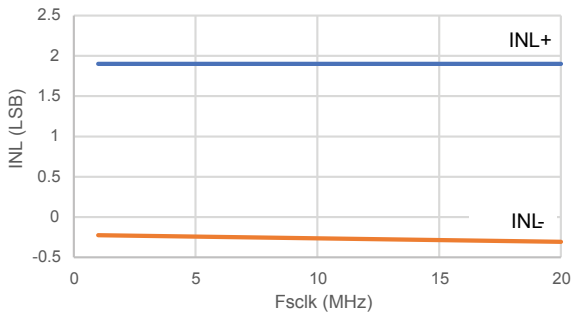
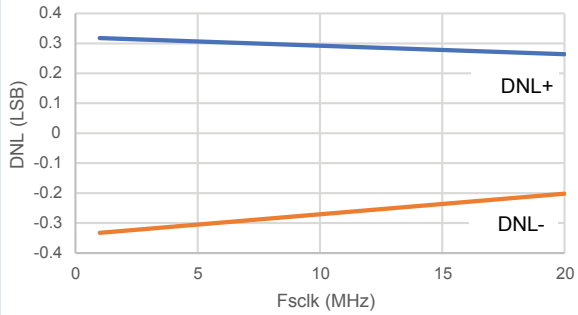



Figure 12. DNL vs. clock frequency (temp.=25 °C)

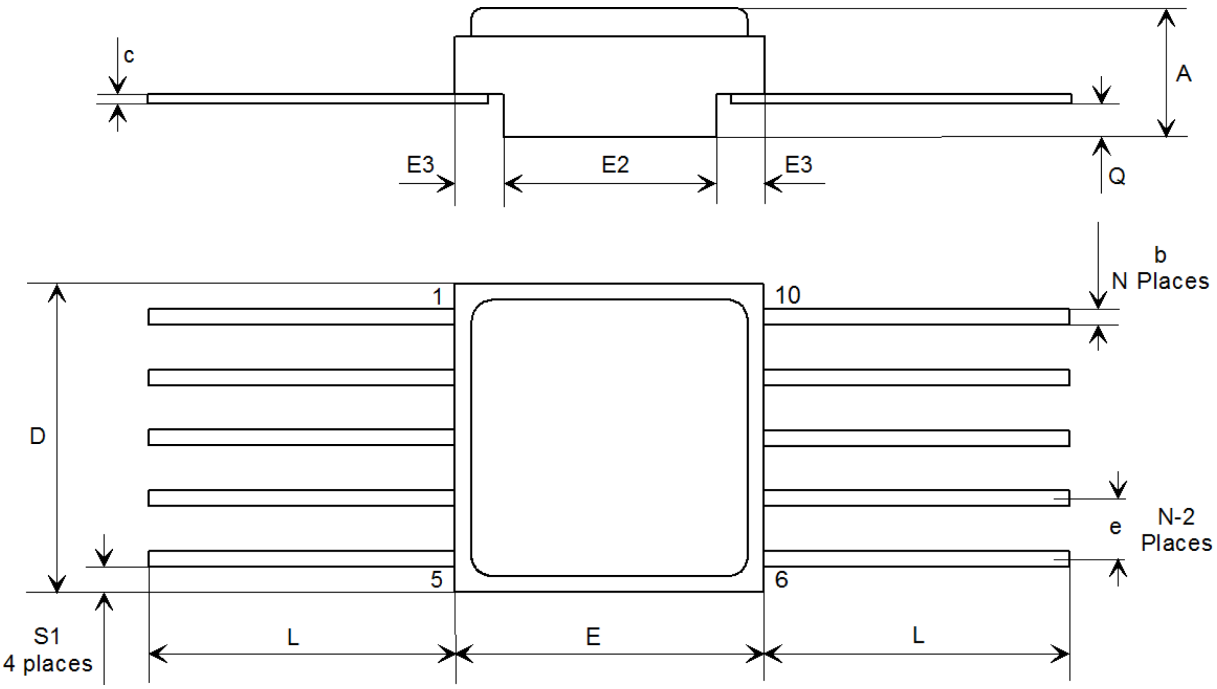


# 5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

## 5.1 Flat-10 package information

Figure 13. **Flat-10 package outline**




*Note: The upper metallic lid is electrically connected to pin 5.*

**Table 6. Flat-10 mechanical data**

| Symbol | mm | | | Inches[1] | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 2.26 | 2.44 | 2.62 | .089 | .096 | .103 |
| b | 0.38 | 0.43 | 0.48 | .015 | .017 | .019 |
| c | 0.102 | 0.127 | 0.152 | .004 | .005 | .006 |
| D | 6.35 | 6.48 | 6.60 | .250 | .255 | .260 |
| E | 6.35 | 6.48 | 6.60 | .250 | .255 | .260 |
| E2 | 4.32 | 4.45 | 4.58 | .170 | .175 | .180 |
| E3 | 0.88 | 1.01 | 1.14 | .035 | .040 | .045 |
| e | | 1.27 | | | .050 | |
| L | 6.35 | | 9.40 | .250 | | .370 |
| Q | 0.66 | 0.79 | 0.92 | .026 | .031 | .036 |
| S1 | 0.16 | 0.485 | 0.81 | .006 | .019 | .032 |
| N | | 10 | | | 10 | |

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*

# 6 Ordering information

| Order code | Description | Package | Lead finishing | Marking[1] | Packing |
|---|---|---|---|---|---|
| **RH-DAC121K1** | Engineering model | Flat-10 | Gold | RH-DAC121K1 | Strip pack |
| **RHRDAC121K01V** [2] | Flight model | | Gold | TBD | |
| **RHRDAC121K02V** [2] | Flight model | | Solder dip | TBD | |

1. *Specific marking only. Complete marking includes the following:*
   - *ST logo*
   - *Date code (date of the package was sealed) in YYWWA (year, week, and lot of index of the week)*
   - *Country of origin (FR= France).*
2. *Under development.*

# 7 Other information

## 7.1 Date code

The date code (date the package was sealed) is structured as follows:

- Engineering model: 3yywwz
- Flight model: yywwz

Where:

yy = last two digits of the year, ww = week digits, z = lot index of the week

## 7.2 Product documentation

Each product shipment includes a set of associated documentation within the shipment box. This documentation depends on the quality level of the products, as detailed in the table below.

The certificate of conformance is provided on paper whatever the quality level. For QML parts, complete documentation, including the certificate of conformance, is provided on a CDROM.

**Table 7. Product documentation**

| Quality level | Item |
|---|---|
| Engineering model | Certificate of conformance including:<br>• Customer name<br>• Customer purchase order number<br>• ST sales order number and item<br>• ST part number<br>• Quantity delivered<br>• Date code<br>• Reference to ST datasheet<br>• Reference to TN1181 on engineering models<br>• ST Rennes assembly lot ID |
| QML-V Flight | Certificate of Conformance including:<br>• Customer name<br>• Customer purchase order number<br>• ST sales order number and item<br>• ST part number<br>• Quantity delivered<br>• Date code<br>• Serial numbers<br>• Group C reference<br>• Group D reference<br>• Reference to applicable SMD<br>• ST Rennes assembly lot ID |
| | Quality control inspection (groups A, B, C, D, E) |
| | Screening electrical data in/out summary |
| | Precap report |
| | PIND (particle impact noise detection) test |
| | SEM (scanning electronic microscope) inspection report |
| | X-ray plates |

## Revision history

Table 8. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 22-Jan-2021 | 1 | Initial release. |

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