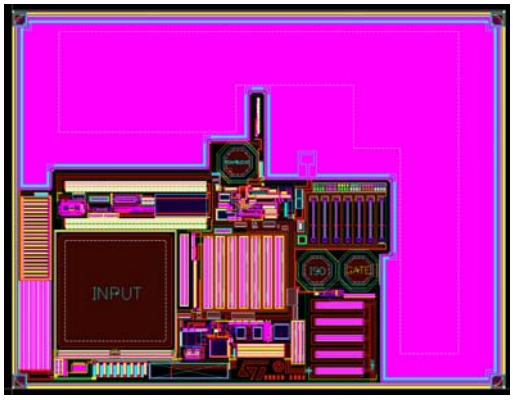
# VNP8T

## Omnifet II fully autoprotected Power MOSFET

**Datasheet - production data**




## Description

The VNP8T is a monolithic device designed in STMicroelectronics® VIPower® M0-3 technology, intended for the replacement of standard Power MOSFETs from DC up to 50 kHz applications.

Built in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

## Features

| Type | $R_{DS(on)}$ | $I_{lim}$ | $V_{clamp}$ |
|---|---|---|---|
| VNP8T | 120 mΩ | 3.5 A | 43 V |

- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Diagnostic feedback through input pin
- ESD protection
- Direct access to the gate of the Power MOSFET (analog driving)
- Compatible with standard Power MOSFETs

**Table 1. Device summary**

| DIE delivery package | Order code |
|---|---|
| D1 (Uncut inked wafer) | VNP8TD1 |
| D8 (Tape & Reel) | VNP8TD8 |

# Contents

# List of tables

# List of figures

# 1 Block diagram and pad configuration

**Figure 1. Block diagram**

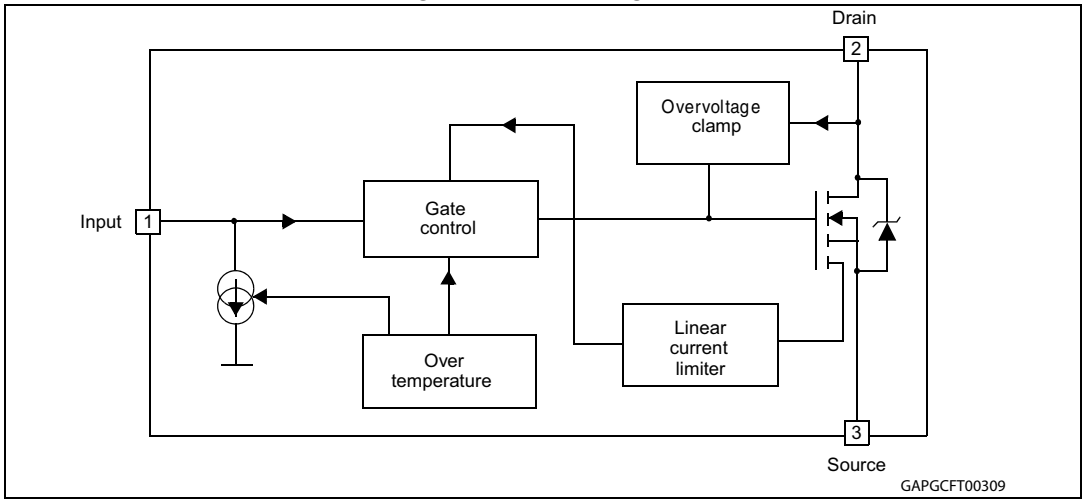



**Figure 2. Pad configuration**

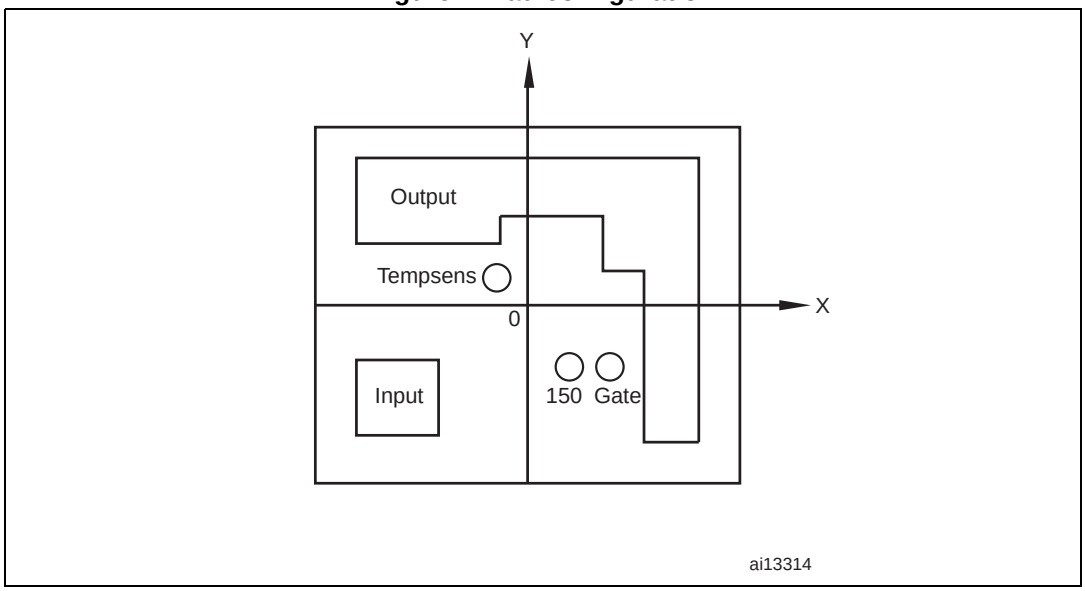



**Table 2. Pad location (axes origin: center of DIE)**

| Pad description | Center pad coordinates | | Pad dimensions | |
|---|---|---|---|---|
| | X (µm) | Y (µm) | X (µm) | Y (µm) |
| Input | -613.5 | -390.2 | 432 | 432 |
| Output | 730 | 29.7 | 250 | 1379.4 |
| Gate(1) | 427.5 | -301.2 | 102 | 102 |
| Drain | Back | | | |

1. This pad is intended for testing purposes only.

**Table 3. Physical characteristics**

| Parameter | Description | Value | Unit |
|---|---|---|---|
| Die size | | 2.21 x 1.72 | mm |
| Back metallization | Ti - Ni - Au | | |
| Front metallization | Al - Si | 3 | µm |
| Passivation layer | Silicon - Nitride | 1.5 | |
| Die thickness | | 280 ±20 | |
| Scribe street width | | 100 | |

# 2 Absolute maximum ratings

Stressing the device above the ratings listed in *Table 4: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in this section for extended periods may affect device reliability.

**Table 4. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage ($V_{IN}$ = 0 V) | Internally clamped | V |
| $V_{IN}$ | Input voltage | | |
| $I_{IN}$ | Input current | ± 20 | mA |
| $R_{IN\ MIN}$ | Minimum input series impedance | 220 | Ω |
| $I_D$ | Drain current | Internally limited | A |
| $I_R$ | Reverse DC output current | -5.5 | |
| $V_{ESD1}$ | Electrostatic discharge (R = 1.5 KΩ; C = 100 pF) | 4000 | V |
| $V_{ESD2}$ | Electrostatic discharge on output pin only (R = 330 Ω; C = 150 pF) | 16500 | |
| $T_j$ | Operating junction temperature | Internally limited | °C |
| $T_{stg}$ | Storage temperature | -55 to 150 | |
| $E_{MAX}$ | Single pulse avalanche energy ($L$ = 8 mH; $I_{out}$ = 3.5 A; $T_j$ = 175 °C) | 95 | mJ |

# 3 Electrical characteristics

Values specified in this section are for -40 °C < $T_j$ < 175 °C, unless otherwise specified.

**Table 5. Off-state**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CLAMP}$ | Drain-source clamp voltage | $V_{IN}$ = 0 V; $I_D$ = 200 mA | 43 | 45 | 55 | V |
| $V_{CLTH}$ | Drain-source clamp threshold voltage | $V_{IN}$ = 0 V; $I_D$ = 2 mA | 36 | | | V |
| $V_{INTH}$ | Input threshold voltage | $V_{DS}$ = $V_{IN}$; $I_D$ = 1 mA | 0.6 | | 2.5 | V |
| $I_{ISS}$ | Supply current from input pin | $V_{DS}$ = 0 V; $V_{IN}$ = 5 V | | 100 | 150 | µA |
| $V_{INCL}$ | Input-source clamp voltage | $I_{IN}$ = 1 mA; | 6 | 6.8 | 8 | V |
| | | $I_{IN}$ = -1 mA | -1.0 | 6.8 | -0.3 | V |
| $I_{DSS}$ | Zero input voltage drain current ($V_{IN}$ = 0 V) | $V_{DS}$ = 13 V; $V_{IN}$ = 0 V; $T_j$ = 25 °C; | | | 30 | µA |
| | | $V_{DS}$ = 4 V; $V_{IN}$ = 0 V; | | | 50 | µA |
| | | $V_{DS}$ = 4 V; $V_{IN}$ = 0 V; $T_j$ = -40 °C to 150 °C | | | 30 | µA |
| | | $V_{DS}$ = 25 V; $V_{IN}$ = 0 V | | | 90 | µA |

**Table 6. On-state**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $R_{DS(on)}$ | Static drain-source on resistance | $V_{IN}$ = 5 V; $I_D$ = 1.5 A; $T_j$ = 25 °C | — | — | 120 | mΩ |
| | | $V_{IN}$ = 5 V; $I_D$ = 1.5 A | — | — | 280 | mΩ |

**Table 7. Dynamic**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $g_{fs}$ (1) | Forward transconductance | $V_{DD}$ = 13 V; $I_D$ = 1.5 A | — | 5.0 | — | S |
| $C_{OSS}$ (1) | Output capacitance | $V_{DS}$ = 13 V; f = 1 MHz; $V_{IN}$ = 0 V | — | 150 | — | pF |

1. Guaranteed by design/characterization on final product.

**Table 8. Switching**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 15 V; $I_D$ = 1.5 A<br>$V_{gen}$ = 5 V; $R_{gen}$ = $R_{IN\ MIN}$ = 220 Ω<br>(see *Figure 3*) | — | 148 | — | ns |
| $t_r$ | Rise time | | — | 473 | — | ns |
| $t_{d(off)}$ | Turn-off delay time | | — | 804 | — | ns |
| $t_f$ | Fall time | | — | 484 | — | ns |
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 15 V; $I_D$ = 1.5 A<br>$V_{gen}$ = 5 V; $R_{gen}$ = 2.2 KΩ<br>(see *Figure 3*) | — | 627 | — | ns |
| $t_r$ | Rise time | | — | 3.1 | — | µs |
| $t_{d(off)}$ | Turn-off delay time | | — | 3.7 | — | µs |
| $t_f$ | Fall time | | — | 2.3 | — | µs |
| $(dI/dt)_{on}$ (1) | Turn-on current slope | $V_{DD}$ = 15 V; $I_D$ = 1.5 A<br>$V_{gen}$ = 5 V; $R_{gen}$ = $R_{IN\ MIN}$ = 220 Ω | — | 1.89 | — | A/µs |
| $Q_i$ (1) | Total input charge | $V_{DD}$ = 12 V; $I_D$ = 1.5 A; $V_{IN}$ = 5 V<br>$I_{gen}$ = 2.13 mA (see *Figure 6*) | — | 10 | — | nC |

1. Guaranteed by design/characterization on final product.

**Table 9. Source drain diode ($T_j$ = 25 °C) (1)**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{SD}$ (2) | Forward on voltage | $I_{SD}$ = 1.5 A; $V_{IN}$ = 0 V | — | 0.8 | — | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 1.5 A; dI/dt = 12 A/µs;<br>$V_{DD}$ = 30 V; L = 200 µH<br>(see *Figure 4*) | — | 107 | — | ns |
| $Q_{rr}$ | Reverse recovery charge | | — | 37 | — | µC |
| $I_{RRM}$ | Reverse recovery current | | — | 0.7 | — | A |

1. Guaranteed by design/characterization on final product.
2. Pulsed: Pulse duration = 300ms, duty cycle 1.5%

**Table 10. Protections**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{lim}$ | Drain current limit | $V_{IN}$ = 5 V; $V_{DS}$ = 13 V | 3.5 | 5 | 7 | A |
| $t_{dlim}$ | Step response current limit | $V_{IN}$ = 5 V; $V_{DS}$ = 13 V | | 10 | | µs |
| $T_{jsh}$ | Overtemperature shutdown | | 175 | 200 | 225 | °C |
| $T_{jrs}$ (1) | Overtemperature reset | | 160 | | | |
| $I_{gf}$ | Fault sink current | $V_{IN}$ = 5 V; $V_{DS}$ = 13 V; $T_j$ = $T_{jsh}$ | 10 | 15 | 20 | mA |
| $E_{as}$ (2) | Single pulse avalanche energy | Starting $T_j$ = 25°C; $V_{DD}$ = 24 V;<br>$V_{IN}$ = 5 V; $R_{gen}$= $R_{IN\ MIN}$ = 220 Ω;<br>L = 24 mH (see *Figure 5* and *Figure 7*) | 100 | | | mJ |

1. Guaranteed by design.
2. Energy capability not tested; its maximum value is guaranteed by design on package products.

# 4 Protection features

During normal operation, the INPUT pin is electrically connected to the gate of the internal Power MOSFET through a low impedance path.

The device then behaves like a standard Power MOSFET and can be used as a switch from DC up to 50 kHz. The only difference from the user's standpoint is that a small DC current $I_{ISS}$ (typ. 100 µA) flows into the INPUT pin in order to supply the internal circuitry.

## 4.1 Overvoltage clamp protection

The device integrates overvoltage clamp protection that is internally set at 45 V. This feature together with the rugged avalanche characteristics of the Power MOSFET stage gives this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.

## 4.2 Linear current limiter circuit

A linear current limiter circuit limits the drain current $I_D$ to $I_{lim}$ whatever the INPUT pin voltages. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold $T_{jsh}$.

## 4.3 Overtemperature and short circuit protections

These are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout occurs in the range 175 to 225 °C, a typical value being 200 °C. The device is automatically restarted when the chip temperature falls to about 10 °C below shutdown temperature.

## 4.4 Status feedback

In the case of an overtemperature fault condition ($T_j > T_{jsh}$), the device tries to sink a diagnostic current $I_{gf}$ through the INPUT pin in order to indicate fault condition. If driven from a low impedance source, this current may be used in order to warn the control circuit of a device shutdown. If the drive impedance is high enough so that the INPUT pin driver is not able to supply the current $I_{gf}$, the INPUT pin falls to 0V.

*Note: However this does not affect the device operation: no requirement is put on the current capability of the INPUT pin driver except to be able to supply the normal operation drive current $I_{ISS}$.*

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL Logic circuit.

**Figure 3. Switching time test circuit for resistive load**

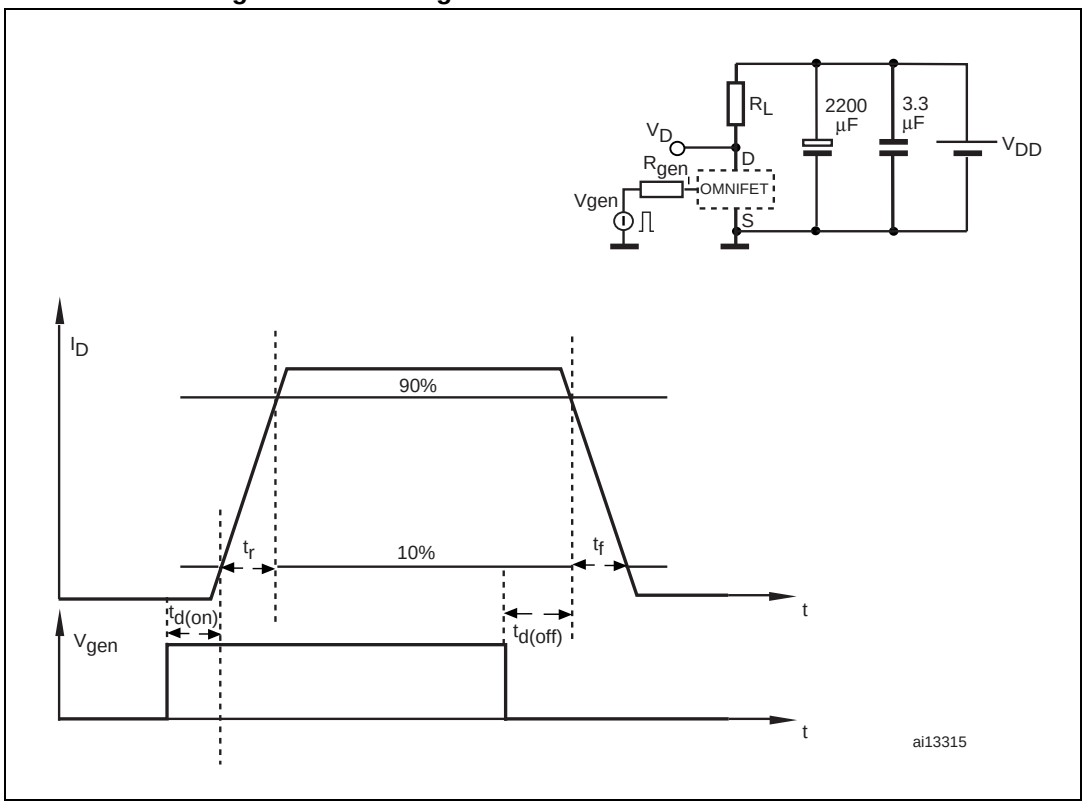



**Figure 4. Test circuit for diode recovery times**

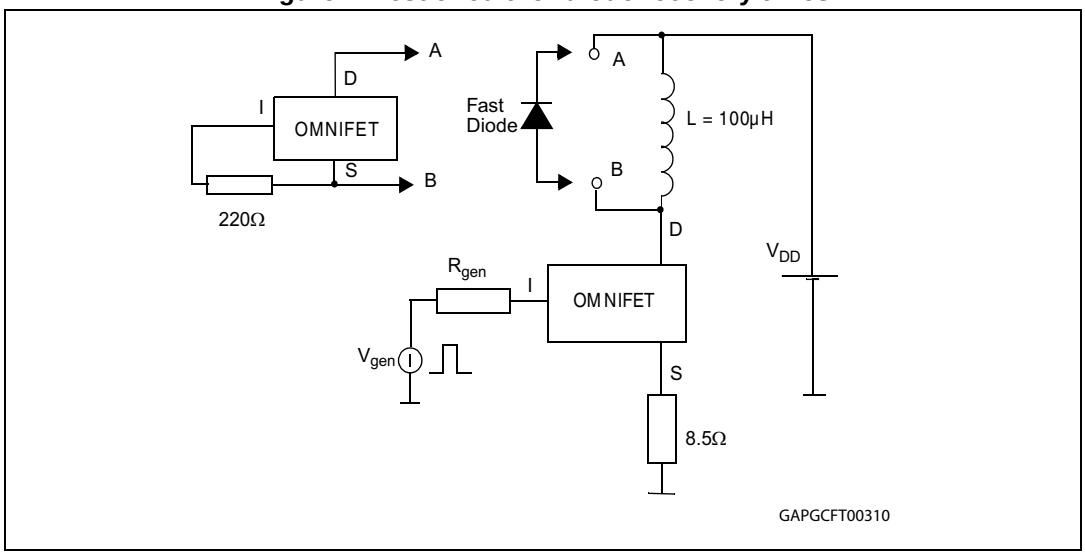


**Figure 5. Unclamped inductive load test circuits**

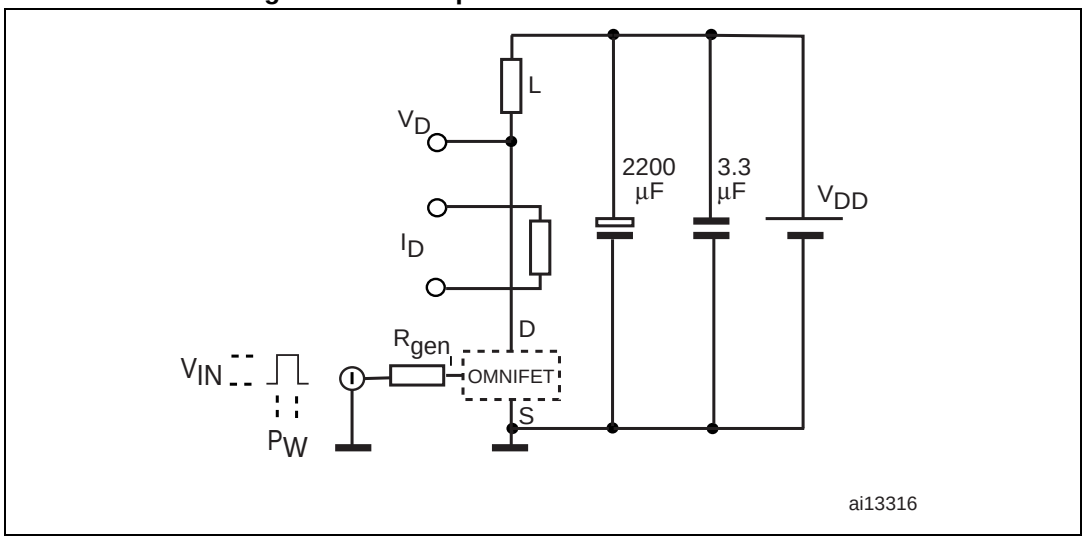



**Figure 6. Input charge test circuit**

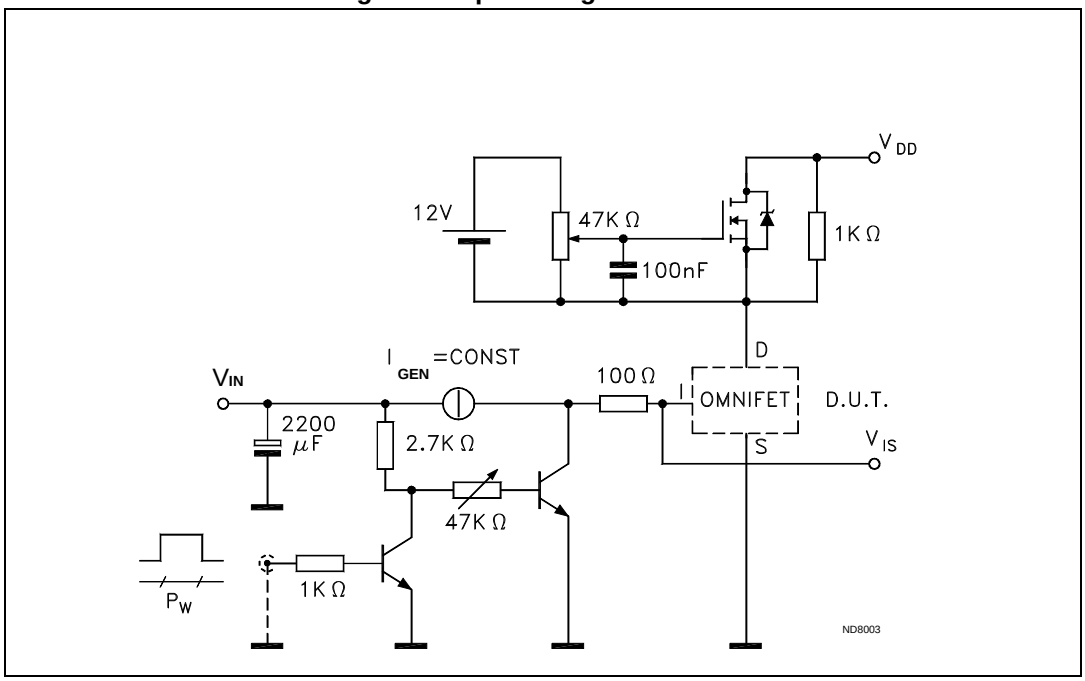
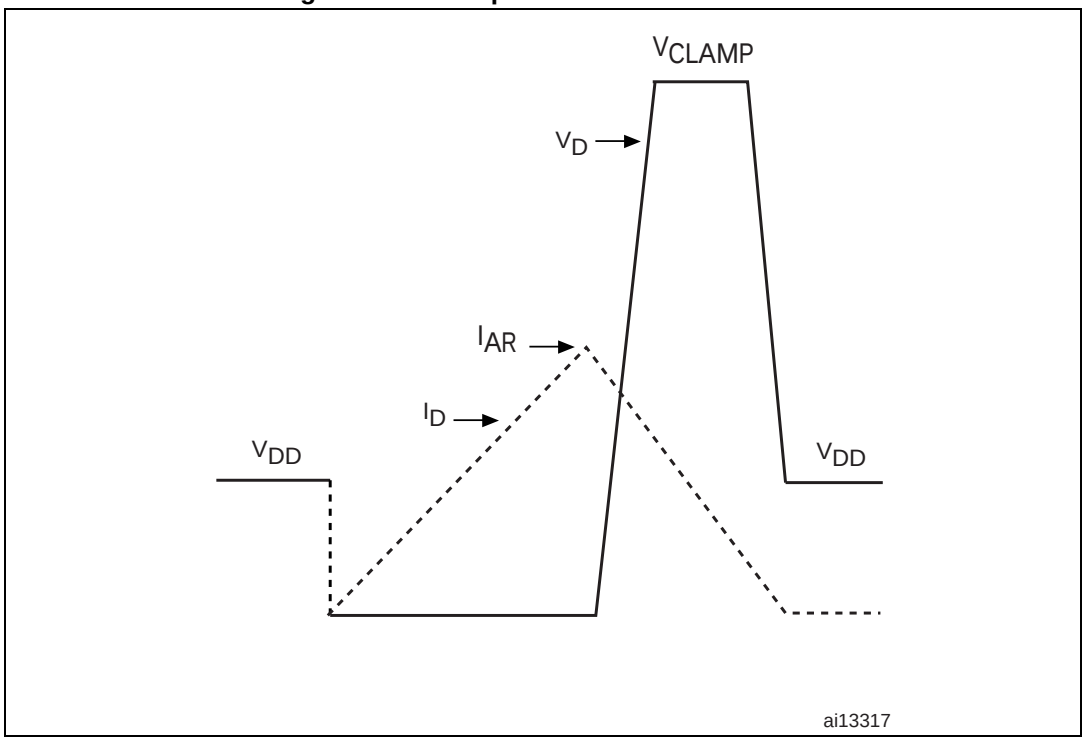


**Figure 7. Unclamped inductive waveforms**



# 5 Package information

## 5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

# 6 DIE package options

**Table 11. DIE delivery package options**

| Package option | Description | Details |
|---|---|---|
| D1 | Wafer tested, inked, uncut; see *Figure 8: DIE delivery package options* | Saw pickup and place subcontract required;<br>Wafer is between a double plastic shell, inside a plastic envelope sealed under vacuum;<br>Minimum number of wafers per box is approximately 5, weight is 1.5 kg. |
| D7 | Wafer tested, inked, cut on sticky foil on 7.5" plastic ring; see *Figure 8: DIE delivery package options* | Suitable for automatic pickup and place machine for sticky foil. Wafer is held by a plastic ring protected by two carton shells, inside a plastic envelope sealed under vacuum.<br>Minimum number of wafers per box is approximately 5, weight is 2 kg. |
| D8 | Wafer tested, inked, cut and packaged in tape and reel.See *Figure 9: Carrier tape information* and *Figure 10: Reel 7 INCH information*. | Suitable for automatic pickup. |

**Figure 8. DIE delivery package options**

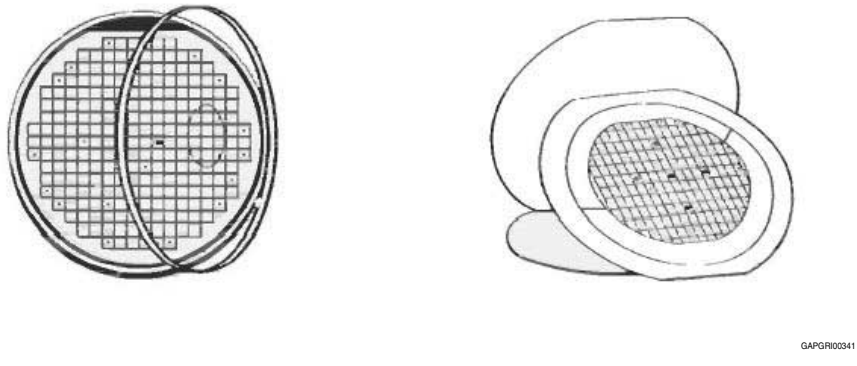



**Figure 9. Carrier tape information**

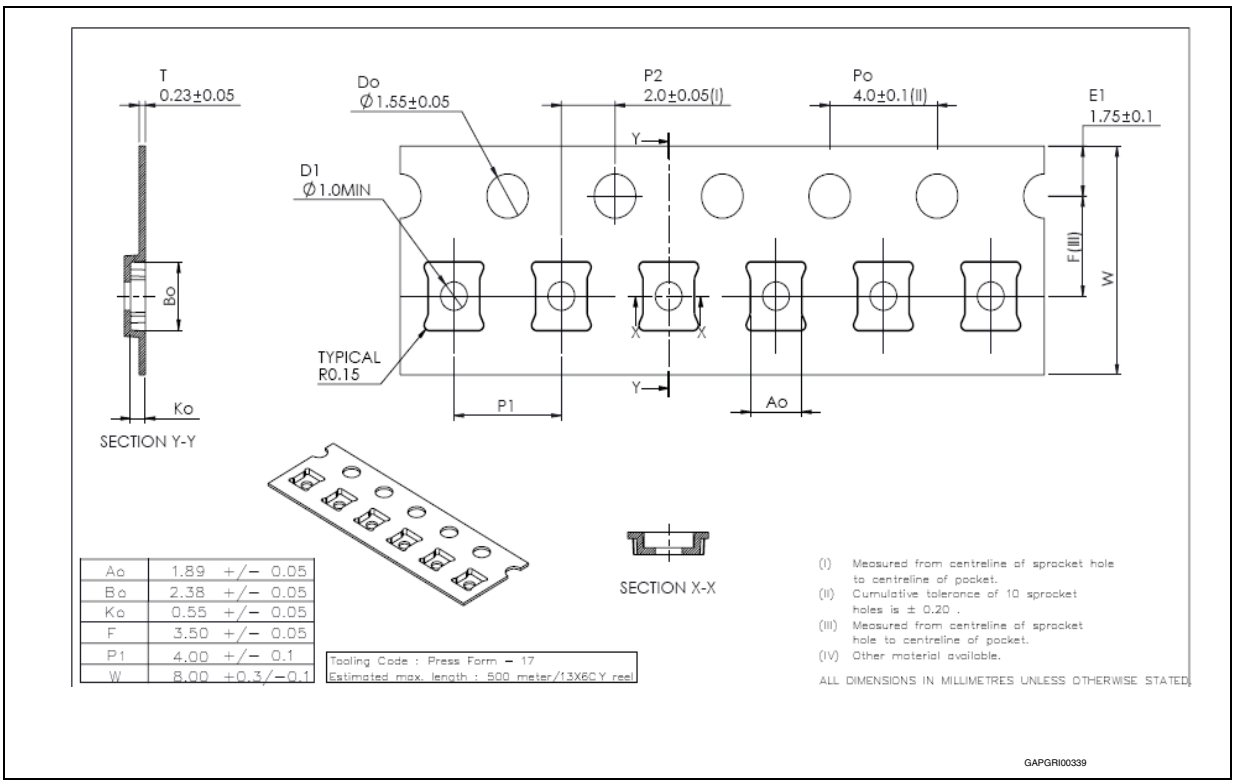
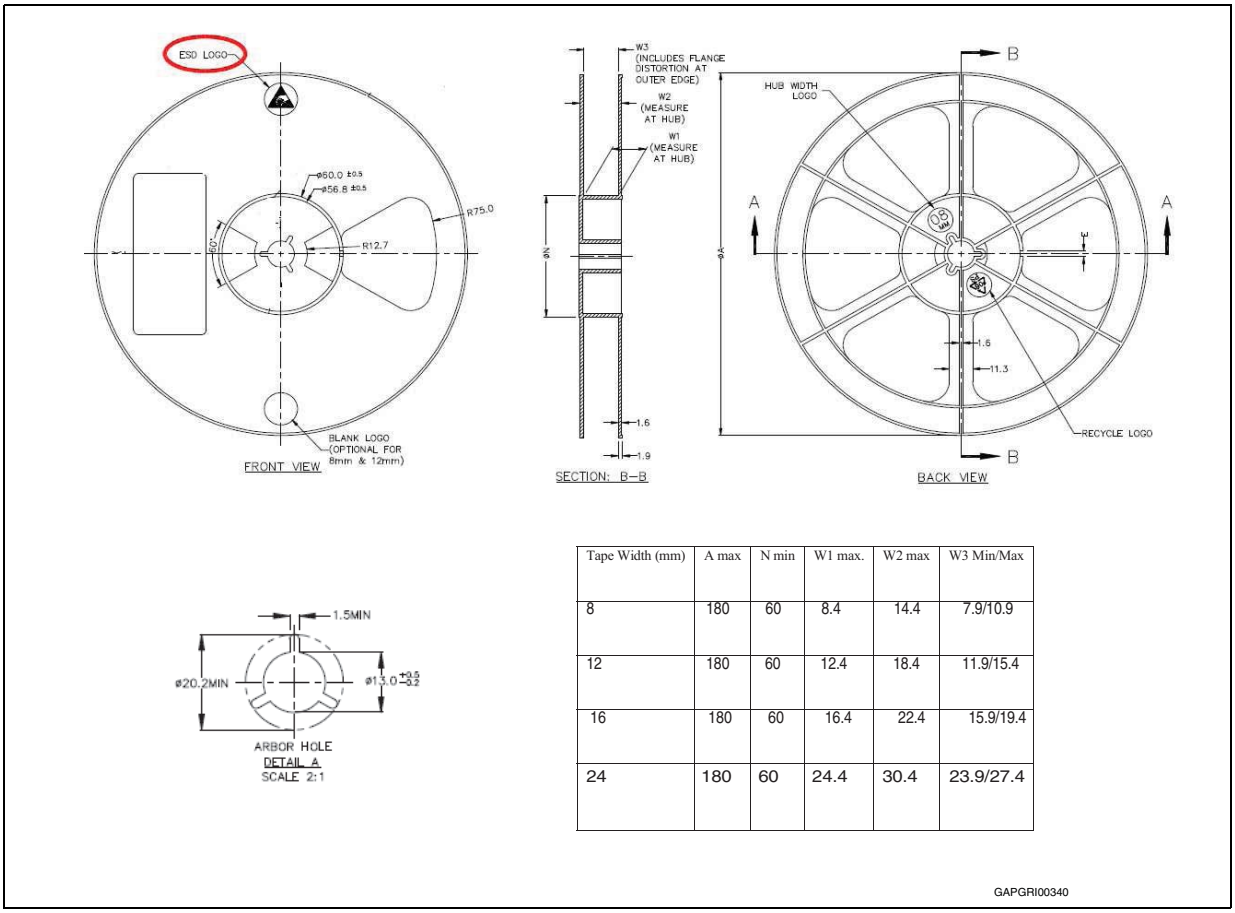

T
0.23±0.05
Do
Ø1.55±0.05
P2
2.0±0.05(I)
Po
4.0±0.1(II)
E1
1.75±0.1
D1
Ø1.0MIN
Y
Bo
Ko
SECTION Y-Y
TYPICAL
R0.15
P1
Ao
X
X
Y
F(III)
W
SECTION X-X
Ao 1.89 +/− 0.05
Bo 2.38 +/− 0.05
Ko 0.55 +/− 0.05
F 3.50 +/− 0.05
P1 4.00 +/− 0.1
W 8.00 +0.3/−0.1
Tooling Code : Press Form − 17
Estimated max. length : 500 meter/13X6CY reel
(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED
GAPGRI00339

**Figure 10. Reel 7 INCH information**




| Tape Width (mm) | A max | N min | W1 max. | W2 max | W3 Min/Max |
|---|---|---|---|---|---|
| 8 | 180 | 60 | 8.4 | 14.4 | 7.9/10.9 |
| 12 | 180 | 60 | 12.4 | 18.4 | 11.9/15.4 |
| 16 | 180 | 60 | 16.4 | 22.4 | 15.9/19.4 |
| 24 | 180 | 60 | 24.4 | 30.4 | 23.9/27.4 |

# 7 Revision history

Table 12. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 14-Mar-2012 | 1 | Initial release |
| 11-Sep-2012 | 2 | Updated test conditions in Table 8.<br>Updated Table 11 and added Figure 9 and 10. |
| 14-Dec-2012 | 3 | Updated *Figure 2: Pad configuration*<br>*Table 10: Protections*:<br>– $T_{jrs}$: added footnote |
| 24-Jun-2013 | 4 | *Features*:<br>– $V_{clamp}$: updated value<br>*Table 4: Absolute maximum ratings*:<br>– $E_{MAX}$: added row<br>*Table 5: Off-state*:<br>– $I_{DSS}$: added test conditions and value |
| 18-Sep-2013 | 5 | Updated disclaimer. |

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