

SECONDARY SIDE SYNCHRONOUS RECTIFICATION CONTROLLER

Description

The APR346 is a secondary side MOSFET driver for synchronous rectification, supports CCM, DCM and Quasi-Resonant Flyback Topologies.

The synchronous rectification can effectively reduce the secondary side rectifier power dissipation and provide high performance solution. By sensing primary MOSFET gate-to-source voltage, the APR346 can output ideal drive signal with less external components. It can provide high performance solution for 5V to 20V output voltage application.

The APR346 is available in SOT26 package.

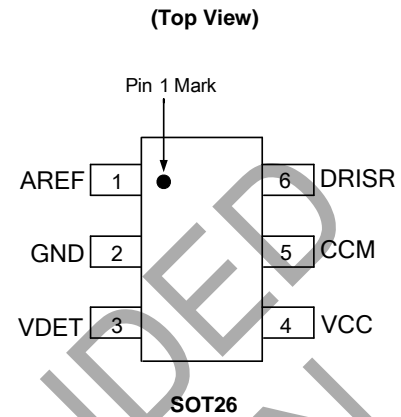
Features

- Synchronous Rectification for CCM, DCM Operation Flyback
- Eliminate Resonant Ring Interference
- Fewest External Components
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

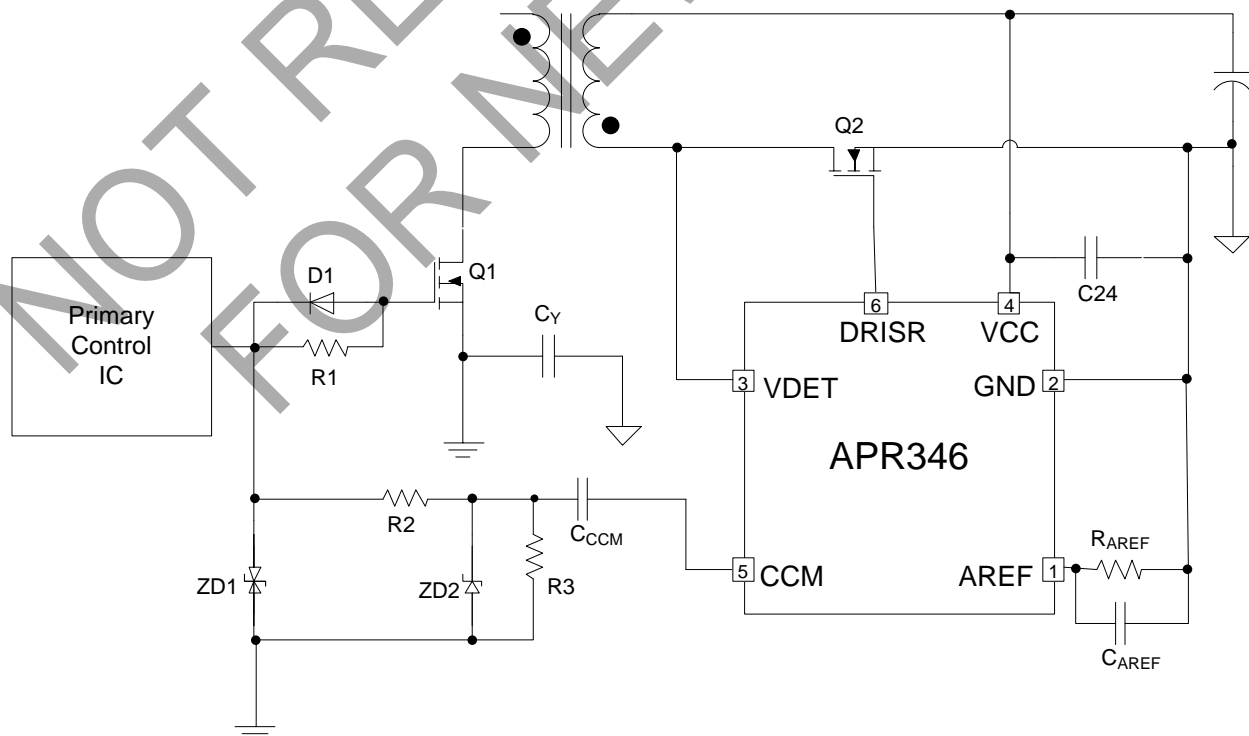
Pin Assignments



Applications

- Adapters/Chargers for Cell/Cordless Phones, ADSL Modems, MP3 and Other Portable Apparatus

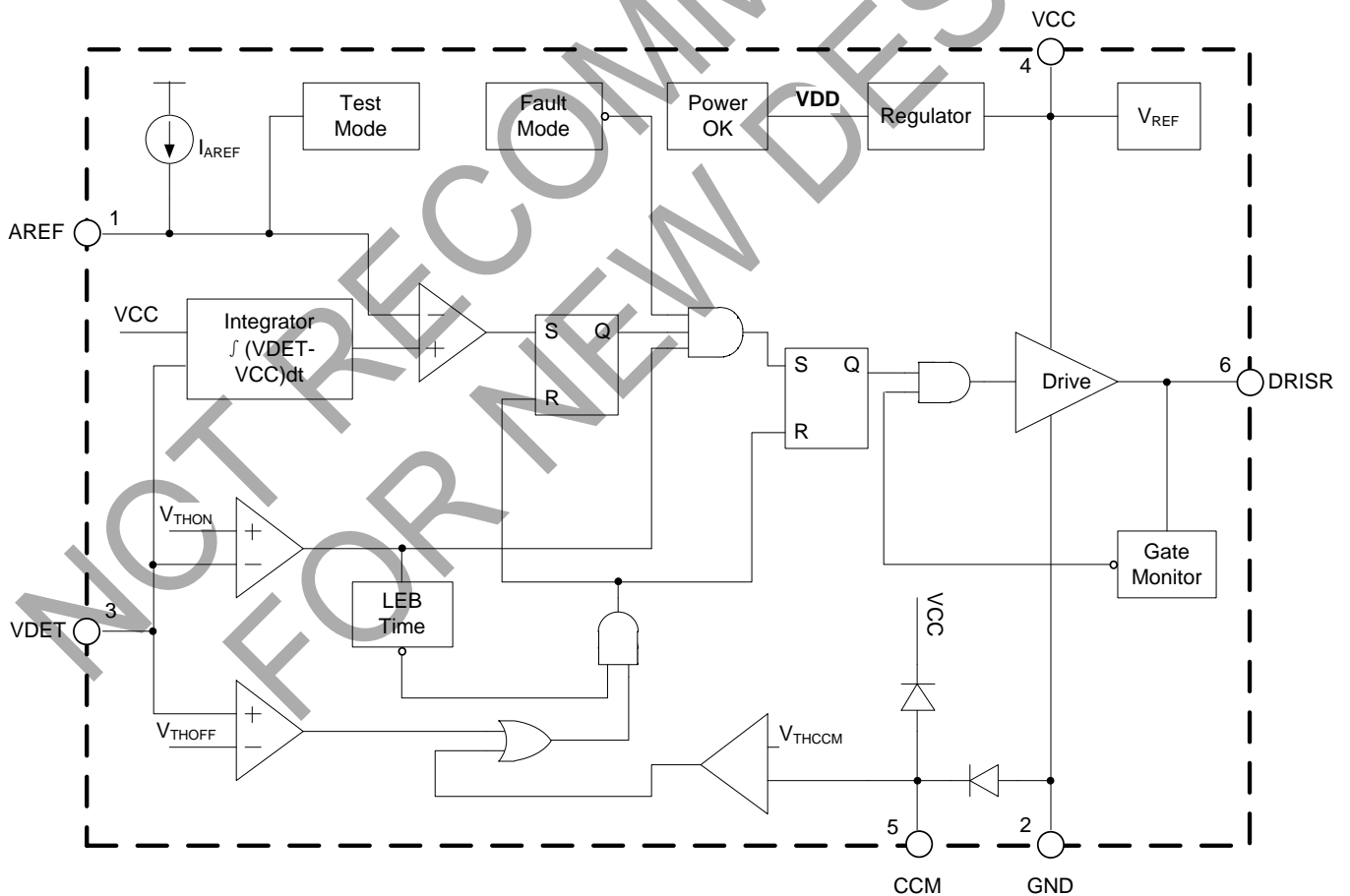
Typical Applications Circuit



Pin Descriptions

| Pin Number | Pin Name | Function |
|------------|----------|---|
| 1 | AREF | Program a voltage reference with a resistor from AREF to GND, to enable synchronous rectification MOSFET drive signal |
| 2 | GND | Ground |
| 3 | VDET | SR MOS drain-to-source voltage sense input, connected to drain pin of SR MOSFET through a resistor |
| 4 | VCC | Power supply, connected with system output |
| 5 | CCM | Primary trigger signal sense input |
| 6 | DRISR | Synchronous rectification MOSFET Gate drive |

Functional Block Diagram



Absolute Maximum Ratings (Note 4)

| Symbol | Parameter | Rating | Unit |
|--------------------|---|-------------|------|
| V _{CC} | Supply Voltage | -0.3 to 28 | V |
| V _{DET} | Voltage at VDET Pin (Note 5) | -0.7 to 160 | V |
| V _{DRISR} | Voltage at DRISR Pin | -0.3 to 20 | V |
| P _D | Power Dissipation at T _A = +25°C | 0.6 | W |
| T _J | Operating Junction Temperature | +150 | °C |
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| T _{LEAD} | Lead Temperature (Soldering, 10s) | +300 | °C |
| θ _{JA} | Thermal Resistance (Junction to Ambient) | 197 | °C/W |
| θ _{JC} | Thermal Resistance (Junction to Case) | 76 | °C/W |

- Notes: 4. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.
5. V_{DET} pin ESD sensitive.

Recommended Operating Conditions

| Symbol | Parameter | Min | Max | Unit |
|-----------------|---------------------|-----|-----|------|
| V _{CC} | Supply Voltage | 0 | 25 | V |
| T _A | Ambient Temperature | -40 | +85 | °C |

Electrical Characteristics (@ $V_{CC} = 5V$, $T_A = -40^{\circ}C < T_A < 85^{\circ}C$, unless otherwise specified.)

| Symbol | Parameter | Condition | Min | Typ. | Max | Unit | |
|--|--|--|-----------------------------|------|-------|------------------|---|
| Supply Voltage (VCC Pin) | | | | | | | |
| $I_{STARTUP}$ | Startup Current | $V_{CC} = V_{STARTUP} - 0.1V$ | – | 150 | 200 | μA | |
| I_{OP} | Operating Current | VDET Pin Floating $V_{CC} = 5V$ | – | 150 | 200 | μA | |
| $V_{STARTUP}$ | Startup Voltage | – | 2.6 | 3.1 | 3.4 | V | |
| – | UVLO | – | 2.3 | 2.8 | 3.1 | V | |
| Gate Driver | | | | | | | |
| V_{THON} | Gate Turn On Threshold | – | 0 | – | 1 | V | |
| V_{THOFF} | Gate Turn Off Threshold | – | -9 | -6 | -3 | mV | |
| t_{DON} | Turn On Delay Time | From V_{THON} to $V_{DRISR} = 1V$ | – | 70 | 130 | ns | |
| t_{DOFF} | Turn Off Propagation Delay Time | From V_{THOFF} to $V_{DRISR} = 4V$ | – | 100 | 150 | ns | |
| t_{RG} | Turn On Rising Time | From 1V to 4V, $V_{CC} = 5V$, $C_L = 4.7nF$ | – | 50 | 100 | ns | |
| t_{FG} | Turn Off Falling Time | From 4V to 1V, $V_{CC} = 5V$, $C_L = 4.7nF$ | – | 20 | 35 | ns | |
| t_{ON_MIN} | Minimum On Time | – | 1.2 | 1.6 | 2 | μs | |
| V_{DRISR} | V_{DRI_CLAMP} | Drive Output Clamp Voltage | $V_{CC} > V_{DRI_CLAMP}$ | – | 15 | – | V |
| | V_{DRI_TONMIN} | Drive Voltage during Minimum On Time | $V_{CC} < = V_{DRI_CLAMP}$ | – | – | V_{CC} | |
| | | | $V_{CC} > = V_{DRI_CLAMP}$ | – | – | V_{DRI_CLAMP} | |
| | V_{DRI_HOLD} | SR Drive Hold Voltage | $V_{CC} < 5V$ | – | – | V_{CC} | |
| $V_{CC} > = 5V$ | | | – | 5 | – | | |
| K_{QS} | (Note 6) | – | 0.325 | 0.42 | 0.515 | $mA \cdot \mu s$ | |
| V_{S_MIN} | Synchronous Rectification (SR) Minimum Operating Voltage (Note 7) | – | – | – | 4.5 | V | |
| Synchronous Rectification Detection | | | | | | | |
| V_{TH_CCM} | V_{DRISR} Rising Threshold | V_{DRISR} Output Transitions from High to Low | – | 0.53 | – | V | |
| t_{DCCM} | CCM Propagation Delay | From CCM Rising to V_{DRISR} Falling 10% | – | 20 | 35 | ns | |

Notes: 6. This item is used to specify the value of RAREF.

 7. This item specifies the minimum SR operating voltage of V_{IN_DC} , $V_{IN_DC} \geq N_{PS} \cdot V_{S_MIN}$.

Synchronous Rectification Principle Description

SR MOSFET Turn on

The APR346 determines the synchronous rectification MOSFET turning on time by monitoring the MOSFET drain-to-source voltage. For both of DCM and CCM operation, the turning on principle is same. When the drain voltage is lower than the turn-on threshold voltage V_{THON} , the IC outputs a positive drive voltage after a turn-on delay time (t_{DON}). The MOSFET will turn on and the current will transfer from the body diode into the MOSFET's channel. Since of parasitic parameter, the voltage on MOSFET drain pin has moderate voltage ringing at this moment, which maybe impact on SR controller V_{DET} voltage sense and bring about turning off fault. To avoid fault situation happening, a Minimum On Time (t_{ONMIN}) blanking period is used that will maintain the power MOSFET on for a minimum amount of time.

In Figure 1, the turn on blanking time t_{ONMIN} is to prevent the MOSFET drain-to-source voltage ringing affect. During this time, the V_{DRISR} is pulled up to V_{CC} ; after t_{ONMIN} , the drive voltage stops be pulled up by the driver, and begins to drop; when V_{DRISR} drops to V_{DRI_HOLD} , it will be held at this voltage until be pulled down.

DCM Turn off Operation

The DCM operation of the SR is described with timing diagram shown in Figure 1.

In the process of drain current decreasing linearly toward zero, the drain-source voltage rises synchronically. When it rises over the turn off threshold voltage V_{THOFF} , the APR346 pulls the drive signal down after a turn-off delay (t_{DOFF}).

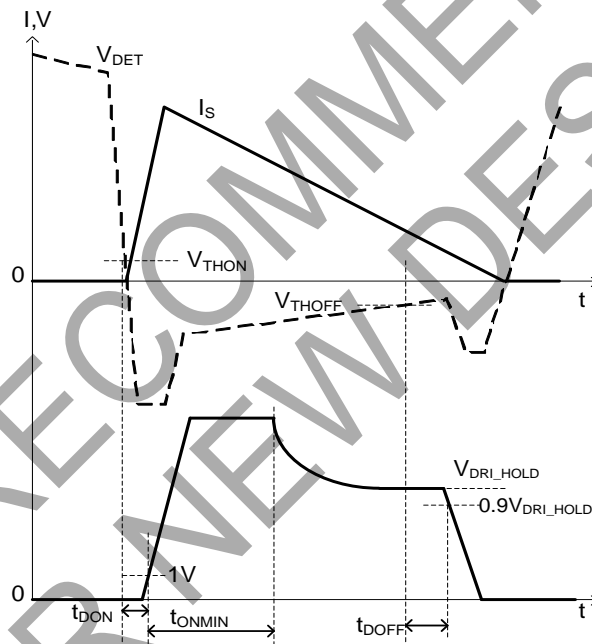


Figure 1. Typical Waveforms of APR346 in DCM

CCM Turn off Operation

The CCM pin is used to sense trigger signal for turning off the SR MOSFET before primary switch turning on in Continuous Conduction Mode (CCM) system. After t_{ONMIN} , if the CCM pin voltage rises over the threshold voltage V_{THCCM} , the drive voltage will be pulled down after a short delay time t_{DCCM} to turn off SR MOSFET. The CCM pin senses trigger signal coming from primary switch turn on signal through a RC networks circuit, a Y-type isolating capacitor C_{CCM} , two resistors R2 and R3. Note variations of these resistors, of C_{CCM} , and of the dV/dt across C_{CCM} require that worst-case tolerances be taken into account when determining the minimum value of C_{CCM} . For example, the value of this resistor will impact the rise time of CCM voltage. The bigger resistor, the slower the CCM voltage rises.

The value of C_Y should be much higher than that of C_{CCM} . If necessary, increase the value of C_Y to ensure that $C_Y \gg C_{CCM}$; do not decrease C_{CCM} .

C_Y is the main common-mode capacitance between the primary and the secondary sides of the system. This is usually a discrete component, whose value ranges from 47pF ~ 2200pF. Aside from any EMI-control purposes, it also serves as the return path for the CCM signal charging and discharging current pulses.

Synchronous Rectification Principle Description (Cont.)

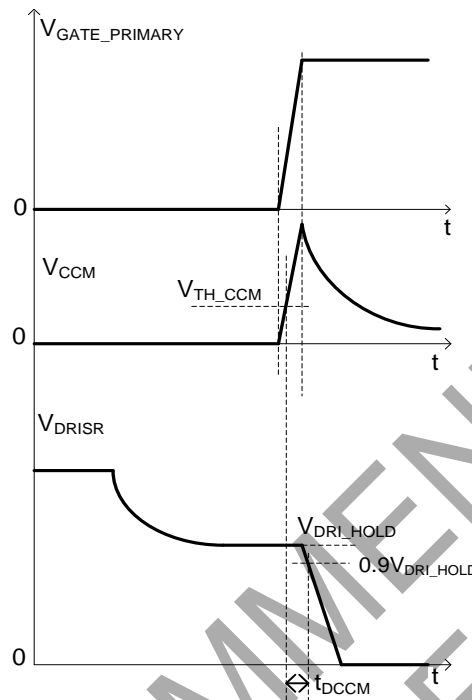


Figure 2. Typical Turn off Waveforms of APR346 in CCM

Minimum On Time

When the controlled MOSFET gate is turned on, some ringing noise is generated. The minimum on-time timer blanks the V_{THOFF} comparator and CCM comparator, keeping the controlled MOSFET on for at least the minimum on time. During the minimum on time, the turn off threshold (DCM and CCM) is totally blanked.

The Value and Meaning of AREF Resistor

As to DCM operation Flyback converter, after secondary rectifier stops conduction, the primary MOSFET Drain-to-source ringing waveform is resulted from the resonant of primary inductance and equivalent switch device output capacitance. This ringing waveform probably leads to Synchronous Rectifier error conduction. To avoid this fault happening, the APR346 has a special function design by means of volt-second product detecting. From the sensed voltage of VDET pin to see, the volt-second product of voltage above V_{CC} at primary switch on time is much higher than the volt-second product of each cycle ringing voltage above V_{CC} . Therefore, before every time Synchronous Rectifier turning on, the APR346 judges if the detected volt-second product of VDET voltage above V_{CC} is higher than a threshold and then turn on synchronous Rectifier. The purpose of AREF resistor is to determine the volt-second product threshold. The APR346 has a parameter, K_{QS} , which converts R_{AREF} value to volt-second product,

$$Area2 = R_{AREF} * K_{QS}$$

In general, Area1 and Area3 value depend on system design and are always fixed after system design frozen. As to Diodes Incorporated's PSR design, the Area1 value changes with primary peak current value and Area3 value generally keeps constant at all of conditions. So the AREF resistor design should consider the worst case, the minimum primary peak current condition. Since of system design parameter distribution, Area1 and Area3 have moderate tolerance. So Area2 should be designed between the middle of Area1 and Area3 to keep enough design margin.

Note: To keep the volt-second product threshold stable, a capacitor is suggested to parallel with AREF resistor. And the recommended value of this capacitor is 20nF.

$$Area3 < R_{AREF} * K_{QS} < Area1$$

Synchronous Rectification Principle Description (Cont.)

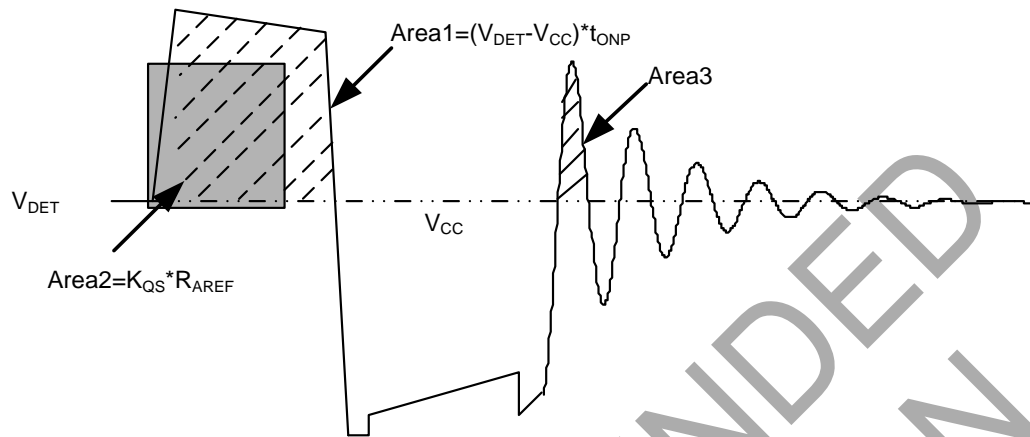


Figure 3. AREF Function

SR Minimum Operating Voltage

The APR346 sets a minimum SR operating voltage by comparing the difference between V_{DET} and output voltage (V_{CC}). The value of $V_{DET} - V_{CC}$ must be higher than its internal reference, then the APR346 will begin to integrate the area of $(V_{DET} - V_{CC}) * t_{ONP}$. If not, the area integrating will not begin and the SR driver will be disabled.

SR Turning Off Timing Impact on PSR CV Sampling

As to synchronous rectification on Flyback power system, SR MOSFET need to turn off in advance of secondary side current decreasing to zero to avoid current flowing reversely. When SR turns off in advance, the secondary current will flow through the body diode. The SR turning off time is determined by the V_{THOFF} at a fixed system. When V_{THOFF} is more close to zero, the SR turning on time gets longer and body diode conduction time gets shorter. Since of the different voltage drop between SR MOSFET and body diode, the PSR feedback signal V_{FB} appears a voltage jump at the time of SR MOSFET turning off. If the PSR CV sampling time t_{SAMPLE} is close to even behind this voltage jump time, there will be system unstable operation issue or the lower output voltage issue.

To ensure stable operating of system, it must be met:

$$t_{BODYDIODE} < t_{ONS} - t_{SAMPLE}$$

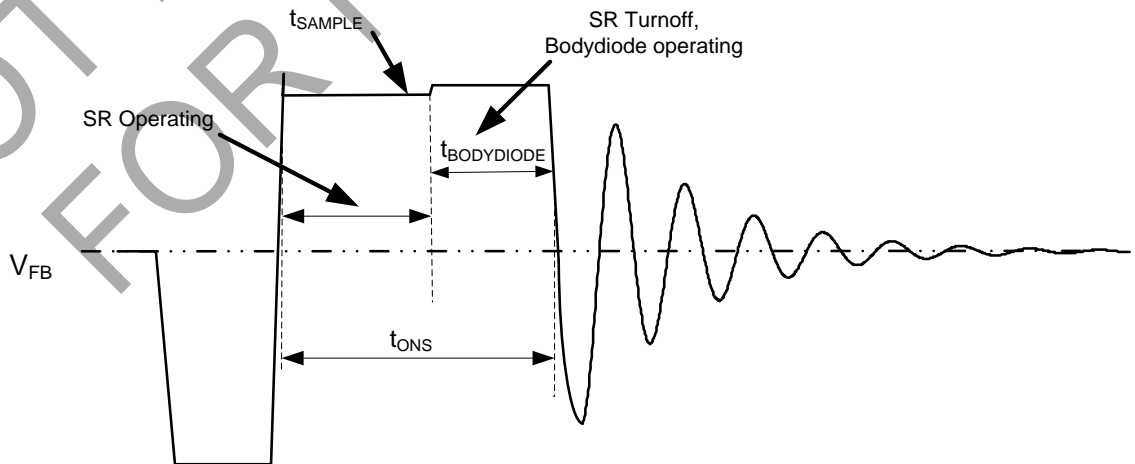


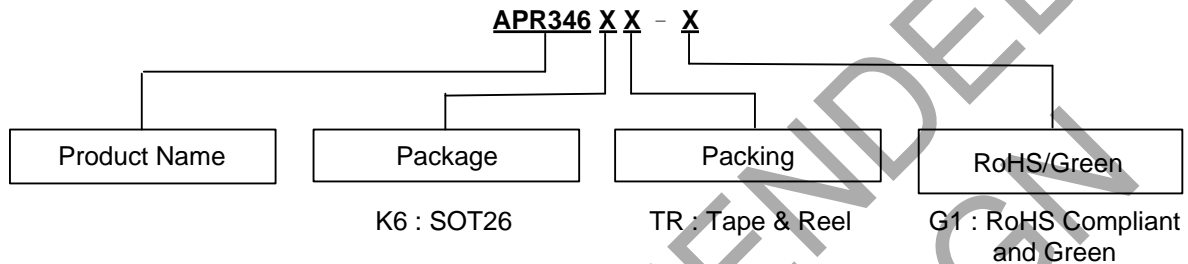
Figure 4. SR Turning Off Timing Impact on PSR CV Sampling

Synchronous Rectification Principle Description (Cont.)

Recommended Application Circuit Parameters

C_{AREF} is suggested to parallel with AREF resistor to keep the volt-second product threshold stable. And the recommended value of C_{AREF} is 20nF. The recommended value of C24 is 100nF.

Ordering Information

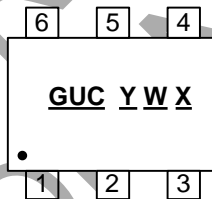


| Package | Temperature Range | Part Number | Marking ID | Packing |
|---------|-------------------|---------------|------------|------------------|
| SOT26 | -40°C to +85°C | APR346K6TR-G1 | GUC | 3000/Tape & Reel |

Marking Information

(1) SOT26

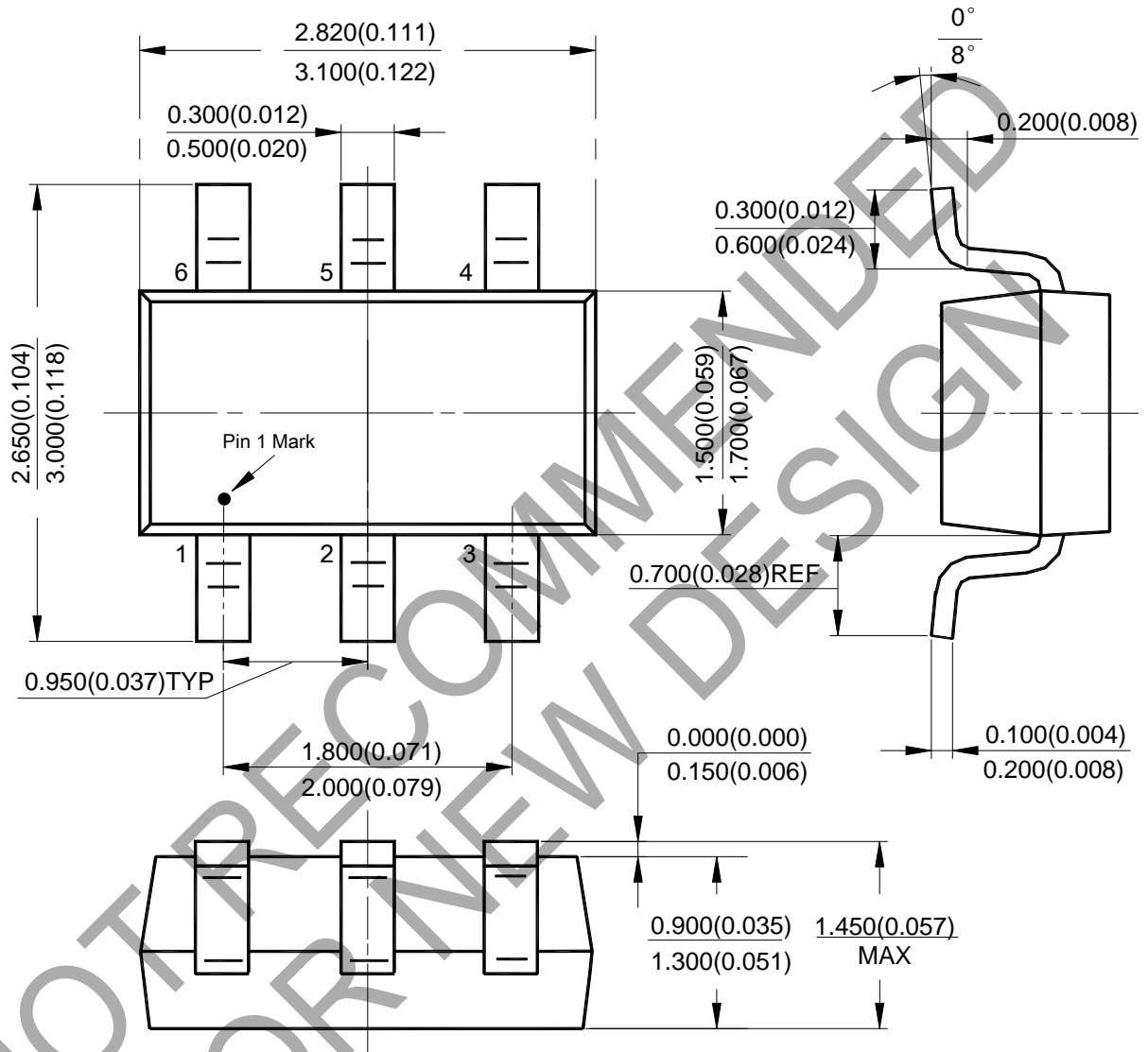
(Top View)



- GUC : Marking ID
- Y : Year 0~9
- W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents 52 and 53 week
- X : Internal Code

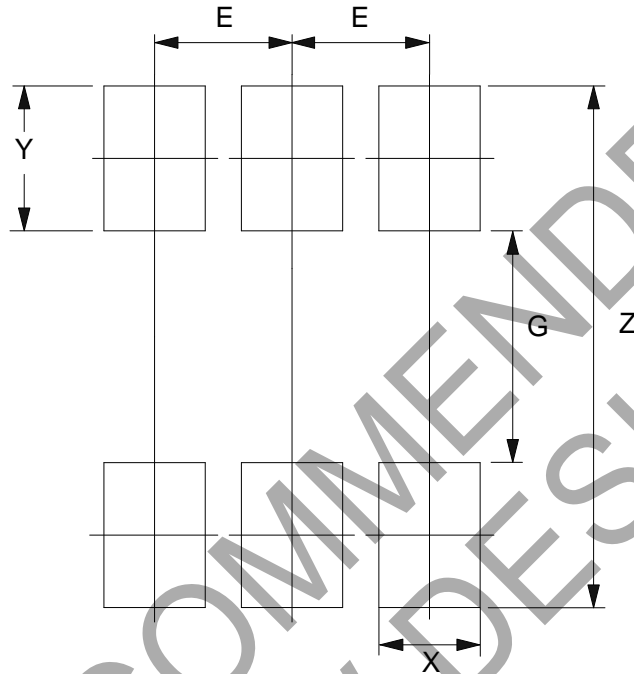
Package Outline Dimensions (All dimensions in mm(inch).)

(1) Package Type: SOT26



Suggested Pad Layout

(1) Package Type: SOT26



| Dimensions | Z (mm)/(inch) | G (mm)/(inch) | X (mm)/(inch) | Y (mm)/(inch) | E (mm)/(inch) |
|------------|------------------|------------------|------------------|------------------|------------------|
| Value | 3.600/0.142 | 1.600/0.063 | 0.700/0.028 | 1.000/0.039 | 0.950/0.037 |

NOT RECOMMENDED FOR NEW DESIGN

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