PI7C9X7958

PCI Express® Octal UART

Datasheet
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A Product Line of Diodes Incorporated

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REVISION HISTORY

Date	Revision Number	Description
09/05/07	0.1	Preliminary Datasheet
10/31/07	0.2	Fixed the diagrams Corrected Chapter 4.2 Pin Description (RREF, GPIO[7] EEPROM Organization Pin, RTS[0] EEPROM Bypass Pin) Updated Chapter 6 PCI Express Registers(6.2.42 [3], 6.2.36 UART Driver Setting, 6.2.41 GPIO Control Register) Revised Chapter 7.1 Registers in I/O Mode Updated Chapter 11 Ordering Info Updated Chapter 8 EEPROM
04/22/08	0.3	Updated 1 Features (Clock prescaler, Data frame size, Power Dissipation) Corrected 3 General Description Updated 4 Pin Assignment (description for shared pins added, MODE_SEL changed to DRIVER_SEL, VAUX changed to VDDCAUX, WAKEUP_L, CLKINP, CLKINN) Added 5.2.4 Mode Selection, 5.2.5 450/550 Mode, 5.2.6 Enhanced 550 Mode, 5.2.7 Enhanced 950 Mode Corrected 5.2.8 Transmit and Receive FIFOs, 5.2.9 Automated Flow Control Modified 5.2.12 Baud Rate Generation Updated 6 PCI Express Register Description (6.2.36, 6.2.42) Updated Format (6.2.20, 6.2.36, 6.2.54, 6.2.55, 6.2.57) Updated Chapter 7 UART Register Description (7.1.6 LCR Bit[5:0], 7.1.7 MCR Bit[5] and Bit[7], 7.1.9 MSR Bit[3:0], 7.2.6 LCR Bit[5:0], 7.2.7 MCR Bit[5] and Bit[7], 7.2.9 MSR Bit[3:0], 7.2.11 DLL, 7.2.12 DLH, 7.2.13 EFR, 7.2.18 ACR Bit[7:2], 7.2.23 CPRM) Updated Chapter 8.3 EEPROM Space Address Map And Description (00h, 0Ah, 40h) Added Chapter 9 Electrical Specification Corrected 9.2 DC Specification Updated 9.3 AC Specification Added 10 Clock Scheme
08/13/08	0.4	Updated Chapter 1 Features (added Industrial Temperature Range) Updated 9.1 Absolute Maximum Ratings: Ambient Temperature with power applied
11/25/08	1.0	Updated 7.1.13 Sample Clock Register and 7.2.27 Sample Clock Register Updated Chapter 12 Ordering Information Removed “Preliminary” and “Confidential” references
03/06/09	1.1	Corrected Figure 3-1 PI7C9X7958 Block Diagram (SYN_UART_CLK removed) Corrected Section 4.2.1 UART Interface (SYNCLK_IN_EN and SYN_UART_CLK removed) Corrected Figure 5-2 Internal Loopback in PI7C7958 Corrected Figure 5-3 Crystal Oscillator as the Clock Source (14.7456 MHz) Corrected Section 7.1.7 Modem Control Register (Bit[5]), 7.1.10 Special Function Register (Bit[4]), 7.2.7 Modem Control Register (Bit[5]), 7.2.10 Special Function Register (Bit[4]), 7.2.29 Receive FIFO Data Registers, 7.2.30 Transmit FIFO Data Register, 7.2.31
04/20/09	1.2	Added internal pull-up and pull-down information to UART Interface, System Interface, Test Signal, and EEPROM pins in Section 4.
09/24/09	1.3	Updated Figure 5-3 Crystal Oscillator as the Clock Source Updated Section 6.2.24 Message Signaled Interrupt (MSI) Next Item Pointer 8Ch Added Section 6.2.25 Message Address Register – Offset 90h Added Section 6.2.26 Message Upper Address Register – Offset 94h Added Section 6.2.27 Message Data Register – Offset 98h
03/18/11	1.4	Updated Section 11 Package Information
06/04/14	1.5	Updated Section 4.1 Pin List (SR_DO and SR_DI) Updated Section 4.2.5 EEPROM Interface (SR_DO and SR_DI) Created for IC Revision B Updated Chapter 12 Ordering Information Added Section 6.2.25 Message Control Register – OFFSET 8Ch
05/11/15	1.6	Updated Table 5-2 Baud Rate Generator Setting Updated Section 7.2.23 CLOCK PRESCALE REGISTER – OFFSET 14h
08/30/17	1.7	Update Logo Updated Section 4.1 PIN LIST of 160-PIN LFBGA Updated Section 4.2.1 UART INTERFACE Updated Table 9.1 Absolute Maximum Ratings Updated Table 9.2 DC Electrical Characteristics Updated Section 12 Ordering Information

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- x1 PCI Express link host interface
- Eight high performance 950-class UARTs
- Compliant with PCI Express Base Specification 1.1
- Compliant with PCI Express CEM Specification 1.1
- Compliant with PCI Power Management 1.2
- Fully 16C550 software compatible UARTs
- 128-byte FIFO for each transmitter and receiver
- Baud rate up to 15 Mbps in asynchronous mode
- Flexible clock prescaler from 4 to 46
- Automated in-band flow control using programmable Xon/Xoff in both directions
- Automated out-of-band flow control using CTS#/RTS# and/or DSR#/DTR#
- Arbitrary trigger levels for receiver and transmitter FIFO interrupts and automatic in-band and out-of-band flow control
- Global Interrupt Status and readable FIFO levels to facilitate implementation of efficient device drivers
- Detection of bad data in the receiver FIFO
- Data framing size including 5, 6, 7, 8 and 9 bits
- Hardware reconfiguration through Microwire compatible EEPROM
- Operations via I/O or memory mapping
- Dual power operation (1.8V for PCIe I/O and core, 3.3V for UART I/O)
- Power dissipation: 0.9 W typical in normal mode
- Industrial Temperature Range -40^{o} to 85^{o}
- 160-pin LFBGA package

2. APPLICATIONS

- Remote Access Servers
- Network / Storage Management
- Factory Automation and Process Control
- Instrumentation
- Multi-port RS-232/ RS-422/ RS-485 Cards
- Point-of-Sale Systems (PoS)
- Industrial PC (IPC)
- Industrial Control
- Gaming Machines
- Building Automation
- Embedded Systems

3. GENERAL DESCRIPTION

The PI7C9X7958 is a PCI Express Octal UART (Universal Asynchronous Receiver-Transmitters) I/O Bridge. It is specifically designed to meet the latest system requirements of high performance and lead (Pb) -free. The bridge can be used in a wide range of applications such as Remote Access Servers, Automation, Process Control, Instrumentation, POS, ATM and Multi-port RS232/ RS422/ RS485 Cards. The PI7C9X7958 provides one x1 PCIe (dual simplex 2.5 Gbps) uplink port, and it is fully compliant with PCI express 1.1 and PCI power management 1.2 specifications. The bridge supports eight high performance UARTs, each of which supports Baud rate up to 15 Mbps in asynchronous mode. The UARTs support in-band and out-band auto flow control, arbitrary trigger level, I/O mapping and memory mapping. The PI7C9X7958 is fully software compatible with 16C550 type device drivers and can be configured to fit the requirements of RS232, RS422 and RS485 applications. The EEPROM interface is provided for system implementation convenience. Some registers can be pre-programmed via hardware pin settings to facilitate system initialization. For programming flexibility, all of the default configuration registers can be overwritten by EEPROM data, such as sub-vendor and sub-system ID.

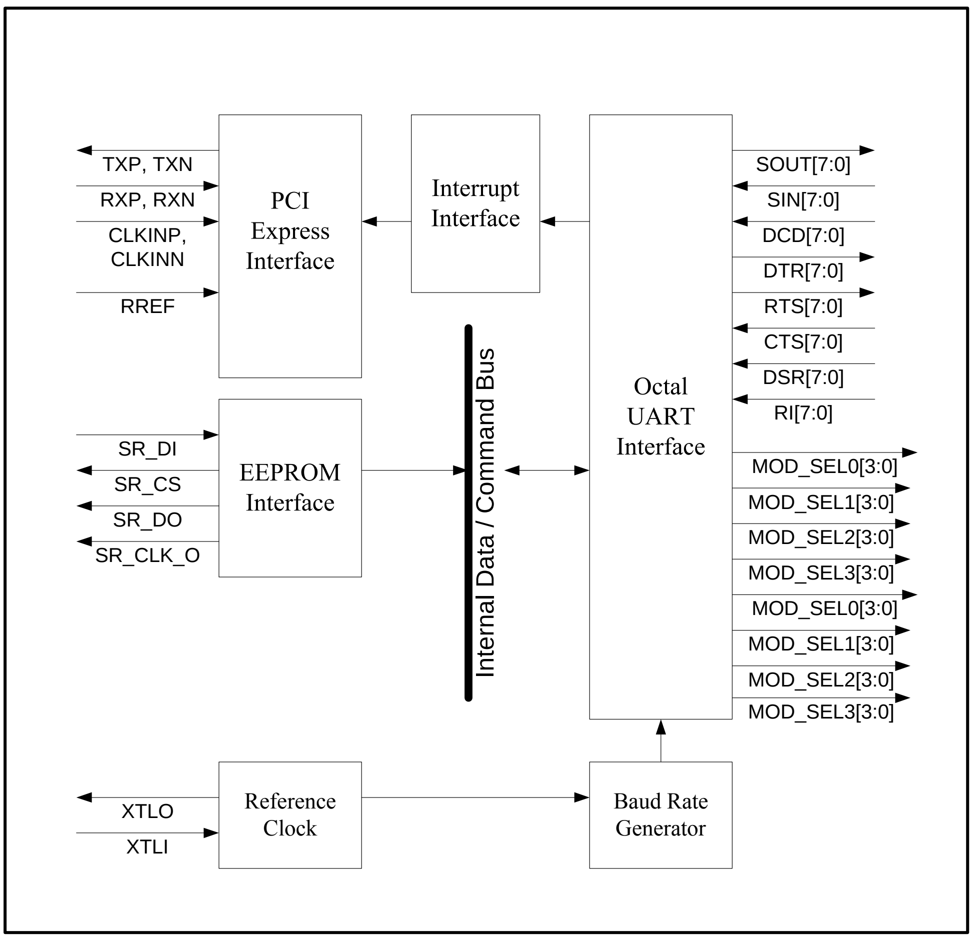

Figure 3-1 PI7C9X7958 Block Diagram

4. PIN ASSIGNMENT

4.1. PIN LIST OF 160-PIN LFBGA

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
A1	SOUT[5]	C13	SOUT[3]	H1	VTT	M3	VDDR
A2	RTS[7]	C14	CTS[2]	H2	VSS	M4	GPIO[2]/DEQ[3]
A3	SOUT[7]	D1	XTLO	H3	VSS	M5	GPIO[5]/RXTERMADJ[0]
A4	RI[6]	D2	XTLI	H4	VDDA	M6	DRIVER_SEL0[3]/DTX[0]
A5	SIN[6]	D3	SCAN_EN	H11	DSR[0]	M7	DRIVER_SEL1[2]/DTX[3]
A6	DTR[6]	D4	CTS[5]	H12	SIN[1]	M8	DRIVER_SEL2[3]
A7	RI[5]	D5	DCD[7]	H13	SOUT[1]/DEBUG_PIN	M9	DRIVER_SEL4[0]
A8	DSR[5]	D6	DTR[7]	H14	RTS[1]/UART_TEST_MODE	M10	DRIVER_SEL5[1]
A9	JTG_TDO	D7	VSS	J1	TXN	M11	VDDR
A10	DCD[4]	D8	DCD[5]	J2	TXP	M12	DRIVER_SEL6[2]
A11	RI[4]	D9	JTG_TMS	J3	VSS	M13	DRIVER_SEL7[3]
A12	SIN[4]	D10	VSS	J4	VDDA	M14	RTS[0]/EEPROM_BYPASS
A13	SOUT[4]	D11	CTS[3]	J11	VSS	N1	PEREST_L
A14	SIN[3]	D12	VDDR	J12	RI[0]	N2	GPIO[0]/DEQ[1]
B1	RTS[5]	D13	DSR[2]	J13	CTS[0]	N3	VSS
B2	RI[7]	D14	DTR[2]	J14	DCD[0]	N4	GPIO[4]/TXTERMADJ[1]
B3	CTS[7]	E1	SR_CS	K1	VDDCAUX	N5	DRIVER_SEL0[0]/HI_DRV
B4	SIN[7]	E2	SR_DO	K2	VSS	N6	DRIVER_SEL1[0]/DTX[1]
B5	DCD[6]	E3	SR_DI	K3	VDDC	N7	DRIVER_SEL1[3]/DEQ[0]
B6	CTS[6]	E4	VSS	K4	VDDA	N8	DRIVER_SEL2[2]
B7	RTS[6]	E11	VSS	K11	DRIVER_SEL7[0]	N9	DRIVER_SEL3[1]
B8	JTG_TRST_L	E12	RTS[3]	K12	DRIVER_SEL7[2]	N10	DRIVER_SEL3[3]
B9	JTG_TDI	E13	SIN[2]	K13	SOUT[0]	N11	DRIVER_SEL5[0]
B10	DSR[4]	E14	RI[1]	K14	SIN[0]	N12	DRIVER_SEL5[3]
B11	DTR[4]	F1	VDDC	L1	RXP	N13	DRIVER_SEL6[0]
B12	RTS[4]	F2	VSS	L2	RXN	N14	DRIVER_SEL7[1]
B13	RI[3]	F3	WAKEUP_L	L3	RREF	P1	TEST
B14	DCD[2]	F4	SR_CLK_O	L4	VDDCAUX	P2	GPIO[1]/DEQ[2]
C1	SIN[5]	F11	DTR[3]	L5	GPIO[6]/RXTERMADJ[1]	P3	GPIO[3]/TXTERMADJ[0]
C2	DTR[5]	F12	RI[2]	L6	DRIVER_SEL0[2]/LO_DRV	P4	GPIO[7]/SR_ORG
C3	VDDR	F13	DCD[1]	L7	VDDC	P5	DRIVER_SEL0[1]/PHY_TM
C4	DSR[7]	F14	DSR[1]	L8	VSS	P6	DRIVER_SEL1[1]/DTX[2]
C5	VDDR	G1	CLKINP	L9	VSS	P7	DRIVER_SEL2[0]
C6	DSR[6]	G2	CLKINN	L10	VSS	P8	DRIVER_SEL2[1]
C7	SOUT[6]	G3	VDDC	L11	DRIVER_SEL6[1]	P9	DRIVER_SEL3[0]
C8	JTG_TCK	G4	VDDA	L12	DRIVER_SEL6[3]	P10	DRIVER_SEL3[2]
C9	CTS[4]	G11	SOUT[2]	L13	VDDC	P11	DRIVER_SEL4[1]
C10	VDDC	G12	RTS[2]	L14	DTR[0]/TEST2	P12	DRIVER_SEL4[2]
C11	DCD[3]	G13	CTS[1]	M1	VSS	P13	DRIVER_SEL4[3]
C12	DSR[3]	G14	DTR[1]	M2	VSS	P14	DRIVER_SEL5[2]

Table 4-1 Pin-List of 160-Pin LFBGA

4.2. PIN DESCRIPTION

4.2.1. UART INTERFACE

PIN NO.	NAME	TYPE	DESCRIPTION
A3, C7, A1, A13, C13, G11, *H13, K13	SOUT [7:0]	O	**UART Serial Data Outputs:** The output pins transmit serial data packets with start and end bits. SOUT[0] and SOUT[1] are output signals with weak internal pull-down resistors. **DEBUG_PIN:** During system initialization, SOUT[1] acts as the DEBUG_IN pin, and it is used to internal debugging used only. In normal operation, it should be low. By default, it is set to '0' without pin strapped.
B4, A5, C1, A12, A14, E13, H12, K14	SIN [7:0]	I	**UART Serial Data Inputs:** The input pins receive serial data packets with start and end bits. The pins are idle high.
D5, B5, D8, A10, C11, B14, F13, J14	DCD [7:0]	I	**Modem Data-Carrier-Detect Input and General Purpose Input (Active Low)**
D6, A6, C2, B11, F11, D14, G14, *L14	DTR [7:0]	O	**Modem Data-Terminal-Ready Output (Active LOW):** If automated DTR# flow control is enabled, the DTR# pin is asserted and deasserted if the receiver FIFO reaches or falls below the programmed thresholds, respectively. DTR[0] and DTR[1] are output signals with weak internal pull-down resistors. **TEST2:** During system initialization, DTR[0] acts as the TEST pin, and it is used for internal debugging used only. In normal operation, it should be low. By default, it is set to '0' without pin strapped.
A2, B7, B1, B12, E12, G12, *H14, *M14	RTS [7:0]	O	**Modem Request-To-Send Output (Active LOW):** If automated RTS# flow control is enabled, the RTS# pin is deasserted and reasserted whenever the receiver FIFO reaches or falls below the programmed thresholds, respectively. RTS[0] and RTS[1] are output signals with weak internal pull-down resistors. **UART_TEST_MODE:** During system initialization, RTS[1] acts as the UART_TEST_MODE pin, and it is used for internal debugging used only. In normal operation, it should be low. By default, it is set to '0' without pin strapped. **EEPROM Bypass:** During system initialization, RTS[0] acts as the EEPROM Bypass pin, and it is used to bypass EEPROM pre-loading. The pin is active-high. When it is asserted at start-up, the EEPROM pre-loading is bypassed, and no configuration data is loaded from the EEPRPOM. Otherwise, configuration data is loaded from the EEPROM.
B3, B6, D4, C9, D11, C14, G13, J13	CTS [7:0]	I	**Modem Clear-To-Send Input (Active LOW):** If automated CTS# flow control is enabled, upon deassertion of the CTS# pin, the transmitter will complete the current character and enter the idle mode until the CTS# pin is reasserted. Note: flow control characters are transmitted regardless of the state of the CTS# pin.
C4, C6, A8, B10, C12, D13, F14, H11	DSR [7:0]	I	**Modem Data-Set-Ready Input (Active LOW):** If automated DSR# flow control is enabled, upon deassertion of the DSR# pin, the transmitter will complete the current character and enter the idle mode until the DSR# pin is reasserted. Note: flow control characters are transmitted regardless of the state of the DSR# pin.
B2, A4, A7, A11, B13, F12, E14, J12	RI [7:0]	I	**Modem Ring-Indicator Input (Active LOW)**
D1	XTLO	O	**Crystal Oscillator Output**

PIN NO.	NAME	TYPE	DESCRIPTION
D2	XTLI	I	**Crystal Oscillator Input Or External Clock Pin:** The maximum frequency supported by this device is 60MHz.
*M6, *L6, *P5, *N5	DRIVER_SEL0 [3:0]	O	**DRIVER_SEL0:** Used to select RS-232/ RS-424/ 4-Wire RS-485/ 2-Wire RS-458 Serial Port Mode for UART 0. DRIVER_SEL0 [3:0] are output signals with weak internal pull-down resistors. **Driver Current Level Control (DTX[0]):** During system initialization, DRIVER_SEL0[3] acts as the DTX[0] pin, and it is used to control the driver current level. By default, it is set to ‘0’ without pin strapped. **Low Driver Control (LO_DRV):** During system initialization, DRIVER_SEL0[2] acts as the LO_DRV pin, and it is used to decrease the nominal value of the PCI Express lane’s driver current level. By default, it is set to ‘0’ without pin strapped. **PHY_TM:** During system initialization, DRIVER_SEL0[1] acts as the PHY_TM pin, and it is used for internal debugging used only. In normal operation, it should be low. By default, it is set to ‘0’ without pin strapped. **High Driver Control (HI_DRV):** During system initialization, DRIVER_SEL0[0] acts as the HI_DRV pin, and it is used to increase the nominal value of the PCI Express lane’s driver current level. By default, it is set ‘0’ without pin strapped.
*N7, *M7, *P6, *N6	DRIVER_SEL1 [3:0]	O	**DRIVER_SEL1:** Used to select RS-232/ RS-424/ 4-Wire RS-485/ 2-Wire RS-458 Serial Port Mode for UART 1. DRIVER_SEL1 [3:0] are output signals with weak internal pull-down resistors. **Driver Equalization Level Control (DEQ[0]):** During system initialization, DRIVER_SEL1[3] acts as the DEQ[0] pin, and it is used to control the driver current level. By default, it is set to ‘0’ without pin strapped. **Driver Current Level Control (DTX[3:1]):** During system initialization, DRIVER_SEL1[2:0] acts as the DTX[3:1] pins, and they are used to control the driver current level. By default, they are set to ‘000’ without pin strapped.
M8, N8, P8, P7	DRIVER_SEL2 [3:0]	O	**DRIVER_SEL2:** Used to select RS-232/ RS-424/ 4-Wire RS-485/ 2-Wire RS-458 Serial Port Mode for UART 2. DRIVER_SEL2[3] is an output signal with a weak internal pull-up resistor, and other DRIVER_SEL2 signals are output signals with internal pull-down resistors.
N10, P10, N9, P9	DRIVER_SEL3 [3:0]	O	**DRIVER_SEL3:** Used to select RS-232/ RS-424/ 4-Wire RS-485/ 2-Wire RS-458 Serial Port Mode for UART 3. DRIVER_SEL3 [3:0] are output signals with weak internal pull-up resistors.
P13, P12, P11, M9	DRIVER_SEL4 [3:0]	O	**DRIVER_SEL4:** Used to select RS-232/ RS-424/ 4-Wire RS-485/ 2-Wire RS-458 Serial Port Mode for UART 4. DRIVER_SEL4 [3:0] are output signals with weak internal pull-up resistors.
N12, P14, M10, N11	DRIVER_SEL5 [3:0]	O	**DRIVER_SEL5:** Used to select RS-232/ RS-424/ 4-Wire RS-485/ 2-Wire RS-458 Serial Port Mode for UART 5. DRIVER_SEL5 [3:0] are output signals with weak internal pull-up resistors.
L12, M12, L11, N13	DRIVER_SEL6 [3:0]	O	**DRIVER_SEL6:** Used to select RS-232/ RS-424/ 4-Wire RS-485/ 2-Wire RS-458 Serial Port Mode for UART 6. DRIVER_SEL6 [3:0] are output signals with weak internal pull-up resistors.
M13, K12, N14, K11	DRIVER_SEL7 [3:0]	O	**DRIVER_SEL7:** Used to select RS-232/ RS-424/ 4-Wire RS-485/ 2-Wire RS-458 Serial Port Mode for UART 7. DRIVER_SEL7 [3:0] are output signals with weak internal pull-up resistors.

4.2.2. PCI EXPRESS INTERFACE

PIN NO.	NAME	TYPE	DESCRIPTION
J2, J1	TXP, TXN	O	**PCI Express Serial Output Signal:** Differential PCI Express output signals.
L1, L2	RXP, RXN	I	**PCI Express Serial Input Signal:** Differential PCI Express input signals.
G1, G2	CLKINP, CLKINN	I	**Reference Input Clock:** Connects to external 100MHz differential clock The input clock signals must be delivered to the clock buffer cell through an AC-coupled interface so that only the AC information of the clock is received, converted, and buffered. It is recommended that a 0.1uF be used in the AC-coupling.
L3	RREF	I	**Reference Resistor:** To accurately set internal bias references, a precision resistor must be connected between **Rref** and **Vss**. The resistor should have a nominal value of 2.1 KΩ and accuracy of +/-1%

4.2.3. SYSTEM INTERFACE

PIN NO.	NAME	TYPE	DESCRIPTION
N1	PEREST_L	I	**System Reset Input**
*P4, *L5, *M5, *N4, *P3, *M4, *P2, *N2	GPIO [7:0]	I/O	**General-Purpose Bi-Direction Signals:** These eight general-purpose pins are programmed as either input-only or bi-directional pins by writing the GPIO output enable control register. GPIO[2] is a bi-directional signal with a weak internal pull-up resistor, and other GPIO pins are bi-directional signals with weak internal pull-down resistors. **EEPROM Organization Pin (SR_ORG):** During system initialization, GPIO[7] acts as the SR_ORG pin, and it is used to select the organization structure of the EEPROM. The pin is active-high. When it is asserted at start-up, the EEPROM configuration data is organized in 16-bit structure. Otherwise, 8-bit structure is used. **Receiver Termination Adjustment (RXTERMADJ[1:0]):** During system initialization, GPIO[6:5] acts as the RXTERMADJ[1:0] pins, and they are used to adjust the receive termination resistor value. By default, they are set to '00' without pin strapped. **Transmit Termination Adjustment (TXTERMADJ[1:0]):** During system initialization, GPIO[4:3] acts as the TXTERMADJ[1:0] pins, and they are used to adjust the transmit termination resistor value. By default, they are set to "00" without pin strapped. **Driver Equalization Level Control (DEQ[3:1]):** During system initialization, GPIO[2:0] acts as the DEQ[3:1] pins, and they are used to control the driver current level. By default, they are set to '100' without pin strapped.
F3	WAKEUP_L	O	**Wakeup Signal (Active LOW):** When the Ring Indicator is received on UART channel 0 in L2 state, the WAKEUP_L is asserted. WAKEUP_L is an output signal with a weak internal pull-down resistor.

4.2.4. TEST SIGNALS

PIN NO.	NAME	TYPE	DESCRIPTION
B9	JTG_TDI	I	**Test Data Input:** When SCAN_EN is high, the pin is used (in conjunction with TCK) to shift data and instructions into the TAP in a serial bit stream. JTG_TDI is an input signal with a weak internal pull-up resistor.
A9	JTG_TDO	O	**Test Data Output:** When SCAN_EN is high, it is used (in conjunction with TCK) to shift data out of the Test Access Port (TAP) in a serial bit stream
D9	JTG_TMS	I	**Test Mode Select:** Used to control the state of the Test Access Port controller. JTG_TMS is an input signal with a weak internal pull-up resistor.
C8	JTG_TCK	I	**Test Clock:** Used to clock state information and data into and out of the chip during boundary scan.
B8	JTG_TRST_L	I	**Test Reset:** Active LOW signal to reset the TAP controller into an initialized state. JTG_TRST_L is an input signal with a weak internal pull-up resistor.
P1	TEST	I	This input signal should be tied to ground during normal operation.
D3	SCAN_EN	I	**Scan Test Enable Pin:** SCAN_EN is an input signal with a weak internal pull-up resistor.

4.2.5. EEPROM INTERFACE

PIN NO.	NAME	TYPE	DESCRIPTION
E1	SR_CS	O	**EEPROM Chip Select:** SR_CS is an output signal with a weak internal pull-up resistor.
E2	SR_DO	O	**EEPROM Data Output:** Serial data output interface to the EEPROM. SR_DO is an output signal with a weak internal pull-up resistor.
E3	SR_DI	I	**EEPROM Data Input:** Serial data input interface to the EEPROM. SR_DI is an input signal with a weak internal pull-up resistor.
F4	SR_CLK_O	O	**EEPROM Clock Output.**

4.2.6. POWER PINS

PIN NO.	NAME	TYPE	DESCRIPTION
C10, F1, G3, K3, L7, L13	VDDC	P	**1.8 V Power Pin:** Used as digital core power pins.
G4, H4, J4, K4	VDDA	P	**1.8 V Power Pin:** Used as analog core power pins.
C3, C5, D12, M3, M11	VDDR	P	**3.3 V Power Pin:** Used as digital I/O power pins.
K1, L4	VDDCAUX	P	**1.8 V Power Pin:** Used as auxiliary power pins.
H1	VTT	P	**1.8V Termination Voltage:** Provides driver termination voltage at transmitter. Should be given the same consideration as VDDCAUX.
D7, D10, E4, E11, F2, H2, H3, J3, J11, K2, L8, L9, L10, M1, M2, N3	VSS	P	**Ground Pin:** Used as ground pins.

5. FUNCTIONAL DESCRIPTION

The PI7C9X7958 is an integrated solution of eight high-performance 16C550 UARTs with one x1 PCI Express host interface. The PCI Express host interface is compliant with the PCI Express Base Specification 1.1, PCI Express CEM Specification 1.1, and PCI Power Management 1.2. In addition, the chip is compliant with the Advanced Configuration Power Interface (ACPI) Specification and the PCI Standard Hot-Plug Controller (SHPC) and Subsystem Specification Revision 1.0. The x1 PCI Express host interface supports up to 2.5 Gbps bandwidth and complete PCI Express configuration register set. The PCI Express interface allows direct access to the configuration and status registers of the UART channels.

The UARTs in the PI7C9X7958 support the complete register set of the 16C550-type devices. The UARTs support Baud Rates up to 15 Mbps in asynchronous mode. Each UART channel has 128-byte deep transmit and receive FIFOs. The high-speed FIFOs reduce CPU utilization and improve data throughput. In addition, the UARTs support enhanced features including automated in-band flow control using programmable Xon/ Xoff in both directions, automated out-band flow control using CTS#/ RTS# and/or DRS#/ DTR#, and arbitrary transmit and receive trigger levels.

5.1. CONFIGURATION SPACE

The PI7C9X7958 has two sets of registers to allow various configuration and status monitoring functions. The PCI Express Configuration Space Registers enable the plug-and-play and auto-configuration when the device is connected to the PCI Express system bus. The UART configuration and internal registers enable the general UART operation functions, status control and monitoring.

5.1.1. PCI Express Configuration Space

The PI7C9X7958 is recognized as a PCI Express endpoint, which is mapped into the configuration space as a single logical device. Each endpoint in the system, including the PI7C9X7958, is part of a Hierarchy Domains originated by the Root Complex, which is a tree with a Root Port at its head in the configuration space. The device configuration registers are implemented for the user to access the functionalities provided by the PCI Express specification. The specification utilizes a flat memory-mapped configuration space to access device configuration registers.

All PCI Express endpoints facilitate a PCI-compatible configuration space to maintain compatibility with PCI software configuration mechanism. PCI Local Bus Specification, Revision 3.0 allocates 256 bytes per device function. PCI Express Base Specification 1.1 extends the configuration space to 4096 bytes to allow enhanced features. The first 256 bytes of the PCI Express Configuration Space are PCI 3.0 compatible region, and the rest of the 4096 bytes are PCI Express Configuration Space. The user can access the PCI 3.0 compatible region either by conventional PCI 3.0 configuration addresses or by the PCI Express memory-mapping addresses. These two types of accesses to the PCI 3.0 compatible region have identical results. The enhanced features in the PCI Express configuration space can only be accessed by PCI Express memory-mapping accesses.

5.1.2. UART Configuration Space

Through the UART registers, the user can control and monitor various functionalities of the UARTs on the PI7C9X7958 including FIFOs, interrupt status, line status, modem status and sample clock. Each of the UART's transmit and receive data FIFOs can be conveniently accessed by reading and writing the registers in the UART configuration space. These registers allow flexible programming capability and versatile device operations of the PI7C9X7958. Each UART is accessed through an 8-byte I/O blocks. The addresses of the UART blocks are offset by the base address referred by the Base Address Register (BAR). The value of the base address is loaded from the I/O or Memory Base Address defined in the PCI Express configuration space.

The PI7C9X7958 also supports enhanced features such as Xon/Xoff, automatic flow control, Baud Rate prescaling and various status monitoring. These enhanced features are available through the memory address offset by the BAR in the PCI Express configuration space.

The basic features available in the registers in I/O mode are also available in the registers in memory-mapping mode. Accesses to these registers are equivalent in these two modes.

The UARTs on the PI7C9X7958 supports operations in 16C450, 16C550 and 16C950 modes. These modes of operation are selected by writing the SFR, FCR and EFR registers. The PI7C9X7958 is backward compatible with these modes of operation.

5.2. DEVICE OPERATION

The PI7C9X7958 is configured by the Root Complex in the bootstrap process during system start-up. The Root Complex performs bus scans and recognizes the device by reading vendor and device IDs. Upon successful device identification, the system then loads device-specific driver software and allocates I/O, memory and interrupt resources. The driver software allows the user to access the functions of the device by reading and writing the UART registers. The PCI Express interface incorporates convenient device operation and high system performance.

5.2.1. Configuration Access

The PI7C9X7958 accepts type 0 configuration read and write accesses defined in the PCI Express Base1.1 Specification. The first 256 bytes of the PCI Express configuration are compatible with PCI 3.0.

5.2.2. I/O Reads/Writes

The PCI Express interface of the PI7C9X7958 decodes incoming transaction packets. If the address is within the region assigned by the I/O Base Address Registers, the transaction is recognized as an I/O Read or Write.

5.2.3. Memory Reads/Writes

Similar to the I/O Read/Write, if the address of the transaction packet is within the memory range, a Memory Read/Write occurs.

5.2.4. Mode Selection

All of the internal UART channels in the I/O Bridge support the 16C450, 16C550, Enhanced 16C550, and Enhanced 950 UART Modes. The mode of the UART operation is selected by toggling the Special Function Register (SFR[5]) and Enhanced Function Register (EFR[4]). The FIFO depth of each mode and the mode selection is tabulated in the table below.

Table 5-1 Mode Selection

UART Mode	SFR[5]	EFR[4]	FIFO Size
450/550	X	0	1/16
Enhanced 550	0	1	128
Enhanced 950	1	1	128

5.2.5. 450/550 Mode

The 450 Mode is inherently supported when 550 Mode is selected. When in the 450 Mode, the FIFOs are in the “Byte Mode”, which refers to the one-byte buffer in the Transmit Holding Register and the Receive Holding Register in each of the UART channels. When in the 550 Mode, the UARTs support an increased FIFO depth of 16.

When EFR[4] is set to “0”, the SFR[5] is ignored, and the 450/550 Mode is selected.

5.2.6. Enhanced 550 Mode

Setting the SFR[5] to “0” and EFR[4] to “1” enables the Enhanced 550 Mode. The Enhanced 550 Mode further increases FIFO depth to 128.

5.2.7. Enhanced 950 Mode

128-deep FIFOs are supported in the Enhanced 950 Mode. When the Enhanced 950 Mode is enabled, the UART channels support additional features:

- Sleep mode
- Special character detection
- Automatic in-band flow control
- Automatic flow control using selectable arbitrary thresholds
- Readable status for automatic in-band and out-of-band flow control
- Flexible clock prescaler
- Programmable sample clock
- DSR/DTR automatic flow control

5.2.8. Transmit and Receive FIFOs

Each channel of the UARTs consists of 128 bytes of transmit FIFOs and 128 bytes of receive FIFOs, namely the Transmit Holding Registers (THR) and the Receive Holding Registers (RHR). The FIFOs provide storage space for the data before they can be transmitted or processed. The THR and RHR operate simultaneously to transmit and read data.

The transmitter reads data from the THR into the Transmit Shift Register (TSR) and removes the data from top of the THR. It then converts the data into serial format with start and stop bits and parity bits if required. If the transmitter completes transmitting the data in the TSR and the THR is empty, the transmitter is in the idle state. The data that arrive most recently are written to the bottom of the THR. If the THR is full, and the user attempts to write data to the THR, a data overrun occurs and the data is lost.

The receiver writes data to the bottom of the RHR when it finishes receiving and decoding the data bits. If the RHR is full when the receiver attempts to write data to it, a data overrun occurs. Any read operation to an empty RHR is invalid.

The empty and full status of the THR and RHR can be determined by reading the empty and full flags in the Line Status Register (LSR). When the transmitter and receiver are ready to transfer data to and from the FIFOs, interrupts are raised to signal this condition. Additionally, the user can use the Receive FIFO Data Counter (RFDC) and Transmit FIFO Data Counter (TFDC) registers to determine the number of items in each FIFO.

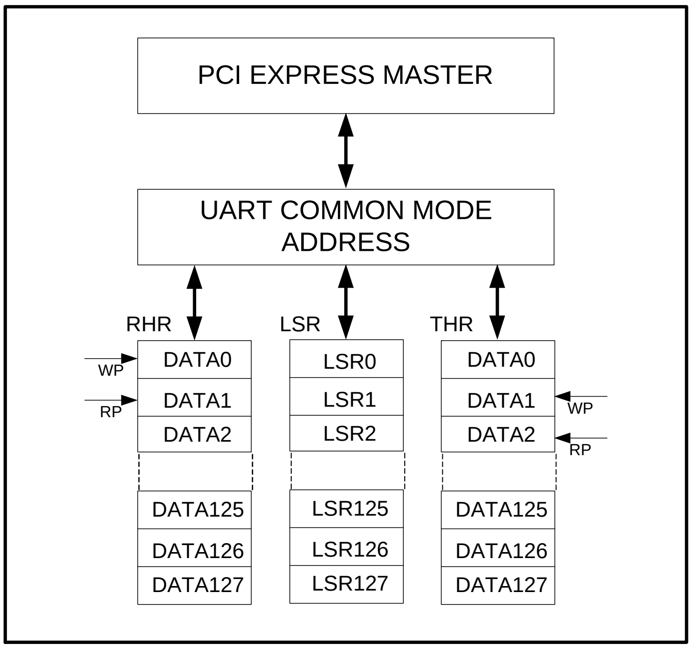

Figure 5-1 Transmit and Receive FIFOs

5.2.9. *Automated Flow Control*

The device uses automatic in-band flow control to prevent data-overrun to the local receive FIFO and remote receive FIFO. This feature works in conjunction with the special character detection. When an XOFF condition is detected, the UART transmitter will suspend any further data transmission after the current character transmission is completed. The transmitter will resume data-transmission as soon as an XON condition is detected. The automatic in-band feature is enabled by the Enhanced Function Register (EFR). EFR[1:0] enables the in-band receive flow control, and EFR[3:2] enables the in-band transmit flow control.

The out-of-band flow control utilizes RTS# and CTS# pins to suspend and resume the data transmission and to prevent data-overrun. An asserted CTS# pin signals the UART to suspend transmission due to a full remote receive FIFO. Upon detecting an asserted CTS# pin, the UART will complete the current character transmission and enters idle mode until the CTS# pin is deasserted.

The UART deasserts RTS# to signal the remote transmitter that the local receive FIFO reaches the programmed upper trigger level. When the local receive FIFO falls below the programmed lower trigger level, the RTS# is reasserted. The automatic out-of-band flow control is enabled by EFR[7:6].

5.2.10. Internal Loopback

The internal loopback capability of the UARTs is enabled by setting Modem Control Register bit-4 (MCR[4]) to 1. When the feature is enabled, the data from the output of the transmit shift register are looped back to the input of the receive shift register. This feature provides the users a way to perform system diagnostics by allowing the UART to receive the same data it is sending.

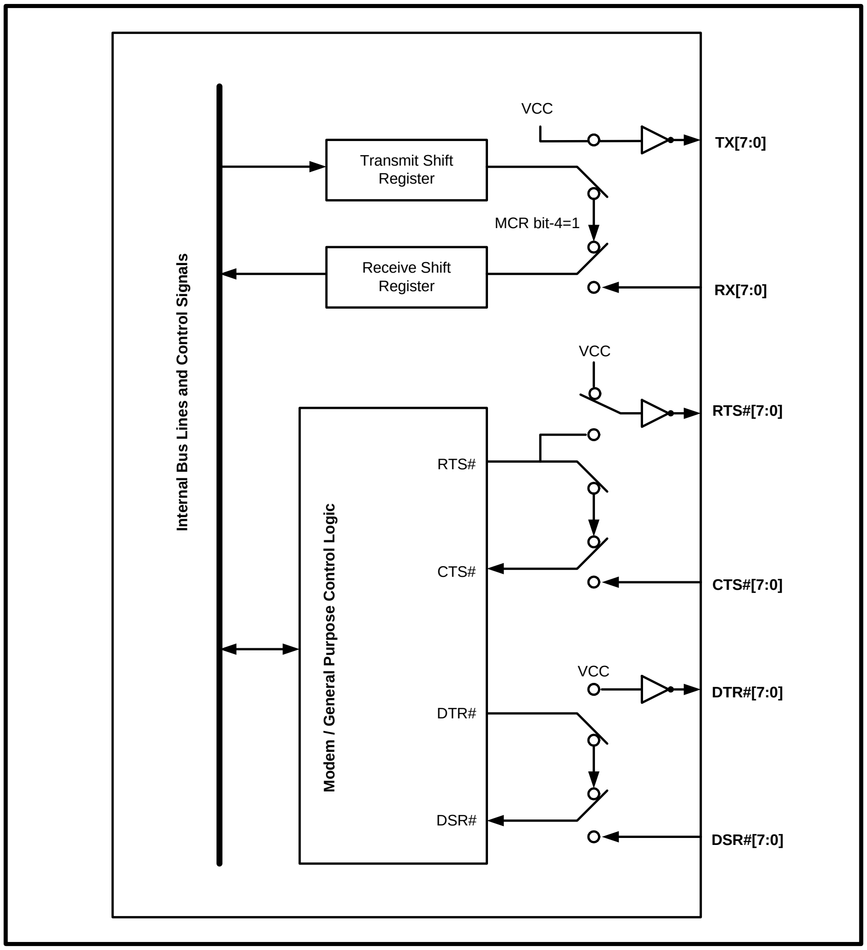

Figure 5-2 Internal Loopback in PI7C9X7958

5.2.11. Crystal Oscillator

The PI7C9X7958 uses a crystal oscillator or an external clock source to provide system clock to the Baud Rate Generator. When a clock source is used, the clock signal should be connected to the XTLI pin, and a 2K pull-up resistor should be connected to the XTLO pin.

When a crystal oscillator is used, the XTLI is the input and XTLO is the output, and the crystal should be connected in parallel with two capacitors.

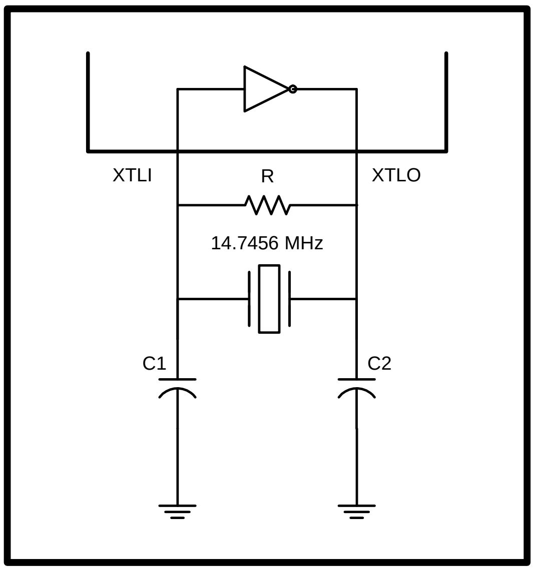

Figure 5-3 Crystal Oscillator as the Clock Source

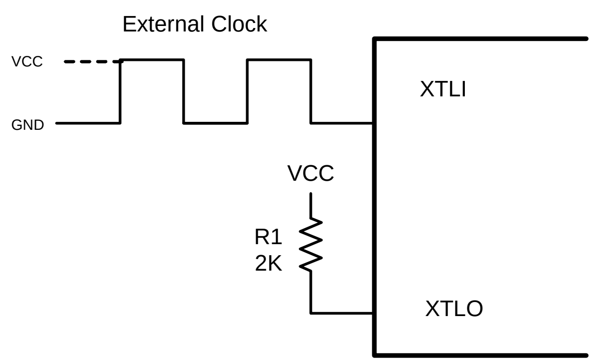

Figure 5-4 External Clock Source as the Clock Source

5.2.12. Baud Rate Generation

The built-in Baud Rate Generator (BRG) allows a wide range of input frequency and flexible Baud Rate generation. To obtain the desired Baud Rate, the user can set the Sample Clock Register (SCR), Divisor Latch Low Register (DLL), Divisor Latch High Register (DLH) and Clock Prescale Registers (CPRM and CPRN). The Baud Rate is generated according to the following equation:

$$BaudRate = \frac{InputFrequency}{Divisor * \Pr escaler}$$

The parameters in the equation above can be programmed by setting the "SCR", "DLL", "DLH", "CPRM" and "CPRN" registers according to the table below.

Table 5-2 Baud Rate Generator Setting

Setting	Description
Divisor	DLL + (256 * DLH)
Prescaler	$2^M * (SampleClock + N)$
SampleClock	$16 - SCR$, (SCR = '0h' to 'Ch')
M	CPRM, (CPRM = '01h' to '02h')
N	CPRN, (CPRN = '0h' to '7h')

To ensure the proper operation of the Baud Rate Generator, users should avoid setting the value '0' to Sample Clock, Divisor and Prescaler.

The following table lists some of the commonly used Baud Rates and the register settings that generate a specific Baud Rate. The examples assume an Input Clock frequency of 14.7456 Mhz. The SCR register is set to '0h', and the CPRM and CPRN registers are set to '1h' and '0h' respectively. In these examples, the Baud Rates can be generated by different combination of the DLH and DLL register values.

Table 5-3 Sample Baud Rate Setting

Baud Rate	DLH	DLL
1,200	3h	00h
2,400	1h	80h
4,800	0h	C0h
9,600	0h	60h
19,200	0h	30h
28,800	0h	20h
38,400	0h	18h
57,600	0h	10h
115,200	0h	08h
921,600	0h	01h

5.2.13. Power Management

The PI7C9X7958 supports the D0, D1, D2 and D3 power states. The device is compliant with PCI Power Management Specification Revision 1.2.

6. PCI EXPRESS REGISTER DESCRIPTION

6.1. REGISTER TYPES

REGISTER TYPE	DEFINITION
HwInt	Hardware Initialization
RO	Read Only
WO	Write Only
RW	Read / Write
RWC	Read / Write 1 to Clear
RWCS	Sticky - Read Only / Write 1 to Clear
RWS	Sticky - Read / Write

6.2. CONFIGURATION REGISTERS

The following table details the allocation of the register fields of the PCI 2.3 compatible type 0 configuration space header.

31 – 24	23 – 16	15 – 8	7 – 0	BYTE OFFSET
Device ID		Vendor ID		00h
Status		Command		04h
Class Code			Revision ID	08h
Reserved	Header Type	Master Latency Timer	Cache Line Size	0Ch
Base Address Register 0				10h
Base Address Register 1				14h
Reserved				18h~28h
Subsystem ID		Subsystem Vendor ID		2Ch
Reserved				30h
Capability Pointer				34h
Reserved				38h
Reserved		Interrupt Pin	Interrupt Line	3Ch
Reserved				40h – 7Fh
Power Management Capabilities		Next ID = 8C	Capability ID = 01	80h
PM Data	PPB Support	Power Management Data		84h
Message Control Register		Next ID =9C	Capability ID = 05	8Ch
Message Address Register				90h
Message Upper Address Register				94h
Message Data Register				98h
VPD Register		Next ID = A4	Capability ID = 03	9Ch
VPD Data Register				A0h
Vendor Define Register(28h)		Next ID = E0	Capability ID = 09	A4h
XPIP CSR0				A8h
XPIP CSR1				ACh
ACK Latency Timer		Replay Time-out counter		B0h
UART Driver Selection				B4h
Power Management Control Parameter				B8h
Debug Register				BCh – C4h
PHY Parameter				C8h
Reserved				CCh – D4h
GPIO Data and Control				D8h
EEPROM Data		EEPROM Control		DCh
PCI Express Capability Register		Next ID = 00h	Capability ID = 10	E0h
Device Capability				E4h
Device Status		Device Control		E8h
Link Capability				ECh

31 – 24	23 – 16	15 – 8	7 – 0	BYTE OFFSET
Link Status		Link Control		F0h
Reserved				F4h - FCh

Other than the PCI 2.3 compatible configuration space header, the I/O bridge also implements PCI express extended configuration space header, which includes advanced error reporting registers. The following table details the allocation of the register fields of PCI express extended capability space header. The first extended capability always begins at offset 100h with a PCI Express Enhanced Capability header and the rest of capabilities are located at an offset greater than 0FFh relative to the beginning of PCI compatible configuration space.

31 – 24	23 – 16	15 – 8	7 – 0	BYTE OFFSET
Next Capability Offset = 000h	Capability Version	PCI Express Extended Capability ID = 001h		100h
Uncorrectable Error Status Register				104h
Uncorrectable Error Mask Register				108h
Uncorrectable Error Severity Register				10Ch
Correctable Error Status Register				110h
Correctable Error Mask Register				114h
Advanced Error Capabilities and Control Register				118h
Header Log Register				11Ch~128h

6.2.1. VENDOR ID REGISTER – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Vendor ID	RO	Identifies Pericom as the vendor of this I/O bridge. The default value may be changed by auto-loading from EEPROM. Reset to 12D8h.

6.2.2. DEVICE ID REGISTER – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	Device ID	RO	Identifies this I/O bridge as the PI7C9X7958. The default value may be changed by auto-loading from EEPROM. Reset to 7958h.

6.2.3. COMMAND REGISTER – OFFSET 04h

BIT	FUNCTION	TYPE	DESCRIPTION
0	I/O Space Enable	RW	Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses. Reset to 0b.
1	Memory Space Enable	RW	Controls a device's response to Memory Space accesses. A value of 0 disables the device response. A value of 1 allows the device to response to memory Space accesses. Reset to 0b.
2	Bus Master Enable	RO	It is not implemented. Hardwired to 0b.
3	Special Cycle Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
4	Memory Write And Invalidate Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
5	VGA Palette Snoop Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
6	Parity Error	RW	Controls the device's response to parity errors. When the bit is set,

BIT	FUNCTION	TYPE	DESCRIPTION
	Response Enable		the device must take its normal action when a parity error is detected. When the bit is 0, the device sets its Detected Parity Error Status bit when an error is detected. Reset to 0b.
7	Wait Cycle Control	RO	Does not apply to PCI Express. Must be hardwired to 0b.
8	SERR# enable	RW	This bit, when set, enables reporting of Non-fatal and Fatal errors detected by the device to the Root Complex. Reset to 0b.
9	Fast Back-to-Back Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
10	Interrupt Disable	RW	Controls the ability of the I/O bridge to generate INTx interrupt Messages. Reset to 0b.
15:11	Reserved	RO	Reset to 00000b.

6.2.4. STATUS REGISTER – OFFSET 04h

BIT	FUNCTION	TYPE	DESCRIPTION
18:16	Reserved	RO	Reset to 000b.
19	Interrupt Status	RO	Indicates that an INTx interrupt Message is pending internally to the device. Reset to 0b.
20	Capabilities List	RO	Set to 1 to enable support for the capability list (offset 34h is the pointer to the data structure) Reset to 1b.
21	66MHz Capable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
22	Reserved	RO	Reset to 0b.
23	Fast Back-to-Back Capable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
24	Master Data Parity Error	RWC	It is not implemented. Hardwired to 0b.
26:25	DEVSEL# Timing	RO	Does not apply to PCI Express. Must be hardwired to 0b.
27	Signaled Target Abort	RWC	Set to 1 (by a completer) whenever completing a request in the I/O bridge side using Completer Abort Completion Status. Reset to 0b.
28	Received Target Abort	RWC	It is not implemented. Hardwired to 0b.
29	Received Master Abort	RWC	It is not implemented. Hardwired to 0b.
30	Signaled System Error	RWC	Set to 1 when the I/O bridge sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Command register is 1. Reset to 0b.
31	Detected Parity Error	RWC	Set to 1 whenever the I/O bridge receives a Poisoned TLP. Reset to 0b.

6.2.5. REVISION ID REGISTER – OFFSET 08h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Revision	RO	Indicates revision number of the I/O bridge. The default value may be changed by auto-loading from EEPROM. Reset to 00h.

6.2.6. CLASS CODE REGISTER – OFFSET 08h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Programming Interface	RO	Read as 02h to indicate no programming interfaces have been defined for PCI-to-PCI bridges
23:16	Sub-Class Code	RO	Read as 00h to indicate device is PCI-to-PCI bridge
31:24	Base Class Code	RO	Read as 07h to indicate device is a bridge device

6.2.7. CACHE LINE REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Cache Line Size	RW	The cache line size register is set by the system firmware and the operating system to system cache line size. This field is implemented by PCI Express devices as a RW field for legacy compatibility purposes but has no impact on any PCI Express device functionality. Reset to 00h.

6.2.8. MASTER LATENCY TIMER REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Latency timer	RO	Does not apply to PCI Express. Must be hardwired to 00h.

6.2.9. HEADER TYPE REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
23:16	Header Type	RO	Read as 00h to indicate that the register layout conforms to the standard PCI-to-PCI bridge layout.

6.2.10. BASE ADDRESS REGISTER 0 – OFFSET 10h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Base Address 0	RW	Use this I/O base address to map the UART 16550 compatible registers. The base address can be allocated to 64 Bytes. Reset to 00000001h.

6.2.11. BASE ADDRESS REGISTER 1 – OFFSET 14h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Base Address 1	RW	Use this memory base address to map the UART 16550 compatible and enhanced registers. The base address can be allocated to 4096 Bytes. Reset to 00000000h

6.2.12. SUBSYSTEM VENDOR REGISTER – OFFSET 2Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Sub Vendor ID	RO	Indicates the sub-system vendor id. The default value may be changed by auto-loading from EEPROM. Reset to 0000h.

6.2.13. SUBSYSTEM ID REGISTER – OFFSET 2Ch

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	Sub System ID	RO	Indicates the sub-system device id. The default value may be changed by auto-loading from EEPROM. Reset to 0000h.

6.2.14. CAPABILITIES POINTER REGISTER – OFFSET 34h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Capabilities Pointer	RO	This optional register points to a linked list of new capabilities implemented by the device. This default value may be changed by auto-loading from EEPROM. The default value is 80h.

6.2.15. INTERRUPT LINE REGISTER – OFFSET 3Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Interrupt Line	RW	Used to communicate interrupt line routing information. POST software will write the routing information into this register as it initializes and configures the system. Reset to 00h.

6.2.16. INTERRUPT PIN REGISTER – OFFSET 3Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Interrupt Pin	RO	Identifies the legacy interrupt Message(s) the device uses. Reset to 01h.

6.2.17. POWER MANAGEMENT CAPABILITY ID REGISTER – OFFSET 80h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Enhanced Capabilities ID	RO	Read as 01h to indicate that these are power management enhanced capability registers.

6.2.18. NEXT ITEM POINTER REGISTER – OFFSET 80h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Item Pointer	RO	The pointer points to the Power Management capability register (8Ch). Reset to 8Ch.

6.2.19. POWER MANAGEMENT CAPABILITIES REGISTER – OFFSET 80h

BIT	FUNCTION	TYPE	DESCRIPTION
18:16	Power Management Revision	RO	Read as 011b to indicate the I/O bridge is compliant to Revision 1.1 of *PCI Power Management Interface Specifications.*
19	PME# Clock	RO	Does not apply to PCI Express. Must be hardwired to 0b.
20	Auxiliary Power	RO	Read as 1b to indicate the I/O bridge forwards the PME# message in D3cold and an auxiliary power source is required.
21	Device Specific Initialization	RO	Read as 0b to indicate the I/O bridge does not have device specific initialization requirements. The default value may be changed by auto-loading from EEPROM.

BIT	FUNCTION	TYPE	DESCRIPTION
24:22	AUX Current	RO	Reset as 111b to indicate the I/O bridge need 375 mA in D3 state. The default value may be changed by auto-loading from EEPROM.
25	D1 Power State Support	RO	Read as 1b to indicate the I/O bridge supports the D1 power management state. The default value may be changed by auto-loading from EEPROM.
26	D2 Power State Support	RO	Read as 1b to indicate the I/O bridge supports the D2 power management state. The default value may be changed by auto-loading from EEPROM.
31:27	PME# Support	RO	Read as 01000b to indicate the I/O bridge supports the forwarding of PME# message in all power states. The default value may be changed by auto-loading from EEPROM.

6.2.20. POWER MANAGEMENT DATA REGISTER – OFFSET 84h

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	Power State	RW	Indicates the current power state of the I/O bridge. Writing a value of D0 causes a hot reset without asserting PEREST_L when the previous state was D3. 00b: D0 state 01b: D1 state 10b: D2 state 11b: D3 hot state Reset to 00b.
2	Reserved	RO	Read as 0b.
3	No_Soft_Reset	RO	When set, this bit indicates that I/O bridge transitioning from D3hot to D0 does not perform an internal reset. When clear, an internal reset is performed when power state transits from D3hot to D0. The default value may be changed by auto-loading from EEPROM. Reset to 0b.
7:4	Reserved	RO	Read as 0h.
8	PME# Enable	RW	When asserted, the I/O bridge will generate the PME# message. Reset to 0b.
12:9	Data Select	RW	Select data registers. Reset to 0h.
14:13	Data Scale	RO	Read as 00b.
15	PME status	RO	Indicates that the PME# message is pending internally to the I/O bridge. Reset to 0b.

6.2.21. PPB SUPPORT EXTENSIONS – OFFSET 84h

BIT	FUNCTION	TYPE	DESCRIPTION
21:16	Reserved	RO	Reset to 000000b.
22	B2_B3 Support for $D3_{HOT}$	RO	Does not apply to PCI Express. Must be hardwired to 0b.
23	Bus Power / Clock Control Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.

6.2.22. PM DATA REGISTER – OFFSET 84h

BIT	FUNCTION	TYPE	DESCRIPTION
31:24	PM Data Register	RO	PM Data Register.

BIT	FUNCTION	TYPE	DESCRIPTION
			Reset to 00h

6.2.23. MESSAGE SIGNALED INTERRUPTS (MSI) Capability ID Register 8Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Enhanced Capability ID	RO	Read as 05h to indicate that this is Message Signaled Interrupt capability register.

6.2.24. MESSAGE SIGNALED INTERRUPTS (MSI) NEXT ITEM POINTER 8Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Item Pointer	RO	The pointer points to the Vendor Specific capability register (9Ch). Reset to 9Ch.

6.2.25. MESSAGE CONTROL REGISTER – OFFSET 8Ch

BIT	FUNCTION	TYPE	DESCRIPTION
16	MSI Enable	RW	0b: The function is prohibited from using MSI to request service 1b: The function is permitted to use MSI to request service and is prohibited from using its INTx # pin Reset to 1'b0.
19:17	Multiple Message Capable	RO	Read as 3'b000.
22:20	Multiple Message Enable	RW	Reset to 3'b000.
23	64-bit address capable	RO	0b: The function is not capable of generating a 64-bit message address 1b: The function is capable of generating a 64-bit message address Reset to 1'b1.
31:24	Reserved	RO	Reset to 8'h00.

6.2.26. MESSAGE ADDRESS REGISTER – OFFSET 90h

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	Reserved	RO	Reset to 00b.
31:2	Message Address	RW	If the message enable bit is set, the contents of this register specify the DWORD aligned address for MSI memory write transaction. Reset to 0.

6.2.27. MESSAGE UPPER ADDRESS REGISTER – OFFSET 94h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Message Upper Address	RW	This register is only effective if the device supports a 64-bit message address is set. Reset to 00000000h.

6.2.28. MESSAGE DATA REGISTER – OFFSET 98h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Message Data	RW	Reset to 0000h.

6.2.29. VPD CAPABILITY ID REGISTER – OFFSET 9Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Enhanced Capabilities ID	RO	Read as 03h to indicate that these are VPD enhanced capability registers.

6.2.30. NEXT ITEM POINTER REGISTER – OFFSET 9Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Item Pointer	RO	The pointer points to the VPD capability register (A4h). Reset to A4h

6.2.31. VPD REGISTER – OFFSET 9Ch

BIT	FUNCTION	TYPE	DESCRIPTION
16	VPD Start	RW	Starts VPD read or write cycle. Assert by software and is de-asserted by hardware. Reset to 0b.
17	VPD Operation	RW	0b: Performs VPD read command to VPD table at the location as specified in VPD address 1b: Performs VPD write command to VPD table at the location as specified in VPD address Reset to 0b.
22:18	VPD Address	RW	Contains DWORD address that is used to generate read or write cycle to the VPD table stored in EEPROM. Reset to 00000b.
31:23	Reserved	RO	Read as 000h.

6.2.32. VPD DATA REGISTER – OFFSET A0h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	VPD Data	RW	When read, it returns the last data read from VPD table at the location as specified in VPD Address. When writes, it places the current data into VPD table at the location as specified in VPD Address. Reset to 00000000h.

6.2.33. VENDOR SPECIFIC CAPABILITY ID REGISTER – OFFSET A4h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Enhanced Capabilities ID	RO	Read as 09h to indicate that these are Vendor Specific capability registers.

6.2.34. NEXT ITEM POINTER REGISTER – OFFSET A4h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Item Pointer	RO	The pointer points to the PCI Express capability register (E0h). Reset to E0h.

6.2.35. LENGTH REGISTER – OFFSET A4h

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	Length Information	RO	The length field provides the information for number of bytes in the capability structure (including the ID and Next pointer bytes). Reset to 28h.

6.2.36. XPIP CSR0 – OFFSET A8h (Test Purpose Only)

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Reserved	RW	Reset to 04001060h.

6.2.37. XPIP CSR1 – OFFSET ACh (Test Purpose Only)

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Reserved	RW	Reset to 004000271h.

6.2.38. REPLAY TIME-OUT COUNTER – OFFSET B0h

BIT	FUNCTION	TYPE	DESCRIPTION
11:0	User Replay Timer	RW	A 12-bit register contains a user-defined value. The default value may be changed by auto-loading from EEPROM. Reset to 000h.
12	Enable User Replay Timer	RW	When asserted, the user-defined replay time-out value would be employed. The default value may be changed by auto-loading from EEPROM. Reset to 0b.
15:13	Reserved	RO	Reset to 000b.

6.2.39. ACKNOWLEDGE LATENCY TIMER – OFFSET B0h

BIT	FUNCTION	TYPE	DESCRIPTION
29:16	User ACK Latency Timer	RW	A 14-bit register contains a user-defined value. The default value may be changed by auto-loading from EEPROM. Reset to 0000h..
30	Enable User ACK Latency	RW	When asserted, the user-defined ACK latency value would be employed. The default value may be changed by auto-loading from EEPROM. Reset to 0b.
31	Reserved	RO	Reset to 0b.

6.2.40. UART DRIVER SETTING – OFFSET B4h

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	UART 0 Transmitter Driver Enable	RW	UART 0 DRIVER. The default value may be changed by auto-loading from EEPROM. 0000b: RS232 0001b: RS422 1011b: RS485-4W 1111b: RS485-2W Reset to 0000b.
7:4	UART 1	RW	UART 1 DRIVER. The default value may be changed by

BIT	FUNCTION	TYPE	DESCRIPTION
	Transmitter Driver Enable		auto-loading from EEPROM. 0000b: RS232 0001b: RS422 1011b: RS485-4W 1111b: RS485-2W Reset to 0000b.
11:8	UART 2 Transmitter Driver Enable	RW	UART 2 DRIVER. The default value may be changed by auto-loading from EEPROM. 0000b: RS232 0001b: RS422 1011b: RS485-4W 1111b: RS485-2W Reset to 0000b.
15:12	UART 3 Transmitter Driver Enable	RW	UART 3 DRIVER. The default value may be changed by auto-loading from EEPROM. 0000b: RS232 0001b: RS422 1011b: RS485-4W 1111b: RS485-2W Reset to 0000b.
19:16	UART 4 Transmitter Driver Enable	RW	UART 4 DRIVER. The default value may be changed by auto-loading from EEPROM. 0000b: RS232 0001b: RS422 1011b: RS485-4W 1111b: RS485-2W Reset to 0000b.
23:20	UART 5 Transmitter Driver Enable	RW	UART 5 DRIVER. The default value may be changed by auto-loading from EEPROM. 0000b: RS232 0001b: RS422 1011b: RS485-4W 1111b: RS485-2W Reset to 0000b.
27:24	UART 6 Transmitter Driver Enable	RW	UART 6 DRIVER. The default value may be changed by auto-loading from EEPROM. 0000b: RS232 0001b: RS422 1011b: RS485-4W 1111b: RS485-2W Reset to 0000b.
31:28	UART 7 Transmitter Driver Enable	RW	UART 7 DRIVER. The default value may be changed by auto-loading from EEPROM. 0000b: RS232 0001b: RS422 1011b: RS485-4W 1111b: RS485-2W Reset to 0000b.

6.2.41. POWER MANAGEMENT CONTROL PARAMENT – OFFSET B8h

BIT	FUNCTION	TYPE	DESCRIPTION
5:0	Power Management Control Parameter	RW	The default value may be changed by auto-loading from EEPROM. Reset to 000001b.
31:6	Reserved	RO	Reset to 0000000h.

6.2.42. DEBUG REGISTER 1 – OFFSET BCh (Test Purpose Only)

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Debug Register 1	RO	Used for test purpose only. Reset to 00000000h.

6.2.43. DEBUG REGISTER 2 – OFFSET C0h (Test Purpose Only)

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Debug Register 2	RO	Used for test purpose only. Reset to 00000000h.

6.2.44. DEBUG REGISTER 3 – OFFSET C4h (Test Purpose Only)

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Debug Register 3	RO	Used for test purpose only. Reset to 00000000h.

6.2.45. DEBUG REGISTER 4 – OFFSET C8h (Test Purpose Only)

BIT	FUNCTION	TYPE	DESCRIPTION
0	Low Driver Current	HwInt	It indicates the status of the strapping pin LODRV. The default value may be changed by auto-loading from EEPROM.
1	High Driver Current	HwInt	It indicates the status of the strapping pin HIDRV. The default value may be changed by auto-loading from EEPROM.
5:2	Driver Transmit Current	HwInt	It indicates the status of the strapping pins DTX[3:0]. The default value may be changed by auto-loading from EEPROM.
9:6	De-emphasis Transmit Equalization	HwInt	It indicates the status of the strapping pins DEQ[3:0]. The default value may be changed by auto-loading from EEPROM.
11:10	Receive Termination Adjustment	HwInt	It indicates the status of the strapping pins RXTRMADJ[1:0]. The default value may be changed by auto-loading from EEPROM.
13:12	Transmit Termination Adjustment	HwInt	It indicates the status of the strapping pins TXTRMADJ[1:0]. The default value may be changed by auto-loading from EEPROM.
31:14	Reserved	RO	Reset to 00000h.

6.2.46. GPIO CONTROL REGISTER – OFFSET D8h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	GPIO Input	RO	The current state of the GPIO[x] pin can be read from bit[x] in this register, where x=7 to 0. The bits are effective only when the corresponding GPIO I/O Enable bits are set to “0”.

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	GPIO I/O Enable	RW	These 8 bits determine whether the GPIO pins are input or output pins. Bit[x+8] corresponds to GPIO[x], where x=7 to 0. If the bit is set to "0", the corresponding GPIO pin is an input pin. If the bit is set to "1", the corresponding GPIO pin is an output pin.
23:16	GPIO Output	RW	The current state of the GPIO[x] pin can be written by bit[x+16] in this register, where x=7 to 0. The bits are effective only when the corresponding GPIO I/O Enable bits are set to "1".
31:24	Reserved	RO	Reserved

6.2.47. EEPROM CONTROL REGISTER – OFFSET DCh

BIT	FUNCTION	TYPE	DESCRIPTION
0	EEPROM Start	RW	Starts the EEPROM read or write cycle. Reset to 0b.
1	Reserved	RO	Reset to 0b.
2	EEPROM Preload Control	RW	Enable preload start. Reset to 0b.
4:3	EEPROM Operation Command	RW	EEPROM Operation Command. 00b: Reserved 01b: Write operation command 10b: Read operation command 11b: Reserved Reset to 00b.
15:5	EEPROM Address	RW	EEPROM RW address. Reset to 000h.
31:16	EEPROM Write DATA Buffer	RW	EEPROM write data buffer register. Reset to 0000h.

6.2.48. PCI EXPRESS CAPABILITY ID REGISTER – OFFSET E0h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Enhanced Capabilities ID	RO	Read as 10h to indicate that these are PCI express enhanced capability registers.

6.2.49. NEXT ITEM POINTER REGISTER – OFFSET E0h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Item Pointer	RO	Read as 00h. No other ECP registers. Reset to 00h.

6.2.50. PCI EXPRESS CAPABILITIES REGISTER – OFFSET E0h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	Capability Version	RO	Read as 0001b to indicate the I/O bridge is compliant to Revision 1.0a of *PCI Express Base Specifications.*
23:20	Device/Port Type	RO	Indicates the type of Legacy PCI Express Endpoint device. Reset to 1h.
24	Slot Implemented	RO	It is not implemented. Hardwired to 0b.
29:25	Interrupt Message Number	RO	It is not implemented. Hardwired to 00000b.
31:30	Reserved	RO	Reset to 00b.

6.2.51. DEVICE CAPABILITIES REGISTER – OFFSET E4h

BIT	FUNCTION	TYPE	DESCRIPTION
2:0	Max_Payload_Size Supported	RO	Indicates the maximum payload size that the I/O bridge can support for TLPs. The I/O bridge supports 128 bytes max payload size. Reset to000b.
4:3	Phantom Functions Supported	RO	It is not implemented. Hardwired to 00b.
5	Extended Tag Field Supported	RO	It is not implemented. Hardwired to 0b.
8:6	Endpoint L0s Acceptable Latency	RO	Acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state. Reset to 000b.
11:9	Endpoint L1 Acceptable Latency	RO	Acceptable total latency that an Endpoint can withstand due to the transition from L1 state to the L0 state. Reset to 000b.
12	Attention Button Present	RO	It is not implemented. Hardwired to 0b.
13	Attention Indicator Present	RO	It is not implemented. Hardwired to 0b.
14	Power Indicator Present	RO	It is not implemented. Hardwired to 0b.
15	Role_Base Error Reporting	RO	When set, indicated that the device implements the functionality originally defined in the Error Reporting ECN. The default value may be changed by auto-loading from EEPROM. Reset to 1b.
17:16	Reserved	RO	Reset to 00b.
25:18	Captured Slot Power Limit Value	RO	In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. This value is set by the Set_Slot_Power_Limit message or hardwired to “00h”. Reset to 00b.
27:26	Captured Slot Power Limit Scale	RO	Specifies the scale used for the Slot Power Limit Value. This value is set by the Set_Slot_Power_Limit message or hardwired to “00b”. Reset to 00b.
31:28	Reserved	RO	Reset to 0h.

6.2.52. DEVICE CONTROL REGISTER – OFFSET E8h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Correctable Error Reporting Enable	RW	0b: Disable Correctable Error Reporting. 1b: Enable Correctable Error Reporting. Reset to 0b.
1	Non-Fatal Error Reporting Enable	RW	0b: Disable Non-Fatal Error Reporting. 1b: Enable Non-Fatal Error Reporting. Reset to 0b.
2	Fatal Error Reporting Enable	RW	0b: Disable Fatal Error Reporting. 1b: Enable Fatal Error Reporting. Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
3	Unsupported Request Reporting Enable	RW	0b: Disable Unsupported Request Reporting. 1b: Enable Unsupported Request Reporting. Reset to 0b.
4	Enable Relaxed Ordering	RO	It is not implemented. Reset to 0b.
7:5	Max_Payload_Size	RW	This field sets maximum TLP payload size for the device. Permissible values that can be programmed are indicated by the Max_Payload_Size Supported in the Device Capabilities register. Any value exceeding the Max_Payload_Size Supported written to this register results into clamping to the Max_Payload_Size Supported value. Reset to 000b.
8	Extended Tag Field Enable	RO	It is not implemented. Hardwired to 0b.
9	Phantom Function Enable	RO	It is not implemented. Hardwired to 0b.
10	Auxiliary (AUX) Power PM Enable	RWS	When set, indicates that the I/O bridge is enabled to draw AUX power independent of PME AUX power. Reset to 0b.
11	Enable No Snoop	RO	It is not implemented. Hardwired to 0b.
14:12	Max_Read_ Request_Size	RO	It is not implemented. Hardwired to 000b.
15	Reserved	RO	Reset to 0b.

6.2.53. *DEVICE STATUS REGISTER – OFFSET E8h*

BIT	FUNCTION	TYPE	DESCRIPTION
16	Correctable Error Detected	RW1C	Asserted when correctable error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.
17	Non-Fatal Error Detected	RW1C	Asserted when non-fatal error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.
18	Fatal Error Detected	RW1C	Asserted when fatal error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.
19	Unsupported Request Detected	RW1C	Asserted when unsupported request is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.
20	AUX Power Detected	RO	Asserted when the AUX power is detected by the I/O bridge Reset to 1b.
21	Transactions Pending	RO	It is not implemented. Hardwired to 0b.
31:22	Reserved	RO	Reset to 000h.

6.2.54. LINK CAPABILITIES REGISTER – OFFSET ECh

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	Maximum Link Speed	RO	Indicates the Maximum Link Speed of the given PCIe Link. Defined encodings are: 0001b, which indicates 2.5 Gb/s Link Reset to 1h.
9:4	Maximum Link Width	RO	Indicates the maximum width of the given PCIe Link. Reset to 000001b (x1).
11:10	Active State Power Management (ASPM) Support	RO	Indicates the level of ASPM supported on the given PCIe Link. The I/O bridge supports L0s and L1 entry. The default value may be changed by auto-loading from EEPROM. Reset to 11b.
14:12	L0s Exit Latency	RO	Indicates the L0s exit latency for the given PCIe Link. The length of time this I/O bridge requires to complete transition from L0s to L0 is in the range of 256ns to less than 512ns. The default value may be changed by auto-loading from EEPROM. Reset to 011b.
17:15	L1 Exit Latency	RO	Indicates the L1 exit latency for the given PCIe Link. The length of time this I/O bridge requires to complete transition from L1 to L0 is in the range of 16us to less than 32us. The default value may be changed by auto-loading from EEPROM. Reset to 000b.
23:18	Reserved	RO	Reset to 00000b.
31:24	Port Number	RO	It is not implemented. Hardwired to 00h.

6.2.55. LINK CONTROL REGISTER – OFFSET F0h

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	Active State Power Management (ASPM) Control	RW	00b: ASPM is Disabled. 01b: L0s Entry Enabled. 10b: L1 Entry Enabled. 11b: L0s and L1 Entry Enabled. Note that the receiver must be capable of entering L0s even when the field is disabled. Reset to 00b.
2	Reserved	RO	Reset to 0h.
3	Read Completion Boundary (RCB)	RO	It is not implemented. Hardwired to 0b.
4	Link Disable	RO	It is not implemented. Hardwired to 0b.
5	Retrain Link	RO	It is not implemented. Hardwired to 0b.
6	Common Clock Configuration	RW	0b: The components at both ends of a link are operating with asynchronous reference clock. 1b: The components at both ends of a link are operating with a distributed common reference clock. Reset to 0b.
7	Extended Synch	RW	When set, it transmits 4096 FTS ordered sets in the L0s state for entering L0 state and transmits 1024 TS1 ordered sets in the L1 state for entering L0 state Reset to 0b.
15:8	RsvdP	RO	Reset to 00h.

6.2.56. LINK STATUS REGISTER – OFFSET F0h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	Link Speed	RO	Indicates the negotiated Link Speed of the given PCIe Link. Defined encodings are: 0001b, which indicates 2.5 Gb/s Link Reset to 1h.
25:20	Negotiated Link Width	RO	Indicates the negotiated width of the given PCIe Link, Reset to 000001b.
26	Training Error	RO	When set, indicates a Link training error occurred. This bit is cleared by hardware upon successful training of the link to the L0 link state. Reset to 0b.
27	Link Training	RO	When set, indicates the link training is in progress. Hardware clears this bit once link training is complete. Reset to 0b.
28	Slot Clock Configuration	RO	It is not implemented. Hardwired to 0b.
31:29	Reserved	RO	Reset to 000b.

6.2.57. PCI EXPRESS ADVANCED ERROR REPORTING CAPABILITY ID REGISTER – OFFSET 100h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Extended Capabilities ID	RO	Read as 0001h to indicate that these are PCI express extended capability registers for advance error reporting.

6.2.58. CAPABILITY VERSION – OFFSET 100h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	Capability Version	RO	Indicates PCI-SIG defined PCI Express capability structure version number. Reset to 1h.

6.2.59. NEXT ITEM POINTER REGISTER – OFFSET 100h

BIT	FUNCTION	TYPE	DESCRIPTION
31:20	Next Capability Offset	RO	Read as 00h. No other ECP registers. Reset to 000h.

6.2.60. UNCORRECTABLE ERROR STATUS REGISTER – OFFSET 104h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Training Error Status	RW1CS	When set, indicates that the Training Error event has occurred. Reset to 0b.
3:1	Reserved	RO	Reset to 000b.
4	Data Link Protocol Error Status	RW1CS	When set, indicates that the Data Link Protocol Error event has occurred. Reset to 0b.
11:5	Reserved	RO	Reset to 0000000b.

BIT	FUNCTION	TYPE	DESCRIPTION
12	Poisoned TLP Status	RW1CS	When set, indicates that a Poisoned TLP has been received or generated. Reset to 0b.
13	Flow Control Protocol Error Status	RW1CS	When set, indicates that the Flow Control Protocol Error event has occurred. Reset to 0b.
14	Completion Timeout Status	RW1CS	When set, indicates that the Completion Timeout event has occurred. Reset to 0b.
15	Completer Abort Status	RW1CS	When set, indicates that the Completer Abort event has occurred. Reset to 0b.
16	Unexpected Completion Status	RW1CS	When set, indicates that the Unexpected Completion event has occurred. Reset to 0b.
17	Receiver Overflow Status	RW1CS	When set, indicates that the Receiver Overflow event has occurred. Reset to 0b.
18	Malformed TLP Status	RW1CS	When set, indicates that a Malformed TLP has been received. Reset to 0b.
19	ECRC Error Status	RW1CS	When set, indicates that an ECRC Error has been detected. Reset to 0b.
20	Unsupported Request Error Status	RW1CS	When set, indicates that an Unsupported Request event has occurred. Reset to 0b.
31:21	Reserved	RO	Reset to 000h.

6.2.61. UNCORRECTABLE ERROR MASK REGISTER – OFFSET 108h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Training Error Mask	RWS	When set, the Training Error event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
3:1	Reserved	RO	Reset to 000b.
4	Data Link Protocol Error Mask	RWS	When set, the Data Link Protocol Error event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
11:5	Reserved	RO	Reset to 0000000b.
12	Poisoned TLP Mask	RWS	When set, an event of Poisoned TLP has been received or generated is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
13	Flow Control Protocol Error Mask	RWS	When set, the Flow Control Protocol Error event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
14	Completion Timeout Mask	RWS	When set, the Completion Timeout event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
15	Completer Abort Mask	RWS	When set, the Completer Abort event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
16	Unexpected Completion Mask	RWS	When set, the Unexpected Completion event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
17	Receiver Overflow Mask	RWS	When set, the Receiver Overflow event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
18	Malformed TLP Mask	RWS	When set, an event of Malformed TLP has been received is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
19	ECRC Error Mask	RWS	When set, an event of ECRC Error has been detected is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
20	Unsupported Request Error Mask	RWS	When set, the Unsupported Request event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
31:21	Reserved	RO	Reset to 000h.

6.2.62. UNCORRECTABLE ERROR SEVERITY REGISTER – OFFSET 10Ch

BIT	FUNCTION	TYPE	DESCRIPTION
0	Training Error Severity	RWS	0b: Non-Fatal. 1b: Fatal. Reset to 1b.
3:1	Reserved	RO	Reset to 000b.
4	Data Link Protocol Error Severity	RWS	0b: Non-Fatal. 1b: Fatal. Reset to 1b.
11:5	Reserved	RO	Reset to 0000000b.
12	Poisoned TLP Severity	RWS	0b: Non-Fatal. 1b: Fatal. Reset to 0b.
13	Flow Control Protocol Error Severity	RWS	0b: Non-Fatal. 1b: Fatal. Reset to 1b.
14	Completion Timeout Error Severity	RWS	0b: Non-Fatal. 1b: Fatal. Reset to 0b.
15	Completer Abort Severity	RWS	0b: Non-Fatal. 1b: Fatal. Reset to 0b.
16	Unexpected Completion Severity	RWS	0b: Non-Fatal. 1b: Fatal. Reset to 0b.
17	Receiver Overflow Severity	RWS	0b: Non-Fatal. 1b: Fatal. Reset to 1b.

BIT	FUNCTION	TYPE	DESCRIPTION
18	Malformed TLP Severity	RWS	0b: Non-Fatal. 1b: Fatal. Reset to 1b.
19	ECRC Error Severity	RWS	0b: Non-Fatal. 1b: Fatal. Reset to 0b.
20	Unsupported Request Error Severity	RWS	0b: Non-Fatal. 1b: Fatal. Reset to 0b.
31:21	Reserved	RO	Reset to 000h .

6.2.63. CORRECTABLE ERROR STATUS REGISTER – OFFSET 110h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Receiver Error Status	RW1CS	When set, the Receiver Error event is detected. Reset to 0b.
5:1	Reserved	RO	Reset to 0h.
6	Bad TLP Status	RW1CS	When set, the event of Bad TLP has been received is detected. Reset to 0b.
7	Bad DLLP Status	RW1CS	When set, the event of Bad DLLP has been received is detected. Reset to 0b.
8	REPLAY_NUM Rollover status	RW1CS	When set, the REPLAY_NUM Rollover event is detected. Reset to 0b.
11:9	Reserved	RO	Reset to 000b.
12	Replay Timer Timeout status	RW1CS	When set, the Replay Timer Timeout event is detected. Reset to 0b.
31:13	Reserved	RO	Reset to 00000h.

6.2.64. CORRECTABLE ERROR MASK REGISTER – OFFSET 114h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Receiver Error Mask	RWS	When set, the Receiver Error event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
5:1	Reserved	RO	Reset to 0h.
6	Bad TLP Mask	RWS	When set, the event of Bad TLP has been received is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
7	Bad DLLP Mask	RWS	When set, the event of Bad DLLP has been received is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
8	REPLAY_NUM Rollover Mask	RWS	When set, the REPLAY_NUM Rollover event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
11:9	Reserved	RO	Reset to 000b.

BIT	FUNCTION	TYPE	DESCRIPTION
12	Replay Timer Timeout Mask	RWS	When set, the Replay Timer Timeout event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
31:13	Reserved	RO	Reset to 00000h .

6.2.65. ADVANCE ERROR CAPABILITIES AND CONTROL REGISTER – OFFSET 118h

BIT	FUNCTION	TYPE	DESCRIPTION
4:0	First Error Pointer	ROS	It indicates the bit position of the first error reported in the Uncorrectable Error Status register. Reset to 00000b.
5	ECRC Generation Capable	RO	When set, it indicates the I/O bridge has the capability to generate ECRC. Reset to 1b.
6	ECRC Generation Enable	RWS	When set, it enables the generation of ECRC when needed. Reset to 0b.
7	ECRC Check Capable	RO	When set, it indicates the I/O bridge has the capability to check ECRC. Reset to 1b.
8	ECRC Check Enable	RWS	When set, the function of checking ECRC is enabled. Reset to 0b.
31:9	Reserved	RO	Reset to 000000h.

6.2.66. HEADER LOG REGISTER – OFFSET From 11Ch to 128h

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	1st DWORD	RO	Hold the 1st DWORD of TLP Header. The Head byte is in big endian.
7:4	2nd DWORD	RO	Hold the 2nd DWORD of TLP Header. The Head byte is in big endian.
11:8	3rd DWORD	RO	Hold the 3rd DWORD of TLP Header. The Head byte is in big endian.
15:12	4th DWORD	RO	Hold the 4th DWORD of TLP Header. The Head byte is in big endian.

7. UART REGISTER DESCRIPTION

7.1. REGISTERS IN I/O MODE

Each UART channel has a dedicated 8-byte register block in I/O mode. The register block can be accessed by the UART I/O Base Address, which is obtained by adding the UART Register Offset to the content of the Base Address Register 0 (BAR0). The following diagram shows the arrangement of individual UART register blocks.

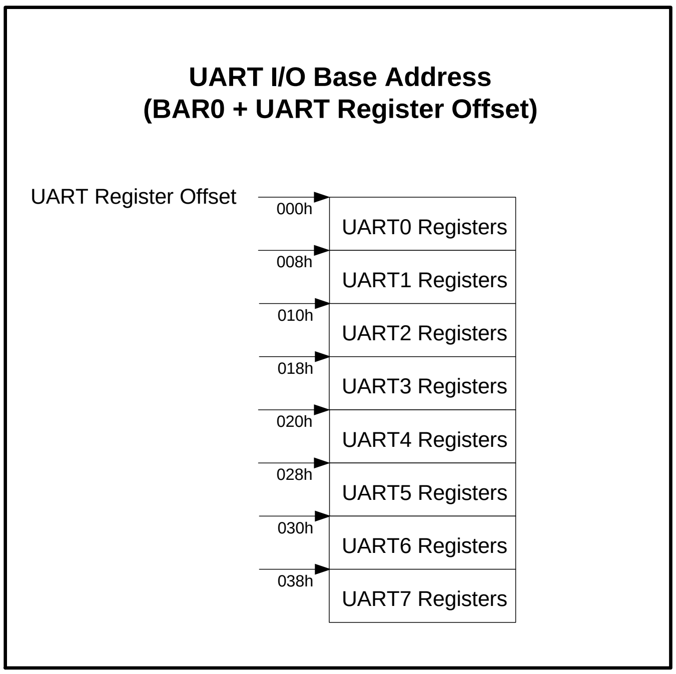

Figure 7-1 UART Register Block Arrangement in I/O Mode

Table 7-1 UART Base Address in I/O Mode

UART	UART I/O Base Address
UART0	BAR0 + 000h
UART1	BAR0 + 008h
UART2	BAR0 + 010h
UART3	BAR0 + 018h
UART4	BAR0 + 020h
UART5	BAR0 + 028h
UART6	BAR0 + 030h
UART7	BAR0 + 038h

Each register in the UART Register Block can be access by adding an offset to the UART I/O Base Address. The following table lists the arrangement of the registers in the UART Register Block in I/O mode.

Table 7-2 Registers in I/O Mode

Offset	Register Name	Mnemonic	Register Type
UART I/O Base Address + 00h	Receive Holding Register	RHR	RO
UART I/O Base Address + 00h	Transmit Holding Register	THR	WO
UART I/O Base Address + 01h	Interrupt Enable Register	IER	RW
UART I/O Base Address + 02h	Interrupt Status Register	ISR	RO
UART I/O Base Address + 02h	FIFO Control Register	FCR	WO
UART I/O Base Address + 03h	Line Control Register	LCR	RW
UART I/O Base Address + 04h	Modem Control Register	MCR	RW
UART I/O Base Address + 05h	Line Status Register	LSR	RO
UART I/O Base Address + 06h	Modem Status Register	MSR	RO
UART I/O Base Address + 07h	Special Function register	SFR	RW
Additional Standard Registers (Required LCR[7] = 1)			
UART I/O Base Address + 00h	Division Latch Low	DLL	RW
UART I/O Base Address + 01h	Division Latch High	DLH	RW
UART I/O Base Address + 02h	Sample Clock Register	SCR	RW

7.1.1. RECEIVE HOLDING REGISTER – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Rx Holding	RO	Data received Reset to 00h.

7.1.2. TRANSMIT HOLDING REGISTER – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Tx Holding	WO	Data to transmit Reset to 00h.

7.1.3. INTERRUPT ENABLE REGISTER – OFFSET 01h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Rx Data Available Interrupt	RW	0b: Disable the Receive Data Ready Interrupt 1b: Enable the Receive Data Ready Interrupt Reset to 0b.
1	Tx Empty Interrupt	RW	0b: Disable the Transmit Holding Register Empty Interrupt 1b: Enable the Transmit Holding Register Empty Interrupt Reset to 0b.
2	Rx Status Interrupt	RW	0b: Disable the Receive Line Status Interrupt 1b: Enable the Receive Line Status Interrupt Reset to 0b.
3	Modem Status Interrupt	RW	0b: Disable the Modem Status Register Interrupt 1b: Enable the Modem Status Register Interrupt Reset to 0b.
4	Xoff/Special character interrupt	RW	0b: Disable the Software Flow Control Interrupt 1b: Enable the Software Flow Control Interrupt Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
5	RTS Interrupt	RW	0b: Disable RTS/DTR Interrupt 1b: Enable RTS/DTR Interrupt Reset to 0b.
6	CTS Interrupt	RW	0b: Disable CTS/DSR interrupt 1b: Enable CTS/DSR interrupt Reset to 0b.
7	Reserved	RW	

7.1.4. INTERRUPT STATUS REGISTER – OFFSET 02h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Interrupt Status	RO	0b: An interrupt is pending 1b: No interrupt pending Reset to C1h.

Priority Level	Interrupt Status Bits								Interrupt Source
	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	
1	1	1	0	0	0	1	1	0	Rx data error
2	1	1	0	0	0	1	0	0	Rx data available
3	1	1	0	0	1	1	0	0	Rx time-out
4	1	1	0	0	0	0	1	0	Tx FIFO empty
5	1	1	0	0	0	0	0	0	Modem status change
6	1	1	0	1	0	0	0	0	Xoff or special character detected
7	1	1	1	0	0	0	0	0	CTS or RTS state changed
X	1	1	0	0	0	0	0	1	No interrupt pending

7.1.5. FIFO CONTROL REGISTER – OFFSET 02h

BIT	FUNCTION	TYPE	DESCRIPTION	
0	FIFO Mode Enable	WO	0b: Disable the FIFO mode 1b: Enable the FIFO mode Reset to 0b.	
1	Rx FIFO Flush	WO	0b: No action 1b: Reset the receive FIFO, self-clear after resetting the FIFO Reset to 0b.	
2	Tx FIFO Flush	WO	0b: No action 1b: Reset the transmit FIFO, self-clear after resetting the FIFO Reset to 0b.	
3	Reserved	WO	Reset to 0b.	
5:4	Tx Trigger Level	WO	In the Enhanced Mode. 00b: 16 01b: 32 10b: 64 11b: 112 Reset to 00b.	
7:6	Rx Trigger Level	WO	In the Non-Enhanced mode 00b: 1 01b: 4 10b: 8 11b: 14	In the Enhanced mode 00b: 15 01b: 31 10b: 63 11b: 111
			Reset to 00b.	

7.1.6. *LINE CONTROL REGISTER – OFFSET 03h*

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>1:0</td><td>Data Length</td><td>RW</td><td>00b: 5-bit data length
01b: 6-bit data length
10b: 7-bit data length
11b: 8-bit data length

Reset to 11b.</td></tr>
<tr><td>2</td><td>Stop-Bit Length</td><td>RW</td><td><table><tr><th>Bit 2 value</th><th>Data length</th><th>Stop bit length</th></tr><tr><td>0</td><td>5,6,7,8</td><td>1</td></tr><tr><td>1</td><td>5</td><td>1.5</td></tr><tr><td>1</td><td>6,7,8</td><td>2</td></tr></table>
Reset to 0b.</td></tr>
<tr><td>5:3</td><td>Parity Type</td><td>RW</td><td><table><tr><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Parity selection</th></tr><tr><td>X</td><td>X</td><td>0</td><td>No parity</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Odd parity</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Even parity</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Mark</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Space</td></tr></table>
Reset to 000b.</td></tr>
<tr><td>6</td><td>Transmission Break</td><td>RW</td><td>0b: No transmit break condition
1b: Force the transmitter output to a space for alerting the remote receiver of a line break condition.

Reset to 0b.</td></tr>
<tr><td>7</td><td>Divisor Latch Enable</td><td>RW</td><td>0b: Data registers are selected
1b: Divisor latch registers are selected

Reset to 0b.</td></tr>
</table>

7.1.7. *MODEM CONTROL REGISTER – OFFSET 04h*

BIT	FUNCTION	TYPE	DESCRIPTION
0	DTR Pin Control	RW	0b: Forces DTR output high 1b: Forces DTR output low Reset to 0b.
1	RTS Pin Control	RW	0b: Forces RTS output high 1b: Forces RTS output low Reset to 0b.
2	Output 1	RW	When the Internal Loopback Mode is enabled by setting Modem Control Register Bit[4], output of the Output1 is routed to RI. Reset to 0b.
3	Output 2	RW	When the Internal Loopback Mode is enabled by setting Modem Control Register Bit[4], output of the Output2 is routed to DCD. Reset to 0b.
4	Internal Loopback Mode	RW	0b: Disables Internal Loopback Mode 1b: Enables Internal Loopback Mode Reset to 0b.

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>5</td><td>AFE</td><td>RW</td><td>Autoflow Control Enable. When the AFE is enabled, autoflow control is enabled. When it is disabled, the diagnostic mode is enabled. In the diagnostic mode, transmitted data is immediately received.

When AFE is set to “1”, MCR Bit 1 is used to enable and disable the auto-RTS.

<table><tr><th>MCR Bit 5 (AFE)</th><th>MCR Bit 1 (RTS)</th><th>Configuration</th></tr><tr><td>1</td><td>1</td><td>Auto-RTS and auto-CTS are enabled (autoflow control enabled).</td></tr><tr><td>1</td><td>0</td><td>Only auto-CTS is enabled.</td></tr><tr><td>0</td><td>x</td><td>Auto-RTS and auto-CTS are disabled.</td></tr></table>
Reset to 0b.</td></tr>
<tr><td>6</td><td>Reserved</td><td></td><td>Reset to 0b.</td></tr>
<tr><td>7</td><td>Enhanced Transmission</td><td>RW</td><td>0b: Insert 1, 1.5 or 2 stop-bits between two transmitted characters.
1b: Insert 0.5 stop-bits between two transmitted characters.

Note: Enabling feature may result in certain compatibility issues. This feature is only recommended when using two Pericom UART devices.

Reset to 0b.</td></tr>
</table>

7.1.8. LINE STATUS REGISTER – OFFSET 05h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Rx Data Available	RO	0b: No data in the receive FIFO 1b: Data in the receive FIFO Reset to 0b.
1	Rx FIFO Overrun	RO	0b: No overrun error 1b: Overrun error Reset to 0b.
2	Rx Parity Error	RO	0b: No parity error 1b: Parity error Reset to 0b.
3	Rx Frame Error	RO	0b: No framing error 1b: Framing error Reset to 0b.
4	Rx Break Error	RO	0b: No break condition 1b: Break condition Reset to 0b.
5	Tx Empty	RO	0b: Tx Holding Register is not empty. 1b: Tx Holding Register is empty. Reset to 0b.
6	Tx Complete	RO	0b: Tx Shift Register is not empty. 1b: Tx Shift Register is empty. Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
7	Rx Data Error	RO	0b: No Rx FIFO error 1b: Rx FIFO error Reset to 0b.

7.1.9. MODEM STATUS REGISTER – OFFSET 06h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Delta CTS	RO	0b: No change in CTS input. 1b: Indicates the CTS input has changed state. This bit is read-clear. Reset to 0b.
1	Delta DSR	RO	0b: No change in DSR input. 1b: Indicates the DSR input has changed state. This bit is read-clear. Reset to 0b.
2	Trailing RI Edge	RO	0b: No change in RI input 1b: Indicates the RI input has changed state from the logic 0 to the logic 1. This bit is read-clear. Reset to 0b.
3	Delta DCD	RO	0b: No change in DCD input 1b: Indicates the DCD input has changed state. This bit is read-clear. Reset to 0b.
4	CTS	RO	0b: The CTS input state is the logic 0 1b: The CTS input state is the logic 1 Reset to 0b.
5	DSR	RO	0b: The DSR input state is the logic 0 1b: The DSR input state is the logic 1 Reset to 0b.
6	RI	RO	The input state of RI pin Reset to 0b.
7	DCD	RO	The input state of DCD pin Reset to 0b.

7.1.10. SPECIAL FUNCTION REGISTER – OFFSET 07h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Force Transmission	RW	Forces transmitter to always to transmit data. 1b: Enabled 0b: Disabled Reset to 0b.
1	Auto DSR and DTR Flow Control	RW	Auto DSR and DTR flow control enable 1b: Enables DSR and DTR auto flow control 0b: Disables DSR and DTR auto flow control Reset to 0b.
2	Reserved	RO	Reset to 0b.
3	Reserved	RO	Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
4	Reserved	RW	Reset to 0b.
5	950 Mode	RW	1b: Enables 950 mode 0b: Non-950 mode Reset to 0b.
6	RFD / LSR Counter Select	RW	1b: OFFSET 15 bit[7:0] acts as the Line Status Register Counter 0b: OFFSET 15 bit[7:0] acts as the Receive FIFO Data Counter Reset to 0b.
7	TFD / SCR Select	RW	1b: OFFSET 16 bit[7:0] acts as the Transmit FIFO Data Counter 0b: OFFSET 16 bit[7:0] acts as the Sample Clock Register Reset to 0b.
7:6	Reserved	RW	Reset to 00b.

7.1.11. DIVISOR LATCH LOW REGISTER – OFFSET 00h, LCR[7] = 1

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Divisor Low	RW	Lower-part of the divisor register Reset to 00h.

7.1.12. DIVISOR LATCH HIGH REGISTER – OFFSET 01h, LCR[7] = 1

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Divisor High	RW	Higher-part of the divisor register Reset to 00h.

7.1.13. SAMPLE CLOCK REGISTER – OFFSET 02h, LCR[7] = 1

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	Sample Clock	RW	This register determines the Sample Clock value (SC) used in the Baud Rate Generator. Please refer to 5.2.12 Baud Rate Generation for more detail 0000b: SC = 16 / 0101b: SC = 11 / 1010b: SC = 6 0001b: SC = 15 / 0110b: SC = 10 / 1011b: SC = 5 0010b: SC = 14 / 0111b: SC = 9 / 1100b: SC = 4 0011b: SC = 13 / 1000b: SC = 8 / Other settings are 0100b: SC = 12 / 1001b: SC = 7 / reserved. Reset to 0h.
7:4	Reserve	R	Reset to 0h.

7.2. REGISTERS IN MEMORY-MAPPING MODE

Each UART channel has a dedicated 512-byte register block in Memory mode. The register block can be accessed by the UART Memory Base Address, which is obtained by adding the UART Register Offset to the content of the Base Address Register 1 (BAR1). The following diagram shows the arrangement of individual UART register blocks.

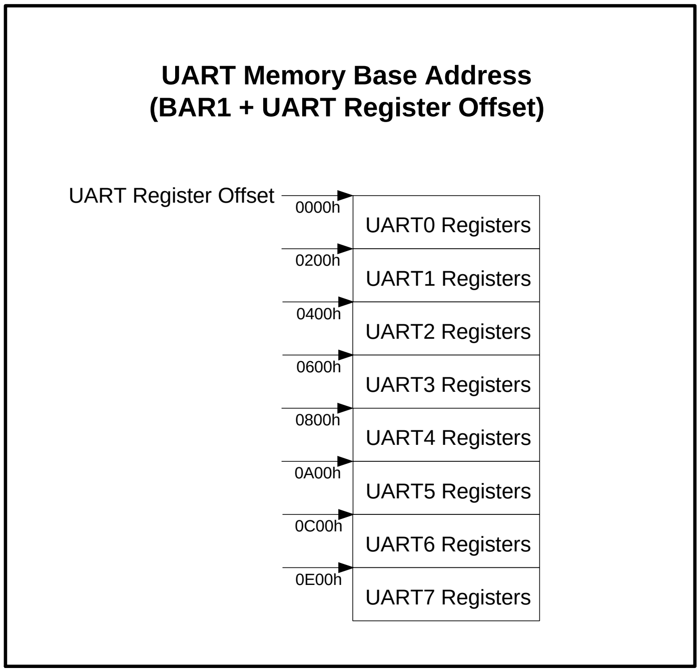

Figure 7-2 UART Register Block Arrangement in Memory Mode

Table 7-3 UART Base Address in Memory Mode

UART	UART I/O Base Address
UART0	BAR1 + 0000h
UART1	BAR1 + 0200h
UART2	BAR1 + 0400h
UART3	BAR1 + 0600h
UART4	BAR1 + 0800h
UART5	BAR1 + 0A00h
UART6	BAR1 + 0C00h
UART7	BAR1 + 0E00h

Each register in the UART Register Block can be access by adding an offset to the UART Memory Base Address. The following table lists the arrangement of the registers in the UART Register Block in memory mode.

Table 7-4 Memory-Map mode

Offset	Register Name	Mnemonic	Register Type
UART Memory Base Address + 00h	Receive Holding Register	RHR	RO
UART Memory Base Address + 00h	Transmit Holding Register	THR	WO
UART Memory Base Address + 01h	Interrupt Enable Register	IER	RW
UART Memory Base Address + 02h	Interrupt Status Register	ISR	RO
UART Memory Base Address + 02h	FIFO Control Register	FCR	WO
UART Memory Base Address + 04h	Line Control Register	LCR	RW
UART Memory Base Address + 04h	Modem Control Register	MCR	RW
UART Memory Base Address + 05h	Line Status Register	LSR	RO
UART Memory Base Address + 06h	Modem Status Register	MSR	RO
UART Memory Base Address + 07h	Special Function Register	SFR	RW
UART Memory Base Address + 08h	Divisor Latch Low	DLL	WO
UART Memory Base Address + 09h	Divisor Latch High	DLH	WO
UART Memory Base Address + 0Ah	Enhanced Function Register	EFR	RW
UART Memory Base Address + 0Bh	XON 1 Character/Special Character 1	XON1	RW
UART Memory Base Address + 0Ch	XON 2 Character/Special Character 2	XON2	RW
UART Memory Base Address + 0Dh	XOFF 1 Character/Special Character 3	XOFF1	RW
UART Memory Base Address + 0Eh	XOFF 2 Character/Special Character 3	XOFF2	RW
UART Memory Base Address + 0Fh	Advanced Status Register	ASR	RW
UART Memory Base Address + 10h	Transmitter Interrupt Trigger Level	TTL	RW
UART Memory Base Address + 11h	Receiver Interrupt Trigger Level	RTL	RW
UART Memory Base Address + 12h	Automatic Flow control lower trigger level	FCL	RW
UART Memory Base Address + 13h	Automatic Flow control lower higher level	FCH	RW
UART Memory Base Address + 14h	Baud rate Prescale	CPR	RW
UART Memory Base Address + 15h	Receive FIFO Data Counter / Line Status Register Counter	RFD / LSR Counter	RO
UART Memory Base Address + 16h	Transmit FIFO Data Counter / Sample Clock Register	TFD Counter / SCR	RW
UART Memory Base Address + 17h	Global Register of LSR	GLSR	RW
UART Memory Base Address + 100h ~17Fh	UART0 FIFO DATA Register. Use this register to map FIFO data content.	FIFO_D	RW
UART Memory Base Address + 180h ~1FFh	UART0 FIFO DATA LSR Register. Use this register to map FIFO data relative LSR content.	FIFO_LSR	RW

7.2.1. RECEIVE HOLDING REGISTER – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Rx Holding	RO	When data are read from the Receive Holding Register (RHR), they are removed from the top of the receiver's associated FIFOs, which holds a queue of data received by the receiver. Data read from the RHR when the FIFOs are empty are invalid. The Line Status Register (LSR) indicates the full or empty status of the FIFOs. Reset to 00h.

7.2.2. TRANSMIT HOLDING REGISTER – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Tx Holding	WO	When data are written to the Transmit Holding Register (THR), they are written to the bottom of the transmitter's associated FIFOs, which holds a queue of data to be transmitted by the transmitter. Data written to the THR when the FIFOs are full are lost. The Line Status Register (LSR) indicates the full or empty status of the FIFOs. Reset to 00h.

7.2.3. INTERRUPT ENABLE REGISTER – OFFSET 01h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Rx Data Available Interrupt	RW	0b: Disable the Receive Data Ready Interrupt 1b: Enable the Receive Data Ready Interrupt Reset to 0b.
1	Tx Empty Interrupt	RW	0b: Disable the Transmit Holding Register Empty Interrupt 1b: Enable the Transmit Holding Register Empty Interrupt Reset to 0b.
2	Rx Error Status	RW	0b: Disable the Receive Line Status Interrupt 1b: Enable the Receive Line Status Interrupt Reset to 0b.
3	Modem Status Interrupt	RW	0b: Disable the Modem Status Register Interrupt 1b: Enable the Modem Status Register Interrupt Reset to 0b.
4	Xoff/Special character interrupt	RW	0b: Disable the Software Flow Control Interrupt 1b: Enable the Software Flow Control Interrupt Reset to 0b.
5	RTS Interrupt	RW	0b: Disable RTS/DTR Interrupt 1b: Enable RTS/DTR Interrupt Reset to 0b.
6	CTS Interrupt	RW	0b: Disable CTS/DSR interrupt 1b: Enable CTS/DSR interrupt Reset to 0b.
7	Reserved	RW	Reset to 0b.

7.2.4. INTERRUPT STATUS REGISTER – OFFSET 02h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Interrupt Status	RO	0b: An interrupt is pending 1b: No interrupt pending Reset to C1h.

Priority Level	Interrupt Status Bits								Interrupt Source
	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	
1	1	1	0	0	0	1	1	0	Rx data error
2	1	1	0	0	0	1	0	0	Rx data available
3	1	1	0	0	1	1	0	0	Rx time-out
4	1	1	0	0	0	0	1	0	Tx FIFO empty
5	1	1	0	0	0	0	0	0	Modem status change
6	1	1	0	1	0	0	0	0	Xoff or special character detected
7	1	1	1	0	0	0	0	0	CTS or RTS state changed
X	1	1	0	0	0	0	0	1	No interrupt pending

7.2.5. FIFO CONTROL REGISTER – OFFSET 02h

BIT	FUNCTION	TYPE	DESCRIPTION	
0	FIFO Mode Enable	WO	0b: Disable the FIFO mode 1b: Enable the FIFO mode Reset to 0b.	
1	Rx FIFO Flush	WO	0b: No action 1b: Reset the receive FIFO, self-clear after resetting the FIFO Reset to 0b.	
2	Tx FIFO Flush	WO	0b: No action 1b: Reset the transmit FIFO, self-clear after resetting the FIFO Reset to 0b.	
3	Reserved	WO	Reset to 0b	
5:4	Tx Trigger Level	WO	In the Enhanced Mode: 00b: 16 01b: 32 10b: 64 11b: 112 Reset to 00b.	
7:6	Rx Trigger Level	WO	In the Non-Enhanced mode 00b: 1 01b: 4 10b: 8 11b: 14	In the Enhanced mode 00b: 15 01b: 31 10b: 63 11b: 111
			Reset to 00b.	

7.2.6. LINE CONTROL REGISTER – OFFSET 03h

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	Data Length	RW	00b: 5-bit data length 01b: 6-bit data length 10b: 7-bit data length 11b: 8-bit data length Reset to 00b.

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>2</td><td>Stop-Bit Length</td><td>RW</td><td><table><tr><td>Bit 2 value</td><td>Data length</td><td>Stop bit length</td></tr><tr><td>0</td><td>5,6,7,8</td><td>1</td></tr><tr><td>1</td><td>5</td><td>1.5</td></tr><tr><td>1</td><td>6,7,8</td><td>2</td></tr></table>
Reset to 0b.</td></tr>
<tr><td>5:3</td><td>Parity Type</td><td>RW</td><td><table><tr><td>Bit 5</td><td>Bit 4</td><td>Bit 3</td><td>Parity selection</td></tr><tr><td>X</td><td>X</td><td>0</td><td>No parity</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Odd parity</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Even parity</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Mark</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Space</td></tr></table>
Reset to 000b.</td></tr>
<tr><td>6</td><td>Transmission Break</td><td>RW</td><td>0b: No transmit break condition
1b: Force the transmitter output to a space for alerting the remote receiver of a line break condition.

Reset to 0b.</td></tr>
<tr><td>7</td><td>Divisor Latch Enable</td><td>RW</td><td>0b: Data registers are selected
1b: Divisor latch registers are selected

Reset to 0b.</td></tr>
</table>

7.2.7. MODEM CONTROL REGISTER – OFFSET 04h

BIT	FUNCTION	TYPE	DESCRIPTION
0	DTR Pin Control	RW	0b: Forces DTR output high 1b: Forces DTR output low Reset to 0b.
1	RTS Pin Control	RW	0b: Forces RTS output high 1b: Forces RTS output low Reset to 0b.
2	Output 1	RW	When the Internal Loopback Mode is enabled by setting Modem Control Register Bit[4], output of the Output1 is routed to RI. Reset to 0b.
3	Output 2	RW	When the Internal Loopback Mode is enabled by setting Modem Control Register Bit[4], output of the Output2 is routed to DCD. Reset to 0b.
4	Internal Loopback Mode	RW	0b: Disables Internal Loopback Mode 1b: Enables Internal Loopback Mode Reset to 0b.

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>5</td><td>AFE</td><td>RW</td><td>Autoflow Control Enable. When the AFE is enabled, autoflow control is enabled. When it is disabled, the diagnostic mode is enabled. In the diagnostic mode, transmitted data is immediately received.

When AFE is set to “1”, MCR Bit 1 is used to enable and disable the auto-RTS.

<table>
<tr><th>MCR Bit 5 (AFE)</th><th>MCR Bit 1 (RTS)</th><th>Configuration</th></tr>
<tr><td>1</td><td>1</td><td>Auto-RTS and auto-CTS are enabled (autoflow control enabled).</td></tr>
<tr><td>1</td><td>0</td><td>Only auto-CTS is enabled.</td></tr>
<tr><td>0</td><td>x</td><td>Auto-RTS and auto-CTS are disabled.</td></tr>
</table>

Reset to 0b.</td></tr>
<tr><td>6</td><td>Reserved</td><td></td><td>Reset to 0b.</td></tr>
<tr><td>7</td><td>Enhanced Transmission</td><td>RW</td><td>0b: Insert 1, 1.5 or 2 stop-bits between two transmitted characters.
1b: Insert 0.5 stop-bits between two transmitted characters.

Note: Enabling feature may result in certain compatibility issues. This feature is only recommended when using two Pericom UART devices.

Reset to 0b.</td></tr>
</table>

7.2.8. LINE STATUS REGISTER – OFFSET 05h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Rx Data Available	RO	0b: No data in the receive FIFO 1b: Data in the receive FIFO Reset to 0b.
1	Rx FIFO Overrun	RO	0b: No overrun error 1b: Overrun error Reset to 0b.
2	Rx Parity Error	RO	0b: No parity error 1b: Parity error Reset to 0b.
3	Rx Frame Error	RO	0b: No framing error 1b: Framing error Reset to 0b.
4	Rx Break Error	RO	0b: No break condition 1b: Break condition Reset to 0b.
5	Tx Empty	RO	0b: Tx Holding Register is not empty. 1b: Tx Holding Register is empty. Reset to 0b.
6	Tx Complete	RO	0b: Tx Shift Register is not empty. 1b: Tx Shift Register is empty. Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
7	Rx Data Error	RO	0b: No Rx FIFO error 1b: Rx FIFO error Reset to 0b.

7.2.9. MODEM STATUS REGISTER – OFFSET 06h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Delta CTS	RO	0b: No change in CTS input. 1b: Indicates the CTS input has changed state. This bit is read-clear. Reset to 0b.
1	Delta DSR	RO	0b: No change in DSR input. 1b: Indicates the DSR input has changed state. This bit is read-clear. Reset to 0b.
2	Delta RI	RO	0b: No change in RI input 1b: Indicates the RI input has changed state from the logic 0 to the logic 1. This bit is read-clear. Reset to 0b.
3	Delta DCD	RO	0b: No change in DCD input 1b: Indicates the DCD input has changed state. This bit is read-clear. Reset to 0b.
4	CTS	RO	0b: The CTS input state is the logic 0 1b: The CTS input state is the logic 1 Reset to 0b.
5	DSR	RO	0b: The DSR input state is the logic 0 1b: The DSR input state is the logic 1 Reset to 0b.
6	RI	RO	The input state of RI pin Reset to 0b.
7	DCD	RO	The input state of DCD pin Reset to 0b.

7.2.10. SPECIAL FUNCTION REGISTER – OFFSET 07h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Force Transmission	RW	Forces transmitter to always to transmit data. 1b: Enabled 0b: Disabled Reset to 0b.
1	Auto DSR and DTR Flow Control	RW	Auto DSR and DTR flow control enable 1b: Enables DSR and DTR auto flow control 0b: Disables DSR and DTR auto flow control Reset to 0b.
2	Reserved	RO	Reset to 0b.
3	Reserved	RO	Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
4	Reserved	RW	Reset to 0b.
5	950 Mode	RW	1b: Enables 950 mode 0b: Non-950 mode Reset to 0b.
6	RFD / LSR Counter Select	RW	1b: OFFSET 15 bit[7:0] acts as the Line Status Register Counter 0b: OFFSET 15 bit[7:0] acts as the Receive FIFO Data Counter Reset to 0b.
7	TFD / SCR Select	RW	1b: OFFSET 16 bit[7:0] acts as the Transmit FIFO Data Counter 0b: OFFSET 16 bit[7:0] acts as the Sample Clock Register Reset to 0b.

7.2.11. DIVISOR LATCH LOW REGISTER – OFFSET 08h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Divisor Low	RW	Lower-part of the divisor register Reset to 00h.

7.2.12. DIVISOR LATCH HIGH REGISTER – OFFSET 09h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Divisor High	RW	Higher-part of the divisor register Reset to 00h.

7.2.13. ENHANCED FUNCTION REGISTER – OFFSET 0Ah

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	In-Band Receive Flow Control Mode	RW	When in-band receive flow control is enabled, the UART compares the received data with the programmed XOFF character(s). When this occurs, the UART will disable transmission as soon as any current character transmission is complete. The UART then compares the received data with the programmed XON character(s). When a match occurs, the UART will re-enable transmission (see section 7.11.6). 00b: In-band receive flow control is disabled. 01b: Single character in-band receive flow control enabled, recognising XON2 as the XON character and XOFF2 as the XOFF character. 10b: Single character in-band receive flow control enabled, recognising XON1 as the XON character and XOFF1 and the XOFF character. 11b: The behavior of the receive flow control is dependent on the configuration of EFR[3:2]. Single character in-band receive flow control is enabled, accepting XON1 or XON2 as valid XON characters and XOFF1 or XOFF2 as valid XOFF characters when EFR[3:2] = “01” or “10”. EFR[1:0] should not be set to “11” when EFR[3:2] is ‘00’. Reset to 00b.
3:2	In-Band Transmit Flow Control Mode	RW	When in-band transmit flow control is enabled, XON/XOFF character are inserted into the data stream whenever the RFL passes the upper trigger level and falls below the lower trigger level respectively. For automatic in-band flow control, bit 4 of EFR must be set. The combinations of software transmit flow control can then be selected by programming EFR[3:2] as follows.

BIT	FUNCTION	TYPE	DESCRIPTION
			00b: In-band transmit flow control is disabled logic. 01b: Single character in-band transmit flow control enabled, using XON2 as the XON character and XOFF2 as the XOFF character. 10b: Single character in-band transmit flow control enabled, using XON1 as the XON character and XOFF1 as the XOFF character. 11b: The value EFR[3:2] = "11" is reserved for future use and should not be used Reset to 00b.
4	Enhanced Mode	RW	0b: Non-Enhanced mode. 1b: Enhanced mode. Enables the Enhanced Mode functions. If use addition function except 16550 mode. Reset to 0b.
5	Special Character Detection Enable	RW	0b: Special character detection is disabled. 1b: While in Enhanced mode (EFR[4]=1), the UART compares the incoming receiver data with the XOFF1 or XOFF2 value and interrupt will be asserted. If In-Band Flow Control is enabled, this bit must be set to '1'. Reset to 0b.
6	Automatic RTS Flow Control Enable	RW	0b: RTS flow control is disabled. 1b: RTS flow control is enabled in Enhanced mode (i.e. EFR[4] = 1), where the RTS# pin will be forced inactive high if the RFL reaches the upper flow control threshold. This will be released when the RFL drops below the lower threshold. 650 and 950-mode drivers should use different threshold level. Reset to 0b.
7	Automatic CTS Flow Control Enable	RW	0b: CTS flow control is disabled (default). 1b: CTS flow control is enabled in Enhanced mode (i.e. EFR[4] = 1), where the data transmission is prevented whenever the CTS# pin is held inactive high. 650 and 950-mode drivers should use different threshold level. Reset to 0b.

7.2.14. XON SPECIAL CHARACTER 1 – OFFSET 0Bh

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	XON1	RW	Xon character 1. Reset to 00h.

7.2.15. XON SPECIAL CHARACTER 2 – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	XON2	RW	Xon character 2. Reset to 00h.

7.2.16. XOFF SPECIAL CHARACTER 1 – OFFSET 0Dh

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	XOFF1	RW	Xoff character 1. Reset to 00h.

7.2.17. XOFF SPECIAL CHARACTER 2 – OFFSET 0Eh

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	XOFF2	RW	Xoff character 2. Reset to 00h.

7.2.18. ADVANCE CONTROL REGISTER – OFFSET 0Fh

BIT	FUNCTION	TYPE	DESCRIPTION
0	Transmitter Terminate Condition	RO	Indicates current transmitter terminate condition. If transmitter is disabled by remote terminate, the condition can be shown by this bit. 1b: Disabled by remote terminate. 0b: The transmitter can transmit data normally. Reset to 0b.
1	Remote TX Disable	RO	Remote TX Disable. 1b: If transmitter has sent XOFF message or RTS message, then DTR is inactive, and then it is enabled. 0b: otherwise Reset to 0b.
2	Xon/Xoff Detect	RO	When receiving a XON/XOFF character from a remote transmitter, this bit is set to '1'. Otherwise, this bit is set to '0'. The bit is read-clear. If the Xoff/Special Character Interrupt is enabled, the Xoff Detect status is also reflected in the Interrupt Status Register (Priority Level 6). 1b: Event true 0b: Event false Reset to 0b.
3	Special Character Detect	RO	When detecting the special characters from a remote transmitter, this bit is set to '1'. Otherwise, this bit is set to '0'. The bit is read-clear. If the Xoff/Special Character Interrupt is enabled, the status is also reflected in the Interrupt Status Register (Priority Level 6). 1b: Event true 0b: Event false Reset to 0b.
7:4	Reserved	RO	Reset to 0000b.

7.2.19. TRANSMIT INTERRUPT TRIGGER LEVEL – OFFSET 10h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	TTL	RW	Transmitter Interrupt Trigger Level. Reset to 00h.

7.2.20. RECEIVE INTERRUPT TRIGGER LEVEL – OFFSET 11h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	RTL	RW	Receiver Interrupt Trigger Level. Reset to 00h.

7.2.21. FLOW CONTROL LOW TRIGGER LEVEL – OFFSET 12h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	FCL	RW	Automatic Flow Control Low Trigger Level. Reset to 00h.

7.2.22. FLOW CONTROL HIGH TRIGGER LEVEL – OFFSET 13h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	FCH	RW	Automatic Flow Control High Trigger Level. Reset to 00h.

7.2.23. CLOCK PRESCALE REGISTER – OFFSET 14h

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	CPRN	RW	N number in calculating the Prescaler, which is used to generate the Baud Rate. Reset to 0000b.
7:4	CPRM	RW	M number in calculating the Prescaler, which is used to generate the Baud Rate. It is recommended that the value of the CPRM be set to “0000”, “0001 or “0010”. Reset to 0000b.

7.2.24. RECEIVE FIFO DATA COUNTER – OFFSET 15h, SFR[6] = 0

The function of this register is selected by the Special Function Register (Offset 07h) bit 6. When SFR[6] is set to ‘1’, this register functions as the Receive FIFO Data Counter. Otherwise, it functions as the Line Status Register Counter.

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Receive FIFO Data Counter	RO	The Receive FIFO Data Counter indicates the amount of data in the Receive FIFO. Reset to 00h.

7.2.25. LINE STATUS REGISTER COUNTER – OFFSET 15h, SFR[6] = 1

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Line Status Register Counter	RO	The Line Status Register Counter indicates the amount of data in the LSR. Reset to 00h.

7.2.26. TRANSMIT FIFO DATA COUNTER – OFFSET 16h, SFR[7] = 1

The function of this register is selected by the Special Function Register (Offset 07h) bit 7. When SFR[7] is set to '1', this register functions as the Transmit FIFO Data Counter. Otherwise, it functions as the Sample Clock Register.

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Transmit FIFO Data Counter	RO	The Transmit FIFO Data Counter indicates the amount of data in the Transmit FIFO. Reset to 00h.

7.2.27. SAMPLE CLOCK REGISTER – OFFSET 16h, SFR[7] = 0

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	Sample Clock	RW	This register determines the Sample Clock value (SC) used in the Baud Rate Generator. Please refer to 5.2.12 Baud Rate Generation for more detail 0000b: SC = 16 0001b: SC = 15 0010b: SC = 14 0011b: SC = 13 0100b: SC = 12 0101b: SC = 11 0110b: SC = 10 0111b: SC = 9 1000b: SC = 8 1001b: SC = 7 1010b: SC = 6 1011b: SC = 5 1100b: SC = 4 Other settings are reserved. Reset to 0h.
7:4	Reserved	RO	Reset to 0h.

7.2.28. GLOBAL LINE STATUS REGISTER – OFFSET 17h

BIT	FUNCTION	TYPE	DESCRIPTION
0	RX Data Available	RO	0b: No data in the receive FIFO 1b: Data in the receive FIFO Reset to 0b.
1	RX FIFO Overrun	RO	0b: No overrun error 1b: Overrun error Reset to 0b.
2	RX Parity Error	RO	0b: No parity error 1b: Parity error Reset to 0b.
3	RX Frame Error	RO	0b: No framing error 1b: Framing error Reset to 0b.
4	RX Break Error	RO	0b: No break condition 1b: Break condition Reset to 0b.
5	TX Empty	RO	0b: Tx Holding Register is not empty. 1b: Tx Holding Register is empty. Reset to 0b.
6	TX Complete	RO	0b: Tx Shift Register is not empty. 1b: Tx Shift Register is empty. Reset to 0b.

BIT	FUNCTION	TYPE	DESCRIPTION
7	RX Data Error	RO	0b: No Rx FIFO error 1b: Rx FIFO error Reset to 0b.

7.2.29. RECEIVE FIFO DATA REGISTERS – OFFSET 100h ~ 17Fh

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Receive FIFO Data	RO	This register is used to map RX FIFO data content. Reset to 00h.

7.2.30. TRANSMIT FIFO DATA REGISTERS – OFFSET 100h ~ 17Fh

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Transmit FIFO Data	WO	This register is used to map TX FIFO to memory space. Reset to 00h.

7.2.31. LINE STATUS FIFO REGISTERS –OFFSET 180h ~ 1FFh

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Line Status FIFO	RO	This register is used to map FIFO data relative LSR content. Reset to 00h.

8. EEPROM INTERFACE

The EEPROM interface consists of five pins: SR_DI (EEPROM data input), SR_DO (EEPROM data output), SR_CS (EEPROM chip select), SR_CLK_O (EEPROM clock output), and SR_ORG (EEPROM organization). The device may control a 93C56 or compatible parts using 2K bits. The EEPROM is used to initialize a number of registers before enumeration. This is accomplished at start-up when RTS[0] is de-asserted, at which time the data from the EEPROM is loaded. The EEPROM interface is organized into a 16-bit base, and the device supplies a 7-bit EEPROM word address.

8.1. AUTO MODE EERPOM ACCESS

The device may access the EEPROM in a WORD or BYTE format, which is decided by the SR_ORG# at start-up. If SR_ORG# is asserted at start-up, EEPROM is accessed using the WORD format. Otherwise, Byte format is used.

8.2. EEPROM MODE AT RESET

During a reset, the device will automatically load the information/data from the EEPROM if the automatic load condition is met. The first offset in the EEPROM contains a signature. If the signature is recognized, and if RTS[0] is de-asserted, the autoload initiates right after the reset.

8.3. EEPROM SPACE ADDRESS MAP AND DESCRIPTION

EEPROM ADDRESS	PCIE REGISTER OFFSET	DEFAULT Value	DESCRIPTION
00h		A868h	**Check Code**
02h	Offset 00h bit[15:0]	12D8h	**Vendor ID**
04h	Offset 00h bit[31:16]	7958h	**Device ID**
06h	Offset 2Ch bit[15:0]	0000h	**Subsytem Vendor ID**
08h	Offset 2Ch bit[31:16]	0000h	**Subsytem ID**
0Ah	Bit[0] - Offset 80h bit[21]	0b	**Device Specific Initialization:** When set, the DSI is required.
	Bit[3:1] - Offset 80h bit[24:22]	111b	**Aux. Current:** When set, the I/O bridge needs 375 mA in D3 state.
	Bit[4] - Offset 80h bit[25]	1b	**D1 Support:** When set, this bridge supports D1 Power Management state.
	Bit[5] - Offset 80h bit[26]	1b	**D2 Support:** When set, this bridge supports D2 Power Management state.
	Bit[10:6] - Offset 80h bit[31:27]	01000b	**PME Support:** When set, the PME supports D1 and D2 Power Management states.
	Bit[11] - Offset 84h bit[3]	1b	**No Soft Reset:** When set, the device does not trigger the Internal Reset Command during the transition from D3hot to D0 power state.
	Bit[13:12] - Offset A8h bit[14:13]	00b	**XPIP CSR0**
0Ch	Offset B0h bit[15:0]	0000h	**Replay Time-out Counter**
0Eh	Offset B0h bit [31:16]	0000h	**Acknowledge Latency Timer**
10h	Bit[1:0] - Offset ECh bit[11:10]	11b	**ASPM Capability Support:** When set, this bridge supports L0s and L1 entry
	Bit[4:2] - Offset ECh bit[14:12]	011b	**Exit L0s Latency Timer**
	Bit[7:5] - Offset ECh bit[17:15]	000b	**Exit L1 Latency Timer**

EEPROM ADDRESS	PCIE REGISTER OFFSET	DEFAULT Value	DESCRIPTION
12h	Offset B4h bit[15:0]	0000h	**UART Transmitter Drive Enable:** RS232/422/485-2W/485-4W Selection for UART 0 to 3
14h	Offset B4h bit[31:16]	0000h	**UART Transmitter Drive Enable:** RS232/422/485-2W/485-4W Selection for UART 4 to 7
16h	Bit[1:0] - Offset B8h bit[17:16]	01b	**PM Control Parameter:** Determines whether this bridge enters L1 or not when D3 condition occurs.
	Bit[3:2] - Offset B8h bit[19:18]	00b	**PM Control Parameter:** Determines the delay counter value when entering L1
	Bit[5:4] - Offset B8h bit[21:20]	00b	**PM Control Parameter:** Determines whether this bridge asserts L0s/L1 handshake protocol
18h	Bit[13:0] - Offset C8h bit[13:0]	0200h	**PHY Parameter**
1Ah	Bit[0] - Offset C4h bit[15]	1b	**Role Based Error Report Enable:** Indicates implement the role-base error reporting
	Bit[15:8] - Offset 34h bit[7:0]	80h	**Capability List Pointer:** Points to a linked list of new capabilities implemented by the device
1Ch	Bit[7:0] - Offset 08h bit[7:0]	00h	**Revision ID:** Indicates revision number of device
40h		12D8h	**Check Code**

9. ELECTRICAL SPECIFICATION

9.1. ABSOLUTE MAXIMUM RATINGS

Table 9-1 Absolute Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	--65°C to 150°C
PCI Express supply voltage to ground potential (VDDA, VDDC, VTT and VDDCAUX)	-0.3v to 2.1v
PCI supply voltage to ground potential (VDDR)	-0.3v to 3.8v
DC input voltage for PCI Express signals	-0.3v to 2.1v

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

9.2. DC SPECIFICATIONS

Table 9-2 DC Electrical Characteristics

Symbol	Min.	Typ.	Max.
VDDA	1.6v	1.8v	2.0v
VDDC	1.6v	1.8v	2.0v
VDDCAUX	1.6v	1.8v	2.0v
VTT	1.6v	1.8v	2.0v
VDDR	3.0v	3.3v	3.6v
VIL			0.8v
VIH	2.0v		
VOL			0.4v
VOH	2.6v		

VDDA: analog power supply for PCI Express Interface
VDDC: digital power supply for the core
VTT: termination power supply for PCI Express Interface
VDDCAUX: auxiliary power supply
VDDR: digital power supply for the I/O
VIH: I/O input high voltage
VIL: I/O input low voltage
VOL: I/O output low voltage
VOH: I/O output High voltage

The typical power consumption of PI7C9X7958 is about 0.9 watt.

9.3. AC SPECIFICATIONS

Table 9-3 Transmitter Characteristics

Symbol	Description	Min	Typical	Max.	Unit
Voltage Parameters					
$V_{TX-DIFF}$[a]	Output voltage compliance @ typical swing				
	$V_{TX-DIFFp}$ (peak-to-peak, single ended)	400	500	600	mV
	$V_{TX-DIFFpp}$ (peak-to-peak, differential)	800	1000	1200	mV

Symbol	Description	Min	Typical	Max.	Unit
V_{SW}	Supported TX output voltage range (pp, differential)	700[b]		1400[c]	mV
V_{OL}	Low-level output voltage		V_{TT} - 1.5 *$V_{TX-DIFFp}$		V
V_{OH}	High-level output voltage		V_{TT} - 0.5$V_{TX-DIFFp}$		V
$V_{TX-CM-AC}$	Transmit common-mode voltage in L0	0.50	V_{TT} - $V_{TX-DIFFp}$	1.45	V
$V_{TX-CM-HiZ}$	Transmit common-mode voltage in L0s (TX) & L1		$V_{TX-CM-AC}$		V
$V_{TX-DE-RATIO}$	De-emphasized differential output voltage	0		-7.96	dB
$V_{TX-IDLE-DIFFp}$	Electric Idle differential peak voltage			20	mV
$V_{TX-RCV-DETECT}$	Voltage change during Receive Detection		$V_{TX-DIFFp}$		mV
$RL_{TX-DIFF}$	Transmitter Differential Return loss	10			dB
RL_{TX-CM}	Transmitter Common Mode Return loss	6			dB
Z_{OSE}	Single-ended output impedance	40	50	60	Ω
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω
$T_{TX-RISE, TTX-FALL}$	Rise / Fall time of TxP, TxN outputs	80		110[d]	ps
Jitter Parameters					
UI	Unit Interval	399.88	400	400.12	ps
$T_{TX-MAX-JITTER}$	Transmitter total jitter (peak-to-peak)			0.30[e]	UI
T_{TX-EYE}	Minimum TX Eye Width (1 - $T_{TX-MAX-JITTER}$)	0.70			UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.15	UI
Timing Parameters					
$L_{TLAT-10}$	Transmitter data latency (for n=10)	9		11	UI
$L_{TLAT-20}$	Transmitter data latency (for n=20)	9		11	UI
$L_{TX-SKEW}$	Transmitter data skew between any 2 lanes	0		2 + 200ps	UI
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid electrical idle after sending an Electrical Idle ordered set			8	ns
T_{EIExit}	Time to exit Electrical Idle (L0s) state into L0		12	16	ns
T_{BTEn}	Time from asserting BeaconTxEn to beacon being transmitted on the lane		30	80	ns

a. Measured with Vtt = 1.2V, HiDrv='0',LowDrv='0' and Dtx='0000'.
b. Minimum swing assumes LoDrv = 1, HiDrv = 0 and Dtx =1100
c. Max swing assumes LoDrv = 0, HiDrv = 1, Dtx = 0010, VTT = 1.8V
d. As measured between 20% and 80% points. Will depend on package characteristics.
e. Measured using PCI Express Compliance Pattern

Table 9-4 Receiver Characteristics

Symbol	Description	Min	Typical	Max.	Unit
Voltage Parameters					
$V_{RX-DIFFp-p}$	Differential input voltage (peak-to-peak)	170		1200	mV
$V_{RX-IDLE-DET-DIFFp-p}$	Differential input threshold voltage (peak-to-peak) to assert TxIdleDetect output	65		175	mV
$V_{RX-CM-AC}$	Receiver common-mode voltage for AC-coupling		0	150	mV
$T_{RX-RISE, TRX-FALL}$	Rise time / Fall time of RxP, RxN inputs			160	Ps
$Z_{RX-DIFF-DC}$	Differential input impedance (DC)	80	100	120	Ω
$Z_{RX-COM-DC}$	Single-ended input impedance	40	50	60	Ω
$Z_{RX-COM-INITIAL-DC}$	Initial input common mode impedance (DC)	5	50	60	Ω
$Z_{RX-COM-HIGH-IMP-DC}$	Powered down input common mode impedance (DC)	200k			Ω

Symbol	Description	Min	Typical	Max.	Unit
$RL_{RX-DIFF}$	Receiver Differential Return Loss[a]	10			dB
RL_{RX-CM}	Receiver Common Mode Return Loss[b]	6			dB
Jitter Parameters					
$T_{RX-MAX-JITTER}$	Receiver total jitter tolerance			0.65	UI
T_{RX-EYE}	Minimum Receiver Eye Width	0.35			UI
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between jitter median and max deviation from median			0.325	UI
Timing Parameters					
LRLAT-10	Receiver data latency for n=10	28		29	bits
LRLAT-20	Receiver data latency for n=20	49		60	bits
TRX-SKEW	Receiver data skew between any 2 lanes	0		1[c]	bits
TBDDly	Beacon-Activity on channel to detection of Beacon[d]			200	us
TRX-IDLE_ENTER	Delay from detection of Electrical Idle condition on the channel to assertion of TxIdleDetect output		10	20	ns
TRX-IDLE_EXIT	Delay from detection of L0s to L0 transition to deassertion of TxIdleDetect output		5	10	ns

a. Over a frequency range of 50 MHz to 1.25 GHz.
b. Over a frequency range of 50 MHz to 1.25 GHz.
c. Assuming synchronized bit streams at the respective receiver inputs.
d. This is a function of beacon frequency

10. CLOCK SCHEME

The PI7C9X7958 requires 100MHz differential clock inputs through CLKINP and CLKINN Pins as shown in the following table.

Table 10-1 Input Clock Requirements

Symbol	Description		Min	Typical	Max.	Unit
$ClkIn_{FREQ}$	Reference input clock range		-	100	-	MHz
$ClkIn_{DC}$	Duty cycle of input clock		40	50	60	%
T_R, T_F	Rise/Fall time of input clock		-	-	0.2	RCUI[a]
V_{SW}	Differential input voltage swing	(zero-to-peak)	0.4		0.8	V

a. RCUI (Reference Clock Unit Interval) refers to the reference clock period

11. PACKAGE INFORMATION

The Package of the PI7C9X7958 is a 160-pin LFBGA. The ball pitch is 0.8mm and the ball size is 0.5mm.

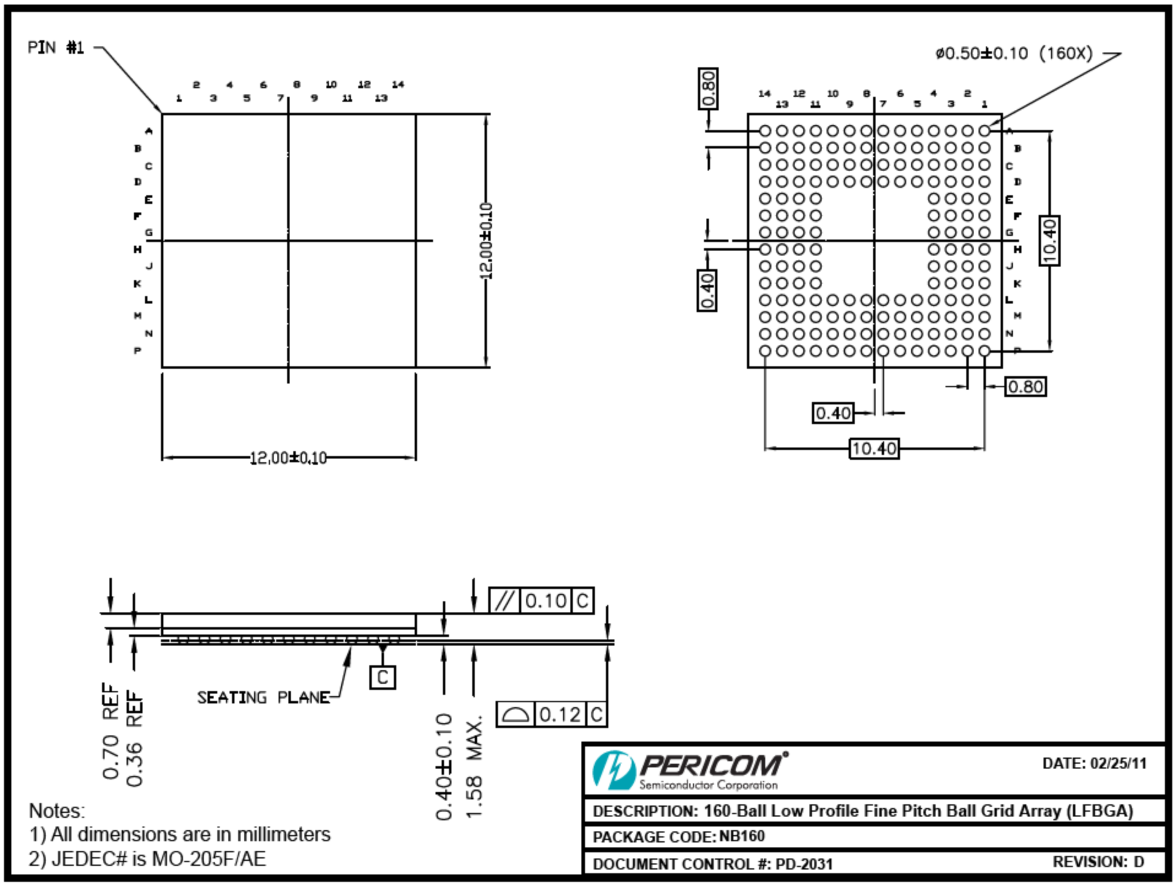

Figure 11-1 Package Outline Drawing

12. Order Information

Part Number	Temperature Range	Package	Pb-Free & Green
PI7C9X7958□NBEX	-40°C to 85°C (Industrial Temperature)	160-pin LFBGA 12mm x 12mm	Yes