Lead-free Green

PI7C9X2G912GP

PCI EXPRESS GEN 2 PACKET SWITCH

5/ 6/ 9-Port/ 12-Lane PCI Express Gen 2 Switch

Green Package Family

DATASHEET

REVISION 8

December 2020

A Product Line of Diodes Incorporated

1545 Barber Lane Milpitas, CA 95035
Telephone: 408-232-9100
FAX: 408-434-1040
Internet: http://www.diodes.com

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REVISION HISTORY

Date	Revision Number	Description
07/09/2015	0.1	Preliminary Datasheet (Short-Form)
08/14/2015	0.2	Updated Section 3 Pin Description Updated Figure 4-1 PI7C9X2G912GP Ball Assignment Updated Section 6-1 Physical Layer Circuit
12/23/2015	0.3	Updated Section 3 Pin Description Updated Section 6 Functional Description Updated Section 7 EEPROM Interface and System Management/I2C Bus Updated Section 8 Register Description Updated Section 9 Clock Scheme Updated Section 10 Power Management Updated Section 11 IEEE 1149.1 Compatible JTAG Controller Updated Section 12 Electrical and Timing Specifications
01/13/2016	0.4	Updated Section 12.2 DC Specifications
03/24/2016	0.5	Updated Section 8.2.87 NT-UP Port Selection Register Updated Section 8.2.88 Hot Plug Configuration Register Removed Section 8.2.182 Clock Buffer Control Register Removed Section 8.2.183 Clock Buffer Port Select Register Added Section 11 Power Sequence
12/23/2016	0.6	Updated Section 8 Register Description Updated Section 7.1.3 EEPROM Space Address Map Updated Table 7-2 Bytes for SMBus Block Write Updated Table 13-2 DC Electrical Characteristics
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05/14/2020	7	Updated Section 1 Features

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		Update Section 3.2 PORT SPECIFIC SIGNALS (12 BALLS) Updated Section 6.1 Physical Layer Circuit Updated Section 16 Ordering Information
12/14/2020	8	For Datasheet Status Change

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1 FEATURES

- 12-lane PCI Express Gen 2 Switch with 9 PCI Express ports
- Supports "Cut-through"(Default) as well as "Store and Forward" mode for packet switching
- 150 ns typical latency for packet routed through Switch without blocking
- Strapped pins configurable with optional EEPROM, SMBus or I2C Bus
- SMBus interface support
- I2C Slave interface support
- Compliant with System Management (SM) Bus, Version 2.0
- Compliant with I2C Bus Specification, Version 2.1
- Compliant with *PCI Express Base Specification Revision 2.1*
- Compliant with *PCI Express CEM Specification Revision 2.0*
- Compliant with *PCI-to-PCI Bridge Architecture Specification Revision 1.2*
- Compliant with *Advanced Configuration Power Interface (ACPI) Specification*
- Reliability, Availability and Serviceability
  - Supports Data Poisoning and End-to-End CRC
  - Advanced Error Reporting and Logging
- Advanced Power Saving
  - Empty downstream ports are set to idle state to minimize power consumption
- Link Power Management
  - Supports L0, L0s, L1, L2, $L2/L3_{Ready}$ and L3 link power states
  - Active state power management for L0s and L1 states
- Device State Power Management
  - Supports D0, $D3_{Hot}$ and $D3_{Cold}$ device power states
- Port Arbitration: Round Robin (RR), Weighted RR and Time-based Weighted RR
- Extended Virtual Channel capability
  - Two Virtual Channels (VC) and Eight Traffic Class (TC) support
  - Disabled VCs' buffer is assigned to enabled VCs for resource sharing
  - Independent TC/VC mapping for each port
  - Provides VC arbitration selections: Strict Priority, Round Robin (RR) and Programmable Weighted RR
- Supports Isochronous Traffic
  - Isochronous traffic class mapped to VC1 only
  - Strict time based credit policing
- Supports up to 512-byte maximum payload size
- Programmable driver current and de-emphasis level at each individual port
- Support Access Control Service (ACS)
- Support Address Translation (AT) packet for SR-IOV application
- Support Alternative Routing ID Interpretation (ARI)
- Support Mutlicast
- Support Serial Hot Plug Controller
- Low Power Dissipation: 1.27W typical in L0 normal mode
- Industrial Temperature Range -40^{o} to $85^{o}C$
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/
- 196-pin LBGA 15mm x 15mm package

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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2 GENERAL DESCRIPTION

Similar to the role of PCI/PCIX Bridge in PCI/PCIX bus architecture, the function of PCI Express (PCIE) Switch is to expand the connectivity to allow more end devices to be reached by host controllers in PCIE serial interconnect architecture. The 12-lane PCIe Switch is in 9-port type configuration. It provides users the flexibility to expand or fan-out the PCI Express lanes based on their application needs.

In the PCI Express Architecture, the PCIE Switch forwards posted and non-posted requests, and completion packets in either downstream or upstream direction concurrently as if a virtual PCI Bridge is in operation on each port. By visualizing the port as a virtual Bridge, the Switch can be logically viewed as two-level cascaded multiple virtual PCI-to-PCI Bridges, where one upstream-port Bridge sits on all downstream-port Bridges. Similar to a PCI Bridge during enumeration, each port is given a unique bus number, device number, and function number by the initiating software. The bus number, device number, and function number are combined to form a destination ID for each specific port. In addition to that, the memory-map and IO address ranges are exclusively allocated to each port as well. After the software enumeration is finished, the packets are routed to the dedicated port based on the embedded address or destination ID. To ensure the packet integrity during forwarding, the Switch is not allowed to split the packets to multiple small packets or merge the received packets into a large transmit packet. Also, the IDs of the requesters and completers are kept unchanged along the path between ingress and egress port.

The Switch employs the architecture of Combined Input and Output Queue (CIOQ) in implementation. The main reason for choosing CIOQ is that the required memory bandwidth of input queue equals to the bandwidth of ingress port rather than increasing proportionally with port numbers as an output queue Switch does. The CIOQ at each ingress port contains separate dedicated queues to store packets. The packets are arbitrated to the egress port based on the PCIe transaction-ordering rule. For the packets without ordering information, they are permitted to pass over each other in case that the addressed egress port is available to accept them. As to the packets required to follow the ordering rule, the Head-Of-Line (HOL) issue becomes unavoidable for packets destined to different egress ports since the operation of producer-consumer model has to be retained; otherwise the system might occur hang-up problem. On the other hand, the Switch places replay buffer at each egress port to defer the packets before sending it out. This can assure the maximum throughput being achieved and therefore the Switch works efficiently. Another advantage of implementing CIOQ in PCIe Switch is that the credit announcement to the counterpart is simplified and streamlined because of the credit-based flow control protocol. The protocol requires that each ingress port maintains the credits independently without checking other ports' credit availability, which is otherwise required by pure output queue architecture.

The Switch supports two virtual channels (VC0, VC1) and eight traffic classes (TC0 ~ TC7) at each port. The ingress port independently assigns packets into the preferred virtual channel while the egress port outputs the packet based on the predefined port and VC arbitration algorithm. For instance, the isochronous packet is given a special traffic class number other than TC0 and mapped into VC1 accordingly. By employing the strict time based credit policy for port arbitration and assigning higher priority to VC1 than VC0, the Switch can therefore guarantee the time-sensitive packet is not blocked by regular traffic to assure the quality of service. In addition, some data-centric applications only carry TC0/VC0 traffic. As a result, there are no packets that would consume VC1 bandwidth. In order to improve the efficiency of buffer usage, the unused VC1 queues can be reassigned to VC0 and enable each of the ingress ports to handle more data traffic bursts. This virtual channel resource relocation feature enhances the performance of the PCIe Switch further.

The Switch provides the advanced feature of Access Control Service (ACS). This feature regulates which components are allowed to communicate with each other within the PCIe multiple-point fabric, and allows the system to have more control over packet routing in the Switch. As a result, peer-to-peer traffic can be facilitated more accurately and efficiently. When the system also implements Address Translation Service (ATS), the peer-to-peer requests with translated address can be routed directly by enabling the corresponding option in ACS to avoid possible performance bottleneck associated with re-direction, which introduces extra latency and may increase link and RC congestion.

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3 PIN DESCRIPTION

3.1 PCI EXPRESS INTERFACE SIGNALS (61 BALLS)

NAME	PIN	TYPE	DESCRIPTION
REFCLKP[2:0]	G2,H13,N7	I	**Reference Clock Input Pairs:** Connect to 100MHz differential clock.
REFCLKN[2:0]	G1,H14,P7	I	
PERP[11:0]	M1,K1,E1,C1, C14,E14,K14, M14,P12,P10, P5,P3	I	**PCI Express Data Serial Input Pairs:** Differential data receive signals in sixteen ports. Please refer to Section 5 for Mapping of the Lanes to transmission and receive pairs and configuration of Port-Lane.
PERN[11:0]	M2,K2,E2,C2, C13,E13,K13, M13,N12,N10, N5,N3	I	
PETP[11:0]	L1,J1,F1,D1, D14,F14,J14, L14,P11,P9, P6, P4	O	**PCI Express Data Serial Output Pairs:** Differential data transmit signals in sixteen ports. Please refer to Section 5 for Mapping of the Lanes to transmission and receive pairs and configuration of Port-Lane.
PETN[11:0]	L2,J2,F2,D2, D13,F13,J13, L13,N11,N9, N6,N4	O	
PERST_L	A13	I	**System Reset (Active LOW):** When PERST_L is asserted, the internal states of whole chip except sticky logics are initialized. Please refer to Table 11-2 for PERST_L Spec.
REXT[2:0]	H1,G14,P8	I	**External Reference Resistor:** Connect an external resistor (1.43K Ohm +/- 1%) to REXT_GND to provide a reference to both the bias currents and impedance calibration circuitry.
REXT_GND[2:0]	H2,G13,N8	I	**External Reference Resistor Ground:** Connect to an external resistor to REXT.

3.2 PORT SPECIFIC SIGNALS (12 BALLS)

NAME	PIN	TYPE	DESCRIPTION
PORTGOOD_L[15:10;3,2,0]	N2,P1,H3,L3,A3, C6,G12,E12,L12	O	**Port Good Status:** These signals indicate the link status of each port. When continuously deasserts, the device is in the condition of link down. When continuously asserts, the link is up and operates at 5GT/s. When blinking, asserts and deasserts with 0.5-second intervals, the link is up and operates at 2.5GT/s. Please refer to Section 5.4 for detail information.
PORTCFG[1:0]	A5,A4	I	**Port-Lane Configuration:** These signals decide Port-Lane configuration. These pins must be pull-up or pull-down by external resistors. Please refer to Section 5 for Port-Lane Mapping. These strapping pins have no built-in internal resistors and can not be left NC. These pins require the external 5.1K-ohm pull-up resistors or 330-ohm pull-down resistors.

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NAME	PIN	TYPE	DESCRIPTION
CFG_TIMER_EN_L	M11	I	**CFG Timer Enable:** When tied high, TS pkts always advertises support for GENII data rate and autonomous change. When tied low, if the LTSSM fails during the Configuration state, TS pkts only advertises GENI data rate and no autonomous change support in next time the LTSSM exists the Detect state. If the LTSSM fails continuously in Configuration state, the LTSSM continues to alternate between GENI and GENII advertisement every time it exists the Detect state. This pin has internal pull-up. If no board trace is connected to this pin, the internal pull-up resistor of this pin is enough. However, if pin is connected to a board trace and not driven, it is recommended that an external 5.1K- ohm pull-up resistor be used.

3.3 EEPROM and SMBUS/I2C SIGNALS (10 BALLS)

NAME	PIN	TYPE	DESCRIPTION
EECK	D12	I/O	**EEPROM Clock:** Clock signal to 4-wire EEPROM interface.
EEDI	B11	O	**EEPROM Data Input:** Diodes 2G912GP outputs data to the Data Input pin of Serial EEPROM.
EEDO	C11	I	**EEPROM Data Output:** Diodes 2G912GP inputs data from the Data Output pin of Serial EEPROM.
EECS_L	C12	O	**EEPROM Chip Select (Active Low):** Diodes 2G912GP asserts this signal to enable Serial EEPROM. **EEPROM Bypass Mode (EEPROM_BYPASS_L):** During system initialization, EECS_L acts as the EEPROM_BYPASS_L pin. When tied low, eeprom function is disabled. When tied high, eeprom function is enabled. This pin has internal pull-up resistor. If no board trace is connected to this pin, the internal pull-up resistor of this pin is enough. However, if pin is connected to a board trace and not driven, it is recommended that an external 5.1K-ohm pull-up resistor be used.
SCL_I2C	B10	OD	**SMBUS/I2C Serial Clock:** System management or I2C Bus Clock. This pin requires an external 5.1K-ohm pull-up resistor.
SDA_I2C	C10	OD	**SMBUS/I2C Serial Data:** Bi-Directional System Management or I2C Bus Data. This pin requires an external 5.1K-ohm pull-up resistor.
I2C_ADDR[2:0]	A11,A10,A9	I	**SMBUS/I2C Slave Address Bit [2:0]:** These pins are used to configure the value of the three least significant bits of the PI7C2G912GP 7-bit Slave address.
SMBUS_EN_L	M8	I	**System Manage Bus Enable:** Select either SMBUS or I2C protocol. When tied high, I2C protocol is selected. When tied low, SMBUS protocol is chosen. This pin has internal pull-up resistor. If no board trace is connected to this pin, the internal pull-up resistor of this pin is enough. However, if pin is connected to a board trace and not driven, it is recommended that an external 5.1K-ohm pull-up resistor be used.

3.4 MISCELLANEOUS SIGNALS (29 BALLS)

NAME	PIN	TYPE	DESCRIPTION
SHCL_I2C	B8	OD	**I2C Clock Signal of Serial Hot Plug Controller:** It is connected to SCL pin of all I2C IO expanders. This pin requires an external 5.1K-ohm pull-up resistor.
SHDA_I2C	B9	OD	**I2C Data Signal of Serial Hot Plug Controller:** It is connected to SDA pin of all I2C IO expanders. This pin requires an external 5.1K-ohm pull-up resistor.
SHPCINT_L	A8	I	**Interrupt Input (Active Low) of Serial Hot Plug Controller:** It is connected to INT# output pin of all I2C IO expanders. When asserted, it notifies Hot Plug Controller to access the port registers of all I/O expanders for touching changed status to de-assert INT#.
GPIO[7:0]	N1,P2,C4,A1, A2,B2,B1,C5	I/O	**General Purpose Input and Output:** These eight general-purpose pins are programmed as either input-only or bi-directional pins by writing the GPIO output enable control register.

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NAME	PIN	TYPE	DESCRIPTION
FATAL_ERR_L	B5	O	**Fatal Error Output:** It is asserted low when a Fatal error is detected.
INTA_L	A14	OD	**Interrupt Output Enable:** When tied low, it indicates that one or more of the following events/errors are detected: Hot Plug events, Link State events, General-Purpose Input Interrupt events, Device-Specific errors, Device-Specific NT Port Link Interface errors and events, NT-Virtual Doorbell events or NT-Link Doorbell events.
DEBUG_SEL[1:0]	M3,B12	I	**Test Only** Must be pulled up by an external 5.1K-ohm resistor.
FAST_MODE_L	B3	I	**Test Only** Must be pulled up by an external 5.1K-ohm resistor.
SERDES_MODE_EN_L	B4	I	**Test Only** Must be pulled up by an external 5.1K-ohm resistor.
TESTMODE[2:0]	N14,N13,P14	I	**Test Only** Must be pulled up by an external 5.1K-ohm resistor. **Gen1 Cap. Only Enable (GEN1CAP_ONLY_EN_L):** During system initialization, TESTMODE[2] acts as the GEN1CAP_ONLY_EN_L pin. When tied high, the max. link speed is set to 5.0 G b/s. When tied low, the max. link speed is set to 2.5G b/s. This pin must be pull-up by 5.1K-ohm or pull-down by 330-ohm external resistor.
PLL_BYPASS_L	B14	I	**Test Only** Must be pulled up by an external 5.1K-ohm resistor.
TEST	M4	I	**Test Only** Must be pulled up by an external 5.1K-ohm resistor.
NC	A12,B13,C3, D3,K3,M12, P13		**Not Connected:** These pins can be just left open.

3.5 JTAG BOUNDARY SCAN SIGNALS (5 Balls)

NAME	PIN	TYPE	DESCRIPTION
TCK	C7	I	**Test Clock:** Used to clock state information and data into and out of the chip during boundary scan. When JTAG boundary scan function is not implemented, this pin should be left open (NC).
TDI	A6	I	**Test Data Input:** Used (in conjunction with TCK) to shift data and instructions into the TAP in a serial bit stream. When JTAG boundary scan function is not implemented, this pin should be left open (NC).
TDO	B7	O	**Test Data Output:** Used (in conjunction with TCK) to shift data out of the Test Access Port (TAP) in a serial bit stream. When JTAG boundary scan function is not implemented, this pin should be left open (NC).
TMS	B6	I	**Test Mode Select:** Used to control the state of the Test Access Port controller. When JTAG boundary scan function is not implemented, this pin should be pulled low through a 330-Ohm pull-down resistor.
TRST_L	A7	I	**Test Reset (Active LOW):** Active LOW signal to reset the TAP controller into an initialized state. When JTAG boundary scan function is not implemented, this pin should be pulled low through a 330-Ohm pull-down resistor.

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3.6 POWER PINS (79 BALLS)

NAME	PIN	TYPE	DESCRIPTION
VDDC	D5,D6,D9,D10,E4, E11,F4,F11,J4, J11,K4,K11,L5, L6,L9,L10	P	**VDDC Supply (1.0V):** Used as digital core power pins.
VDDR	D4,D11,L4,L11	P	**VDDR Supply (2.5V):** Used as digital I/O power pins.
AVDD	D7,D8,G4,G11, H4,H11,L7,L8	P	**AVDD Supply (1.0V):** Used as PCI Express analog power pins.
AVDDH	C8,G3,H12,M7	P	**AVDDH Supply (2.5V):** Used as PCI Express analog high voltage power pins.
VSS	C9,E3,E5,E6,E7, E8,E9,E10,F3,F5, F6,F7,F8,F9,F10, F12,G5,G6,G7,G8, G9,G10,H5,H6, H7,H8,H9,H10,J3, J5,J6,J7,J8,J9, J10, J12,K5,K6,K7,K8, K9,K10,K12,M5, M6,M9,M10	P	**Ground:** Used as ground pins.

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4 PIN DESCRIPTION

4.1 PIN LIST of 196-BALL LBGA

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
A1	GPIO[4]	D8	AVDD	H1	REXT[2]	L8	AVDD
A2	GPIO[3]	D9	VDDC	H2	REXT_GND[2]	L9	VDDC
A3	PORT_GOOD_L[11]	D10	VDDC	H3	PORT_GOOD_L[13]	L10	VDDC
A4	PORTCFG[0]	D11	VDDR	H4	AVDD	L11	VDDR
A5	PORTCFG[1]	D12	EECK	H5	VSS	L12	PORT_GOOD_L[0]
A6	TDI	D13	PETN[7]	H6	VSS	L13	PETN[4]
A7	TRST_L	D14	PETP[7]	H7	VSS	L14	PETP[4]
A8	SHPCINT_L	E1	PERP[9]	H8	VSS	M1	PERP[11]
A9	I2C_ADDR[0]	E2	PERN[9]	H9	VSS	M2	PERN[11]
A10	I2C_ADDR[1]	E3	VSS	H10	VSS	M3	DEBUG_SEL[1]
A11	I2C_ADDR[2]	E4	VDDC	H11	AVDD	M4	TEST
A12	NC	E5	VSS	H12	AVDDH	M5	VSS
A13	PERST_L	E6	VSS	H13	REFCLKP[1]	M6	VSS
A14	INTA_L	E7	VSS	H14	REFCLKN[1]	M7	AVDDH
B1	GPIO[1]	E8	VSS	J1	PETP[10]	M8	SMBUS_EN_L
B2	GPIO[2]	E9	VSS	J2	PETN[10]	M9	VSS
B3	FAST_MODE_L	E10	VSS	J3	VSS	M10	VSS
B4	SERDES_MODE_EN_L	E11	VDDC	J4	VDDC	M11	CFG_TIMER_EN_L
B5	FATAL_ERR_L	E12	PORT_GOOD_L[2]	J5	VSS	M12	NC
B6	TMS	E13	PERN[6]	J6	VSS	M13	PERN[4]
B7	TDO	E14	PERP[6]	J7	VSS	M14	PERP[4]
B8	SHCL_I2C	F1	PETP[9]	J8	VSS	N1	GPIO[7]
B9	SHDA_I2C	F2	PETN[9]	J9	VSS	N2	PORT_GOOD_L[15]
B10	SCL_I2C	F3	VSS	J10	VSS	N3	PERN[0]
B11	EEDI	F4	VDDC	J11	VDDC	N4	PETN[0]
B12	DEBUG_SEL[0]	F5	VSS	J12	VSS	N5	PERN[1]
B13	NC	F6	VSS	J13	PETN[5]	N6	PETN[1]
B14	PLL_BYPASS_L	F7	VSS	J14	PETP[5]	N7	REFCLKP[0]
C1	PERP[8]	F8	VSS	K1	PERP[10]	N8	REXT_GND[0]
C2	PERN[8]	F9	VSS	K2	PERN[10]	N9	PETN[2]
C3	NC	F10	VSS	K3	NC	N10	PERN[2]
C4	GPIO[5]	F11	VDDC	K4	VDDC	N11	PETN[3]
C5	GPIO[0]	F12	VSS	K5	VSS	N12	PERN[3]
C6	PORT_GOOD_L[10]	F13	PETN[6]	K6	VSS	N13	TESTMODE[1]
C7	TCK	F14	PETP[6]	K7	VSS	N14	TESTMODE[2]
C8	AVDDH	G1	REFCLKN[2]	K8	VSS	P1	PORT_GOOD_L[14]
C9	VSS	G2	REFCLKP[2]	K9	VSS	P2	GPIO[6]
C10	SDA_I2C	G3	AVDDH	K10	VSS	P3	PERP[0]
C11	EEDO	G4	AVDD	K11	VDDC	P4	PETP[0]
C12	EECS_L	G5	VSS	K12	VSS	P5	PERP[1]
C13	PERN[7]	G6	VSS	K13	PERN[5]	P6	PETP[1]
C14	PERP[7]	G7	VSS	K14	PERP[5]	P7	REFCLKN[0]
D1	PETP[8]	G8	VSS	L1	PETP[11]	P8	REXT[0]
D2	PETN[8]	G9	VSS	L2	PETN[11]	P9	PETP[2]
D3	NC	G10	VSS	L3	PORT_GOOD_L[12]	P10	PERP[2]
D4	VDDR	G11	AVDD	L4	VDDR	P11	PETP[3]
D5	VDDC	G12	PORT_GOOD_L[3]	L5	VDDC	P12	PERP[3]
D6	VDDC	G13	REXT_GND[1]	L6	VDDC	P13	NC
D7	AVDD	G14	REXT[1]	L7	AVDD	P14	TESTMODE[0]

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	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	GPIO[4]	GPIO[3]	PORT_GOOD_L[11]	PORTCFG[0]	PORTCFG[1]	TDI	TRST_L	SHPCINT_L	I2C_ADDR[0]	I2C_ADDR[1]	I2C_ADDR[2]	NC	PERST_L	INTA_L	A
B	GPIO[1]	GPIO[2]	FAST_MODE_L	SERDES_MODE_EN_L	FATAL_ERR_L	TMS	TDO	SHCL_I2C	SHDA_I2C	SCL_I2C	EEDI	DEBUG_SEL[0]	NC	PLL_BYPASS_L	B
C	PERP[8]	PERN[8]	NC	GPIO[5]	GPIO[0]	PORT_GOOD_L[10]	TCK	AVDDH	VSS	SDA_I2C	EEDO	EECS_L	PERN[7]	PERP[7]	C
D	PETP[8]	PETN[8]	NC	VDDR	VDDC	VDDC	AVDD	AVDD	VDDC	VDDC	VDDR	EECK	PETN[7]	PETP[7]	D
E	PERP[9]	PERN[9]	VSS	VDDC	VSS	VSS	VSS	VSS	VSS	VSS	VDDC	PORT_GOOD_L[2]	PERN[6]	PERP[6]	E
F	PETP[9]	PETN[9]	VSS	VDDC	VSS	VSS	VSS	VSS	VSS	VSS	VDDC	VSS	PETN[6]	PETP[6]	F
G	REFCLKN[2]	REFCLKP[2]	AVDDH	AVDD	VSS	VSS	VSS	VSS	VSS	VSS	AVDD	PORT_GOOD_L[3]	REXT_GND[1]	REXT[1]	G
H	REXT[2]	REXT_GND[2]	PORT_GOOD_L[13]	AVDD	VSS	VSS	VSS	VSS	VSS	VSS	AVDD	AVDDH	REFCLKP[1]	REFCLKN[1]	H
J	PETP[10]	PETN[10]	VSS	VDDC	VSS	VSS	VSS	VSS	VSS	VSS	VDDC	VSS	PETN[5]	PETP[5]	J
K	PERP[10]	PERN[10]	NC	VDDC	VSS	VSS	VSS	VSS	VSS	VSS	VDDC	VSS	PERN[5]	PERP[5]	K
L	PETP[11]	PETN[11]	PORT_GOOD_L[12]	VDDR	VDDC	VDDC	AVDD	AVDD	VDDC	VDDC	VDDR	PORT_GOOD_L[0]	PETN[4]	PETP[4]	L
M	PERP[11]	PERN[11]	DEBUG_SEL[1]	TEST	VSS	VSS	AVDDH	SMBUS_EN_L	VSS	VSS	CFG_TIMER_EN_L	NC	PERN[4]	PERP[4]	M
N	GPIO[7]	PORT_GOOD_L[15]	PERN[0]	PETN[0]	PERN[1]	PETN[1]	REFCLKP[0]	REXT_GND[0]	PETN[2]	PERN[2]	PETN[3]	PERN[3]	TESTMODE[1]	TESTMODE[2]	N
P	PORT_GOOD_L[14]	GPIO[6]	PERP[0]	PETP[0]	PERP[1]	PETP[1]	REFCLKN[0]	REXT[0]	PETP[2]	PERP[2]	PETP[3]	PERP[3]	NC	TESTMODE[0]	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 4-1 PI7C9X2G912GP Ball Assignment

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5 MODE SELECTION AND PORT-LANE MAPPING

5.1 MODE SELECTION

PI7C9X2G912GP can be configured into 9 Port-12 Lane, 6 Port-12 Lane and 5 Port-12 Lane modes by setting PORTCFG[1:0] pins.

PORTCFG[1]	PORTCFG[0]	Functional Mode
0	0	9Port-12Lane Configuration
0	1	6Port-12Lane Configuration
1	0	5Port-12Lane Configuration
1	1	Reserved

5.2 LANE MAPPING

The table below shows the mapping of the lanes to the transmission and receives pairs.

Lane	TX Pair	RX Pair
Lane 0	PETP[0]PETN[0]	PERP[0]PERN[0]
Lane 1	PETP[1]PETN[1]	PERP[1]PERN[1]
Lane 2	PTTP[2]PETN[2]	PERP[2]PERN[2]
Lane 3	PETP[3]PETN[3]	PERP[3]PERN[3]
Lane 4	PETP[4]PETN[4]	PERP[4]PERN[4]
Lane 5	PTTP[5]PETN[5]	PERP[5]PERN[5]
Lane 6	PETP[6]PETN[6]	PERP[6]PERN[6]
Lane 7	PETP[7]PETN[7]	PERP[7]PERN[7]
Lane 8	PETP[8]PETN[8]	PERP[8]PERN[8]
Lane 9	PTTP[9]PETN[9]	PERP[9]PERN[9]
Lane 10	PETP[10]PETN[10]	PERP[10]PERN[10]
Lane 11	PETP[11]PETN[11]	PERP[11]PERN[11]

5.3 PORT-LANE MAPPING

The table below shows the mapping of the lanes to ports in different functional modes.

Functional Mode	912	612	512
Lane 0	P0	P0	P0
Lane 1	P0	P0	P0
Lane 2	P0	P0	P0
Lane 3	P0	P0	P0
Lane 4	P2	P2	P2
Lane 5	P10	P2	P2
Lane 6	P12	P2	P7
Lane 7	P14	P2	P7
Lane 8	P3	P3	P3
Lane 9	P11	P11	P3
Lane 10	P13	P13	P9
Lane 11	P15	P15	P9

Notes:
P0: upstream port
P2~P3, P10~P15: downstream ports

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5.4 PORT-PORTGOOD_L MAPPING

The table below shows the mapping of PORTGOOD_L strapping pins to ports in different functional modes.

PORTGOOD_L	912	612	512
PORTGOOD_L[0]	P0	P0	P0
PORTGOOD_L[2]	P2	P2	P2
PORTGOOD_L[3]	P3	P3	P3
PORTGOOD_L[10]	P10	-	-
PORTGOOD_L[11]	P11	P11	P7
PORTGOOD_L[12]	P12	-	-
PORTGOOD_L[13]	P13	P13	P9
PORTGOOD_L[14]	P14	-	-
PORTGOOD_L[15]	P15	P15	-

Notes:
P0: upstream port
P2~P3, P10~P15: downstream ports

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6 FUNCTIONAL DESCRIPTION

Multiple virtual PCI-to-PCI Bridges (VPPB), connected by a virtual PCI bus, reside in the Switch. Each VPPB contains the complete PCIe architecture layers that consist of the physical, data link, and transaction layer. The packets entering the Switch via one of VPPBs are first converted from serial bit-stream into parallel bus signals in physical layer, stripped off the link-related header by data link layer, and then relayed up to the transaction layer to extract out the transaction header. According to the address or ID embedded in the transaction header, the entire transaction packets are forwarded to the destination VPPB for formatting as a serial-type PCIe packet through the transmit circuits in the data link layer and physical layer. The following sections describe these function elements for processing PCIe packets within the Switch.

6.1 PHYSICAL LAYER CIRCUIT

The physical layer circuit design is based on the **P**HY **I**nterface for **P**CI **E**xpress Architecture (PIPE). It contains Physical Media Attachment (PMA) and Physical Coding Sub-layer (PCS) blocks. PMA includes Serializer/ Deserializer (SERDES), PLL[1], Clock Recovery module, receiver detection circuits, beacon transmitter, electrical idle detector, and input/output buffers. PCS consists of framer, 8B/10B encoder/decoder, receiver elastic buffer, and PIPE PHY control/status circuitries. To provide the flexibility for port configuration, each lane has its own control and status signals for MAC to access individually. The main functions of physical layer circuits include the conversion between serial-link and parallel bus, provision of clock source for the Switch, resolving clock difference in receiver end, and detection of physical layer errors.

In order to meet the needs of different application, the drive amplitude, de-emphasis and equalization of each transmitting channels can be adjusted using EEPROM, SMBUS or I2C individually. De-emphasis of -3.5 db is implemented by the transmitters when full swing signaling is used, while an offset can be individually applied to each channel.

6.1.1 RECEIVER DETECTION

The physical layer circuits implement receiver detection, which detects the presence of an attached 50 ohm to ground termination as per PCI Express Specification. The detect circuits determine if the voltage levels of the receiver have crossed the internal threshold after a configurable time determined by the Receiver Detection Threshold field in the PHY Parameter 2 Register (offset 858h, bit[6:4]) as listed in Table 6-1, which can be configured by EEPROM, SMBUS or I2C settings.

Table 6-1 Receiver Detection Threshold Settings

Receiver Detection Threshold	Threshold
000	1.0 us
001	2.0 us
010	4.0 us (Recommended)
011	5.0 us
100	7.0 us
101	Reserved
110	Reserved
111	Reserved

[1] Multiple lanes could share the PLL.

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6.1.2 RECEIVER SIGNAL DETECTION

Receiver signal idling is detected with levels above a programmable threshold specified by Receiver Signal Detect field in the PHY Parameter 2 Register (offset 858h, bit[21:20]) as listed in Table 6-3, and can be configured on a per-port basis via EEPROM, SMBUS or I2C settings.

Table 6-2 Receiver Signal Detect Threshold

Receiver Signal Detect	Min (mV ppd)	Max (mV ppd)
00	50	150
01 (Recommended)	65	175
10	75	200
11	120	240

6.1.3 RECEIVER EQUALIZATION

The receiver implements programmable equalizer via the Receiver Equalization field in the PHY Parameter 2 Register (offset 858h, bit[25:22] and bit[29:26]) as listed in Table 6-5, which can be configured on a per-port basis via EEPROM, SMBUS or I2C settings.

Table 6-3 Receiver Equalization Settings

Receiver Equalization	Equalization
0000 (Recommended)	Off
0010	Low
0110	Medium
1110	High

6.1.4 TRANSMITTER SWING

The PCI Express transmitters support implementations of both full voltage swing and half (low) voltage swing. In full swing signaling mode, the transmitters implement de-emphasis, while in half swing mode, the transmitters do not. The Transmitter Swing field in the PHY Parameter 2 Register (offset 858h, bit[30]) is used for the selection of full swing signaling or half swing signaling, which can be configured on a per-port basis via EEPROM, SMBUS or I2C settings.

Table 6-4 Transmitter Swing Settings

Transmitter Swing	Mode	De-emphasis
0	Full Voltage Swing	Implemented
1	Half Voltage Swing	Not implemented

6.1.5 DRIVE AMPLITUDE AND DE-EMPHASIS SETTINGS

Depending on the operation condition (voltage swing and de-emphasis condition), one of the Drive Amplitude Base Level fields in the PHY Parameter 0 Register (offset 8B0h) and one of the Drive De-Emphasis Base Level fields in the PHY Parameter 1 Register (offset 854h) are active for configuration of the amplitude and de-emphasis.

In addition, optional offset values can be added to the drive amplitude and drive de-emphasis on a per-port basis via EEPROM settings. The final drive amplitude and drive de-emphasis are the summation of the base level value and the offset value. The offset value for drive amplitude is 25 mV pd, and 6.25 mV pd for drive de-emphasis.

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The driver output waveform is the synthesis of amplitude and de-emphasis as shown in Figure 6-1. The driver amplitude without de-emphasis is specified as a peak differential voltage level (mVpd), and the driver de-emphasis modifies the driver amplitude.

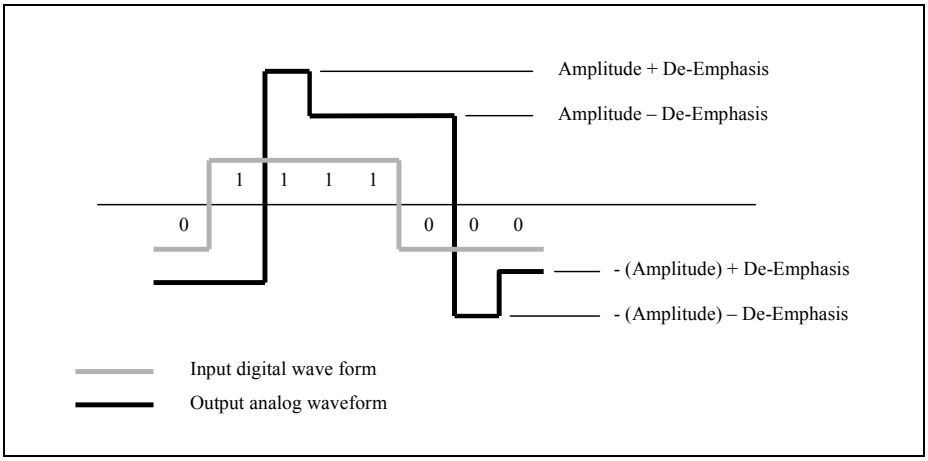

Figure 6-1 Driver Output Waveform

6.1.6 DRIVE AMPLITUDE

Only one of the Drive Amplitude Level field in the PHY Parameter 0 Register (offset 8B0h, bit[20:16], bit[25:21] and bit[30:26]) listed in Table 6-8 is active depending on the de-emphasis and swing condition. The settings and the corresponding values of the amplitude level are listed in Table 6-9, which can be configured by EEPROM, SMBUS or I2C settings.

Table 6-5 Drive Amplitude Base Level Registers

Active Register	De-Emphasis Condition	Swing Condition
Drive Amplitude Level (3P5 Nom)	-3.5 db	Full
Drive Amplitude Level (6P0 Nom)	-6.0 db	Full
Drive Amplitude Level (Half)	N/A	Half

Table 6-6 Drive Amplitude Base Level Settings

Setting	Amplitude (mV pd)	Setting	Amplitude (mV pd)	Setting	Amplitude (mV pd)
00000	0	00111	175	01110	350
00001	25	01000	200	01111	375
00010	50	01001	225	10000	400
00011	75	01010	250	10001	425
00100	100	01011	275	10010	450
00101	125	01100	300	10011	475
00110	150	01101	325	Others	Reserved

Note:
1. Nominal levels. Actual levels will vary with temperature, voltage and board effects.
2. The maximum nominal amplitude of the output driver is 475 mV pd. Combined values of driver amplitude and de-emphasis greater than 475 mV pd should be avoided.
3. At higher amplitudes, actual swings will be less than the theoretical value due to process variations and environment factors, such as voltage overhead compression, package losses, board losses, and other effects.

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6.1.7 DRIVE DE-EMPHASIS

The Drive De-Emphasis Level field in the PHY Parameter 1 Register (offset 854h, bit[20:16], bit[25:21] and bit[30:26]) listed in Table 6-12 controls the de-emphasis base level. The settings and the corresponding values of the de-emphasis level are listed in Table 6-13, which can be configured by EEPROM, SMBUS or I2C settings.

Table 6-7 Drive De-Emphasis Base Level Register

Register	De-Emphasis Condition
C_EMP_POST_GEN1_3P5_NOM	-3.5 db
C_EMP_POST_GEN2_3P5_NOM	-3.5 db
C_EMP_POST_GEN2_6P0_NOM	-6.0 db

Table 6-8 Drive De-Emphasis Base Level Settings

Setting	De-Emphasis (mV pd)	Setting	De-Emphasis (mV pd)	Setting	De-Emphasis (mV pd)
00000	0.0	01011	68.75	10110	137.5
00001	6.25	01100	75.0	10111	143.75
00010	12.5	01101	81.25	11000	150.0
00011	18.75	01110	87.5	11001	156.25
00100	25.0	01111	93.75	11010	162.5
00101	31.25	10000	100.0	11011	168.75
00110	37.5	10001	106.25	11100	175.0
00111	43.75	10010	112.5	11101	181.25
01000	50.0	10011	118.75	11110	187.5
01001	56.25	10100	125.0	11111	194.75
01010	62.5	10101	131.25	-	-

Note:
1. Nominal levels. Actual levels will vary with temperature, voltage and board effects.
2. The maximum nominal amplitude of the output driver is 475 mV pd. Combined values of driver amplitude and de-emphasis greater than 475 mV pd should be avoided.
3. At higher amplitudes, actual swings will be less than the theoretical value due to process variations and environment factors, such as voltage overhead compression, package losses, board losses, and other effects.

6.1.8 TRANSMITTER ELECTRICAL IDLE LATENCY

After the last character of the PCI Express transmission, the output current is reduced, and a differential voltage of less than 20 mV with common mode of VTX-CM-DC is established within 20 UI. This delay time is programmable via Transmitter PHY Latency field in the PHY Parameter 2 Register (offset 858h, bit[3:0]), which can be configured by EEPROM, SMBUS or I2C settings.

6.2 DATA LINK LAYER (DLL)

The Data Link Layer (DLL) provides a reliable data transmission between two PCI Express points. An ACK/NACK protocol is employed to guarantee the integrity of the packets delivered. Each Transaction Layer Packet (TLP) is protected by a 32-bit LCRC for error detection. The DLL receiver performs LCRC calculation to determine if the incoming packet is corrupted in the serial link. If an LCRC error is found, the DLL transmitter would issue a NACK data link layer packet (DLLP) to the opposite end to request a re-transmission, otherwise an ACK DLLP would be sent out to acknowledge on reception of a good TLP.

In the transmitter, a retry buffer is implemented to store the transmitted TLPs whose corresponding ACK/NACK DLLP have not been received yet. When an ACK is received, the TLPs with sequence number equals to and smaller than that carried in the ACK would be flushed out from the buffer. If a NACK is received or no ACK/NACK is returned from the link partner after the replay timer expires, then a replay mechanism built in DLL transmitter is

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triggered to re-transmit the corresponding packet that receives NACK or time-out and any other TLP transmitted after that packet.

Meanwhile, the DLL is also responsible for the initialization, updating, and monitoring of the flow-control credit. All of the flow control information is carried by DLLP to the other end of the link. Unlike TLP, DLLP is guarded by 16-bit CRC to detect if data corruption occurs.

In addition, the Media Access Control (MAC) block, which is consisted of LTSSM, multiple lanes de-skew, scrambler/de-scrambler, clock correction from inserting skip order-set, and PIPE-related control/status circuits, is implemented to interface physical layer with data link layer.

6.3 TRANSACTION LAYER RECEIVE BLOCK (TLP DECAPSULATION)

The receiving end of the transaction layer performs header information retrieval and TC/VC mapping (see section 5.5), and it validates the correctness of the transaction type and format. If the TLP is found to contain an illegal header or the indicated packet length mismatches with the actual packet length, then a Malformed TLP is reported as an error associated with the receiving port. To ensure end-to-end data integrity, a 32-bit ECRC is checked against the TLP at the receiver if the digest bit is set in header.

6.4 ROUTING

The transaction layer implements three types of routing protocols: ID-based, address-based, and implicit routing. For configuration reads, configuration writes, transaction completion, and user-defined messages, the packets are routed by their destination ID constituted of bus number, device number, and function number. Address routing is employed to forward I/O or memory transactions to the destination port, which is located within the address range indicated by the address field carried in the packet header. The packet header indicates the packet types including memory read, memory write, IO read, IO write, Message Signaling Interrupt (MSI) and user-defined message. Implicit routing is mainly used to forward system message transactions such as virtual interrupt line, power management, and so on. The message type embedded in the packet header determines the routing mechanism.

If the incoming packet cannot be forwarded to any other port due to a miss to hit the defined address range or targeted ID, this is considered as Unsupported Request (UR) packet, which is similar to a master abort event in PCI protocol.

6.5 TC/VC MAPPING

The 3-bit TC field defined in the header identifies the traffic class of the incoming packets. To enable the differential service, a TC/VC mapping table at destination port that is pre-programmed by system software or EEPROM pre-load is utilized to cast the TC labeled packets into the desired virtual channel. Note that TC0 traffic is mapped into VC0 channel by default. After the TC/VC mapping, the receive block dispatches the incoming request, completion, or data into the appropriate VC0 and VC1 queues.

6.6 QUEUE

In PCI Express, it defines six different packet types to represent request, completion, and data. They are respectively Posted Request Header (PH), Posted Request Data payload (PD), Non-Posted Request Header (NPH), Non-Posted Data Payload (NPD), Completion Header (CPLH) and Completion Data payload (CPLD). Each packet with different type would be put into a separate queue in order to facilitate the following ordering processor. Since NPD

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usually contains one DW, it can be merged with the corresponding NPH into a common queue named NPHD. Except NPHD, each virtual channel (VC0 or VC1) has its own corresponding packet header and data queue. When only VC0 is needed in some applications, VC1 can be disabled and its resources assigned to VC0 by asserting VC1_EN (Virtual Channel 1 Enable) to low.

6.6.1 PH

PH queue provides TLP header spaces for posted memory writes and various message request headers. Each header space occupies sixteen bytes to accommodate 3 DW or 4 DW headers. There are two PH queues for VC0 and VC1 respectively.

6.6.2 PD

PD queue is used for storing posted request data. If the received TLP is of the posted request type and is determined to have payload coming with the header, the payload data would be put into PD queue. There are two PD queues for VC0 and VC1 respectively.

6.6.3 NPHD

NPHD queue provides TLP header spaces for non-posted request packets, which include memory read, IO read, IO write, configuration read, and configuration write. Each header space takes twenty bytes to accommodate a 3-DW header, s 4-DW header, s 3-WD header with 1-DW data, and a 4-DW header with 1-DW data. There is only one NPHD queue for VC0, since non-posted request cannot be mapped into VC1.

6.6.4 CPLH

CPLH queue provides TLP header space for completion packets. Each header space takes twelve bytes to accommodate a 3-DW header. Please note that there are no 4-DW completion headers. There are two CPLH queues for VC0 and VC1 respectively.

6.6.5 CPLD

CPLD queue is used for storing completion data. If the received TLP is of the completion type and is determined to have payload coming with the header, the payload data would be put into CPLD queue. There are two CPLD queues for VC0 and VC1 respectively.

6.7 TRANSACTION ORDERING

Within a VPPB, a set of ordering rules is defined to regulate the transactions on the PCI Express Switch including Memory, IO, Configuration and Messages, in order to avoid deadlocks and to support the Producer-Consumer model. The ordering rules defined in table 6-9 apply within a single Traffic Class (TC). There is no ordering requirement among transactions within different TC labels. Since the transactions with the same TC label are not allowed to map into different virtual channels, it implies no ordering relationship between the traffic in VC0 and VC1.

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Table 6-9 Summary of PCI Express Ordering Rules

Row Pass Column	Posted Request	Read Request	Non-posted Write Request	Read Completion	Non-posted Write Completion
Posted Request	Yes/No[1]	Yes[5]	Yes[5]	Yes[5]	Yes[5]
Read Request	No[2]	Yes	Yes	Yes	Yes
Non-posted Write Request	No[2]	Yes	Yes	Yes	Yes
Read Completion	Yes/No[3]	Yes	Yes	Yes	Yes
Non-Posted Write Completion	Yes[4]	Yes	Yes	Yes	Yes

1. When the Relaxed Ordering Attribute bit is cleared, the Posted Request transactions including memory write and message request must complete on the egress bus of VPPB in the order in which they are received on the ingress bus of VPPB. If the Relaxed Ordering Attribute bit is set, the Posted Request is permitted to pass over other Posted Requests occurring before it.

2. A Read Request transmitting in the same direction as a previously queued Posted Request transaction must push the posted write data ahead of it. The Posted Request transaction must complete on the egress bus before the Read Request can be attempted on the egress bus. The Read transaction can go to the same location as the Posted data. Therefore, if the Read transaction were to pass the Posted transaction, it would return stale data.

3. When the Relaxed Ordering Attribute bit is cleared, a Read completion must ‘‘pull’’ ahead of previously queued posted data transmitting in the same direction. In this case, the read data transmits in the same direction as the posted data, and the requestor of the read transaction is on the same side of the VPPB as the completer of the posted transaction. The posted transaction must deliver to the completer before the read data is returned to the requestor. If the Relaxed Ordering Attribute bit is set, then a read completion is permitted to pass a previously queued Memory Write or Message Request.

4. Non-Posted Write Completions are permitted to pass a previous Memory Write or Message Request transaction. Such transactions are actually transmitting in the opposite directions and hence have no ordering relationship.

5. Posted Request transactions must be given opportunities to pass Non-posted Read and Write Requests as well as Completions. Otherwise, deadlocks may occur when some older bridges, which do not support delayed transactions are mixed with PCIe Switch in the same system. A fairness algorithm is used to arbitrate between the Posted Write queue and the Non-posted transaction queue

6.8 PORT ARBITRATION

Among multiple ingress ports, the port arbitration built in the egress port determines which incoming packets to be forwarded to the output port. The arbitration algorithm contains hardware fixed Round Robin, 128-phase Weighted Round-Robin and programmable 128-phase time-based WRR. The port arbitration is held within the same VC channel. It means that each port has two port arbitration circuitries for VC0 and VC1 respectively. At the upstream ports, in addition to the inter-port packets, the intra-port packet such as configurations completion would also join the arbitration loop to get the service from Virtual Channel 0.

6.9 VC ARBITRATION

After port arbitration, VC arbitration is executed among different VC channels within the same source. Three arbitration algorithms are provided to choose the appropriate VC: Strict Priority, Round Robin or Weighted Round Robin.

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6.10 FLOW CONTROL

PCI Express employs Credit-Based Flow Control mechanism to make buffer utilization more efficient. The transaction layer transmitter ensures that it does not transmit a TLP to an opposite receiver unless the receiver has enough buffer space to accept the TLP. The transaction layer receiver has the responsibility to advertise the free buffer space to an opposite transmitter to avoid packet stale. In this Switch, each port has its own separate queues for different traffic types and the credits are sent to data link layer on the fly. The data link layer compares the current available credits with the monitored ones and reports the updated credit to the counterpart. If no new credit is acquired, the credit reported is scheduled for every 30 us to prevent the link from entering retrain. On the other hand, the receiver at each egress port gets the usable credits from the opposite end in a link. The output port broadcasts them to all the other ingress ports to get packet transmission.

6.11 TRANSATION LAYER TRANSMIT BLOCK (TLP ENCAPSULATION)

The transmit portion of transaction layer performs the following functions. They construct the all types of forwarded TLP generated from VC arbiter, respond with the completion packets when the local resource (i.e. configuration register) is accessed, and regenerate the message that terminates at receiver to RC if acting as an upstream port.

6.12 Access Control Service

Traditionally, the packet routing between the peer-to-peer downstream ports is determined by either the address or ID field embedded in the packet header. ACS provides a mechanism for customer to selectively control access between PCI Express Endpoints attached to the downstream ports of packet switch. If ACS is enabled in the ingress port, the peer-to-peer packet forwarding will follow the rule sets of ACS rather than the destination ID or address. ACS is implemented as a set of capabilities and control registers in the associated hardware component. It brings the following benefits such as preventing the silent data corruption presented in Requests from being incorrectly routed to a peer Endpoint, validating every Request transaction between two downstream components and enabling direct routing of peer-to-peer Memory Requests whose addresses have been Translated when ATS system is being used.

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7 EEPROM INTERFACE AND SYSTEM MANAGEMENT/I2C BUS

The EEPROM interface consists of four pins: EESK (EEPROM clock), EEDI (EEPROM serial data input), EEDO (EEPROM serial data output) and EECS (EEPROM chip select). The Switch supports 2-, or 3-byte address SPI EEPROM parts and automatically determines the appropriate addressing mode. The EEPROM is used to initialize a number of registers before enumeration. This is accomplished after PERST_L is de-asserted, at which time the data from the EEPROM is loaded. The EEPROM interface is organized into a 16-bit base, and the Switch supplies an 8-bit EEPROM word address.

7.1 EEPROM INTERFACE

7.1.1 AUTO MODE EEPROM ACCESS

The Switch may access the EEPROM in a WORD format by utilizing the auto mode through a hardware sequencer. The EEPROM start-control, address, and read/write commands can be accessed through the configuration register. Before each access, the software should check the Autoload Status bit before issuing the next start.

7.1.2 EEPROM MODE AT RESET

During a reset, the Switch will automatically load the information/data from the EEPROM if the automatic load condition is met. The first offset in the EEPROM contains a signature. If the signature is recognized, the autoload initiates right after the reset.

During the autoload, the Bridge will read sequential words from the EEPROM and write to the appropriate registers. Before the Bridge registers can be accessed through the host, the autoload condition should be verified by reading bit [4] offset 87Ch (EEPROM Autoload Status). The host access is allowed only after the status of this bit is set to '1' which indicates that the autoload initialization sequence is complete.

7.1.3 EEPROM SPACE ADDRESS MAP

EEPROM Address	Value	Description
00h	1516h	EEPROM signature
02h	EEPROM_BYTE_SIZE	EEPROM size byte count
04h	CFG_OFFSET_ADDR	1st Configuration Register Address Bit[9:0]: configuration register dword address Bit[15:10]: port number
06h	CFG_LOW_DATA	1st Configuration Register Data (low word)
08h	CFG_HIGH_DATA	1st Configuration Register Data (high word)
0Ah	CFG_OFFSET_ADDR	2nd Configuration Register Address
0Ch	CFG_LOW_DATA	2nd Configuration Register Data (low word)
0Eh	CFG_HIGH_DATA	2nd Configuration Register Data (high word)
…	…	…
FFFFh	CFG_HIGH_DATA	Last Configuration Register Data (high word)

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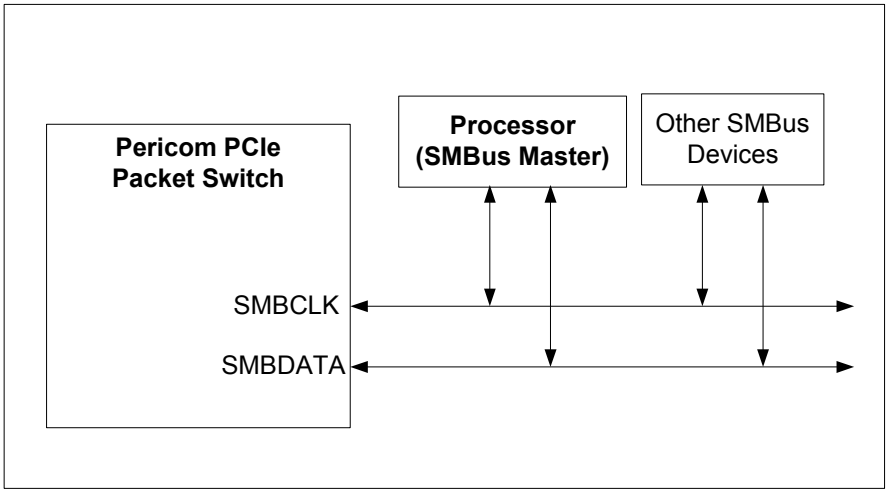
7.2 SMBUS INTERFACE

The Packet Switch provides the System Management Bus (SMBus), a two-wire interface through which a simple device can communicate with the rest of the system. The SMBus interface on the Packet Switch is a bi-directional slave interface. It can receive data from the SMBus master or send data to the master. The interface allows full access to the configuration registers. A SMBus master, such as the processor or other SMBus devices, can read or write to every RW configuration register (read/write register). In addition, the RO and HwInt registers (read-only and hardware initialized registers) that can be auto-loaded by the EEPROM interface can also be read and written by the SMBus interface. This feature allows increases in the system expandability and flexibility in system implementation.

Figure 7-1 SMBus Architecture Implementation



The SMBus interface on the Packet Switch consists of one SMBus clock pin (SCL_I2C), a SMBus data pin (SDA_I2C), and 3 SMBus address pins (I2C_ADDR[2:0]). The SMBus clock pin provides or receives the clock signal. The SMBus data pin facilitates the data transmission and reception. Both of the clock and data pins are bi-directional. The SMBus address pins determine the address to which the Packet Switch responds to. The SMBus address pins generate addresses according to the following table:

Table 7-1 SMBus Address Pin Configuration

BIT	SMBus Address
0	I2C_ADDR[0]
1	I2C_ADDR[1]
2	I2C_ADDR[2]
3	1
4	1
5	1
6	0

Software can change the SMBus Slave address, by programming the SMBus/I2C Control Register SMBus/I2C Device Address field.

The PI7C9X2G912GP also supports Packet Error Checking and Packet Error Code (PEC) generation, as explained in the SMBus v2.0.

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PI7C9X2G912GP supports three commands:

- Block Write (command BEh) is used to write CFG registers
- Block Write (command BAh), followed by Block Read (command BDh), are used to read CFG registers
- Block Read - Block Write Process Call (commands BAh, CDh) can also be used to read CFG registers

7.2.1 SMBUS BLOCK WRITE

The Block Write command is used to write to the PI7C9X2G912GP registers. General SMBus Block Writes are illustrated in Figure 7-2 and Figure 7-3. Table 7-2 explains the elements used in Figure 7-2 and Figure 7-3.

Figure 7-2 SMBus Block Write Command Format, to Write to a PI7C9X2G912GP Register without PEC

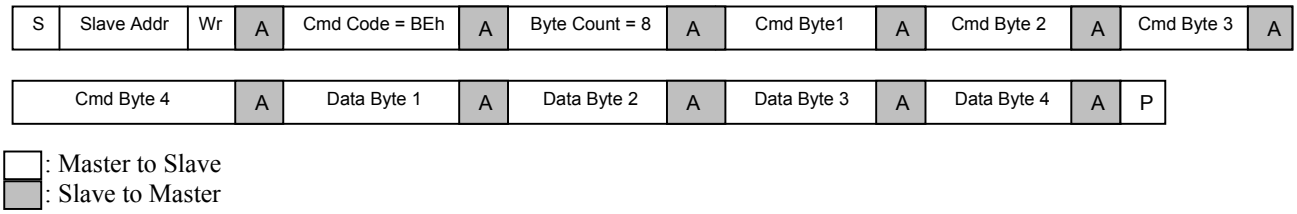
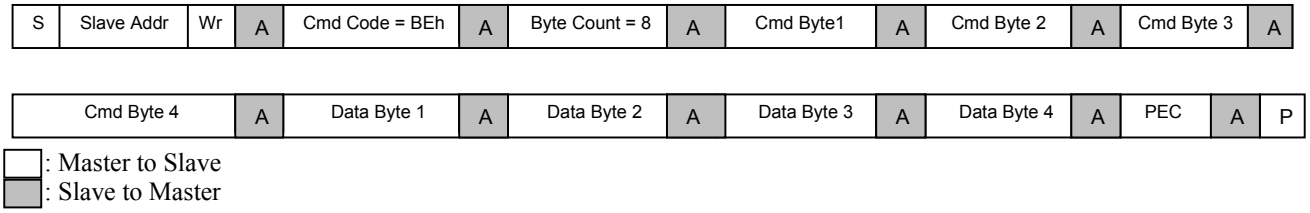


Figure 7-3 SMBus Block Write Command Format, to Write to a PI7C9X2G912GP Register with PEC



Block Write transactions that are received with incorrect Cmd Code are NACKed, starting from the wrong byte setting, and including subsequent bytes in the packet. For example, if the Byte Count value is not 8, the PI7C9X2G912GP NACKs the byte corresponding to the Byte Count value, as well as any Data bytes following within the same packet.

The byte after Data Byte 4, if present, is taken as the PEC byte, and if present, the PEC is checked. If a packet fails Packet Error Checking, the PI7C9X2G912GP drops the packet (ignores the Write), and returns NACK for the PEC byte, to the SMBus Master. Packet Error Checking can be disabled, by setting the SMBus/I^{2}C Control Register PEC Check Disable bit. The Byte Count value, by definition, does not include the PEC byte.

Table 7-2 Bytes for SMBus Block Write

Field (Byte) On Bus	Bit(s)	Value/ Description
S	1	**START** condition
P	1	**STOP** condition
A	1	**Acknowledge** (this bit position may be 0 for an ACK or 1 for a NACK)
Command Code	7:0	**BEh** for Block Write
Byte Count	7:0	**08h** = 8 bytes to follow (4 Command and 4 Data bytes). The PEC byte is not counted.
Command Byte 1	7:3	**Reserved**
	2:0	**Command** 011b = Write register 100b = Read register
	7:4	**Reserved**
	3:0	**Port Select[4:1]**

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Command Byte 2		2nd Command byte, bits [3:0], and 3rd Command byte, bit 7, combine to form a 5-bit Port Select.
Command Byte 3	7	**Port Select[0]** 2nd Command byte, bits [3:0], and 3rd Command byte, bit 7, combine to form a 5-bit Port Select. Port Select[4:0] is used to select Port to access. 00h, 02h, 03h – Port 0, Port 2, Port 3 0Ah~0Fh – Port 10 ~ Port 15 01h, 04h-09h and 11h – 1Fh are reserved
	6	**Reserved**
	5:2	**Byte Enable** **Bit** **Description** 2 Byte Enable for Data Byte 4 (PI7C9X2G912GP register bits [7:0]) 3 Byte Enable for Data Byte 3 (PI7C9X2G912GP register bits [15:8]) 4 Byte Enable for Data Byte 2 (PI7C9X2G912GP register bits [23:16]) 5 Byte Enable for Data Byte 1 (PI7C9X2G912GP register bits [31:24]) 0 = Corresponding PI7C9X2G912GP register byte will not be modified 1 = Corresponding PI7C9X2G912GP register byte will be modified
	1:0	**PI7C9X2G912GP Register Address [11:10]**
Command Byte 4	7:0	**PI7C9X2G912GP Register Address [9:2]** Note: Address bits[1:0] are fixed to 0.
Data Byte 1	7:0	**Data write to register bits [31:24]**
Data Byte 2	7:0	**Data write to register bits [23:16]**
Data Byte 3	7:0	**Data write to register bits [15:8]**
Data Byte 4	7:0	**Data write to register bits [7:0]**
PEC	7:0	**Packet Error Code**

Table 7-3 is a sample to write SSID/SSVID register (offset F8h) in Port 1. The register value is 1234_5678h, with all bytes enabled, and without PEC. The default SMBus Address is 1101000b.

Table 7-3 Sample SMBus Block Write Byte Sequence

Byte Number	Byte Type	Value	Description
1	Address	70h	Bits [7:1] for the PI7C9X2G912GP default Slave address of 38h, with bit 0 Cleared to indicate a Write.
2	Command Code	BEh	Command Code for register Write, using a Block Write
3	Byte Count	08h	Byte Count. Four Command Bytes and Four Data Bytes
4	Command Byte 1	03h	For Write command
5	Command Byte 2	00h	Bits [3:0] - Port Select [4:1] (for Port 1)
6	Command Byte 3	BCh	Bit 7 is Port Select[0] Bit 6 is reserved Bits [5:2] are the for Byte Enables; all are active Bits [1:0] are register Address bits [11:10]
7	Command Byte 4	3Eh	PI7C9X2G912GP Register Address bits [9:2] (for offset F8h)
8	Data Byte 1	12h	Data Byte for register bits [31:24]
9	Data Byte 2	34h	Data Byte for register bits [23:16]
10	Data Byte 3	56h	Data Byte for register bits [15:8]
11	Data Byte 4	78h	Data Byte for register bits[7:0]

7.2.2 SMBUS BLOCK READ

A Block Read command is used to read PI7C9X2G912GP CFG registers. Similar to CFG register Reads using I^2C, a SMBus Write sequence must first be performed to select the register to read, followed by a SMBus Read of the corresponding register. There are two ways a PI7C9X2G912GP register can be read:

- Use a Block Write, followed by a Block Read. The Block Write sets up the parameters including Port Number, register address and Byte Enables, and the Block Read performs the actual Read operation.
- Use a Block Read - Block Write Process Call. This command is defined by the SMBus v2.0, and performs a Block Write and Block Read, using a single command. The Block Write portion of the message sets up the

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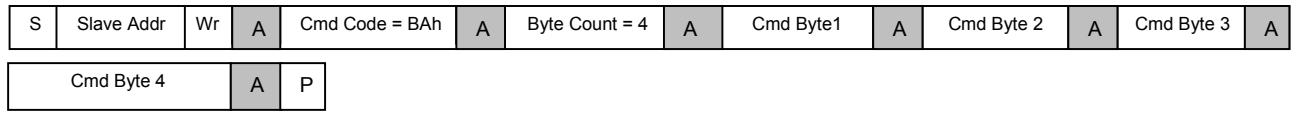
register to be read, and then a repeated START followed by the Block Read portion of the message returns the register data specified by the Block Write

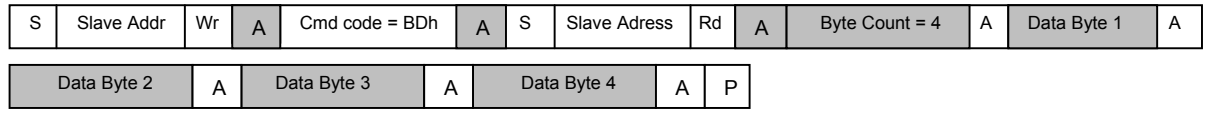
The PI7C9X2G912GP always NACKs any incorrect command sequences, starting with the wrong Byte. Upon receiving the Block Read command, the PI7C9X2G912GP returns a PEC to the Master, if after the 4th byte of register data, the Master still requests one more Byte. As a Slave, the PI7C9X2G912GP recognizes the end of the Master's Read cycle, by observing the Master's NACK response for the last Data Byte transmitted by the PI7C9X2G912GP.

Incorrect command sequences are always NACK, starting with the byte that is incorrect. (Refer to Table 7-4.) On the Block Read command, a PEC is returned to the Master, if after the 4th byte of CSR data, the return Master still requests for one additional byte. As a Slave, the PI7C9X2G912GP will know the end of the Master Read cycle, by observing the NACK for the last byte read from the Master.

Figure 7-4 SMBus Block Write to Set up Read, and Resulting Read that Returns CFG Register Value



A Block Write to set up Read



A Block Read which returns CFG Register Value

: Master to Slave
: Slave to Master

Table 7-4 Bytes for SMBus Block Read

Field (Byte) On Bus	Bit(s)	Value/ Description
S	1	**START** condition
P	1	**STOP** condition
A	1	**Acknowledge** (this bit position may be 0 for an ACK or 1 for a NACK)
Command Code	7:0	**BAh**, to set up Read, using Block Writes
Byte Count	7:0	**04h**, 4 Command bytes
Command Byte 1	7:3	**Reserved**
	2:0	**Command** 011b = Write register 100b = Read register
Command Byte 2	7:4	**Reserved**
	3:0	**Port Select[4:1]** 2nd Command byte, bits [3:0], and 3rd Command byte, bit 7, combine to form a 5-bit Port Select.
Command Byte 3	7	**Port Select[0]** 2nd Command byte, bits [3:0], and 3rd Command byte, bit 7, combine to form a 5-bit Port Select. Port Select[4:0] is used to select Port to access. 00h, 01h, 03h – Port 0, Port 1, Port 3 0Ah~0Fh – Port 10 ~ Port 15 01h, 04h-09h and 11h – 1Fh are reserved
	6	**Reserved**
	5:2	**Byte Enable** **Bit** **Description** 2 Byte Enable for Data Byte 4 (PI7C9X2G912GP register bits [7:0]) 3 Byte Enable for Data Byte 3 (PI7C9X2G912GP register bits [15:8])

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		4 Byte Enable for Data Byte 2 (PI7C9X2G912GP register bits [23:16]) 5 Byte Enable for Data Byte 1 (PI7C9X2G912GP register bits [31:24]) 0 = Corresponding PI7C9X2G912GP register byte will not be modified 1 = Corresponding PI7C9X2G912GP register byte will be modified
	1:0	**PI7C9X2G912GP Register Address [11:10]**
Command Byte 4	7:0	**PI7C9X2G912GP Register Address [9:2]** Note: Address bits[1:0] are fixed to 0.
Command Code	7:0	**BDh for Block Read**
Data Byte 1	7:0	**Return value for CFG register bits [31:24]**
Data Byte 2	7:0	**Return value for CFG register bits [23:16]**
Data Byte 3	7:0	**Return value for CFG register bits [15:8]**
Data Byte 4	7:0	**Return value for CFG register bits [7:0]**

Table 7-5, Table 7-6, Table 7-7 and Table 7-8 are a sample to Read SSID/SSVID register (offset F8h) in Port 1. The register value is 0000_0000h, with all bytes enabled, and without PEC. The default SMBus Address is 1101000b.

Table 7-5 SMBus Block Write Portion

Byte Number	Byte Type	Value	Description
1	Address	70h	Bits [7:1] for the PI7C9X2G912GP default Slave address of 38h, with bit 0 Cleared to indicate a Write.
2	Command Code	BAh	Command Code for register Write, using a Block Write
3	Byte Count	04h	Byte Count. Four Command Bytes
4	Command Byte 1	04h	For Read command
5	Command Byte 2	00h	Bits [3:0] - Port Select [4:1] (for Port 1)
6	Command Byte 3	BCh	Bit 7 is Port Select[0] Bit 6 is reserved Bits [5:2] are the for Byte Enables; all are active Bits [1:0] are register Address bits [11:10]
7	Command Byte 4	3Eh	PI7C9X2G912GP Register Address bits [9:2] (for offset F8h)

Table 7-6 SMBus Block Read Portion

Byte Number	Byte Type	Value	Description
1	Address	70h	Bits [7:1] value for the PI7C9X2G912GP Slave address of 38h, with bit 0 Cleared to indicate to indicate a Write.
2	Block Read Command Code	BDh	Command code for Block Read of PI7C9X2G912GP registers.

Table 7-7 SMBus Read Command following Repeat START from Master

Byte Number	Byte Type	Value	Description
1	Address	71h	Bits [7:1] value for the PI7C9X2G912GP Slave address of 38h, with bit 0 Set to indicate a Read.

Table 7-8 SMBus Return Bytes

Byte Number	Byte Type	Value	Description
1	Byte Count	04h	Four Bytes in register
2	Data Byte 1	00h	Register data [31:24]
3	Data Byte 2	00h	Register data [23:16]
4	Data Byte 3	00h	Register data [15:8]
5	Data Byte 4	00h	Register data [7:0]

7.2.3 CSR READ, USING SMBUS BLOCK READ – BLOCK WRITE PROCESS CALL

A general SMBus Block Read - Block Write Process Call sequence is illustrated in Figure 7-5. Alternatively, a general SMBus Block Read - Block Write Process Call with PEC sequence is illustrated in Figure 7-6.

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Using this command, the register to be read can be set up and read back with one SMBus cycle (a transaction with a START and ending in STOP). There is no STOP condition before the repeated START condition. The command format for the Block Write part of this command has the same sequence as in Table 7-5, except that the Command Code changes to CDh, as illustrated below. Other Bytes remain the same as used in the sequence for SMBus Block Write followed by Block Read. Table 7-9 lists the Command format for Block Read.

Figure 7-5 CSR Read Operation Using SMBus Block Read – Block Write Process Call

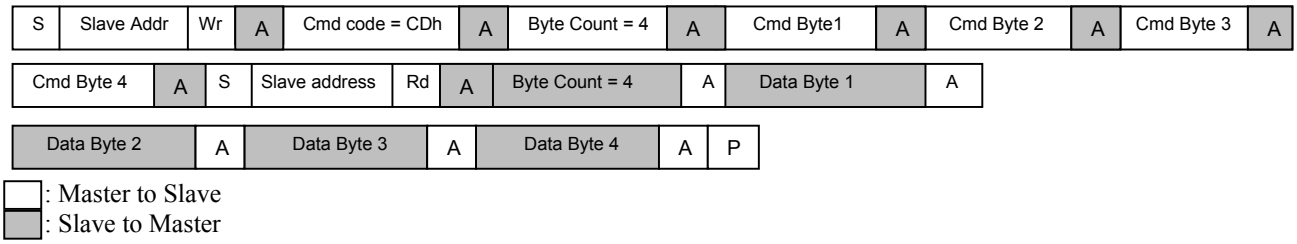

Figure 7-6 CSR Read Operation Using SMBus Block Read – Block Write Process Call with PEC

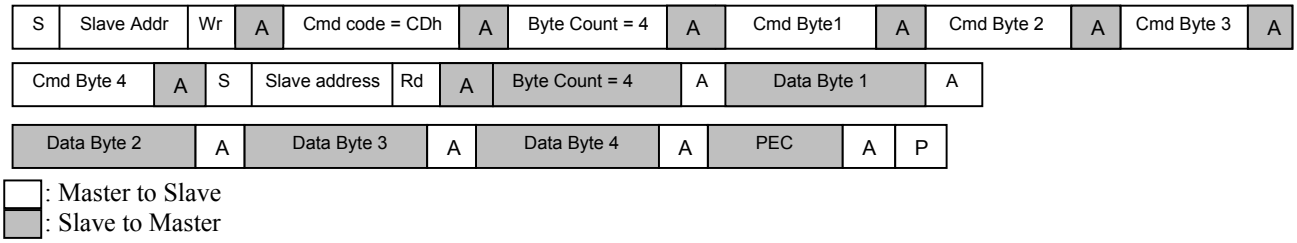

Table 7-9 Command Format for SMBus Block Read

Field (Byte) On Bus	Bit(s)	Value/Description
Command Code	7:0	CDh for Block Read (Process Call Read)

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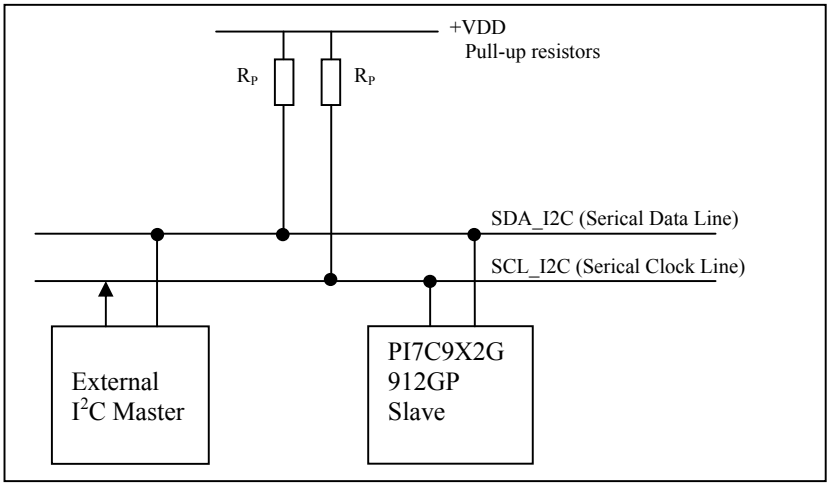
7.3 I²C SLAVE INTERFACE

Inter-Integrated Circuit (I²C) is a bus used to connect Integrated Circuits (ICs). Multiple ICs can be connected to an I²C Bus, and I²C devices that have I²C mastering capability can initiate a Data transfer. I²C is used for Data transfers between ICs at relatively low rates (100 Kbps), and is used in a variety of applications. For further details regarding I²C Buses, refer to the *I²C Bus v2.1*.

The PI7C9X2G912GP is an I²C Slave. Slave operations allow the PI7C9X2G912GP Configuration registers to be read from or written to by an I²C Master, external from the device. I²C is a sideband mechanism that allows the device Configuration registers to be programmed, read from, or written to, independent of the PCI Express upstream Link.

Figure 7-7 Standard Devices to I²C Bus Connection Block Diagram



The I²C interface on the Packet Switch consists of a I²C clock pin (SCL_I2C), a I²C data pin (SDA_I2C), and 3 I²C address pins (I2C_ADDR[2:0]). The I²C clock pin provides or receives the clock signal. The I²C data pin facilitates the data transmission and reception. Both of the clock and data pins are bi-directional. The I²C address pins determine the address to which the Packet Switch responds to. The I²C address pins generate addresses according to the following table:

Table 7-10 I²C Address Pin Configuration

BIT	I2C Address
0	I2C_ADDR[0]
1	I2C_ADDR[1]
2	I2C_ADDR[2]
3	1
4	1
5	1
6	0

Software can change the I²C Slave address, by programming the SMBus/I²C Control Register SMBus/I²C Device Address field.

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7.3.1 I²C REGISTER WRITE ACCESS

The PI7C9X2G912GP Configuration registers can be read from and written to, based upon I²C register Read and Write operations, respectively. An I²C Write packet consists of Address Phase bytes and Command Phase bytes, followed by one to four additional I²C Data bytes. Table 7-11 defines mapping of the I²C Data bytes to the Configuration register Data bytes.

The I²C packet starts with the S (START condition) bit. Data bytes are separated by the A (Acknowledge Control Packet (ACK)) or N (Negative Acknowledge (NAK)) bit. The packet ends with the P (STOP condition) bit.
If the Master generates an invalid command， the targeted PI7C9X2G912GP register is not modified.
The PI7C9X2G912GP considers the 1st Data byte of the 4-byte Data phase, following the four Command bytes in the Command phase, as register Byte 3 (bits [31:24]). The next three Data bytes access register Bytes 2 through 0, respectively. Four Data bytes are required, regardless of the Byte Enable Settings in the Command phase. The Master can then generate either a STOP condition (to finish the transfer) or a repeated START condition (to start a new transfer). If the I²C Master sends more than the four Data bytes (violating PI7C9X2G912GP protocol), further details regarding J2C protocol, the PI7C9X2G912GP returns a NAK for the extra Data byte(s).

Table 7-12 describes each I²C Command byte for Write access. In the packet described in Figure 7-8, Command Bytes 0 through 3 for Writes follow the format specified in Table 7-12.

Table 7-11 I²C Register Write Access

I2C Data Byte Order	PCI Express Configuration Register Byte
0	Written to register Byte 3
1	Written to register Byte 2
2	Written to register Byte 1
3	Written to register Byte 0

Table 7-12 I²C Command Format for Write Access

Byte	Bit(s)	Description
1st (0)	7:3	**Reserved**
	2:0	**Command** 011b = Write register
2nd (1)	7:4	**Reserved**
	3:0	**Port Select[4:1]** 2nd Command byte, bits [3:0], and 3rd Command byte, bit 7, combine to form a 5-bit Port Select.
3rd (2)	7	**Port Select[0]** 2nd Command byte, bits [3:0], and 3rd Command byte, bit 7, combine to form a 5-bit Port Select. Port Select[4:0] is used to select Port to access. 00h, 02h, 03h – Port 0, Port 2, Port 3 0Ah~0Fh – Port 10 ~ Port 15 01h, 04h-09h and 11h – 1Fh are reserved
	6	**Reserved**
	5:2	**Byte Enable** **Bit** **Description** 2 Byte Enable for Data Byte 4 (PI7C9X2G912GP register bits [7:0]) 3 Byte Enable for Data Byte 3 (PI7C9X2G912GP register bits [15:8]) 4 Byte Enable for Data Byte 2 (PI7C9X2G912GP register bits [23:16]) 5 Byte Enable for Data Byte 1 (PI7C9X2G912GP register bits [31:24]) 0 = Corresponding PI7C9X2G912GP register byte will not be modified 1 = Corresponding PI7C9X2G912GP register byte will be modified
	1:0	**PI7C9X2G912GP Register Address [11:10]**
4th (3)	7:0	**PI7C9X2G912GP Register Address [9:2]** Note: Address bits[1:0] are fixed to 0.

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Figure 7-8 I²C Write Packet

I²C Write Packet Address Phase Byte

Address Cycle			
START	**7654321**	**0**	**ACK/NAK**
S	Slave Address [7:1]	Read/Write Bit 0 = Write	A

I2C Write Packet Command Phase Byte

Command Cycle							
76543210	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**
Command Byte 0	A	Command Byte 1	A	Command Byte 2	A	Command Byte 3	A

I²C Write Packet Data Phase Byte

Write Cycle								
76543210	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**STOP**
Register Byte 3	A	Register Byte 2	A	Register Byte 1	A	Register Byte 0	A	P

The following tables illustrate a sample I2C packet for writing the PI7C9X2G912GP SSID/SSVID register (offset F8h) for Port 0, with data 1234_5678h.

Note: *The PI7C9X2G912GP has a default I²C Slave address [6:0] value of 38h, with the I2C_ADDR[2:0] input having a value of 000. The byte sequence on the I²C Bus, as listed in the following tables, occurs after the START and before the STOP bits, by which the I²C Master frames the transfer.*

Figure 7-9 I²C Register Write Access Example

I²C Register Write Access Example – Address Cycle

Phase	Value	Description
Address	70h	Bits [7:1] for PI7C9X2G912GP I²C Slave Address (38h) with last bit (bit 0) for Write = 0

I²C Register Write Access Example – Command Cycle

Byte	Value	Description
0	03h	[7:3] Reserved [2:0] Command, 011b = Write register
1	00h for Port 0	[7:4] Reserved [3:0] Port Select[4:1]
2	3Ch for Port 0	[7] Port Select[0] [6] Reserved [5:2] Byte Enable, all active. [1:0] PI7C9X2G912GP Register Address, Bits [11:10]
3	3Eh	[7:0] PI7C9X2G912GP Register Address, Bits [9:2]

I²C Register Write Access Example – Data Cycle

Byte	Value	Description
0	12h	Data to Write for Byte 3
1	34h	Data to Write for Byte 2
2	56h	Data to Write for Byte 1
3	78h	Data to Write for Byte 0

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Figure 7-10 I²C Write Command Packet Example

I²C Write Packet Address Phase Bytes

1st Cycle			
START	**7654321**	**0**	**ACK/NAK**
S	Slave Address 0111_000b	Read/Write Bit 0 = Write	A

I²C Write Packet Command Phase Bytes

Command Cycle							
76543210	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**
Command Byte 0 0000_0011b	A	Command Byte 1 0000_0000b	A	Command Byte 2 0011_1100b	A	Command Byte 3 0011_1110b	A

I²C Write Packet Data Phase Bytes

Write Cycle								
76543210	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**STOP**
Register Byte 3	A	Register Byte 2	A	Register Byte 1	A	Register Byte 0	A	P

7.3.2 I²C REGISTER READ ACCESS

When the I²C Master attempts to read a PI7C9X2G912GP register, two packets are transmitted. The 1st packet consists of Address and Command Phase bytes to the Slave. The 2nd packet consists of Address and Data Phase bytes.

According to the I²C Bus, v2.1, a Read cycle is triggered when the Read/Write bit (bit 0) of the 1st cycle is Set. The Command phase reads the requested register content into the internal buffer. When the I²C Read access occurs, the internal buffer value is transferred on to the I²C Bus, starting from Byte 3 (bits [31: 24]), followed by the subsequent bytes, with Byte 0 (bits [7:0]) being transferred last. If the I²C Master requests more than four bytes, the PI7C9X2G912GP re-transmits the same byte sequence, starting from Byte 3 of the internal buffer.

The 1st and 2nd I²C Read packets perform the following functions:

- 1st packet - Selects the register to read
- 2nd packet - Reads the register (sample 2nd packet provided is for a 7-bit PI7C9X2G912GP I²C Slave address)

Although two packets are shown for the I²C Read, the I²C Master can merge the two packets together into a single packet, by not generating the STOP at the end of the first packet (Master does not relinquish the bus) and generating REPEAT START.

Table 7-13 describes each I²C Command byte for Read access. In the packet described in Figure 7-11, Command Bytes 0 through 3 for Reads follow the format specified in Table 7-13.

Table 7-13 I²C Command Format for Read Access

Byte	Bit(s)	Description
1st (0)	7:3	**Reserved**
	2:0	**Command** 100b = Read register
2nd (1)	7:4	**Reserved**
	3:0	**Port Select, Bits [4:1]** 2nd Command byte, bit [3:0], and 3rd Command byte, bit 7, combine to form a 5-bit Port Select.
3rd (2)	7	**Port Select[0]** 2nd Command byte, bits [3:0], and 3rd Command byte, bit 7, combine to form a 5-bit Port Select.

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Byte	Bit(s)	Description
		Port Select[4:0] is used to select Port to access. 00h, 01h, 03h – Port 0, Port 1, Port 3 0Ah~0Fh – Port 10 ~ Port 15 01h, 04h-09h and 11h – 1Fh are reserved
	6	**Reserved**
	5:2	**Byte Enable** **Bit** **Description** 2 Byte Enable for Data Byte 4 (PI7C9X2G912GP register bits [7:0]) 3 Byte Enable for Data Byte 3 (PI7C9X2G912GP register bits [15:8]) 4 Byte Enable for Data Byte 2 (PI7C9X2G912GP register bits [23:16]) 5 Byte Enable for Data Byte 1 (PI7C9X2G912GP register bits [31:24]) 0 = Corresponding PI7C9X2G912GP register byte will not be modified 1 = Corresponding PI7C9X2G912GP register byte will be modified
	1:0	**PI7C9X2G912GP Register Address [11:10]**
4th (3)	7:0	**PI7C9X2G912GP Register Address [9:2]** Note: Address bits[1:0] are fixed to 0.

Figure 7-11 I²C Read Command Packet

I²C Read Command Packet Address Phase Byte (1st Packet)

1st Cycle			
START	**7654321**	**0**	**ACK/NAK**
S	Slave Address[7:1]	Read/Write Bit 0 = Write	A

I²C Read Command Packet Command Phase Byte (1st Packet)

Write Cycle							
76543210	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**
Command Byte 0	A	Command Byte 1	A	Command Byte 2	A	Command Byte 3	A

I²C Read Data Packet Address Phase Byte (2nd Packet)

1st Cycle			
START	**7654321**	**0**	**ACK/NAK**
S	Slave Address[7:1]	Read/Write Bit 1 = Read	A

I²C Read Data Packet Data Phase Byte (2nd Packet)

Write Cycle								
76543210	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**STOP**
Register Byte 3	A	Register Byte 2	A	Register Byte 1	A	Register Byte 0	A	P

The following tables illustrate a sample I2C packet for reading the PI7C9X2G912GP SSID/SSVID register (offset F8h) for Port 0. The default value for SSID/SSVID register is 0000_0000h.

Note: *The PI7C9X2G912GP has a default I²C Slave address [6:0] value of 38h, with the I2C_ADDR[2:0] inputs having a value of 000. The byte sequence on the I²C Bus, as listed in the following tables, occurs after the START and before the STOP bits, by which the I²C Master frames the transfer.*

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Figure 7-12 I²C Register Read Access Example

I²C Register Read Access Example – Address Cycle (1st Packet)

Phase	Value	Description
Address	70h	Bits [7:1] for PI7C9X2G912GP I²C Slave Address (38h) with last bit (bit 0) for Write = 0

I²C Register Read Access Example – Command Cycle (1st Packet)

Byte	Value	Description
0	04h	[7:3] Reserved [2:0] Command , 100b = Read register
1	00h for Port 0	[7:4] Reserved [3:0] Port Select[4:1]
2	3Ch for Port 0	[7] Port Select[0] [6] Reserved [5:2] Byte Enable, All active. [1:0] PI7C9X2G912GP Register Address, Bits [11:10]
3	3Eh	[7:0] PI7C9X2G912GP Register Address, Bits [9:2]

I²C Register Read Access Example – 2nd Packet

Phase	Value	Description
Address	71h	Bits [7:1] for PI7C9X2G912GP I2C Slave Address (38h) with last bit (bit 0) for Read = 1
Read	00h	Byte 3 of Register Read
	00h	Byte 2 of Register Read
	00h	Byte 1 of Register Read
	00h	Byte 0 of Register Read

Figure 7-13 I²C Read Command Packet

I²C Read Command Packet Address Phase Bytes (1st Packet)

1st Cycle			
START	**7654321**	**0**	**ACK/NAK**
S	Slave Address 0111_000b	Read/Write Bit 0 = Write	A

I²C Read Command Packet Command Phase Bytes (1st Packet)

Command Cycle						
76543210	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**
Command Byte 0 0000_0100b	A	Command Byte 1 0000_0000b	A	Command Byte 2 0011_1100b	A	Command Byte 3 0011_1110b

I²C Read Data Packet Address Phase Bytes (2nd Packet)

1st Cycle			
START	**7654321**	**0**	**ACK/NAK**
S	Slave Address [7:1] 0111_000b	Read/Write Bit 1 = Read	A

I²C Read Data Packet Data Phase Bytes (2nd Packet)

Command Cycle							
76543210	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**ACK/NAK**	**76543210**	**Stop**
Register Byte3 0000_0000b	A	Register Byte2 0000_0000b	A	Register Byte1 0000_0000b	A	Register Byte0 0000_00000b	P

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8 REGISTER DESCRIPTION

8.1 REGISTER TYPES

This chapter details the Packet Switch registers, including
- Bit names
- Description of register functions
- Type, refer to Table 8-1
- Whether the default value can be modified by EEPROM and/or I2C/SMBUS
- Default value

Table 8-1 Register Types

REGISTER TYPE	DEFINITION
HwInt	Hardware Initialization
RO	Read Only
RW	Read / Write
RW1C	Read / Write 1 to Clear
RsvdP	RO and must return 0 when read.

8.2 TRANSPARENT MODE CONFIGURATION REGISTERS

When the port of the Switch is set to operate at the transparent mode, it is represented by a logical PCI-to-PCI Bridge that implements type 1 configuration space header. The following table details the allocation of the register fields of the PCI 2.3 compatible type 1 configuration space header.

31 –24	23 – 16	15 – 8	7 –0	BYTE OFFSET
Device ID		Vendor ID		00h
Primary Status		Command		04h
Class Code			Revision ID	08h
Reserved	Header Type	Primary Latency Timer	Cache Line Size	0Ch
Base Address 0 for Upstream Port) / Reserved for Downstream Ports				10h
Base Address 1 for Upstream Port) / Reserved for Downstream Ports				14h
Secondary Latency Timer	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number	18h
Secondary Status		I/O Limit Address	I/O Base Address	1Ch
Memory Limit Address		Memory Base Address		20h
Prefetchable Memory Limit Address		Prefetchable Memory Base Address		24h
Prefetchable Memory Base Address Upper 32-bit				28h
Prefetchable Memory Limit Address Upper 32-bit				2Ch
I/O Limit Address Upper 16-bit		I/O Base Address Upper 16-bit		30h
Reserved			Capability Pointer to 40h	34h
Reserved				38h
Bridge Control		Interrupt Pin	Interrupt Line	3Ch
Power Management Capabilities		Next Item Pointer=48h	Capability ID=01h	40h
PM Data	PPB Support Extensions	Power Management Data		44h
Message Control		Next Item Pointer=68h	Capability ID=05h	48h
Message Address				4Ch
Message Upper Address				50h
Reserved		Message Data		54h
Reserved				58h – 64h
PCI Express Capabilities Register		Next Item Pointer=A4h	Capability ID=10h	68h
Device Capabilities				6Ch
Device Status		Device Control		70h
Link Capabilities				74h
Link Status		Link Control		78h

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31 –24	23 – 16	15 – 8	7 –0	BYTE OFFSET
Slot Capabilities				7Ch
Slot Status		Slot Control		80h
Reserved				84h – 88h
Device Capabilities 2				8Ch
Device Status 2		Device Control 2		90h
Link Capabilities 2				94h
Link Status 2		Link Control 2		98h
Slot Capabilities 2				9Ch
Slot Status 2		Slot Control 2		A0h
Reserved		Next Item Pointer=00h	SSID/SSVID Capability ID=0Dh	A4h
SSID		SSVID		A8h
Reserved				ACh – E0h
BAR 0-1 Configuration				E4h
Reserved				E8h - FCh

Other than the PCI 2.3 compatible configuration space header, the Switch also implements PCI express extended configuration space header, which includes advanced error reporting, virtual channel, and power budgeting capability registers. The following table details the allocation of the register fields of PCI express extended capability space header. The first extended capability always begins at offset 100h with a PCI Express Enhanced Capability header and the rest of capabilities are located at an offset greater than 0FFh relative to the beginning of PCI compatible configuration space.

31 –24	23 – 16	15 - 8	7 –0	BYTE OFFSET
Next Capability Offset=FB4h	Cap. Version	PCI Express Extended Capability ID=0003h		100h
Serial Number Lower DW				104h
Serial Number Upper DW				108h
Reserved				10Ch – 134h
Next Capability Offset=148h	Cap. Version	PCI Express Extended Capability ID=0004h		138h
Reserved			Data Select Register	13Ch
Data Register				140h
Reserved			Power Budget Capability Register	144h
Next Capability Offset= 270h (Up) 520h (Down)	Cap. Version	PCI Express Extended Capability ID=0002h		148h
Port VC Capability Register 1				14Ch
VC Arbitration Table Offset=4h	Port VC Capability Register 2			150h
Port VC Status		Port VC Control		154h
Port Arbitration Table Offset=5h	VC Resource Capability Register (0)			158h
VC Resource Control Register (0)				15Ch
VC Resource Status Register (0)		Reserved		160h
Port Arbitration Table Offset=6h	VC Resource Capability Register (1)			164h
VC Resource Control Register (1)				168h
VC Resource Status Register (1)		Reserved		16Ch
Reserved				170h – 184h
VC Arbitration Table 0				188h
VC Arbitration Table 1				18Ch
VC Arbitration Table 2				190h
VC Arbitration Table 3				194h
Port VC0 Arbitration Table 0 (Low)				198h
Port VC0 Arbitration Table 0 (Upper)				19Ch
Port VC0 Arbitration Table 1 (Low)				1A0h
Port VC0 Arbitration Table 1 (Upper)				1A4h
Port VC1 Arbitration Table 0 (Low)				1A8h
Port VC1 Arbitration Table 0 (Upper)				1ACh
Port VC1 Arbitration Table 1 (Low)				1B0h
Port VC1 Arbitration Table 1 (Upper)				1B4h

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31 –24	23 – 16	15 - 8	7 –0	BYTE OFFSET
Reserved				1B8h – 1C4h
ECC Error Check Disable				1C8h
Reserved				1CCh – 1D8h
UP Port Selection				1DCh
Power Manager Hot Plug Configuration				1E0h
Reserved				1E4h – 1F0h
Software Lane Status				1F4h
Reserved				1F8h – 204h
De-emphasis Control		Rate Control		208h
Reserved		Compliance Mode		20Ch
Reserved				210h – 21Ch
Even Port Physical Layer Control and Status				220h
Odd Port Physical Layer Control and Status				224h
Reserved				228h – 22Ch
Even Port Disable / Quiet / Test Pattern Rate				230h
Odd Port Disable / Quiet / Test Pattern Rate				234h
Reserved				238h – 26Ch
Next Capability Offset=900h	Cap version	PCI Express Extended Capability ID=001Eh		270h
L1 PM Substates Capability				274h
L1 PM Substates Control 1				278h
L1 PM Substates Control 2				27Ch
Reserved				280h – 340h
SMBUS Control and Status				344h
Hot Plug Select				348h
Disable Downstream Port Hot Reset				34Ch
Reserved				350h – 51Ch
Next Capability Offset=270h	Cap version	PCI Express Extended Capability ID=000Dh		520h
ACS Control		ACS Capability		524h
Reserved			Egress Control Vector	528h
Reserved				52Ch – 628h
GPIO 0-15 Direction Control				62Ch
GPIO 16-31Direction Control				630h
Reserved				634h
GPIO Input De-bounce				638h
GPIO 0-15 Input Data				63Ch
GPIO 16-31 Input Data				640h
GPIO 0-15 Output Data				644h
GPIO 16-31 Output Data				648h
GPIO 0-31 Interrupt Polarity				64Ch
GPIO 0-31 Interrupt Status				650h
GPIO 0-31 Interrupt Mask				654h
Reserved				658h-840h
XPIP_CSR0				844h
XPIP_CSR1				848h
Decode VGA	Reserved			84Ch
Switch Operation Mode				850h
PHY Parameter 1		XPIP_CSR2		854h
PHY Parameter 2				858h
PHY Parameter 3				85Ch
PHY Parameter 4				860h
XPIP_CSR3				864h
XPIP_CSR4				868h
XPIP_CSR5				86Ch
Non Transfer Mode				870h
Operation Mode				874h
Device Specific PM Event				878h
EEPROM Control				87Ch
EEPROM Address and Data				880h
Debugout Control				884h
Debugout Data				888h
LTSSM CSR				88Ch
MAC CSR 1				890h

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31 –24	23 – 16	15 - 8	7 –0	BYTE OFFSET
Reserved				894h – 8A0h
Power Saving Disable				8A4h
Transaction Layer CSR				8A8h
ACK Latency Timer		Replay Time-out Counter		8ACh
PHY Parameter 0		Port Misc 0		8B0h
XPIP_CSR7	XPIP_CSR6	Port Misc 1		8B4h
Reserved		Port Misc 2		8B8h
LED Display CSR				8BCh
Reserved				8C0h - 8FCh
Next Capability Offset=000h	Cap. Version	PCI Express Extended Capability ID=0012h		900h
Multi-Case Control		Multi-Case Capability		904h
Multi-Case Base Address 0				908h
Multi-Case Base Address 1				90Ch
Multi-Case Receive				910h
Reserved				914h
Multi-Case Block All				918h
Reserved				91Ch
Multi-Case Block Untranslated				920h
Reserved				924h – FACh
EEPROM_Scratchpad				FB0h
Next Capability Offset= 138h (Up) 148h (Down)	Cap. Version	PCI Express Extended Capability ID=0001h		FB4h
Uncorrectable Error Status Register				FB8h
Uncorrectable Error Mask Register				FBCh
Uncorrectable Error Severity Register				FC0h
Correctable Error Status Register				FC4h
Correctable Error Mask Register				FC8h
Advanced Error Capabilities and Control Register				FCCh
Header Log Register 0				FD0h
Header Log Register 1				FD4h
Header Log Register 2				FD8h
Header Log Register 3				FDCh
Reserved				FE0h – FF4h

8.2.1 VENDOR ID REGISTER – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
15:0	Vendor ID	RO	Identifies Pericom as the vendor of this device.	Yes	12D8h

8.2.2 DEVICE ID REGISTER – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:16	Device ID	RO	Identifies this device as the PI7C9X2G912GP.	Yes	2912h

8.2.3 COMMAND REGISTER – OFFSET 04h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	I/O Space Enable	RW	0b: Ignores I/O transactions on the primary interface 1b: Enables responses to I/O transactions on the primary interface	No/Yes	0
1	Memory Space Enable	RW	0b: Ignores memory transactions on the primary interface 1b: Enables responses to memory transactions on the primary interface	No/Yes	0

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BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
2	Bus Master Enable	RW	0b: Does not initiate memory or I/O transactions on the upstream port and handles as an Unsupported Request (UR) to memory and I/O transactions on the downstream port. For Non-Posted Requests, a completion with UR completion status must be returned 1b: Enables the Switch Port to forward memory and I/O Read/Write transactions in the upstream direction	No/Yes	0
3	Special Cycle Enable	RsvdP	Not Support.	No	0
4	Memory Write And Invalidate Enable	RsvdP	Not support.	No	0
5	VGA Palette Snoop Enable	RsvdP	Not Support.	No	0
6	Parity Error Response Enable	RW	0b: Switch may ignore any parity errors that it detects and continue normal operation 1b: Switch must take its normal action when a parity error is detected	No/Yes	0
7	Wait Cycle Control	RsvdP	Not Support.	No	0
8	SERR# enable	RW	0b: Disables the reporting of Non-fatal and Fatal errors detected by the Switch to the Root Complex 1b: Enables the Non-fatal and Fatal error reporting to Root Complex	No/Yes	0
9	Fast Back-to-Back Enable	RsvdP	Not Support.	No	0
10	Interrupt Disable	RW	Controls the ability of a PCI Express device to generate INTx Interrupt Messages. In the Switch, this bit does not affect the forwarding of INTx messages from the downstream ports.	No/Yes	0
15:11	Reserved	RsvdP	Not Support.	No	0000_0b

8.2.4 PRIMARY STATUS REGISTER – OFFSET 04h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
18:16	Reserved	RsvdP	Not Support.	No	000b
19	Interrupt Status	RO	Indicates that an INTx Interrupt Message is pending internally to the device. In the Switch, the forwarding of INTx messages from the downstream device of the Switch port is not reflected in this bit. Must be hardwired to 0.	No	0
20	Capabilities List	RO	Set to 1b to enable support for the capability list (offset 34h is the pointer to the data structure).	No	1
21	66MHz Capable	RO	Does not apply to PCI Express. Must be hardwired to 0.	No	0
22	Reserved	RsvdP	Not Support.	No	0
23	Fast Back-to-Back Capable	RsvdP	Not Support.	No	0
24	Master Data Parity Error	RW1C	Set to 1b (by a requester) whenever a Parity error is detected or forwarded on the primary side of the port in a Switch. If the Parity Error Response Enable bit is cleared, this bit is never set.	No/Yes	0
26:25	DEVSEL# timing	RsvdP	Not Support.	No	00b
27	Signaled Target Abort	RsvdP	Not Support.	No	0
28	Received Target Abort	RsvdP	Not Support.	No	0
29	Received Master Abort	RsvdP	Not Support.	No	0
30	Signaled System Error	RW1C	Set to 1b when the Switch sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Command register is 1.	No/Yes	0
31	Detected Parity Error	RW1C	Set to 1b whenever the primary side of the port in a Switch receives a Poisoned TLP.	No/Yes	0

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8.2.5 REVISION ID REGISTER – OFFSET 08h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
7:0	Revision	RO	Indicates revision number of device.	Yes	00h

8.2.6 CLASS REGISTER – OFFSET 08h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
15:8	Programming Interface	RO	Read as 00h to indicate no programming interfaces have been defined for PCI-to-PCI Bridges.	No	00h
23:16	Sub-Class Code	RO	Read as 04h to indicate device is a PCI-to-PCI Bridge.	No	04h
31:24	Base Class Code	RO	Read as 06h to indicate device is a Bridge device.	No	06h

8.2.7 CACHE LINE REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
7:0	Cache Line Size	RW	The cache line size register is set by the system firmware and the operating system cache line size. This field is implemented by PCI Express devices as a RW field for legacy compatibility, but it has no impact on any PCI Express device functionality.	No/Yes	00h

8.2.8 PRIMARY LATENCY TIMER REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
15:8	Primary Latency Timer	RsvdP	Not Support.	No	00h

8.2.9 HEADER TYPE REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
22:16	Header Type	RO	Read as 01h to indicate that the register layout conforms to the standard PCI-to-PCI Bridge layout.	No	01h
23	Multi-Function Device	RO	0b: Single function device 1b: Multiple functions device	No	1 for Up 0 for Down

8.2.10 BASE ADDRESS 0 REGISTER – OFFSET 10h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	Memory Space Indicator	RO	0b: indicate Memory Base address 1b: indicate I/O Base address	No	0
2:1	64-bit Addressing	RO	00b: 32-bit addressing 10b: 64-bit addressing Others: Reserved	No	00b
3	Prefetchable	RO	0b: Non-prefetchable 1b: Prefetchable	No	0
16:4	Reserved	RsvdP	Not Support.	No	0-0h
31:17	Base Address 0	RW	Use this Memory base address to map the packet switch registers.	No/Yes	0-0h

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8.2.11 BASE ADDRESS 1 REGISTER – OFFSET 14h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:0	Base Address 1	RO/RW	RO when the Base Address 0 register is not 64-bit addressing (offset 10h[2:1] is not 10b). RW when the Base Address 0 register is 64-bit addressing. Base Address 1 is used to provide the upper 32 Address bits when offset 10h[2:1] is set to 10b.	No/Yes	0000_0000h

8.2.12 PRIMARY BUS NUMBER REGISTER – OFFSET 18h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
7:0	Primary Bus Number	RW	Indicates the number of the PCI bus to which the primary interface is connected. The value is set in software during configuration.	No/Yes	00h

8.2.13 SECONDARY BUS NUMBER REGISTER – OFFSET 18h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
15:8	Secondary Bus Number	RW	Indicates the number of the PCI bus to which the secondary interface is connected. The value is set in software during configuration.	No/Yes	00h

8.2.14 SUBORDINATE BUS NUMBER REGISTER – OFFSET 18h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
23:16	Subordinate Bus Number	RW	Indicates the number of the PCI bus with the highest number that is subordinate to the Bridge. The value is set in software during configuration.	No/Yes	00h

8.2.15 SECONDARY LATENCY TIMER REGISTER – OFFSET 18h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:24	Secondary Latency Timer	RsvdP	Not Support.	No	00h

8.2.16 I/O BASE ADDRESS REGISTER – OFFSET 1Ch

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
3:0	32-bit Indicator	RO	Read as 1h to indicate 32-bit I/O addressing.	No	1h
7:4	I/O Base Address [15:12]	RW	Defines the bottom address of the I/O address range for the Bridge to determine when to forward I/O transactions from one interface to the other. The upper 4 bits correspond to address bits [15:12] and are writable. The lower 12 bits corresponding to address bits [11:0] are assumed to be 0. The upper 16 bits corresponding to address bits [31:16] are defined in the I/O base address upper 16 bits address register.	No/Yes	0h

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8.2.17 I/O LIMIT ADDRESS REGISTER – OFFSET 1Ch

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
11:8	32-bit Indicator	RO	Read as 1h to indicate 32-bit I/O addressing.	No	1h
15:12	I/O Limit Address [15:12]	RW	Defines the top address of the I/O address range for the Bridge to determine when to forward I/O transactions from one interface to the other. The upper 4 bits correspond to address bits [15:12] and are writable. The lower 12 bits corresponding to address bits [11:0] are assumed to be FFFh. The upper 16 bits corresponding to address bits [31:16] are defined in the I/O limit address upper 16 bits address register.	No/Yes	0h

8.2.18 SECONDARY STATUS REGISTER – OFFSET 1Ch

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
20:16	Reserved	RsvdP	Not Support.	No	0_0000b
21	66MHz Capable	RsvdP	Not Support.	No	0
22	Reserved	RsvdP	Not Support.	No	0
23	Fast Back-to-Back Capable	RsvdP	Not Support.	No	0
24	Master Data Parity Error	RW1C	Set to 1b (by a requester) whenever a Parity error is detected or forwarded on the secondary side of the port in a Switch. If the Parity Error Response Enable bit is cleared, this bit is never set.	No/Yes	0
26:25	DEVSEL_L timing	RsvdP	Not Support.	No	00b
27	Signaled Target Abort	RsvdP	Not Support.	No	0
28	Received Target Abort	RsvdP	Not Support.	No	0
29	Received Master Abort	RsvdP	Not Support.	No	0
30	Received System Error	RW1C	Set to 1b when the Switch sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Bridge Control register is 1.	No/Yes	0
31	Detected Parity Error	RW1C	Set to 1b whenever the secondary side of the port in a Switch receives a Poisoned TLP.	No/Yes	0

8.2.19 MEMORY BASE ADDRESS REGISTER – OFFSET 20h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
3:0	Reserved	RsvdP	Not Support.	No	0h
15:4	Memory Base Address [31:20]	RW	Defines the bottom address of an address range for the Bridge to determine when to forward memory transactions from one interface to the other. The upper 12 bits correspond to address bits [31:20] and are able to be written to. The lower 20 bits corresponding to address bits [19:0] are assumed to be 0.	No/Yes	000h

8.2.20 MEMORY LIMIT ADDRESS REGISTER – OFFSET 20h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
19:16	Reserved	RsvdP	Not Support.	No	0h
31:20	Memory Limit Address [31:20]	RW	Defines the top address of an address range for the Bridge to determine when to forward memory transactions from one interface	No/Yes	000h

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			to the other. The upper 12 bits correspond to address bits [31:20] and are writable. The lower 20 bits corresponding to address bits [19:0] are assumed to be FFFFFh.		

8.2.21 PREFETCHABLE MEMORY BASE ADDRESS REGISTER – OFFSET 24h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
3:0	64-bit addressing	RO	Read as 1h to indicate 64-bit addressing.	No	1h
15:4	Prefetchable Memory Base Address [31:20]	RW	Defines the bottom address of an address range for the Bridge to determine when to forward memory read and write transactions from one interface to the other. The upper 12 bits correspond to address bits [31:20] and are writable. The lower 20 bits are assumed to be 0. The memory base register upper 32 bits contain the upper half of the base address.	No/Yes	000h

8.2.22 PREFETCHABLE MEMORY LIMIT ADDRESS REGISTER – OFFSET 24h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
19:16	64-bit addressing	RO	Read as 1h to indicate 64-bit addressing.	No	1h
31:20	Memory Limit Address [31:20]	RW	Defines the top address of an address range for the Bridge to determine when to forward memory transactions from one interface to the other. The upper 12 bits correspond to address bits [31:20] and are writable. The lower 20 bits corresponding to address bits [19:0] are assumed to be FFFFFh.	No/Yes	000h

8.2.23 PREFETCHABLE MEMORY BASE ADDRESS UPPER 32-BITS REGISTER – OFFSET 28h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:0	Prefetchable Memory Base Address, Upper 32-bits [63:32]	RW	Defines the upper 32-bits of a 64-bit bottom address of an address range for the Bridge to determine when to forward memory read and write transactions from one interface to the other.	No/Yes	0000_0000h

8.2.24 PREFETCHABLE MEMORY LIMIT ADDRESS UPPER 32-BITS REGISTER – OFFSET 2Ch

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:0	Prefetchable Memory Limit Address, Upper 32-bits [63:32]	RW	Defines the upper 32-bits of a 64-bit top address of an address range for the Bridge to determine when to forward memory read and write transactions from one interface to the other.	No/Yes	0000_0000h

8.2.25 I/O BASE ADDRESS UPPER 16-BITS REGISTER – OFFSET 30h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
15:0	I/O Base Address, Upper 16-bits [31:16]	RW	Defines the upper 16-bits of a 32-bit bottom address of an address range for the Bridge to determine when to forward I/O transactions from one interface to the other.	No/Yes	0000h

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8.2.26 I/O LIMIT ADDRESS UPPER 16-BITS REGISTER – OFFSET 30h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:16	I/O Limit Address, Upper 16-bits [31:16]	RW	Defines the upper 16-bits of a 32-bit top address of an address range for the Bridge to determine when to forward I/O transactions from one interface to the other.	No/Yes	0000h

8.2.27 CAPABILITY POINTER REGISTER – OFFSET 34h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
7:0	Capability Pointer	RO	Indicates next capability pointer.	Yes	40h

8.2.28 INTERRUPT LINE REGISTER – OFFSET 3Ch

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
7:0	Interrupt Line	RW	Indicates the Interrupt Line.	No/Yes	00h

8.2.29 INTERRUPT PIN REGISTER – OFFSET 3Ch

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
15:8	Interrupt Pin	RO	The Switch implements INTA virtual wire interrupt signals to represent hot-plug events at downstream ports. 0b: disable INTA 1b: enable INTA	Yes	00h for Up 01h for Down

8.2.30 BRIDGE CONTROL REGISTER – OFFSET 3Ch

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
16	Parity Error Response	RW	0b: Ignore Poisoned TLPs on the secondary interface 1b: Enable the Poisoned TLPs reporting and detection on the secondary interface	No/Yes	0
17	S_SERR# Enable	RW	0b: Disables the forwarding of EER_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary interface 1b: Enables the forwarding of EER_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary interface	No/Yes	0
18	ISA Enable	RW	0b: Forwards downstream all I/O addresses in the address range defined by the I/O Base, I/O Base, and Limit registers 1b: Forwards upstream all I/O addresses in the address range defined by the I/O Base and Limit registers that are in the first 64KB of PCI I/O address space (top 768 bytes of each 1KB block)	No/Yes	0
19	VGA Enable	RW	0b: Ignores access to the VGA memory or IO address range 1b: Forwards transactions targeted at the VGA memory or IO address range VGA memory range starts from 000A 0000h to 000B FFFFh VGA IO addresses are in the first 64KB of IO address space. AD [9:0] is in the ranges 3B0 to 3BBh and 3C0h to 3DFh.	No/Yes	0
20	VGA 16-bit Decode	RW	0b: Executes 10-bit address decoding on VGA I/O accesses 1b: Executes 16-bit address decoding on VGA I/O accesses	No/Yes	0

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BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
21	Master Abort Mode	RsvdP	Not Support.	No	0
22	Secondary Bus Reset	RW	0b: Does not trigger a hot reset on the corresponding PCI Express Port 1b: Triggers a hot reset on the corresponding PCI Express Port At the downstream port, it asserts PORT_RST# to the attached downstream device. At the upstream port, it asserts the PORT_RST# at all the downstream ports.	No/Yes	0
23	Fast Back-to-Back Enable	RsvdP	Not Support.	No	0
24	Primary Master Timeout	RsvdP	Not Support.	No	0
25	Secondary Master Timeout	RsvdP	Not Support.	No	0
26	Master Timeout Status	RsvdP	Not Support.	No	0
27	Discard Timer SERR# Enable	RsvdP	Not Support.	No	0
31:28	Reserved	RsvdP	Not Support.	No	0h

8.2.31 POWER MANAGEMENT CAPABILITIES REGISTER – OFFSET 40h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
7:0	Enhanced Capabilities ID	RO	Read as 01h to indicate that these are power management enhanced capability registers.	No	01h
15:8	Next Item Pointer	RO	Indicates next capability pointer.	Yes	48h
18:16	Power Management Revision	RO	Read as 011b to indicate the device is compliant to Revision 1.2 of *PCI Power Management Interface Specifications.*	No	011b
19	PME# Clock	RO	Does not apply to PCI Express. Must be hardwired to 0.	No	0
20	Reserved	RsvdP	Not Support.	No	0
21	Device specific Initialization	RO	Read as 0b to indicate Switch does not have device specific initialization requirements.	Yes	0
24:22	AUX Current	RO	Reset to 000b.	Yes	000b
25	D1 Power State Support	RO	Read as 0b to indicate Switch does not support the D1 power management state.	Yes	0
26	D2 Power State Support	RO	Read as 0b to indicate Switch does not support the D2 power management state.	Yes	0
31:27	PME# Support	RO	Read as 19h to indicate Switch supports the forwarding of PME# message in D0, D3 and D4 states.	Yes	19h

8.2.32 POWER MANAGEMENT DATA REGISTER – OFFSET 44h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
1:0	Power State	RW	Indicates the current power state of the Switch. Writing a value of D0 when the previous state was D3 cause a hot reset without asserting DWNRST_L. 00b: D0 state 01b: D1 state 10b: D2 state 11b: D3 hot state	No/Yes	00b
2	Reserved	RsvdP	Not Support.	No	0
3	No_Soft_Reset	RO	When set, this bit indicates that device transitioning from D3hot to D0 does not perform an internal reset. When clear, an internal reset is performed when power state transits from D3hot to D0.	Yes	1

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BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
7:4	Reserved	RsvdP	Not Support.	No	0h
8	PME# Enable	RW	When asserted, the Switch will generate the PME# message.	No/Yes	0
12:9	Data Select	RW / RO	Select data registers. RW if offset 870h[1]=1 and RO if offset 870h[1]=0.	No/Yes	0h
14:13	Data Scale	RO	Reset to 00b.	No	00b
15	PME Status	RW1C	Read as 0b as the PME# message is not implemented.	No	0

8.2.33 PPB SUPPORT EXTENSIONS REGISTER – OFFSET 44h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
21:16	Reserved	RsvdP	Not Support.	No	00h
22	B2_B3 Support for $D3_{HOT}$	RsvdP	Not Support.	No	0
23	Bus Power / Clock Control Enable	RsvdP	Not Support.	No	0

8.2.34 DATA REGISTER– OFFSET 44h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:24	Data Register	RO	Data Register.	Yes	00h

8.2.35 MSI CAPABILITIES REGISTER – OFFSET 48h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
7:0	Enhanced Capabilities ID	RO	Read as 05h to indicate that this is message signal interrupt capability register.	No	05h
15:8	Next Item Pointer	RO	Indicates next capability pointer.	Yes	68h
16	MSI Enable	RW	0b: The function is prohibited from using MSI to request service 1b: The function is permitted to use MSI to request service and is prohibited from using its INTx # pin	No/Yes	0
19:17	Multiple Message Capable	RO	Read as 000b.	No	000b
22:20	Multiple Message Enable	RW	Reset to 000b.	No/Yes	000b
23	64-bit address capable	RO	0b: The function is not capable of generating a 64-bit message address 1b: The function is capable of generating a 64-bit message address	No	1b
31:24	Reserved	RO	Not Support.	No	00h

8.2.36 MESSAGE ADDRESS REGISTER – OFFSET 4Ch

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
1:0	Reserved	RsvdP	Not Support.	No	00b
31:2	Message Address	RW	If the message enable bit is set, the contents of this register specify the DWORD aligned address for MSI memory write transaction.	No/Yes	0-0h

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8.2.37 MESSAGE UPPER ADDRESS REGISTER – OFFSET 50h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:0	Message Upper Address	RW	This register is only effective if the device supports a 64-bit message address is set.	No/Yes	0000_0000h

8.2.38 MESSAGE DATA REGISTER – OFFSET 54h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
15:0	Message Data	RW	Message data.	No/Yes	0000h

8.2.39 PCI EXPRESS CAPABILITIES REGISTER – OFFSET 68h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
7:0	Enhanced Capabilities ID	RO	Read as 10h to indicate that these are PCI express enhanced capability registers.	No	10h
15:8	Next Item Pointer	RO	Indicates next capability pointer.	Yes	A4h
19:16	Capability Version	RO	Read as 2h to indicate the device is compliant to Revision .2.0 of *PCI Express Base Specifications*.	No	2h
23:20	Device/Port Type	RO	Indicates the type of PCI Express logical device. 0101b: upstream port 0110b: downstream port	No	5h for Up 6h for Down
24	Slot Implemented	RO	Valid for downstream ports only. When set, indicates that the PCIe Link associated with this Port is connected to a slot. This field is valid for downstream ports of the Switch.	Yes	0 for Up 1 for Down
29:25	Interrupt Message Number	RO	No MSI messages are generated in the transparent mode.	No	00_000b
31:30	Reserved	RsvdP	Not Support.	No	00b

8.2.40 DEVICE CAPABILITIES REGISTER – OFFSET 6Ch

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
2:0	Max_Payload_Size Supported	RO	Indicates the maximum payload size that the device can support for TLPs. 000b: 128 payload size 001b: 256 payload size 010b: 512 payload size	Yes	001b
4:3	Phantom Functions Supported	RO	Indicates the support for use of unclaimed function numbers as Phantom functions. Read as 00b, since the Switch does not act as a requester.	No	00b
5	Extended Tag Field Supported	RO	Indicates the maximum supported size of Tag field as a Requester. Read as 0, since the Switch does not act as a requester.	No	0
8:6	Endpoint L0s Acceptable Latency	RO	Acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state. For Switch, the ASPM software would not check this value.	No	000b
11:9	Endpoint L1 Acceptable Latency	RO	Acceptable total latency that an Endpoint can withstand due to the transition from L1 state to the L0 state. For Switch, the ASPM software would not check this value.	No	000b
14:12	Reserved	RsvdP	Not Support.	No	000b

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BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
15	Role_Based Error Reporting	RO	When set, indicates that the device implements the functionality originally defined in the Error Reporting ECN.	Yes	1
17:16	Reserved	RsvdP	Not Support.	No	00b
25:18	Captured Slot Power Limit Value	RO	It applies to Upstream Port only. In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. This value is set by the Set_Slot_Power_Limit message or hardwired to 0.	No	00h
27:26	Captured Slot Power Limit Scale	RO	It applies to Upstream Port only. Specifies the scale used for the Slot Power Limit Value. This value is set by the Set_Slot_Power_Limit message or hardwired to 0.	No	00b
31:28	Reserved	RsvdP	Not Support.	No	0h

8.2.41 DEVICE CONTROL REGISTER – OFFSET 70h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	Correctable Error Reporting Enable	RW	0b: Disable Correctable Error Reporting 1b: Enable Correctable Error Reporting	No/Yes	0
1	Non-Fatal Error Reporting Enable	RW	0b: Disable Non-Fatal Error Reporting 1b: Enable Non-Fatal Error Reporting	No/Yes	0
2	Fatal Error Reporting Enable	RW	0b: Disable Fatal Error Reporting 1b: Enable Fatal Error Reporting	No/Yes	0
3	Unsupported Request Reporting Enable	RW	0b: Disable Unsupported Request Reporting 1b: Enable Unsupported Request Reporting	No/Yes	0
4	Enable Relaxed Ordering	RO	When set, it permits the device to set the Relaxed Ordering bit in the attribute field of transaction. Since the Switch can not either act as a requester or alter the content of packet it forwards, this bit always returns '0' when read.	No	0
7:5	Max_Payload_Size	RW	This field sets maximum TLP payload size for the device. Permissible values that can be programmed are indicated by the Max_Payload_Size Supported in the Device Capabilities register. Any value exceeding the Max_Payload_Size Supported written to this register results into clamping to the Max_Payload_Size Supported value.	No/Yes	000b
8	Extended Tag Field Enable	RW	Does not apply to PCI Express Switch. Returns '0' when read.	No	0
9	Phantom Function Enable	RW	Does not apply to PCI Express Switch. Returns '0' when read.	No	0
10	Auxiliary (AUX) Power PM Enable	RO	When set, indicates that a device is enabled to draw AUX power independent of PME AUX power.	No	0
11	Enable No Snoop	RO	When set, it permits to set the No Snoop bit in the attribute field of transaction. Since the Switch cannot either act as a requester or alter the content of packet it forwards, this bit always returns '0' when read.	No	0
14:12	Max_Read_ Request_Size	RO	This field sets the maximum Read Request size for the device as a Requester. Since the Switch does not generate read request by itself, these bits are hardwired to 0.	No	000b
15	Reserved	RsvdP	Not Support.	No	0

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8.2.42 DEVICE STATUS REGISTER – OFFSET 70h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
16	Correctable Error Detected	RW1C	Asserted when correctable error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.	No/Yes	0
17	Non-Fatal Error Detected	RW1C	Asserted when non-fatal error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.	No/Yes	0
18	Fatal Error Detected	RW1C	Asserted when fatal error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.	No/Yes	0
19	Unsupported Request Detected	RW1C	Asserted when unsupported request is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.	No/Yes	0
20	AUX Power Detected	RO	Asserted when the AUX power is detected by the Switch	No	0
21	Transactions Pending	RO	Each port of Switch does not issue Non-posted Requests on its own behalf, so this bit is hardwired to 0.	No	0
31:22	Reserved	RsvdP	Not Support.	No	0-0h

8.2.43 LINK CAPABILITIES REGISTER – OFFSET 74h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
3:0	Maximum Link Speed	RO	Indicates the maximum speed of the Express link. 0001b: 2.5 Gb/s 0010b: 5.0 Gb/s Others: Reserved	No	2h
9:4	Maximum Link Width	HWInt RO	Indicates the maximum width of the given PCIe Link. 00_0001b: x1 link 00_0010b: x2 link 00_0100b: x4 link Others: Reserved	No	04h, 02h or 01h
11:10	Active State Power Management (ASPM) Support	RO	Indicates the level of ASPM supported on the given PCIe Link. Each port of Switch supports L0s and L1 entry.	Yes	01b
14:12	L0s Exit Latency	RO	Indicates the L0s exit latency for the given PCIe Link. The length of time this port requires to complete transition from L0s to L0 is in the range of 256ns to less than 512ns.	Yes	011b
17:15	L1 Exit Latency	RO	Indicates the L1 exit latency for the given PCIe Link. The length of time this port requires to complete transition from L1 to L0 is less than 1us.	Yes	000b
18	Clock Power Management	RO	For upstream port, a value of 1b indicates that component tolerates the removal of any reference clock via CLKREQ#. For downstream ports, this bit must be hardwired to 0.	Yes	1 for Up 0 for Down
19	Surprise Down Capability Enable	RO	Valid for downstream ports only.	Yes	0
20	Data Link Layer Active Reporting Capable	RO	For downstream ports, this bit must be set to 1b if the component supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine. For a hot-plug capable downstream port, this bit must be set to 1b. For upstream port, this bit must be hardwired to 0.	No	0
21	Link BW Notify Cap.	RO	Valid for downstream ports only.	Yes	0 for Up 1 for Down
23:22	Reserved	RsvdP	Not Support.	No	0

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BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:24	Port Number	RO	Indicates the PCIe Port Number for the given PCIe Link.	Yes	00h for Up 01 h for Port 1 02h for Port 2 03h for Port 3 ….

8.2.44 LINK CONTROL REGISTER – OFFSET 78h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
1:0	Active State Power Management (ASPM) Control	RW	00b: ASPM is Disabled 01b: L0s Entry Enabled 10b: L1 Entry Enabled 11b: L0s and L1 Entry Enabled Note that the receiver must be capable of entering L0s even when the field is disabled	No/Yes	00b
2	Reserved	RsvdP	Not Support.	No	0
3	Read Completion Boundary (RCB)	RsvdP	Not Support.	No	0
4	Link Disable	RW	At upstream port, it is not allowed to disable the link, so this bit is hardwired to '0'. For downstream ports, it disables the link when this bit is set.	No/Yes	0
5	Retrain Link	RW	At upstream port, it is not allowed to retrain the link, so this bit is hardwired to 0. For downstream ports, it initiates Link Retraining when this bit is set. This bit always returns '0' when read.	No/Yes	0
6	Common Clock Configuration	RW	0b: The components at both ends of a link are operating with synchronous reference clock 1b: The components at both ends of a link are operating with a distributed common reference clock	No/Yes	0
7	Extended Synch	RW	When set, it transmits 4096 FTS ordered sets in the L0s state for entering L0 state and transmits 1024 TS1 ordered sets in the L1 state for entering L0 state.	No/Yes	0
8	Enable Clock Power Management	RW	Valid for upstream port only- 0b: clock power management is disabled and must hold CLKREQ# low 1b: device is permitted to use CLKREQ# to power manage Link clock	No/Yes	0
9	HW Autonomous Width Disable	RW	Reset to 0b.	No/Yes	0
10	Link Bandwidth Management Interrupt Enable	RW	Valid for downstream ports only.	No/Yes	0
11	Link Autonomous Bandwidth Interrupt Enable	RW	Valid for downstream ports only.	No/Yes	0
15:12	Reserved	RsvdP	Not Support.	No	0h

8.2.45 LINK STATUS REGISTER – OFFSET 78h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
19:16	Link Speed	RO	Indicate the negotiated speed of the Express link. 0001b: 2.5 Gb/s 0010b: 5.0 Gb/s	No	1h

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BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
25:20	Negotiated Link Width	RO	Indicates the negotiated width of the given PCIe link. 00_0001b: x1 link 00_0010b: x2 link 00_0100b: x4 link	No	00_0001b
26	Training Error	RO	When set, indicates a Link training error occurred. This bit is cleared by hardware upon successful training of the link to the L0 link state.	No	0
27	Link Training	RO	When set, indicates the link training is in progress. Hardware clears this bit once link training is complete.	No	0
28	Slot Clock Configuration	RO	0b: the Switch uses an independent clock irrespective of the presence of a reference on the connector 1b: the Switch uses the same reference clock that the platform provides on the connector	Yes	1 for Up 0 for Down
29	Data Link Layer Link Active	RO	Indicates the status of the Data Link Control and Management State Machine. 1b: indicate the DL_Active state 0b: otherwise	No	0
30	Link Bandwidth Management Status	RW1C	Valid for downstream port only.	No/Yes	0
31	Link Autonomous Bandwidth Status	RW1C	Valid for downstream port only.	No/Yes	0

8.2.46 SLOT CAPABILITIES REGISTER – OFFSET 7Ch (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	Attention Button Present	RO	When set, it indicates that an Attention Button is implemented on the chassis for this slot.	Yes	1
1	Power Controller Present	RO	When set, it indicates that a Power Controller is implemented for this slot.	Yes	1
2	MRL Sensor Present	RO	When set, this bit indicates that an MRL Sensor is implemented on the chassis for this slot.	Yes	1
3	Attention Indicator Present	RO	When set, it indicates that an Attention Indicator is implemented on the chassis for this slot	Yes	1
4	Power Indicator Present	RO	When set, it indicates that a Power Indicator is implemented on the chassis for this slot.	Yes	1
5	Hot-Plug Surprise	RO	When set, it indicates that a device present in this slot might be removed from the system without any prior notification.	Yes	0
6	Hot-Plug Capable	HWInt RO	When set, it indicates that this slot is capable of supporting Hot-Plug operation. Without external I/O expander connected, the default value will be clear to 0.	Yes	0
14:7	Slot Power Limit Value	RO	In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. Writes to this register also cause the Port to send the Set_Slot_Power_Limit message.	Yes	19h
16:15	Slot Power Limit Scale	RO	Specifies the scale used for the Slot Power Limit Value. Writes to this register also cause the Port to send the Set_Slot_Power_Limit message.	Yes	00b
17	EM_INTRELOCK Present	RO	When set, it indicates that an Electromechanical Interlock Present is implemented on the chassis for this slot.	Yes	0
18	No Command Completed Support	RO	When set, it indicates that this slot does not generate software notification when an issued command is completed by the Hot-Plug Controller.	Yes	0
31:19	Physical Slot Number	RO	It indicates the physical slot number attached to this Port.	Yes	02h for Port 2 03h for Port 3 …

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8.2.47 SLOT CONTROL REGISTER – OFFSET 80h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	Attention Button Pressed Enable	RW	When set, it enables the generation of Hot-Plug interrupt or wakeup event on an attention button pressed event.	No/Yes	0
1	Power Fault Detected Enable	RW	When set, it enables the generation of Hot-Plug interrupt or wakeup event on a power fault event.	No/Yes	0
2	MRL SENOR ENABLE	RW	When set, it enables the generation of Hot-Plug interrupt or wakeup event on a MRL sensor event.	No/Yes	0
3	Presence Detect Changed Enable	RW	When set, it enables the generation of Hot-Plug interrupt or wakeup event on a presence detect changed event.	No/Yes	0
4	Command Completed Interrupt Enable	RW	When set, it enables the generation of Hot-Plug interrupt when the Hot-Plug Controller completes a command. It is valid when offset 7Ch[18]=0b.	No/Yes	0
5	Hot-Plug Interrupt Enable	RW	When set, it enables generation of Hot-Plug interrupt on enabled Hot-Plug events.	No/Yes	0
7:6	Attention Indicator Control	RW	Controls the display of Attention Indicator. 00b: Reserved 01b: On 10b: Blink 11b: Off Writes to this register also cause the Port to send the ATTENTION_INDICATOR_* Messages.	No/Yes	11b
9:8	Power Indicator Control	RW	Controls the display of Power Indicator. 00b: Reserved 01b: On 10b: Blink 11b: Off Writes to this register also cause the Port to send the POWER_INDICATOR_* Messages.	No/Yes	11b when bit[2]=1 01b when bit[2]=0
10	Power Controller Control	RW	0b: reset the power state of the slot (Power On) 1b: set the power state of the slot (Power Off)	No/Yes	1 when bit[2]=1 0 when bit[2]=0
11	EM_INTRELOCK Control	RW	When set, it enables the generation of Hot-Plug interrupt or wakeup event on an electromechanical interlock present event.	No/Yes	0
12	Data Link Layer State Changed Enable	RW	When set, it enables the generation of Hot-Plug interrupt or wakeup event on a data link layer state changed event.	No/Yes	0
15:13	Reserved	RsvdP	Not Support.	No	000b

8.2.48 SLOT STATUS REGISTER – OFFSET 80h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
16	Attention Button Pressed	RW1C	When set, it indicates the Attention Button is pressed.	No/Yes	0
17	Power Fault Detected	RW1C	When set, it indicates a Power Fault is detected.	No/Yes	0
18	MRL Sensor Changed	RW1C	When set, it indicates a MRL Sensor Changed is detected.	No/Yes	0
19	Presence Detect Changed	RW1C	When set, it indicates a Presence Detect Changed is detected.	No/Yes	0
20	Command Completed	RW1C	When set, it indicates the Hot-Plug Controller completes an issued command.	No/Yes	0
21	MRL Sensor State	RO	Reflects the status of MRL Sensor. 0b: MRL Closed 1b: MRL Opened	No	0

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BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
22	Presence Detect State	RO	Indicates the presence of a card in the slot. 0b: Slot Empty 1b: Card Present in slot This register is implemented on all downstream ports that implement slots. For downstream ports not connected to slots (where the Slot Implemented bit of the PCI Express Capabilities register is 0b), this bit returns 1b.	No	0
23	EM_INTRELOCK Status	RO	Indicates the Electromechanical Interlock's current status. 0b: Electromechanical Interlock is disengaged 1b: Electromechanical Interlock is engaged	No	0
24	Data Link Layer State Changed	RW1C	This bit is set when the value reported in the Data Link Layer Link Active field of the Link Status register is changed.	No/Yes	0
31:25	Reserved	RsvdP	Not Support.	No	0-0h

8.2.49 DEVICE CAPABILITIES REGISTER 2 – OFFSET 8Ch

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
4:0	Reserved	RsvdP	Not Support.	No	0_0000b
5	ARI Forwarding Supported	RO	0b: ARI forwarding is not supported 1b: ARI forwarding is supported Valid for downstream ports only.	No/Yes	0 for Up 1 for Down
31:6	Reserved	RsvdP	Not Support.	No	0-0h

8.2.50 DEVICE CONTROL REGISTER 2 – OFFSET 90h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
4:0	Reserved	RsvdP	Not Support.	No	0_0000b
5	ARI Forwarding Enable	RW	0b: Disable 1b: Enable Valid for downstream ports only.	No/Yes	0
31:6	Reserved	RsvdP	Not Support.	No	0-0h

8.2.51 DEVICE STATUS REGISTER 2 – OFFSET 90h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:16	Device Status 2	RO	Not Support.	No	0000h

8.2.52 LINK CAPABILITIES REGISTER 2 – OFFSET 94h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:0	Link Capability 2	RO	Not Support.	No	0000_0000h

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8.2.53 LINK CONTROL REGISTER 2 – OFFSET 98h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
3:0	Target Link Speed	RW	0001b: target link speed set to 2.5 Gb/s 0010b: target link speed set to 5.0 Gb/s Others: Reserved	No/Yes	2h
4	Enter Compliance	RW	1b: enter compliance mode	No/Yes	0
5	HW_AutoSpeed_Dis	RW	Reset to 0b.	No/Yes	0
6	Select_Deemp	RW	Valid for downstream ports only. 0b: Select -6.0db de-emphasis 1b: Select -3.5db de-emphasis	Yes	0 for Up 1 for Down
9:7	Tran_Margin	RW	Reset to 000b.	No/Yes	000b
10	Enter Modify Compliance	RW	Valid for upstream port only.	No/Yes	0
11	Compliance SOS	RW	Valid for upstream port only.	No/Yes	0
12	Compliance_Deemp	RW	Valid for upstream port only.	No/Yes	0
15:13	Reserved	RsvdP	Not Support.	No	000b

8.2.54 LINK STATUS REGISTER 2 – OFFSET 98h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
16	Current De-emphasis level	RO	0b:current de-emphasis level is -3.5db 1b: current de-emphasis level is -6.0db	No	0 for Up 1 for Down
31:17	Reserved	RO	Not Support.	No	0-0h

8.2.55 SLOT CAPABILITIES REGISTER 2 – OFFSET 9Ch

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:0	Slot Capability 2	RO	Not Support.	No	0000_0000h

8.2.56 SLOT CONTROL REGISTER 2 – OFFSET A0h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
15:0	Slot Control 2	RO	Not Support.	No	0000h

8.2.57 SLOT STATUS REGISTER 2 – OFFSET A0h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:16	Slot Status 2	RO	Not Support.	No	0000h

8.2.58 SSID/SSVID CAPATILITIES REGISTER – OFFSET A4h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
7:0	SSID/SSVID Capabilities ID	RO	Read as 0Dh to indicate that these are SSID/SSVID capability registers.	No	0Dh
15:8	Next Item Pointer	RO	Read as 00h. No other ECP registers.	Yes	00h

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BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:16	Reserved	RsvdP	Not Support.	No	0000h

8.2.59 SUBSYSTEM VENDOR ID REGISTER – OFFSET A8h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
15:0	SSVID	RO	Indicates the sub-system vendor id.	Yes	12D8h

8.2.60 SUBSYSTEM ID REGISTER – OFFSET A8h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:16	SSID	RO	Indicates the sub-system device id.	Yes	2912h

8.2.61 BAR 0-1 CONFIGURATION REGISTER – OFFSET E4h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
1:0	BAR0 Type	RW	Decides whether BAR0 is 32 or 64 bit addressing. 00b: Disable BAR0/1 01b: Reserved 10b: 32-bit addressing 11b: 64-bit addressing	Yes	10b
2	BAR0 Prefetchable	RW	0b: Non Prefetchable 1b: Prefetchable	Yes	0
31:3	Reserved	RsvdP	Not Support.	No	0-0h

8.2.62 DEVICE SERIAL NUMBER ENHANCED CAPABILITY HEADER REGISTER – OFFSET 100h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
15:0	Extended Capabilities ID	RO	Read as 0003h to indicate that these are PCI express extended capability registers for device serial number extend capability register.	No	0003h
19:16	Capability Version	RO	Must be 1h for this version.	No	1h
31:20	Next Capability Offset	RO	Indicates next capability pointer.	Yes	FB4h

8.2.63 DEVICE SERIAL NUMBER LOWER DW REGISTER – OFFSET 104h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:0	Device serial number 1st DW	RO	First dword for device serial number.	Yes	0000_0000h

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8.2.64 DEVICE SERIAL NUMBER HIGHER DW REGISTER – OFFSET 108h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:0	Device serial number 2nd DW	RO	Second dword for device serial number.	Yes	0000_0000h

8.2.65 PCI EXPRESS POWER BUDGETING ENHANCED CAPABILITY HEADER REGISTER – OFFSET 138h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
15:0	Extended Capabilities ID	RO	Read as 0004h to indicate that these are PCI express extended capability registers for power budgeting.	No	0004h
19:16	Capability Version	RO	Must be 1h for this version.	No	01h
31:20	Next Capability Offset	RO	Indicates next capability pointer.	Yes	148h

8.2.66 DATA SELECT REGISTER – OFFSET 13Ch (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
7:0	Data Selection	RW	It indexes the power budgeting data reported through the data register. When 00h, it selects D0 Max power budget When 01h, it selects D0 Sustained power budget Other values would return zero power budgets, which means not supported.	No/Yes	00h
31:8	Reserved	RsvdP	Not Support.	No	0-0h

8.2.67 POWER BUDGETING DATA REGISTER – OFFSET 140h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
7:0	Base Power	RO	It specifies the base power value in watts. This value represents the required power budget in the given operation condition.	Yes	04h if 13Ch=0 03h if 13Ch=1
9:8	Data Scale	RO	It specifies the scale to apply to the base power value.	Yes	00b
12:10	PM Sub State	RO	It specifies the power management sub state of the given operation condition. It is initialized to the default sub state.	No	000b
14:13	PM State	RO	It specifies the power management state of the given operation condition. It defaults to the D0 power state.	Yes	00b
17:15	Type	RO	It specifies the type of the given operation condition which is controlled by offset 13Ch[7:0]. It defaults to the Maximum power state.	Yes	111b if 13Ch=0 011b if 13Ch=1
20:18	Power Rail	RO	It specifies the power rail of the given operation condition..	No	010b
31:21	Reserved	RsvdP	Not Support.	No	0-0h

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8.2.68 POWER BUDGET CAPABILITY REGISTER – OFFSET 144h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	System Allocated	RO	When set, it indicates that the power budget for the device is included within the system power budget.	Yes	1
31:1	Reserved	RsvdP	Not Support.	No	0-0h

8.2.69 PCI EXPRESS VIRTUAL CHANNEL ENHANCED CAPABILITY HEADER REGISTER – OFFSET 148h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
15:0	Extended Capabilities ID	RO	Read as 0002h to indicate that these are PCI express extended capability registers for virtual channel.	No	02h
19:16	Capability Version	RO	Read as 1h.	No	01h
31:20	Next Capability Offset	RO	Indicates next capability pointer.	Yes	270h for Up 520h for Down

8.2.70 PORT VC CAPABILITY REGISTER 1 – OFFSET 14Ch

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
2:0	Extended VC Count	RO	Indicates the number of extended Virtual Channels in addition to the default VC supported by the Switch.	Yes	000b
3	Reserved	RsvdP	Not Support.	No	0
6:4	Low Priority Extended VC Count	RO	Indicates the number of extended Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group.	Yes	000b
7	Reserved	RO	Not Support.	No	0
9:8	Reference Clock	RO	Indicates the reference clock for Virtual Channels that support time-based WRR Port Arbitration. Defined encoding is 00b for 100 ns reference clock.	No	00b
11:10	Port Arbitration Table Entry Size	RO	Read as 10b to indicate the size of Port Arbitration table entry in the device is 4 bits.	No	10b
31:12	Reserved	RsvdP	Not Support.	No	0000_0h

8.2.71 PORT VC CAPABILITY REGISTER 2 – OFFSET 150h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
7:0	VC Arbitration Capability	RO	It indicates the types of VC Arbitration supported by the device for the LPVC group. This field is valid when LPVC is greater than 0. The Switch supports Hardware fixed arbitration scheme, e.g., Round Robin and Weight Round Robin arbitration with 32 phases in LPVC.	No	00h
23:8	Reserved	RsvdP	Not Support.	No	0000h
31:24	VC Arbitration Table Offset	RO	It indicates the location of the VC Arbitration Table as an offset from the base address of the Virtual Channel Capability register in the unit of DQWD (16 bytes).	No	00h if VC1=0 04h if VC1=1

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8.2.72 PORT VC CONTROL REGISTER – OFFSET 154h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	Load VC Arbitration Table	WO	When set, the programmed VC Arbitration Table is applied to the hardware. This bit always returns '0' when read.	Yes	0
3:1	VC Arbitration Select	RW	This field is used to configure the VC Arbitration by selecting one of the supported VC Arbitration schemes. The valid values for the schemes supported by Switch are 0b and 1b. Other value than these written into this register will be treated as default.	No/Yes	000b
15:4	Reserved	RsvdP	Not Support.	No	000h

8.2.73 PORT VC STATUS REGISTER – OFFSET 154h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
16	VC Arbitration Table Status	RO	When set, it indicates that any entry of the VC Arbitration Table is written by software. This bit is cleared when hardware finishes loading values stored in the VC Arbitration Table after the bit of "Load VC Arbitration Table" is set.	No	0
31:17	Reserved	RsvdP	Not Support.	No	0-0h

8.2.74 VC RESOURCE CAPABILITY REGISTER (0) – OFFSET 158h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
7:0	Port Arbitration Capability	RO	It indicates the types of Port Arbitration supported by the VC resource. The Switch supports Hardware fixed arbitration scheme, e.g., Round Robin, Weight Round Robin (WRR) arbitration with 128 phases (3~4 enabled ports) and Time-based WRR with 128 phases (3~4 enabled ports). Note that the Time-based WRR is only valid in VC1.	No	03h
13:8	Reserved	RsvdP	Not Support.	No	00_0000h
14	Advanced Packet Switching	RO	When set, it indicates the VC resource only supports transaction optimized for Advanced Packet Switching (AS).	No	0
15	Reject Snoop Transactions	RsvdP	Not Support.	No	0
22:16	Maximum Time Slots	RO	It indicates the maximum numbers of time slots (minus one) are allocated for Isochronous traffic.	No	3Fh
23	Reserved	RsvdP	Not Support.	No	0
31:24	Port Arbitration Table Offset	RO	It indicates the location of the Port Arbitration Table (n) as an offset from the base address of the Virtual Channel Capability register in the unit of DQWD (16 bytes).	No	05h

8.2.75 VC RESOURCE CONTROL REGISTER (0) – OFFSET 15Ch

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
7:0	TC/VC Map	RW	This field indicates the TCs that are mapped to the VC resource. Bit locations within this field correspond to TC values. When the bits in this field are set, it means that the corresponding TCs are mapped to the VC resource. Bit 0 of this filed is read-only and must be set to "1" for the VC0.	Yes	FFh
15:8	Reserved	RsvdP	Not Support.	No	00h
16	Load Port Arbitration Table	RW	When set, the programmed Port Arbitration Table is applied to the hardware. This bit always returns '0' when read.	No/Yes	0

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BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
19:17	Port Arbitration Select	RW	This field is used to configure the Port Arbitration by selecting one of the supported Port Arbitration schemes. The permissible values for the schemes supported by Switch are 000b and 011b at VC0, other value than these written into this register will be treated as default.	No/Yes	000b
23:20	Reserved	RsvdP	Not Support.	No	0h
26:24	VC ID	RO	This field assigns a VC ID to the VC resource.	No	000b
30:27	Reserved	RsvdP	Not Support.	No	0h
31	VC Enable	RW	0b: it disables this Virtual Channel 1b: it enables this Virtual Channel	No	1

8.2.76 VC RESOURCE STATUS REGISTER (0) – OFFSET 160h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
15:0	Reserved	RsvdP	Not Support.	No	0000h
16	Port Arbitration Table Status	RO	When set, it indicates that any entry of the Port Arbitration Table is written by software. This bit is cleared when hardware finishes loading values stored in the Port Arbitration Table after the bit of "Load Port Arbitration Table" is set.	No	0
17	VC Negotiation Pending	RO	When set, it indicates that the VC resource is still in the process of negotiation. This bit is cleared after the VC negotiation is complete.	No	0
31:18	Reserved	RsvdP	Not Support.	No	0-0h

8.2.77 VC RESOURCE CAPABILITY REGISTER (1) – OFFSET 164h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
7:0	Port Arbitration Capability	RO	It indicates the types of Port Arbitration supported by the VC resource. The Switch supports Hardware fixed arbitration scheme, e.g., Round Robin, Weight Round Robin (WRR) arbitration with 128 phases (3~4 enabled ports) and Time-based WRR with 128 phases (3~4 enabled ports). Note that the Time-based WRR is only valid in VC1.	No	00h if VC1=0 13h if VC1=1
13:8	Reserved	RsvdP	Not Support.	No	0-0h
14	Advanced Packet Switching	RO	When set, it indicates the VC resource only supports transaction optimized for Advanced Packet Switching (AS).	No	0
15	Reject Snoop Transactions	RO	This bit is not applied to PCIe Switch.	No	0
22:16	Maximum Time Slots	RO	It indicates the maximum numbers of time slots (minus one) are allocated for Isochronous traffic.	Yes	00h if VC1=0 3Fh if VC1=1
23	Reserved	RsvdP	Not Support.	No	0
31:24	Port Arbitration Table Offset	RO	It indicates the location of the Port Arbitration Table (n) as an offset from the base address of the Virtual Channel Capability register in the unit of DQWD (16 bytes).	No	00h if VC1=0 06h if VC1=1

8.2.78 VC RESOURCE CONTROL REGISTER (1) – OFFSET 168h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
7:0	TC/VC Map	RW	This field indicates the TCs that are mapped to the VC resource. Bit locations within this field correspond to TC values. When the bits in this field are set, it means that the corresponding TCs are mapped to the VC resource. Bit 0 of this filed is read-only and must be set to "0" for the VC1.	Yes	00h
15:8	Reserved	RsvdP	Not Support.	No	00h

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BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
16	Load Port Arbitration Table	RW	When set, the programmed Port Arbitration Table is applied to the hardware. This bit always returns 0b when read.	No/Yes	0
19:17	Port Arbitration Select	RW	This field is used to configure the Port Arbitration by selecting one of the supported Port Arbitration schemes. The permissible values for the schemes supported by Switch are 000b, 011b and 100b at VC1, other value than these written into this register will be treated as default.	No/Yes	000b
23:20	Reserved	RsvdP	Not Support.	No	0h
26:24	VC ID	RW	This field assigns a VC ID to the VC resource.	No/Yes	000b if VC1=0 001b if VC1=1
30:27	Reserved	RsvdP	Not Support.	No	0h
31	VC Enable	RW	0b: it disables this Virtual Channel 1b: it enables this Virtual Channel	No/Yes	0

8.2.79 VC RESOURCE STATUS REGISTER (1) – OFFSET 16Ch

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
15:0	Reserved	RsvdP	Not Support.	No	0000h
16	Port Arbitration Table Status	RO	When set, it indicates that any entry of the Port Arbitration Table is written by software. This bit is cleared when hardware finishes loading values stored in the Port Arbitration Table after the bit of "Load Port Arbitration Table" is set.	No	0
17	VC Negotiation Pending	RO	When set, it indicates that the VC resource is still in the process of negotiation. This bit is cleared after the VC negotiation is complete.	No	0
31:18	Reserved	RsvdP	Not Support.	No	0-0h

8.2.80 VC ARBITRATION TABLE REGISTER – OFFSET 188h

The VC arbitration table is a read-write register array that contains a table for VC arbitration. Each table entry allocates four bits, of which three bits are used to represent VC ID and one bit is reserved. A total of 32 entries are used to construct the VC arbitration table. The layout for this register array is shown below.

Table 8-2 Register Array Layout for VC Arbitration

31 - 28	27 - 24	23 - 20	19 - 16	15 - 12	11 - 8	7 - 4	3 - 0	Byte Location	EEPROM/ I2C-SMBUS	DEFAULT
Phase [7]	Phase [6]	Phase [5]	Phase [4]	Phase [3]	Phase [2]	Phase [1]	Phase [0]	00h	No/Yes	0000_0000h
Phase [15]	Phase [14]	Phase [13]	Phase [12]	Phase [11]	Phase [10]	Phase [9]	Phase [8]	04h	No/Yes	0000_0000h
Phase [23]	Phase [22]	Phase [21]	Phase [20]	Phase [19]	Phase [18]	Phase [17]	Phase [16]	08h	No/Yes	0000_0000h
Phase [31]	Phase [30]	Phase [29]	Phase [28]	Phase [27]	Phase [26]	Phase [25]	Phase [24]	0Ch	No/Yes	0000_0000h

8.2.81 PORT ARBITRATION TABLE REGISTER (0) and (1) – OFFSET 198h and 1A8h

The Port arbitration table is a read-write register array that contains a table for Port arbitration. Each table entry allocates two bits to represent Port Number. The table entry size is dependent on the number of enabled ports (refer to bit 10 and 11 of Port VC capability register 1). The arbitration table contains 32 entries if three or four ports are to be enabled. The following table shows the register array layout for the size of entry equal to two.

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Table 8-3 Table Entry Size in 4 Bits

31 - 24	23 - 16	15 - 8	7 - 0	Byte Location	EEPROM/ I2C-SMBUS	DEFAULT
Phase [7:6]	Phase [5:4]	Phase [3:2]	Phase [1:0]	00h	No/Yes	0000_0000h
Phase [15:14]	Phase [13:12]	Phase [11:10]	Phase [9:8]	04h	No/Yes	0000_0000h
Phase [23:22]	Phase [21:20]	Phase [19:18]	Phase [17:16]	08h	No/Yes	0000_0000h
Phase [31:30]	Phase [29:28]	Phase [27:26]	Phase [25:24]	0Ch	No/Yes	0000_0000h

8.2.82 ECC ERROR CHECK DISABLE REGISTER – OFFSET 1C8h (Global)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
3:0	Reserved	RW	Test used only.	No/Yes	000
4	Enable INTA_L for Hot Plug or Link State Event	RW	0b: Send an INTx Message for Hot Plug or Link State Event 1b: Assert INTA_L for Hot Plug or Link State Event	No/Yes	0
5	Reserved	RW	Test used only.	No/Yes	0
6	Enable INTA_L for GPIO-Generated Interrupts	RW	0b: Send an INTx Message for GPIO Interrupt Requests 1b: Assert INTA_L for GPIO Interrupt Requests	No/Yes	0
31: 7	Reserved	RsvdP	Not Support.	No	0-0h

8.2.83 UP PORT SELECTION REGISTER – OFFSET 1DCh (Global)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
7:0	Reserved	RsvdP	Not Support.	No	00h
11:8	UP_PORT_SEL[0]	HWInt RW	Used to select Upstream Port when Bit[15]=1. Bit[9]: used to set PORTCFG[0] Bit[11]: used to set PORTCFG[1]	No/Yes	0h
14:12	Reserved	RsvdP	Not Support.	No	000
15	Software_CFG_Mode	RW	When set to 1, UP Port is decided by Bit[11:8].	No/Yes	0
23:16	Reserved	RsvdP	Not Support.	No	00h
27:24	Reserved	RsvdP	Not Support.	No	0h
31:28	Reserved	RsvdP	Not Support.	No	0h

8.2.84 HOT PLUG CONFIGURATION REGISTER – OFFSET 1E0h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
1:0	Reserved	RsvdP	Not Support.	No	00b
2	HPC_PME_TURN_ OFF_En	RW	Valid for downstream ports only. 0b: disable to send out PME_TURN_OFF message. 1b: enable to send out PME_TURN_OFF message.	Yes	0
4:3	HPC_Timer	RW	Valid for downstream ports only. Used to set hot plug port timer. 00b: Reserved 01b: 128 ms 10b: 256 ms 11b: 512 ms	Yes	01b
5	Reserved	RsvdP	Not Support.	No	0

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BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
6	HPC_PG_ ActiveLow_En	RW	Valid for downstream ports only. 0b: PWR_GOODx pins are Active high. 1b: PWR_GOODx pins are Active low.	Yes	0
11:7	Reserved	RsvdP	Not Support.	No	0-0h
12	NT_Serial_HotPlug _En	RW	Valid for NT port only. 0b: disable serial hot plug capability on NT port. 1b: enable serial hot plug capability on NT port.	No	0
14:7	Reserved	RsvdP	Not Support.	No	0-0h
15	IOE_Cmd_In_ Progress	RO	Indicates that the Write command to an IOE (I/O Expander) GPIOx Output Data register is still in progress.	No	0
16	HPC_Serial_HotPlug _Disable	RW	Valid for upstream port only. 0b: enable serial hot plug capability for all downstream ports. 1b: disable serial hot plug capability for all downstream ports.	Yes	0
17	IOE_40Bit_En	RW	Valid for upstream port only. 0b: enable 16-pin IOE for all downstream ports. 1b: enable 40-pin IOE for all downstream ports.	Yes	0
18	HPC_GPIO_Dir	RW	0b: set GPIO direction to input pin 1b: set GPIO direction to output pin	Yes	0
19	HPC_GPIO_Value	RW	I/O Expander GPIO Value.	Yes	0
20	HPC_I/O_Reload	RW	1b: the value of Hotplug Controller Output pin is reloaded. This bit is self clearing.	Yes	0
26:21	HPC_Output_Reload _Value	RW	When Bit [20] is set, values from this field are reloaded.	Yes	000b
31:27	Reserved	RsvdP	Not Support.	No	0000_0b

8.2.85 SOFTWARE LANE STATUS REGISTER – OFFSET 1F4h (Global)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:0	Software Lane Status	RO	Indicates current lane status. 0b: link down 1b: link up Bit[3:0]: for Lane 3 to Lane 0 Bit[15:12]: for Lane 11 to Lane 8 Bit[19:16]: for Lane 7 to Lane 4 Others: Reserved	No	0000_0000h

8.2.86 DE-EMPHASIS AND RATE CONTROL REGISTER – OFFSET 208h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
15:0	Rate Ctrl	RW	Test used only. 0h: GEN1 speed 1h: GEN2 speed	No/Yes	0000h
31:16	De-emphasis Ctrl	RW	Test used only. 0h: -6 dB 1h: -3.5 dB	No/Yes	0000h

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8.2.87 COMPLIANCE MODE CONTROL REGISTER – OFFSET 20Ch

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
15:0	Compliance Mode	RW	Test used only. 1h: enter Compliance mode	No/Yes	0000h
31:16	Reserved	RsvdP	Not Support.	No	0000h

8.2.88 EVEN PORT PHYSICAL LAYER COMMAND AND STATUS REGISTER – OFFSET 220h (Global)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	PORT0_Loopback_ CMD	RW	Test used only.	No/Yes	0
1	PORT0_Scramble_ Disable_CMD	RW	Test used only.	No/Yes	0
2	PORT0_Compliance _Receive	RW	Test used only.	No/Yes	0
3	Reserved	RsvdP	Not Support.	No	0
4	PORT2_Loopback_ CMD	RW	Test used only.	No/Yes	0
5	PORT2_Scramble_ Disable_CMD	RW	Test used only.	No/Yes	0
6	PORT2_Compliance _Receive	RW	Test used only.	No/Yes	0
19:7	Reserved	RsvdP	Not Support.	No	0-0b
20	PORT10_Loopback_ CMD	RW	Test used only.	No/Yes	0
21	PORT10_Scramble_ Disable_CMD	RW	Test used only.	No/Yes	0
22	PORT10_Compliance_Receive	RW	Test used only.	No/Yes	0
23	Reserved	RsvdP	Not Support.	No	0
24	PORT12_Loopback_ CMD	RW	Test used only.	No/Yes	0
25	PORT12_Scramble_ Disable_CMD	RW	Test used only.	No/Yes	0
26	PORT12_Compliance_Receive	RW	Test used only.	No/Yes	0
27	Reserved	RsvdP	Not Support.	No	0
28	PORT14_Loopback_ CMD	RW	Test used only.	No/Yes	0
29	PORT14_Scramble_ Disable_CMD	RW	Test used only.	No/Yes	0
30	PORT14_Compliance_Receive	RW	Test used only.	No/Yes	0
31	Reserved	RsvdP	Not Support.	No	0

8.2.89 ODD PORT PHYSICAL LAYER COMMAND AND STATUS REGISTER – OFFSET 224h (Global)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
3:0	Reserved	RsvdP	Not Support.	No	0h
4	PORT3_Loopback_ CMD	RW	Test used only.	No/Yes	0

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BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
5	PORT3_Scramble_ Disable_CMD	RW	Test used only.	No/Yes	0
6	PORT3_Compliance _Receive	RW	Test used only.	No/Yes	0
19:7	Reserved	RsvdP	Not Support.	No	0-0b
20	PORT11_Loopback_ CMD	RW	Test used only.	No/Yes	0
21	PORT11_Scramble_ Disable_CMD	RW	Test used only.	No/Yes	0
22	PORT11_ Compliance_Receive	RW	Test used only.	No/Yes	0
23	Reserved	RsvdP	Not Support.	No	0
24	PORT13_Loopback_ CMD	RW	Test used only.	No/Yes	0
25	PORT13_Scramble_ Disable_CMD	RW	Test used only.	No/Yes	0
26	PORT13_ Compliance_Receive	RW	Test used only.	No/Yes	0
27	Reserved	RsvdP	Not Support.	No	0
28	PORT15_Loopback_ CMD	RW	Test used only.	No/Yes	0
29	PORT15_Scramble_ Disable_CMD	RW	Test used only.	No/Yes	0
30	PORT15_ Compliance_Receive	RW	Test used only.	No/Yes	0
31	Reserved	RsvdP	Not Support.	No	0

8.2.90 EVEN PORT DISABLE/QUIET/TEST PATTERN RATE REGISTER – OFFSET 230h (Global)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
7:0	Even Port Disable	RW	0b: enable LTSSM operation. 1b: force LTSSM in the Detect.Quiet state. Bit[0]: for Port 0 Bit[1]: for Port 2 Bit[5]: for Port 10 Bit[6]: for Port 12 Bit[7]: for Port 14 Others: Reserved	No/Yes	00h
15:8	Even Port Quiet	RW	0b: LTSSM is allowed to exit the Detect.Quiet state 1b: LTSSM remains in the Detect.Quiet state Bit[0]: for Port 0 Bit[1]: for Port 2 Bit[5]: for Port 10 Bit[6]: for Port 12 Bit[7]: for Port 14 Others: Reserved	No/Yes	00h
23:16	Even Port Test Pattern Rate	RW	Test used only.	No/Yes	00h
31:24	Reserved	RsvdP	Not Support.	No	00h

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8.2.91 ODD PORT DISABLE/QUIET/TEST PATTERN RATE REGISTER – OFFSET 234h (Global)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
7:0	Odd Port Disable	RW	0b: enable LTSSM operation 1b: force LTSSM in the Detect.Quiet state Bit[1]: for Port 3 Bit[5]: for Port 11 Bit[6]: for Port 13 Bit[7]: for Port 15 Others: Reserved	No/Yes	00h
15:8	Odd Port Quiet	RW	0b: LTSSM is allowed to exit the Detect.Quiet state 1b: LTSSM remains in the Detect.Quiet state Bit[1]: for Port 3 Bit[5]: for Port 11 Bit[6]: for Port 13 Bit[7]: for Port 15 Others: Reserved	No/Yes	00h
23:16	Odd Port Test Pattern Rate	RW	Test used only.	No/Yes	00h
31:24	Reserved	RsvdP	Not Support.	No	00h

8.2.92 LI PM SUBSTATES ENHANCED CAPABILITY HEADER – OFFSET 270h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
15:0	PCI Express Extended Capability ID	RO	Read as 001Eh to indicate PCI Express Extended Capability ID for L1 PM Substates Extended Capability.	No	001Eh
19:16	Capability Version	RO	Must be 1h for this version.	No	1h
31:20	Next Capability Offset	RO	Indicates next capability pointer.	Yes	900h

8.2.93 L1 PM SUBSTATES CAPABILITY REGISTER – OFFSET 274h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	Reserved	RsvdP	Not Support.	No	0
1	PCI-PM L1.1 Supported	RO	When set this bit indicates that PCI-PM L1.1 is supported and must be set by all ports implementing L1 PM Substates.	Yes	1
2	Reserved	RO	Not Support.	No	0
3	ASPM L1.1 Supported	RO	When set this bit indicates that ASPM L1.1 is supported.	Yes	0
4	L1 PM Substates Supported	RO	When set this bit indicates that this port supports L1 PM Substates.	Yes	1
31:5	Reserved	RsvdP	Not Support.	No	0-0h

8.2.94 L1 PM SUBSTATES CONTROL 1 REGISTER – OFFSET 278h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	Reserved	RsvdP	Not Support.	No	0
1	PCI-PM L1.1 Enable	RW	When set this bit enables PCI-PM L1.1. Required for both upstream and downstream ports.	No/Yes	0

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BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
2	Reserved	RsvdP	Not Support.	No	0
3	ASPM L1.1 Enable	RW	When set this bit enables ASPM L1.1. Required for both upstream and downstream ports.	No/Yes	0
31:4	Reserved	RsvdP	Not Support.	No	0-0h

8.2.95 L1 PM SUBSTATES CONTROL 2 REGISTER – OFFSET 27Ch

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:0	Reserved	RsvdP	Not Support.	No	0000_0000h

8.2.96 SMBUS CONTROL AND STATUS REGISTER – OFFSET 344h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	SMBus Enable	HWInt RW	0b: disable SMBUS, enable I2C 1b: enable SMBUS	No/Yes	0
7:1	SMBUS Address	HwInt RW	Set SMBUS Address. Bit [3:1] are decided by the status of strapped pins (GPIO[7:5]).	No/Yes	0111_000b
8	ARP_Disable	RW	Test used only.	No/Yes	1
9	PEC Check Disable	RW	0b: enable PEC check 1b: disable PEC check	No/Yes	1
10	AV Flag	RW	Test used only.	No/Yes	0
11	AR Flag	RW	Test used only.	No/Yes	0
13:12	UDID Addr Type	RW	Test used only.	No/Yes	00b
14	UDID PEC Support	RW	Test used only	No/Yes	1
15	Reserved	RsvdP	Not Support.	No	0
23:16	UDID Vendor ID	RW	Test used only.	No/Yes	B0h
26:24	UDID Revision ID	RW	Test used only.	No/Yes	001b
27	Fty Test 0	RW	Test used only.	No/Yes	0
28	SMBUS In Progress	RO	0b: SMBUS interface is idle. 1b: SMBUS interface is busy.	No	0
29	PEC Check Fail	RO	0b: PEC check successfully 1b: PEC check failed	No	0
30	Unsupported SMBUS Command	RO	0b: supported command. 1b: unsupported command.	No	0
31	Reserved	RO	Not Support.	No	1

8.2.97 DISABLE DOWNSTREAM PORT HOT RESET REGISTER – OFFSET 34Ch (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	DN_Hot_Reset_Dis	RW	Disable downstream port hot reset.	Yes	0
31:1	Reserved	RsvdP	Not Support.	No	0-0h

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8.2.98 ACS ENHANCED CAPABILITY HEADER REGISTER – OFFSET 520h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
15:0	PCI Express Extended Capability ID	RO	Read as 000Dh to indicate PCI Express Extended Capability ID for ACS Extended Capability.	No	0Dh
19:16	Capability Version	RO	Must be 1h for this version.	No	1h
31:20	Next Capability Offset	RO	Indicates next capability pointer.	Yes	270h

8.2.99 ACS CAPABILITY REGISTER – OFFSET 524h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	ACS Source Validation	RO	Indicates the implements of ACS Source Validation.	No	1
1	ACS Translation Blocking	RO	Indicates the implements of ACS Translation Blocking.	No	1
2	ACS P2P Request Redirect	RO	Indicates the implements of ACS P2P Request Redirect.	No	1
3	ACS P2P Completion Redirect	RO	Indicates the implements of ACS P2P Completion Redirect	No	1
4	ACS Upstream Forwarding	RO	Indicates the implements of ACS Upstream Forwarding.	No	1
5	ACS P2P Egress control	RO	Indicates the implements of ACS P2P Egress control.	No	1
6	ACS Direct Translated P2P	RO	Indicates the implements of ACS Direct Translated P2P.	No	1
7	Reserved	RsvdP	Not Support.	No	0
15:8	Egress Control Vector Size	RO	Encodings 01h – FFh directly indicate the number of applicable bits in the Egress Control Vector.	No	10h
16	ACS Source Validation Enable	RW	0b: disable the source validation 1b: enable the source validation	No/Yes	0
17	ACS Translation Blocking Enable	RW	0b: disable ACS translation blocking 1b: enable ACS translation blocking	No/Yes	0
18	ACS P2P Request Redirect	RW	0b: disable ACS P2P request redirect 1b: enable ACS P2P request redirect	No/Yes	0
19	ACS P2P Completion Redirect Enable	RW	0b: disable ACS P2P completion redirect 1b: enable ACS P2P completion redirect	No/Yes	0
20	ACS Upstream Forwarding Enable	RW	0b: disable ACS upstream forwarding 1b: enables ACS upstream forwarding	No/Yes	0
21	ACS P2P Egress control Enable	RW	0b: disable ACS P2P egress control 1b: enable ACS P2P egress control	No/Yes	0
22	ACS Direct Translated P2P Enable	RW	0b: disable ACS direct translated P2P 1b: enable ACS Direct Translated P2P	No/Yes	0
31:23	Reserved	RsvdP	Not Support.	No	00h

8.2.100 EGRESS CONTROL VECTOR REGISTER – OFFSET 528h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
15:0	Egress Control Vector	RW	When a given bit is set, peer-to-peer requests targeting the associated Port are blocked or redirected.	No/Yes	0000h
31:16	Reserved	RsvdP	Not Support.	No	0000h

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8.2.101 GPIO 0-15 DIRECTION CONTROL REGISTER – OFFSET 62Ch (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	GPIO[0] Source/Destination	RW	As Input: 0b: Input Data Register (offset 63Ch[0] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[0] Output Data register (offset 644h[0]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 0	No/Yes	0
1	GPIO[0] Direction Control	RW	0b: Input 1b: Output	No/Yes	0
2	GPIO[1] Source/Destination	RW	As Input: 0b: Input Data Register (offset 63Ch[1] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[1] Output Data register (offset 644h[1]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 1	No/Yes	0
3	GPIO[1] Direction Control	RW	0b: Input 1b: Output	No/Yes	0
4	GPIO[2] Source/Destination	RW	As Input: 0b: Input Data Register (offset 63Ch[2] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[2] Output Data register (offset 644h[2]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 2	No/Yes	0
5	GPIO[2] Direction Control	RW	0b: Input 1b: Output	No/Yes	0
6	GPIO[3] Source/Destination	RW	As Input: 0b: Input Data Register (offset 63Ch[3] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[3] Output Data register (offset 644h[3]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 3	No/Yes	0
7	GPIO[3] Direction Control	RW	0b: Input 1b: Output	No/Yes	0
8	GPIO[4] Source/Destination	RW	As Input: 0b: Input Data Register (offset 63Ch[4] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[4] Output Data register (offset 644h[4]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 4	No/Yes	0
9	GPIO[4] Direction Control	RW	0b: Input 1b: Output	No/Yes	0
10	GPIO[5] Source/Destination	RW	As Input: 0b: Input Data Register (offset 63Ch[5] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[5] Output Data register (offset 644h[5]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 5	No/Yes	0
11	GPIO[5] Direction Control	RW	0b: Input 1b: Output	No/Yes	0
12	GPIO[6] Source/Destination	RW	As Input: 0b: Input Data Register (offset 63Ch[6] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[6] Output Data register (offset 644h[6]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 6	No/Yes	0
13	GPIO[6] Direction Control	RW	0b: Input 1b: Output	No/Yes	0

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BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
14	GPIO[7] Source/Destination	RW	As Input: 0b: Input Data Register (offset 63Ch[7] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[7] Output Data register (offset 644h[7]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 7	No/Yes	0
15	GPIO[7] Direction Control	RW	0b: Input 1b: Output	No/Yes	0
16	GPIO[8] Source/Destination	RW	As Input: 0b: Input Data Register (offset 63Ch[8] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[8] Output Data register (offset 644h[8]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 8	No/Yes	0
17	GPIO[8] Direction Control	RW	0b: Input 1b: Output	No/Yes	0
18	GPIO[9] Source/Destination	RW	As Input: 0b: Input Data Register (offset 63Ch[9] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[9] Output Data register (offset 644h[9]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 9	No/Yes	0
19	GPIO[9] Direction Control	RW	0b: Input 1b: Output	No/Yes	0
20	GPIO[10] Source/Destination	RW	As Input: 0b: Input Data Register (offset 63Ch[10] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[10] Output Data register (offset 644h[10]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 10	No/Yes	0
21	GPIO[10] Direction Control	RW	0b: Input 1b: Output	No/Yes	0
22	GPIO[11] Source/Destination	RW	As Input: 0b: Input Data Register (offset 63Ch[11] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[11] Output Data register (offset 644h[11]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 11	No/Yes	0
23	GPIO[11] Direction Control	RW	0b: Input 1b: Output	No/Yes	0
24	GPIO[12] Source/Destination	RW	As Input: 0b: Input Data Register (offset 63Ch[12] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[12] Output Data register (offset 644h[12]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 12	No/Yes	0
25	GPIO[12] Direction Control	RW	0b: Input 1b: Output	No/Yes	0
26	GPIO[13] Source/Destination	RW	As Input: 0b: Input Data Register (offset 63Ch[13] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[13] Output Data register (offset 644h[13]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 13	No/Yes	0
27	GPIO[13] Direction Control	RW	0b: Input 1b: Output	No/Yes	0
28	GPIO[14] Source/Destination	RW	As Input: 0b: Input Data Register (offset 63Ch[14] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[14] Output Data register (offset 644h[14]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 14	No/Yes	0
29	GPIO[14] Direction Control	RW	0b: Input 1b: Output	No/Yes	0

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BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
30	GPIO[15] Source/Destination	RW	As Input: 0b: Input Data Register (offset 63Ch[15] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[15] Output Data register (offset 644h[15]) 1b: Serial Hot Plug PERST# output for Hot Plug Port 15	No/Yes	0
31	GPIO[15] Direction Control	RW	0b: Input 1b: Output	No/Yes	0

8.2.102 GPIO 16-31 DIRECTION CONTROL REGISTER – OFFSET 630h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	GPIO[16] Source/Destination	RW	As Input: 0b: Input Data Register (offset 640h[0] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[16] Output Data register (offset 648h[0]) 1b: Reserved	No/Yes	0
1	GPIO[16] Direction Control	RW	0b: Input 1b: Output	No/Yes	0
2	GPIO[17] Source/Destination	RW	As Input: 0b: Input Data Register (offset 640h[1] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[17] Output Data register (offset 648h[1]) 1b: Reserved	No/Yes	0
3	GPIO[17] Direction Control	RW	0b: Input 1b: Output	No/Yes	0
4	GPIO[18] Source/Destination	RW	As Input: 0b: Input Data Register (offset 640h[2] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[18] Output Data register (offset 648h[2]) 1b: Reserved	No/Yes	0
5	GPIO[18] Direction Control	RW	0b: Input 1b: Output	No/Yes	0
6	GPIO[19] Source/Destination	RW	As Input: 0b: Input Data Register (offset 640h[3] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[19] Output Data register (offset 648h[3]) 1b: Reserved	No/Yes	0
7	GPIO[19] Direction Control	RW	0b: Input 1b: Output	No/Yes	0
8	GPIO[20] Source/Destination	RW	As Input: 0b: Input Data Register (offset 640h[4] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[20] Output Data register (offset 648h[4]) 1b: Reserved	No/Yes	0
9	GPIO[20] Direction Control	RW	0b: Input 1b: Output	No/Yes	0
10	GPIO[21] Source/Destination	RW	As Input: 0b: Input Data Register (offset 640h[5] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[21] Output Data register (offset 648h[5]) 1b: Reserved	No/Yes	0
11	GPIO[21] Direction Control	RW	0b: Input 1b: Output	No/Yes	0

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BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
12	GPIO[22] Source/Destination	RW	As Input: 0b: Input Data Register (offset 640h[6] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[22] Output Data register (offset 648h[6]) 1b: Reserved	No/Yes	0
13	GPIO[22] Direction Control	RW	0b: Input 1b: Output	No/Yes	0
14	GPIO[23] Source/Destination	RW	As Input: 0b: Input Data Register (offset 640h[7] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[23] Output Data register (offset 648h[7]) 1b: Reserved	No/Yes	0
15	GPIO[23] Direction Control	RW	0: Input 1: Output	No/Yes	0
16	GPIO[24] Source/Destination	RW	As Input: 0b: Input Data Register (offset 640h[8] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[24] Output Data register (offset 648h[8]) 1b: Reserved	No/Yes	0
17	GPIO[24] Direction Control	RW	0b: Input 1b: Output	No/Yes	0
18	GPIO[25] Source/Destination	RW	As Input: 0b: Input Data Register (offset 640h[9] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[25] Output Data register (offset 648h[9]) 1b: Reserved	No/Yes	0
19	GPIO[25] Direction Control	RW	0b: Input 1b: Output	No/Yes	0
20	GPIO[26] Source/Destination	RW	As Input: 0b: Input Data Register (offset 640h[10] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[26] Output Data register (offset 648h[10]) 1b: Reserved	No/Yes	0
21	GPIO[26] Direction Control	RW	0b: Input 1b: Output	No/Yes	0
22	GPIO[27] Source/Destination	RW	As Input: 0b: Input Data Register (offset 640h[11] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[27] Output Data register (offset 648h[11]) 1b: Reserved	No/Yes	0
23	GPIO[27] Direction Control	RW	0b: Input 1b: Output	No/Yes	0
24	GPIO[28] Source/Destination	RW	As Input: 0b: Input Data Register (offset 640h[12] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[28] Output Data register (offset 648h[12]) 1b: Reserved	No/Yes	0
25	GPIO[28] Direction Control	RW	0b: Input 1b: Output	No/Yes	0
26	GPIO[29] Source/Destination	RW	As Input: 0b: Input Data Register (offset 640h[13] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[29] Output Data register (offset 648h[13]) 1b: Reserved	No/Yes	0
27	GPIO[29] Direction Control	RW	0b: Input 1b: Output	No/Yes	0

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BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
28	GPIO[30] Source/Destination	RW	As Input: 0b: Input Data Register (offset 640h[14] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[30] Output Data register (offset 648h[14]) 1b: Reserved	No/Yes	0
29	GPIO[30] Direction Control	RW	0b: Input 1b: Output	No/Yes	0
30	GPIO[31] Source/Destination	RW	As Input: 0b: Input Data Register (offset 640h[15] 1b: General Interrupt (INTx, MSI or PEX_INTA#) As Output: 0b: From GPIO[31] Output Data register (offset 648h[15]) 1b: Reserved	No/Yes	0
31	GPIO[31] Direction Control	RW	0b: Input 1b: Output	No/Yes	0

8.2.103 GPIO INPUT DE-BOUNCE REGISTER – OFFSET 638h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:0	GPIOx Input De-Bounce Control	RW	Controls de-bounce when the corresponding GPIOx signal is configured as an input. Bit[31:0] correspond to GPIO[31:0] respectively. 0b: GPIOx input is not de-bounced 1b: GPIOx input is de-bounced	No/Yes	0000_0000h

8.2.104 GPIO 0-15 INPUT DATA REGISTER – OFFSET 63Ch (Global)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	GPIO[0] Input Data	RO	GPIO[0] Input Data Return 0 if GPIO[0] is configured as an output (offset 62Ch[1]=1) Return the state of GPIO[0] pin if GPIO[0] is configured as an input (offset 62Ch[1]=0)	No/Yes	1
1	GPIO[1] Input Data	RO	GPIO[1] Input Data Return 0 if GPIO[1] is configured as an output (offset 62Ch[3]=1) Return the state of GPIO[1] pin if GPIO[1] is configured as an input (offset 62Ch[3]=0)	No/Yes	1
2	GPIO[2] Input Data	RO	GPIO[2] Input Data Return 0 if GPIO[2] is configured as an output (offset 62Ch[5]=1) Return the state of GPIO[2] pin if GPIO[2] is configured as an input (offset 62Ch[5]=0)	No/Yes	0
3	GPIO[3] Input Data	RO	GPIO[3] Input Data Return 0 if GPIO[3] is configured as an output (offset 62Ch[7]=1) Return the state of GPIO[3] pin if GPIO[3] is configured as an input (offset 62Ch[7]=0)	No/Yes	1
4	GPIO[4] Input Data	RO	GPIO[4] Input Data Return 0 if GPIO[4] is configured as an output (offset 62Ch[9]=1) Return the state of GPIO[4] pin if GPIO[4] is configured as an input (offset 62Ch[9]=0)	No/Yes	0
5	GPIO[5] Input Data	RO	GPIO[5] Input Data Return 0 if GPIO[5] is configured as an output (offset 62Ch[11]=1) Return the state of GPIO[5] pin if GPIO[5] is configured as an input (offset 62Ch[11]=0)	No/Yes	1
6	GPIO[6] Input Data	RO	GPIO[6] Input Data Return 0 if GPIO[6] is configured as an output (offset 62Ch[13]=1) Return the state of GPIO[6] pin if GPIO[6] is configured as an input (offset 62Ch[13]=0)	No/Yes	0

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BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
7	GPIO[7] Input Data	RO	GPIO[7] Input Data Return 0 if GPIO[7] is configured as an output (offset 62Ch[15]=1) Return the state of GPIO[7] pin if GPIO[7] is configured as an input (offset 62Ch[15]=0)	No/Yes	1
8	GPIO[8] Input Data	RO	GPIO[8] Input Data Return 0 if GPIO[8] is configured as an output (offset 62Ch[17]=1) Return the state of GPIO[8] pin if GPIO[8] is configured as an input (offset 62Ch[17]=0)	No/Yes	0
9	GPIO[9] Input Data	RO	GPIO[9] Input Data Return 0 if GPIO[9] is configured as an output (offset 62Ch[19]=1) Return the state of GPIO[9] pin if GPIO[9] is configured as an input (offset 62Ch[19]=0)	No/Yes	1
10	GPIO[10] Input Data	RO	GPIO[10] Input Data Return 0 if GPIO[10] is configured as an output (offset 62Ch[21]=1) Return the state of GPIO[10] pin if GPIO[10] is configured as an input (offset 62Ch[21]=0)	No/Yes	0
11	GPIO[11] Input Data	RO	GPIO[11] Input Data Return 0 if GPIO[11] is configured as an output (offset 62Ch[23]=1) Return the state of GPIO[11] pin if GPIO[11] is configured as an input (offset 62Ch[23]=0)	No/Yes	1
12	GPIO[12] Input Data	RO	GPIO[12] Input Data Return 0 if GPIO[12] is configured as an output (offset 62Ch[25]=1) Return the state of GPIO[12] pin if GPIO[12] is configured as an input (offset 62Ch[25]=0)	No/Yes	0
13	GPIO[13] Input Data	RO	GPIO[13] Input Data Return 0 if GPIO[13] is configured as an output (offset 62Ch[27]=1) Return the state of GPIO[13] pin if GPIO[13] is configured as an input (offset 62Ch[27]=0)	No/Yes	1
14	GPIO[14] Input Data	RO	GPIO[14] Input Data Return 0 if GPIO[14] is configured as an output (offset 62Ch[29]=1) Return the state of GPIO[11] pin if GPIO[11] is configured as an input (offset 62Ch[29]=0)	No/Yes	0
15	GPIO[15] Input Data	RO	GPIO[15] Input Data Return 0 if GPIO[15] is configured as an output (offset 62Ch[31]=1) Return the state of GPIO[15] pin if GPIO[15] is configured as an input (offset 62Ch[31]=0)	No/Yes	1
31:16	Reserved	RsvdP	Not Support.	No	0000h

8.2.105 GPIO 16-31 INPUT DATA REGISTER – OFFSET 640h (Global)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	GPIO[16] Input Data	RO	GPIO[16] Input Data Return 0 if GPIO[16] is configured as an output (offset 630h[1]=1) Return the state of GPIO[16] pin if GPIO[16] is configured as an input (offset 630h[1]=0)	No/Yes	0
1	GPIO[17] Input Data	RO	GPIO[17] Input Data Return 0 if GPIO[17] is configured as an output (offset 630h[3]=1) Return the state of GPIO[17] pin if GPIO[17] is configured as an input (offset 630h[3]=0)	No/Yes	1
2	GPIO[18] Input Data	RO	GPIO[18] Input Data Return 0 if GPIO[18] is configured as an output (offset 630h[5]=1) Return the state of GPIO[18] pin if GPIO[18] is configured as an input (offset 630h[5]=0)	No/Yes	0

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BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
3	GPIO[19] Input Data	RO	GPIO[19] Input Data Return 0 if GPIO[19] is configured as an output (offset 630h[7]=1) Return the state of GPIO[19] pin if GPIO[19] is configured as an input (offset 630h[7]=0)	No/Yes	1
4	GPIO[20] Input Data	RO	GPIO[20] Input Data Return 0 if GPIO[20] is configured as an output (offset 630h[9]=1) Return the state of GPIO[20] pin if GPIO[20] is configured as an input (offset 630h[9]=0)	No/Yes	0
5	GPIO[21] Input Data	RO	GPIO[21] Input Data Return 0 if GPIO[21] is configured as an output (offset 630h[11]=1) Return the state of GPIO[21] pin if GPIO[21] is configured as an input (offset 630h[11]=0)	No/Yes	1
6	GPIO[22] Input Data	RO	GPIO[22] Input Data Return 0 if GPIO[22] is configured as an output (offset 630h[13]=1) Return the state of GPIO[22] pin if GPIO[22] is configured as an input (offset 630h[13]=0)	No/Yes	0
7	GPIO[23] Input Data	RO	GPIO[23] Input Data Return 0 if GPIO[23] is configured as an output (offset 630h[15]=1) Return the state of GPIO[23] pin if GPIO[23] is configured as an input (offset 630h[15]=0)	No/Yes	1
8	GPIO[24] Input Data	RO	GPIO[24] Input Data Return 0 if GPIO[24] is configured as an output (offset 630h[17]=1) Return the state of GPIO[24] pin if GPIO[24] is configured as an input (offset 630h[17]=0)	No/Yes	0
9	GPIO[25] Input Data	RO	GPIO[25] Input Data Return 0 if GPIO[25] is configured as an output (offset 630h[19]=1) Return the state of GPIO[25] pin if GPIO[25] is configured as an input (offset 630h[19]=0)	No/Yes	1
10	GPIO[26] Input Data	RO	GPIO[26] Input Data Return 0 if GPIO[26] is configured as an output (offset 630h[21]=1) Return the state of GPIO[26] pin if GPIO[26] is configured as an input (offset 630h[21]=0)	No/Yes	0
11	GPIO[27] Input Data	RO	GPIO[27] Input Data Return 0 if GPIO[27] is configured as an output (offset 630h[23]=1) Return the state of GPIO[27] pin if GPIO[27] is configured as an input (offset 630h[23]=0)	No/Yes	1
12	GPIO[28] Input Data	RO	GPIO[28] Input Data Return 0 if GPIO[28] is configured as an output (offset 630h[25]=1) Return the state of GPIO[28] pin if GPIO[28] is configured as an input (offset 630h[25]=0)	No/Yes	0
13	GPIO[29] Input Data	RO	GPIO[29] Input Data Return 0 if GPIO[29] is configured as an output (offset 630h[27]=1) Return the state of GPIO[29] pin if GPIO[29] is configured as an input (offset 630h[27]=0)	No/Yes	1
14	GPIO[30] Input Data	RO	GPIO[30] Input Data Return 0 if GPIO[30] is configured as an output (offset 630h[29]=1) Return the state of GPIO[30] pin if GPIO[30] is configured as an input (offset 630h[29]=0)	No/Yes	0
15	GPIO[31] Input Data	RO	GPIO[31] Input Data Return 0 if GPIO[31] is configured as an output (offset 630h[31]=1) Return the state of GPIO[31] pin if GPIO[31] is configured as an input (offset 630h[31]=0)	No/Yes	1
31:16	Reserved	RsvdP	Not Support.	No/Yes	0000h

8.2.106 GPIO 0-15 OUTPUT DATA REGISTER – OFFSET 644h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	GPIO[0] Output Data	RW	GPIO[0] Output Data The value written to this bit is driven to GPIO[0] output if GPIO[0] is configured as an output (offset 62Ch[1]=1)	No/Yes	0

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BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
1	GPIO[1] Output Data	RW	GPIO[1] Output Data The value written to this bit is driven to GPIO[1] output if GPIO[1] is configured as an output (offset 62Ch[3]=1)	No/Yes	0
2	GPIO[2] Output Data	RW	GPIO[2] Output Data The value written to this bit is driven to GPIO[2] output if GPIO[2] is configured as an output (offset 62Ch[5]=1)	No/Yes	0
3	GPIO[3] Output Data	RW	GPIO[3] Output Data The value written to this bit is driven to GPIO[3] output if GPIO[3] is configured as an output (offset 62Ch[7]=1)	No/Yes	0
4	GPIO[4] Output Data	RW	GPIO[4] Output Data The value written to this bit is driven to GPIO[4] output if GPIO[4] is configured as an output (offset 62Ch[9]=1)	No/Yes	0
5	GPIO[5] Output Data	RW	GPIO[5] Output Data The value written to this bit is driven to GPIO[5] output if GPIO[5] is configured as an output (offset 62Ch[11]=1)	No/Yes	0
6	GPIO[6] Output Data	RW	GPIO[6] Output Data The value written to this bit is driven to GPIO[6] output if GPIO[6] is configured as an output (offset 62Ch[13]=1)	No/Yes	0
7	GPIO[7] Output Data	RW	GPIO[7] Output Data The value written to this bit is driven to GPIO[7] output if GPIO[7] is configured as an output (offset 62Ch[15]=1)	No/Yes	0
8	GPIO[8] Output Data	RW	GPIO[8] Output Data The value written to this bit is driven to GPIO[8] output if GPIO[8] is configured as an output (offset 62Ch[17]=1)	No/Yes	0
9	GPIO[9] Output Data	RW	GPIO[9] Output Data The value written to this bit is driven to GPIO[9] output if GPIO[9] is configured as an output (offset 62Ch[19]=1)	No/Yes	0
10	GPIO[10] Output Data	RW	GPIO[10] Output Data The value written to this bit is driven to GPIO[10] output if GPIO[10] is configured as an output (offset 62C[21]=1)	No/Yes	0
11	GPIO[11] Output Data	RW	GPIO[11] Output Data The value written to this bit is driven to GPIO[11] output if GPIO[11] is configured as an output (offset 62Ch[23]=1)	No/Yes	0
12	GPIO[12] Output Data	RW	GPIO[12] Output Data The value written to this bit is driven to GPIO[12] output if GPIO[12] is configured as an output (offset 62Ch[25]=1)	No/Yes	0
13	GPIO[13] Output Data	RW	GPIO[13] Output Data The value written to this bit is driven to GPIO[13] output if GPIO[13] is configured as an output (offset 62Ch[27]=1)	No/Yes	0
14	GPIO[14] Output Data	RW	GPIO[14] Output Data The value written to this bit is driven to GPIO[14] output if GPIO[14] is configured as an output (offset 62Ch[29]=1)	No/Yes	0
15	GPIO[15] Output Data	RW	GPIO[15] Output Data The value written to this bit is driven to GPIO[15] output if GPIO[15] is configured as an output (offset 62Ch[31]=1)	No/Yes	0
31:16	Reserved	RsvdP	Not Support.	No	0000h

8.2.107 GPIO 16-31 OUTPUT DATA REGISTER – OFFSET 648h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	GPIO[16] Output Data	RW	GPIO[16] Output Data The value written to this bit is driven to GPIO[16] output if GPIO[16] is configured as an output (offset 630h[1]=1)	No/Yes	0
1	GPIO[17] Output Data	RW	GPIO[17] Output Data The value written to this bit is driven to GPIO[17] output if GPIO[17] is configured as an output (offset 630h[3]=1)	No/Yes	0
2	GPIO[18] Output Data	RW	GPIO[18] Output Data The value written to this bit is driven to GPIO[18] output if GPIO[18] is configured as an output (offset 630h[5]=1)	No/Yes	0

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BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
3	GPIO[19] Output Data	RW	GPIO[19] Output Data The value written to this bit is driven to GPIO[19] output if GPIO[19] is configured as an output (offset 630h[7]=1)	No/Yes	0
4	GPIO[20] Output Data	RW	GPIO[20] Output Data The value written to this bit is driven to GPIO[20] output if GPIO[20] is configured as an output (offset 630h[9]=1)	No/Yes	0
5	GPIO[21] Output Data	RW	GPIO[21] Output Data The value written to this bit is driven to GPIO[21] output if GPIO[21] is configured as an output (offset 630h[11]=1)	No/Yes	0
6	GPIO[22] Output Data	RW	GPIO[22] Output Data The value written to this bit is driven to GPIO[22] output if GPIO[22] is configured as an output (offset 630h[13]=1)	No/Yes	0
7	GPIO[23] Output Data	RW	GPIO[23] Output Data The value written to this bit is driven to GPIO[23] output if GPIO[23] is configured as an output (offset 630h[15]=1)	No/Yes	0
8	GPIO[24] Output Data	RW	GPIO[24] Output Data The value written to this bit is driven to GPIO[24] output if GPIO[24] is configured as an output (offset 630h[17]=1)	No/Yes	0
9	GPIO[25] Output Data	RW	GPIO[25] Output Data The value written to this bit is driven to GPIO[25] output if GPIO[25] is configured as an output (offset 630h[19]=1)	No/Yes	0
10	GPIO[26] Output Data	RW	GPIO[26] Output Data The value written to this bit is driven to GPIO[26] output if GPIO[26] is configured as an output (offset 630h[21]=1)	No/Yes	0
11	GPIO[27] Output Data	RW	GPIO[27] Output Data The value written to this bit is driven to GPIO[27] output if GPIO[27] is configured as an output (offset 630h[23]=1)	No/Yes	0
12	GPIO[28] Output Data	RW	GPIO[28] Output Data The value written to this bit is driven to GPIO[28] output if GPIO[28] is configured as an output (offset 630h[25]=1)	No/Yes	0
13	GPIO[29] Output Data	RW	GPIO[29] Output Data The value written to this bit is driven to GPIO[29] output if GPIO[29] is configured as an output (offset 630h[27]=1)	No/Yes	0
14	GPIO[30] Output Data	RW	GPIO[30] Output Data The value written to this bit is driven to GPIO[30] output if GPIO[30] is configured as an output (offset 630h[29]=1)	No/Yes	0
15	GPIO[31] Output Data	RW	GPIO[31] Output Data The value written to this bit is driven to GPIO[31] output if GPIO[31] is configured as an output (offset 630h[31]=1)	No/Yes	0
31:16	Reserved	RsvdP	Not Support.	No	0000h

8.2.108 GPIO 0-31 INTERRUPT POLARITY REGISTER – OFFSET 64Ch (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:0	GPIO Interrupt Polarity	RW	Controls whether GPIO Interrupt input is Active-Low or Active-High for the corresponding GPIOx signal. Bit[31:0] correspond to GPIO[31:0] respectively. 0b: GPIO Interrupt input is Active-Low 1b: GPIO Interrupt input is Active-High	No/Yes	0000_0000h

8.2.109 GPIO 0-31 INTERRUPT STATUS REGISTER – OFFSET 650h (Global)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:0	GPIO Interrupt Status	RO	Indicates whether GPIO interrupt are inactive or active for the corresponding GPIOx signal. Bit[31:0] correspond to GPIO[31:0]	No	5555_5554h

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			respectively. 0b: GPIO interrupt is inactive 1b: GPIO interrupt is active		

8.2.110 GPIO 0-31 INTERRUPT MASK REGISTER – OFFSET 654h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:0	GPIO Interrupt Mask	RW	Indicates whether GPIO interrupts are masked or not masked for the corresponding GPIOx signal. Bit[31:0] correspond to GPIO[31:0] respectively. 0b: GPIO interrupt is unmasked 1b: GPIO interrupt is masked	No/Yes	0000_0000h

8.2.111 XPIP_CSR 0 REGISTER – OFFSET 844h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:0	XPIP_CSR0	RW	XPIP_CSR 0 value. Bit[2]: Cross_Link_En	Yes	0400_1060h

8.2.112 XPIP_CSR 1 REGISTER – OFFSET 848h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:0	XPIP_CSR1	RW	XPIP_CSR 1 value.	Yes	0400_0800h

8.2.113 DECODE VGA REGISTER – OFFSET 84Ch

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
30:0	Reserved	RsvdP	Not Support.	No	0-0h
31	Decode VGA Enable	RO	0b: Disable VGA decode 1b: Enable VGA decode	Yes	1

8.2.114 SWITCH OPERATION MODE REGISTER – OFFSET 850h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	Store-Forward	RW	When set, a store-forward mode is used. Otherwise, the chip is working under cut-through mode.	Yes	0

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BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
2:1	Cut-through Threshold	RW	Cut-through Threshold. When forwarding a packet from low-speed port to high-speed mode, the chip provides the capability to adjust the forwarding threshold. 00b: the threshold is set at the middle of forwarding packet 01b: the threshold is set ahead 1-cycle of middle point 10b: the threshold is set ahead 2-cycle of middle point. 11b: the threshold is set ahead 3-cycle of middle point.	Yes	01b
3	Port Arbitration Mode	RW	When set, the round-robin arbitration will stay in the arbitrated port even if the credit is not enough but request is pending. When clear, the round-robin arbitration will always go to the requesting port, which the outgoing credit is enough for the packet queued in the port.	Yes	0
4	Credit Update Mode	RW	When set, the frequency of releasing new credit to the link partner will be one credit per update. When clear, the frequency of releasing new credit to the link partner will be two credits per update.	Yes	0
5	Ordering on Different Egress Port Mode	RW	When set, there has ordering rule on packets for different egress port.	Yes	0
6	Ordering on Different Tag of Completion Mode	RW	When set, there has ordering rule between completion packet with different tag.	Yes	1
7	NonPost TLP Store-Forward	RW	When set, for Non-port TLP store-forward mode is used. Otherwise, Non-post TLP is working under cut-through mode. When write '1', this bit is changed to '0'. When write '0', this bit is changed to '1'.	Yes	1
31:8	Reserved	RsvdP	Not Support.	No	0000_00h

8.2.115 XPIP_CSR 2 REGISTER – OFFSET 854h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
7:0	FTS Number	RW	Indicates FTS number.	Yes	80h
9:8	Scrambler Control	RW	Reset to 00b.	Yes	00b
10	L0s	RW	Reset to 0b.	Yes	0
11	Compliance to Detect	RW	Reset to 0b.	Yes	0
13:12	Change_Speed_Sel	RW	Reset to 00b.	Yes	00b
14	Change_Speed_En	RW	Reset to 0b.	Yes	0
15	Reserved	RsvdP	Not Support.	No	0

8.2.116 PHY PARAMETER 1 REGISTER – OFFSET 854h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
20:16	C_EMP_POST_GEN1_3P5_NOM (Golbal)	RW	Set the de-emphasis level for GEN1, -3.5db. Please refer to Section 6.1.7 for more detail information.	Yes	1_0101b
25:21	C_EMP_POST_GEN2_3P5_NOM (Global)	RW	Set the de-emphasis level for GEN2, -3.5db. Please refer to Section 6.1.7 for more detail information.	Yes	10_101b
30:26	C_EMP_POST_GEN2_6P0_NOM (Global)	RW	Set the de-emphasis level for GEN2, -6.0db. Please refer to Section 6.1.7 for more detail information.	Yes	111_01b
31	Reserved	RO	Not Support.	No	0

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8.2.117 PHY PARAMETER 2 REGISTER – OFFSET 858h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
3:0	C_TX_PHY_ LATENACY (Global)	RW	Set the transmitter electrical idle latency. Please refer to Section 6.1.8 for more detail information. It is set by Upstream Port Only.	Yes	7h
6:4	C_REC_DETEC_ USEC (Global)	RW	Set the receiver detection threshold. Please refer to Section 6.1.1 for more detail information. It is set by Upstream Port Only.	Yes	010b
7	Reserved	RsvdP	Not Support.	No	0
8	P_CDR_FREQLOO P_EN	RW	Reset to 0b.	Yes	1
10:9	P_CDR_ THRESHOLD	RW	Reset to 01b.	Yes	10b
12:11	P_CDR_FREQLOO P_GAIN	RW	Reset to 01b.	Yes	11b
15:13	Reserved	RsvdP	Not Support.	No	000b
16	P_DRV_LVL_MGN _DELATA_EN	RW	Reset to 0b.	Yes	0
17	P_DRV_LVL_NOM _DELATA_EN	RW	Reset to 0b.	Yes	0
18	P_EMP_POST_MG N_DELATA_EN	RW	Reset to 0b.	Yes	0
19	P_EMP_POST_NO M_DELATA_EN	RW	Reset to 0b.	Yes	0
21:20	P_RX_SIGDET_ LVL	RW	Set the receiver signal detection threshold. Please refer to Section 6.1.2 for more detail information.	Yes	01b
25:22	P_RX_EQ_1	RW	Set the receiver equalization for GEN1 link. Please refer to Section 6.1.3 for more detail information.	Yes	0h
29:26	P_RX_EQ_2	RW	Set the receiver equalization for GEN2 link. Please refer to Section 6.1.3 for more detail information.	Yes	0h
30	P_TXSWING	RW	Set the transmitter swing. Please refer to Section 6.1.4 for more detail information. 0b: full voltage swing with de-emphasis 1b: half voltage swing without de-emphasis	Yes	0
31	Reserved	RsvdP	Not Support.	No	0

8.2.118 PHY PARAMETER 3 REGISTER – OFFSET 85Ch

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
6:0	PHY Parameter 3 (Per Port)	RW	PHY's Lane mode.	Yes	00h
14:7	Reserved	RsvdP	Not Support.	No	00h
31:15	PHY Parameter 3 (Global)	RW	PHY's delta value setting. It is set by Upstream Port Only.	Yes	0001h

8.2.119 PHY PARAMETER 4 REGISTER - OFFSET 860h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
14:0	PHY TX Margin Parameter (Global)	RW	PHY Tx margin parameter.	Yes	116Bh
31:15	Reserved	RsvdP	Not Support.	No	0-0h

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8.2.120 XPIP_CSR 3 REGISTER – OFFSET 864h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:0	XPIP_CSR3	RW	XPIP_CSR3 value.	Yes	000F_0000h

8.2.121 XPIP_CSR 4 REGISTER – OFFSET 868h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:0	XPIP_CSR4 (Global)	RW	XPIP_CSR 4 value.	Yes	0000_0000h

8.2.122 XPIP_CSR 5 REGISTER – OFFSET 86Ch

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
29:0	XPIP_CSR5[29:0]	RW	Bit[10]: Default ACK Latency Timer Enable 0b: disable default ack latency timer 1b: enable default ack latency timer	Yes	3308_0008h
30	DO_CHG_DATA_ RATE_CTRL	RW	DO_CHG_DATA_RATE_CTRL.	Yes	1 for Up 0 for Down
31	Gen1_Cap_Only	RW	0b: report GEN2 capability 1b: report GEN1 capability	Yes	0

8.2.123 NON TRANSFER MODE REGISTER – OFFSET 870h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	TX_SOF_FORM	RO	Test used only.	Yes	0
1	PM Data Select Register R/W Enable	RO	Test used only.	Yes	0
2	ARB_Abort_Sel	RO	Test used only.	Yes	1
3	4K Boundary Check Enable	RO	Test used only.	Yes	0
4	FIFOERR_FIX_SEL	RO	Test used only.	No	1
5	ORDER RULE5 Enable	RW	Test used only.	Yes	0
6	Ordering Frozen Disable for Post Pkt	RW	Test used only.	Yes	0
7	Ordering Frozen Disable for NP Pkt	RW	Test used only.	Yes	0
11:8	Reserved	RsvdP	Not Support.	No	0h
12	ARB_VCFLG_SEL	RO	Test used only.	Yes	1
13	Reserved	RsvdP	Not Support.	No	0
14	Non-Trans_Mode	HwInt RO	Indicates the status of strapping pin NT_EN_L.	Yes	0
15	GNT_FAIL2IDLE	RO	Test used only.	Yes	1
31:16	Reserved	RsvdP	Not Support.	No	0000h

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8.2.124 OPERATION MODE REGISTER – OFFSET 874h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
15:0	Operation Mode	HwInt RO	Bit[0]: Memory Bist Bit[1]: IDDRB Bit[2]: FAST_MODE Bit[3]: DEBUG_MODE Bit[4]: PHY_MODE Bit[5]: Reserved Bit[6]: PORT_CFG[0] Bit[7]: Reserved Bit[8]: PORT_CFG[1] Bit[9]: PLCSEL Bit[10]: SCAN_MODE Bit[15:11]: Reserved	No	0022h for 912 mode 0062h for 612 mode 0122h for 512 mode
23:16	Reserved	RsvdP	Not Support.	No	00h
27:24	L1PM Option	RW	Set L1PM option.	Yes	0h
31:28	Reserved	RsvdP	Not Support.	No	0h

8.2.125 DEVICE SPECIFIC POWER MANAGEMENT EVENT– OFFSET 878h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	Device Specific PME Capability	RO	0b: disable device specific PME. 1b: enable device specific PME.	Yes	0
1	PME Turnoff Message Request	RW	Request to send PME turnoff message.	No/Yes	0
2	Port Power	RW	Control GPIO[4:0] pins when Device Specific PME Capability is enabled. Downstream port 1 controls GPIO[0], Downstream port 2 controls GPIO[1], … and so on. It is valid when Device Specific PME Capability is enabled.	No/Yes	1
3	Port Reset	RW	This bit when reset asserts an active low reset signal to the attached device. When set, the reset signal is de-asserted. It is valid when Device Specific PME Capability is enabled.	No/Yes	1
15:4	Reserved	RsvdP	Not Support.	No	000h
17:16	Link Status	RO	These two bits represent the link status of device connected to the downstream port. 00b: L0 01b: L0s 10b: L1 11b: L2/L3	No	00b
31:18	Reserved	RsvdP	Not Support.	No	0-0h

8.2.126 EEPROM CONTROL REGISTER – OFFSET 87Ch (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	EEPROM Start	RW	Starts the EEPROM read or write cycle. 1b: start read or write cycle	No/Yes	0
3:1	Reserved	RsvdP	Not Support.	No	000b
4	EEPROM Autoload Status	RO	0b: EEPROM autoload was unsuccessfully or is disabled 1b: EEPROM autoload occurred successfully after PERST_L.	No	0
5	EEPROM is Audoload Disabled	RW	0b: EEPROM autoload is enabled 1b: EEPROM autoload is disabled	No/Yes	0

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BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
7:6	EEPROM Clock Rate	RW	Determines the frequency of the EEPROM clock which is derived from the primary clock. 01b: PEXCLK/4 (PEXCLK is 250 MHz) Others: Reserved	No/Yes	01b
15:8	EEPROM Status	RO	Indicate the eeprom status.	No	00h
23:16	EEPROM Command	RW	01h: write STATUS register 02h: EEPROM write 03h: EEPROM read 04h: disable write operation 05h: read STATUS register 06h: enable write operation C7h: erase entire EEPROM	No/Yes	00h
30:24	Reserved	RsvdP	Not Support.	No	00h
31	Size 64K Mode	RW	0b: EEPROM size is less or equal to 64K 1b: EEPROM size is larger 64K	No/Yes	0

8.2.127 EEPROM ADDRESS AND DATA REGISTER – OFFSET 880h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
15:0	EEPROM Address	RW	Contains the EEPROM address.	No/Yes	0000h
31:16	EEPROM Data	RW	Contains the EEPROM data.	No/Yes	0000h

8.2.128 DEBUGOUT CONTROL REGISTER – OFFSET 884h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
4:0	Debug Mode Select	RW	Debug mode select.	No/Yes	0_0000b
7:5	Debug Port_Select_S1	RW	Debug port select s1.	No/Yes	000b
8	DebugPort_ Select_S2	RW	Debugport select s2.	No/Yes	0
9	Debug Output Start	RW	Start to select debug output data.	No/Yes	0
31:10	Reserved	RsvdP	Not Support.	No	0-0h

8.2.129 DEBUGOUT DATA REGISTER – OFFSET 888h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:0	Debug Output Data	RO	Contains the debug output data.	No	0000_0000h

8.2.130 LTSSM_CSR REGISTER – OFFSET 88Ch (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
7:0	LTSSM_CSR	RW	Bit[2]: Pseudo MRL_PDC_En 0b: disable pseudo MRL_PDC function 1b: enable pseudo MRL_PDC function	Yes	00h
31:8	Reserved	RsvdP	Not Support.	No	0000_00h

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8.2.131 MAC_CSR REGISTER – OFFSET 890h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
15:0	Reserved	RsvdP	Not Support.	No	0000h
31:16	MAC_CSR	RW	MAC CSR value.	Yes	0004h

8.2.132 POWER SAVING DISABLE REGISTER – OFFSET 8A4h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	Power Saving Disable	RW	Disable power saving. 0b: enable power saving 1b: disable power saving	Yes	0
31:1	Reserved	RsvdP	Not Support.	No	0-0h

8.2.133 TRANSACTION LAYER CSR REGISTER – OFFSET 8A8h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	Egress_Reqcredit_ Starve	RW	Test used only.	Yes	1
1	MF_Credit_Update_ Dis	RW	Test used only.	Yes	0
2	MC_Cap_Dis	RW	Test used only.	Yes	0
3	MEM_Sharing_Dis	RO	Test used only.	Yes	0
31:4	Reserved	RsvdP	Not Support.	No	0-0h

8.2.134 REPLAY TIME-OUT COUNTER REGISTER – OFFSET 8ACh

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
11:0	User Replay Timer	RW	A 12-bit register contains a user-defined value.	Yes	000h
12	Enable User Replay Timer	RW	When asserted, the user-defined replay time-out value is be employed. 0b: use the default replay time-out value 1b: use the user-defined replay time-out value on bit[11:0]	Yes	0
15:13	Reserved	RsvdP	Not Support.	No	000b

8.2.135 ACKNOWLEDGE LATENCY TIMER REGISTER – OFFSET 8ACh

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
29:16	User ACK Latency Timer	RW	A 14-bit register contains a user-defined value.	Yes	0-0h
30	Enable User ACK Latency	RW	When asserted, the user-defined ACK latency value is be employed. 0b: use the default ack latency value 1b: use the user-defined ack latency value on bit[29:16]	Yes	0
31	Reserved	RsvdP	Not Support.	No	0

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8.2.136 PORT MISC 0 REGISTER – OFFSET 8B0h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
7:0	Reserved	RsvdP	Not Support.	No	00h
13:8	Power Management Control Parameter	RW	Power Management Control parameter.	Yes	00_0001b
14	RX Polarity Inversion Disable	RW	0b: enable rx polarity inversion circuit 1b: disable rx polarity inversion circuit	Yes	0
15	Compliance Pattern Parity Control Disable	RW	0b: enable compliance pattern parity control 1b: disable compliance pattern parity control It is set by Upstream Port Only.	Yes	0

8.2.137 PHY PARAMETER 0 REGISTER – OFFSET 8B0h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
20:16	C_DRV_LVL_3P5_ NOM (Global)	RW	Set drive amplitude level. Please refer to Section 6.1.6 for more detail information.	Yes	1_0011b
25:21	C_DRV_LVL_6P0_ NOM (Global)	RW	Set drive amplitude level. Please refer to Section 6.1.6 for more detail information.	Yes	10_011b
30:26	C_DRV_LVL_HAL F_NOM (Global)	RW	Set drive amplitude level. Please refer to Section 6.1.6 for more detail information.	Yes	000_10b
31	Reserved	RsvdP	Not Support.	No	0

8.2.138 PORT MISC 1 REGISTER – OFFSET 8B4h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
7:0	Reserved	RsvdP	Not Support.	No	00h
9:8	DO_CHG_DATA_C NT_SEL	RW	The trying number for doing change data rate.	Yes	00b
10	Port Disable	RW	Disable this port. 0b: enable port 1b: disable port	Yes	0
11	Reset Select	RW	Reset select. It is valid for upstream port only.	Yes	1
15:12	Reserved	RsvdP	Not Support.	No	000b

8.2.139 XPIP_CSR 6 REGISTER – OFFSET 8B4h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
23:16	XPIP_CSR6	RW	XPIP_CSR 6 value.	Yes	78h

8.2.140 XPIP_CSR 7 REGISTER – OFFSET 8B4h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
25:24	REV_TS_CTR	RW	Test used only.	Yes	00
29:26	MAC Control Parameter	RW	Test used only.	Yes	0h
30	Line_Loopback	RW	Test used only.	Yes	0

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BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31	P35_GEN2_MODE (Global)	RW	Test used only.	Yes	0

8.2.141 PORT MISC 2 REGISTER – OFFSET 8B8h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	Change_Role_En	RW	Test used only.	Yes	0
1	IPCore_Role	RW	Test used only.	Yes	0
31:2	Reserved	RsvdP	Not Support.	No	0-0h

8.2.142 LED DISPLAY CSR REGISTER – OFFSET 8BCh (Global)

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
5:0	LED Display Mode Select	RW	Test used only.	Yes	00_0000b
7:6	Reserved	RsvdP	Not Support.	No	00b
13:8	Hotplug_Misc	RW	Bit[11:8] are used to control reset pulse for HotPlug function. Bit[8]: enable Bit[9]: issue reset pulse three times Bit[11:10]: control the width of the reset pulse 00b: 128 ms 01b: 256 ms 10b: 1 sec 11b: 2 sec Bit[12]: Reserved Bit[13]: enable the synchronize between IOE Interrupt and Hot-Plug state machine	Yes	0h
31:14	Reserved	RsvdP	Not Support.	No	0-0h

8.2.143 MULTI-CAST ENHANCED CAPABILITY HEADER REGISTER – OFFSET 900h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
15:0	Extended Capabilities ID	RO	Read as 0012h to indicate that these are PCI express extended capability registers for multi-cast capability.	No	0012h
19:16	Capability Version	RO	Read as 1h.	No	1h
31:20	Next Capability Offset	RO	Pointer points to 000h.	Yes	000h

8.2.144 MULTI-CAST CAPABILITY REGISTER – OFFSET 904h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
5:0	MC_Max_Group	RO	Value indicates the max. number of Multicast Groups that the component supports.	No	00_0001b
14:6	Reserved	RO	Not Support.	No	0
15	MC_ECRC_ Regeneration_ Supported	RO	If set, indicates that ECRC regeneration is supported.	No	0

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8.2.145 MULTI-CAST CONTROL REGISTER – OFFSET 904h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
16	MC_Num_Group	RW	Value indicates the number of Multicast Groups configured for use.	No/Yes	00h
30:17	Reserved	RsvdP	Not Support.	No	0-0h
31	MC_ECRC_ Regeneration_ Supported	RW	When set, the Multicast mechanism is enabled for the component.	No/Yes	0

8.2.146 MULTI-CAST BASE ADDRESS 0 REGISTER – OFFSET 908h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
5:0	MC_Index_Position	RW	The location of the LSB of the Multicast Group number within the address.	No/Yes	00h
11:6	Reserved	RsvdP	Not Support.	No	00h
31:12	MC_Base_Address [31:12]	RW	The base address of the Multicast address range.	No/Yes	0-0h

8.2.147 MULTI-CAST BASE ADDRESS 1 REGISTER – OFFSET 90Ch

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:0	MC_Base_Address [63:32]	RW	The base address of the Multicast address range.	No/Yes	0000-0000h

8.2.148 MULTI-CAST RECEIVER REGISTER – OFFSET 910h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
1:0	MC_Receive	RW	For each bit that's Set, this Function gets a copy of any Multicast TLPs for the associated Multicast Group.	No/Yes	00
31:2	Reserved	RsvdP	Not Support.	No	0-0h

8.2.149 MULTI-CAST BLOCK ALL REGISTER – OFFSET 918h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
1:0	MC_Block_All	RW	For each bit that is Set, this Function is blocked from sending TLPs to the associated Multicast Group.	No/Yes	00
31:2	Reserved	RsvdP	Not Support.	No	0-0h

8.2.150 MULTI-CAST BLOCK UNTRANSLATED REGISTER – OFFSET 920h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
1:0	MC_Block_ Untranslated	RW	For each bit that is Set, this Function is blocked from sending TLPs containing Untranslated Addresses to the associated MCG.	No/Yes	00
31:2	Reserved	RsvdP	Not Support.	No	0-0h

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8.2.151 EEPROM_SCRATCHPAD REGISTER - OFFSET FB0h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:0	EEPROM_ Scratchpad	RO	Test used only.	Yes	0000_0000h

8.2.152 PCI EXPRESS ADVANCED ERROR REPORTING ENHANCED CAPABILITY HEADER REGISTER – OFFSET FB4h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
15:0	Extended Capabilities ID	RO	Read as 0001h to indicate that these are PCI express extended capability registers for advance error reporting.	No	0001h
19:16	Capability Version	RO	Read as 1h.	No	1h
31:20	Next Capability Offset	RO	Pointer points to the Power Budgeting Extended Capability structure for upstream port / the Port VC Extended Capability structure for downstream ports.	Yes	138h for Up 148h for Down

8.2.153 UNCORRECTABLE ERROR STATUS REGISTER – OFFSET FB8h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	Training Error Status	RW1C	When set, indicates that the Training Error event has occurred.	No/Yes	0
3:1	Reserved	RsvdP	Not Support.	No	000
4	Data Link Protocol Error Status	RW1C	When set, indicates that the Data Link Protocol Error event has occurred.	No/Yes	0
11:5	Reserved	RsvdP	Not Support.	No	0-0b
12	Poisoned TLP Status	RW1C	When set, indicates that a Poisoned TLP has been received or generated.	No/Yes	0
13	Flow Control Protocol Error Status	RW1C	When set, indicates that the Flow Control Protocol Error event has occurred.	No/Yes	0
14	Completion Timeout Status	RW1C	When set, indicates that the Completion Timeout event has occurred.	No/Yes	0
15	Completer Abort Status	RW1C	When set, indicates that the Completer Abort event has occurred.	No/Yes	0
16	Unexpected Completion Status	RW1C	When set, indicates that the Unexpected Completion event has occurred.	No/Yes	0
17	Receiver Overflow Status	RW1C	When set, indicates that the Receiver Overflow event has occurred.	No/Yes	0
18	Malformed TLP Status	RW1C	When set, indicates that a Malformed TLP has been received.	No/Yes	0
19	ECRC Error Status	RW1C	When set, indicates that an ECRC Error has been detected.	No/Yes	0
20	Unsupported Request Error Status	RW1C	When set, indicates that an Unsupported Request event has occurred.	No/Yes	0
21	ACS Violation Status	RW1C	When set, indicates that an ACS Violation event has occurred.	No/Yes	0
22	Reserved	RsvdP	Not Support.	No	0
23	MC Blocked TLP Status	RW1C	When set, indicates that an MC Blocked TLP event has occurred.	No/Yes	0
31:24	Reserved	RsvdP	Not Support.	No	00h

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8.2.154 UNCORRECTABLE ERROR MASK REGISTER – OFFSET FBCh

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	Training Error Mask	RW	When set, the Training Error event is not logged in the Header Log register and not issued as an Error Message to RC either.	No/Yes	0
3:1	Reserved	RsvdP	Not Support.	No	000b
4	Data Link Protocol Error Mask	RW	When set, the Data Link Protocol Error event is not logged in the Header Log register and not issued as an Error Message to RC either.	No/Yes	0
11:5	Reserved	RsvdP	Not Support.	No	0-0b
12	Poisoned TLP Mask	RW	When set, an event of Poisoned TLP is not logged in the Header Log register and not issued as an Error Message to RC either.	No/Yes	0
13	Flow Control Protocol Error Mask	RW	When set, the Flow Control Protocol Error event is not logged in the Header Log register and not issued as an Error Message to RC either.	No/Yes	0
14	Completion Timeout Mask	RW	When set, the Completion Timeout event is not logged in the Header Log register and not issued as an Error Message to RC either.	No/Yes	0
15	Completer Abort Mask	RW	When set, the Completer Abort event is not logged in the Header Log register and not issued as an Error Message to RC either.	No/Yes	0
16	Unexpected Completion Mask	RW	When set, the Unexpected Completion event is not logged in the Header Log register and not issued as an Error Message to RC either.	No/Yes	0
17	Receiver Overflow Mask	RW	When set, the Receiver Overflow event is not logged in the Header Log register and not issued as an Error Message to RC either.	No/Yes	0
18	Malformed TLP Mask	RW	When set, an event of Malformed TLP is not logged in the Header Log register and not issued as an Error Message to RC either.	No/Yes	0
19	ECRC Error Mask	RW	When set, an event of ECRC Error is not logged in the Header Log register and not issued as an Error Message to RC either.	No/Yes	0
20	Unsupported Request Error Mask	RW	When set, the Unsupported Request event is not logged in the Header Log register and not issued as an Error Message to RC either.	No/Yes	0
21	ACS Violation Mask	RW	When set, the ACS Violation event is not logged in the Header Log register and not issued as an Error Message to RC either.	No/Yes	0
22	Reserved	RsvdP	Not Support.	No	0
23	MC Blocked TLP Mask	RW	When set, the MC Blocked TLP event is not logged in the Header Log register and not issued as an Error Message to RC either.	No/Yes	0
31:24	Reserved	RsvdP	Not Support.	No	00h

8.2.155 UNCORRECTABLE ERROR SEVERITY REGISTER – OFFSET FC0h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	Training Error Severity	RW	0b: Non-Fatal 1b: Fatal	No/Yes	1
3:1	Reserved	RsvdP	Not Support.	No	000b
4	Data Link Protocol Error Severity	RW	0b: Non-Fatal 1b: Fatal	No/Yes	1
11:5	Reserved	RsvdP	Not Support.	No	0-0b
12	Poisoned TLP Severity	RW	0b: Non-Fatal 1b: Fatal	No/Yes	0
13	Flow Control Protocol Error Severity	RW	0b: Non-Fatal 1b: Fatal	No/Yes	1
14	Completion Timeout Error Severity	RW	0b: Non-Fatal 1b: Fatal	No/Yes	0
15	Completer Abort Severity	RW	0b: Non-Fatal 1b: Fatal	No/Yes	0
16	Unexpected Completion Severity	RW	0b: Non-Fatal 1b: Fatal	No/Yes	0

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BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
17	Receiver Overflow Severity	RW	0b: Non-Fatal 1b: Fatal	No/Yes	1
18	Malformed TLP Severity	RW	0b: Non-Fatal 1b: Fatal	No/Yes	1
19	ECRC Error Severity	RW	0b: Non-Fatal 1b: Fatal	No/Yes	0
20	Unsupported Request Error Severity	RW	0b: Non-Fatal 1b: Fatal	No/Yes	0
21	ACS Violation Severity	RW	0b: Non-Fatal 1b: Fatal	No/Yes	0
22	Reserved	RsvdP	Not Support.	No	0
23	MC Blocked TLP Severity	RW	0b: Not-Fatal 1b: Fatal	No/Yes	0
31:24	Reserved	RsvdP	Not Support.	No	00h

8.2.156 CORRECTABLE ERROR STATUS REGISTER – OFFSET FC4h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	Receiver Error Status	RW1C	When set, the Receiver Error event is detected.	No/Yes	0
5:1	Reserved	RsvdP	Not Support.	No	0_000b
6	Bad TLP Status	RW1C	When set, the event of Bad TLP has been received is detected.	No/Yes	0
7	Bad DLLP Status	RW1C	When set, the event of Bad DLLP has been received is detected.	No/Yes	0
8	REPLAY_NUM Rollover status	RW1C	When set, the REPLAY_NUM Rollover event is detected.	No/Yes	0
11:9	Reserved	RsvdP	Not Support.	No	000b
12	Replay Timer Timeout status	RW1C	When set, the Replay Timer Timeout event is detected.	No/Yes	0
13	Advisory Non-Fatal Error status	RW1C	When set, the Advisory Non-Fatal Error event is detected.	No/Yes	0
31:14	Reserved	RsvdP	Not Support.	No	0-0h

8.2.157 CORRECTABLE ERROR MASK REGISTER – OFFSET FC8h

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
0	Receiver Error Mask	RW	When set, the Receiver Error event is not logged in the Header Log register and not issued as an Error Message to RC either.	No/Yes	0
5:1	Reserved	RsvdP	Not Support.	No	0_000b
6	Bad TLP Mask	RW	When set, the event of Bad TLP has been received is not logged in the Header Log register and not issued as an Error Message to RC either.	No/Yes	0
7	Bad DLLP Mask	RW	When set, the event of Bad DLLP has been received is not logged in the Header Log register and not issued as an Error Message to RC either.	No/Yes	0
8	REPLAY_NUM Rollover Mask	RW	When set, the REPLAY_NUM Rollover event is not logged in the Header Log register and not issued as an Error Message to RC either.	No/Yes	0
11:9	Reserved	RsvdP	Not Support.	No	000b
12	Replay Timer Timeout Mask	RW	When set, the Replay Timer Timeout event is not logged in the Header Log register and not issued as an Error Message to RC either.	No/Yes	0
13	Advisory Non-Fatal Error Mask	RW	When set, the Advisory Non-Fatal Error event is not logged in the Header Long register and not issued as an Error Message to RC either.	No/Yes	1
31:14	Reserved	RsvdP	Not Support.	No	0-0h

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8.2.158 ADVANCE ERROR CAPABILITIES AND CONTROL REGISTER – OFFSET FCCh

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
4:0	First Error Pointer	RO	It indicates the bit position of the first error reported in the Uncorrectable Error Status register.	No	0_0000b
5	ECRC Generation Capable	RO	When set, it indicates the Switch has the capability to generate ECRC.	No	1
6	ECRC Generation Enable	RW	When set, it enables the generation of ECRC when needed.	No/Yes	0
7	ECRC Check Capable	RO	When set, it indicates the Switch has the capability to check ECRC.	No	1
8	ECRC Check Enable	RW	When set, the function of checking ECRC is enabled..	No/Yes	0
31:9	Reserved	RsvdP	Not Support.	No	0-0h

8.2.159 HEADER LOG REGISTER – OFFSET From FD0h to FDCh

BIT	FUNCTION	TYPE	DESCRIPTION	EEPROM/ I2C-SMBUS	DEFAULT
31:0	1st DWORD	RO	Hold the 1st DWORD of TLP Header. The Head byte is in big endian.	No	0000_0000h
63:32	2nd DWORD	RO	Hold the 2nd DWORD of TLP Header. The Head byte is in big endian.	No	0000_0000h
95:64	3rd DWORD	RO	Hold the 3rd DWORD of TLP Header. The Head byte is in big endian.	No	0000_0000h
127:96	4th DWORD	RO	Hold the 4th DWORD of TLP Header. The Head byte is in big endian.	No	0000_0000h

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9 CLOCK SCHEME

The PI7C9X2G912GP requires 100MHz differential clock inputs through REFCLKP and REFCLKN Pins as shown in the following table.

Table 9-1 DC Electrical Characteristics

Description	Symbol	Min	Typ	Max	Unit
Reference Clock Frequency*	f_i		100		MHz
Accuracy	A_i	-300		+300	ppm
Duty Cycle	DC_i	45		55	%
> 1.5 MHz to Nyquist RMS jitter after applying PCIe filter function	$T_{REFCLK-HF-RMS}$	-		3.1	ps RMS
10 kHz - 1.5 MHz RMS jitter	$T_{REFCLK-LF-RMS}$	-		3.0	ps RMS
Spread Spectrum Clock frequency	SSC_{freq}	30		33	kHz

* Does not include ±300ppm. Only certain clock frequencies will produce valid PCI Express data.

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10 POWER MANAGEMENT

The PI7C9X2G912GP supports D0, D1, D2, D3-hot, and D3-cold Power States. The PCI Express Physical Link Layer of the PI7C9X2G912GP device supports the PCI Express Link Power Management with L0, L0s, L1, L2/L3 ready and L3 Power States.

PI7C9X2G912GP also supports ASPM (Active State Power Management) to facilitate the link power saving.

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11 POWER SEQUENCE

As long as PERST# is active, all PCI Express functions are held in reset. The main supplies ramp up to their specified levels (2.5V). Sometime during this stabilization time, the REFCLK starts and stabilizes. After there has been time (100 ms) for the power and clock to become stable, PERST# is deasserted high and the PCI Express functions can start up.

It is recommended to power up the I/O voltage (2.5V) first and then the core voltage (1.0V) or power up I/O voltage and core voltage simultaneously.

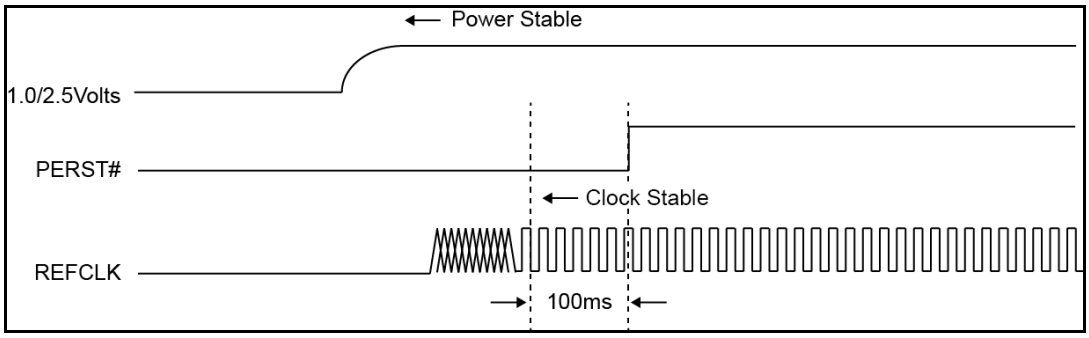

Figure 11-1 Initial Power-Up Sequence

Power-down sequence is the reverse of power-up sequence.

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12 IEEE 1149.1 COMPATIBLE JTAG CONTROLLER

An IEEE 1149.1 compatible Test Access Port (TAP) controller and associated TAP pins are provided to support boundary scan in PI7C9X2G912GP for board-level continuity test and diagnostics. The TAP pins assigned are TCK, TDI, TDO, TMS and TRST_L. All digital input, output, input/output pins are tested except TAP pins.

12.1 INSTRUCTION REGISTER

The IEEE 1149.1 Test Logic consists of a TAP controller, an instruction register, and a group of test data registers including Bypass and Boundary Scan registers. The TAP controller is a synchronous 16-state machine driven by the Test Clock (TCK) and the Test Mode Select (TMS) pins. An independent power on reset circuit is provided to ensure the machine is in TEST_LOGIC_RESET state at power-up.

PI7C9X2G912GP implements a 5-bit Instruction register to control the operation of the JTAG logic. The defined instruction codes are shown in the following table. Those bit combinations that are not listed are equivalent to the BYPASS (11111) instruction.

Table 12-1 Instruction Register Codes

Instruction	Operation Code (binary)	Register Selected	Operation
EXTEST	00000	Boundary Scan	Drives / receives off-chip test data
SAMPLE	00001	Boundary Scan	Samples inputs / pre-loads outputs
HIGHZ	00101	Bypass	Tri-states output and I/O pins except TDO pin
CLAMP	00100	Bypass	Drives pins from boundary-scan register and selects Bypass register for shifts
IDCODE	01100	Device ID	Accesses the Device ID register, to read manufacturer ID, part number, and version number
BYPASS	11111	Bypass	Selected Bypass Register
INT_SCAN	00010	Internal Scan	Scan test
MEM_BIST	01010	Memory BIST	Memory BIST test

12.2 BYPASS REGISTER

The required bypass register (one-bit shift register) provides the shortest path between TDI and TDO when a bypass instruction is in effect. This allows rapid movement of test data to and from other components on the board. This path can be selected when no test operation is being performed on the PI7C9X2G912GP.

12.3 DEVICE ID REGISTER

This register identifies Pericom as the manufacturer of the device and details the part number and revision number for the device.

Table 12-2 JTAG Device ID Register

Bit	Type	Value	Description
31-28	RO	0001	Version number
27-12	RO	0001011000010110	Last 4 digits (hex) of the die part number
11-1	RO	01000111111	Pericom identifier assigned by JEDEC
0	RO	1	Fixed bit equal to 1'b1

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12.4 BOUNDARY SCAN REGISTER

The boundary scan register has a set of serial shift-register cells. A chain of boundary scan cells is formed by connected the internal signal of the PI7C9X2G912GP package pins. The VDD, VSS, and JTAG pins are not in the boundary scan chain. The input to the shift register is TDI and the output from the shift register is TDO. There are 4 different types of boundary scan cells, based on the function of each signal pin.

The boundary scan register cells are dedicated logic and do not have any system function. Data may be loaded into the boundary scan register master cells from the device input pins and output pin-drivers in parallel by the mandatory SAMPLE and EXTEST instructions. Parallel loading takes place on the rising edge of TCK.

12.5 JTAG BOUNDARY SCAN REGISTER ORDER

Table 12-3 JTAG Boundary Scan Register Definition

Boundary Scan Register Number	Pin Name	Ball Location	Type	Tri-state Control Cell
0			Internal	
1			Internal	
2			Internal	
3			Internal	
4			Internal	
5			Internal	
6			Internal	
7			Internal	
8	PORTGOOD_L[10]	C6	Output3	9
9			Control	
10			Internal	
11			Internal	
12	FATAL_ERR_L	B5	Output3	13
13			Control	
14			Internal	
15			Internal	
16	PORTCFG[0]	A4	Input	
17			Internal	
18	PORTCFG[1]	A5	Input	
19			Internal	
20			Internal	
21			Internal	
22			Internal	
23			Internal	
24			Internal	
25			Internal	
26			Internal	
27			Internal	
28			Internal	
29			Internal	
30			Internal	
31	PORTGOOD_L[11]	A3	Output3	32
32			Control	
33			Internal	
34			Internal	
35	SERDES_MODE_EN_L	B4	Input	
36			Internal	
37			Internal	
38			Internal	
39			Internal	
40			Internal	
41			Internal	

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Boundary Scan Register Number	Pin Name	Ball Location	Type	Tri-state Control Cell
42			Internal	
43			Internal	
44			Internal	
45	FAST_MODE_L	B3	Input	
46			Internal	
47			Internal	
48			Internal	
49			Internal	
50			Internal	
51	GPIO[4]	A1	Birdir	52
52			Control	
53	GPIO[3]	A2	Birdir	54
54			Control	
55	GPIO[1]	B1	Birdir	56
56			Control	
57			Internal	
58			Internal	
59			Internal	
60			Internal	
61	GPIO[2]	B2	Birdir	62
62			Control	
63	GPIO[0]	C5	Birdir	64
64			Control	
65			Internal	
66			Internal	
67			Internal	
68			Internal	
69	GPIO[5]	C4	Birdir	70
70			Control	
71			Internal	
72			Internal	
73			Internal	
74			Internal	
75			Internal	
76			Internal	
77			Internal	
78			Internal	
79	PORTGOOD_L[13]	H3	Output3	80
80			Control	
81			Internal	
82			Internal	
83			Internal	
84			Internal	
85			Internal	
86			Internal	
87			Internal	
88			Internal	
89			Internal	
90			Internal	
91	PORTGOOD_L[12]	L3	Output3	92
92			Control	
93			Internal	
94			Internal	
95	GPIO[7]	N1	Birdir	96
96			Control	
97			Internal	
98	PORTGOOD_L[14]	P1	Output3	99
99			Control	
100			Internal	
101			Internal	
102	PORTGOOD_L[15]	N2	Output3	103
103			Control	
104			Internal	

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Boundary Scan Register Number	Pin Name	Ball Location	Type	Tri-state Control Cell
105			Internal	
106	GPIO[6]	P2	Birdir	107
107			Control	
108			Internal	
109			Internal	
110			Internal	
111			Internal	
112			Internal	
113			Internal	
114	DEBUG_SEL[1]	M3	Input	
115			Internal	
116	TEST	M4	Input	
117			Internal	
118			Internal	
119			Internal	
120	SMBUS_EN_L	M8	Input	
121			Internal	
122			Internal	
123			Internal	
124			Internal	
125			Internal	
126	CFG_TIMER_EN_L	M11	Input	
127			Internal	
128			Internal	
129			Internal	
130			Internal	
131			Internal	
132			Internal	
133			Internal	
134			Internal	
135			Internal	
136			Internal	
137			Internal	
138			Internal	
139			Internal	
140			Internal	
141	TESTMODE[0]	P14	Input	
142			Internal	
143	TESTMODE[1]	N13	Input	
144			Internal	
145	TESTMODE[2]	N14	Input	
146			Internal	
147			Internal	
148			Internal	
149	PORTGOOD_L[0]	L12	Output3	150
150			Control	
151			Internal	
152			Internal	
153			Internal	
154			Internal	
155			Internal	
156			Internal	
157			Internal	
158			Internal	
159			Internal	
160			Internal	
161			Internal	
162			Internal	
163	PORTGOOD_L[3]	G12	Output3	164
164			Control	
165			Internal	
166			Internal	
167			Internal	

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Boundary Scan Register Number	Pin Name	Ball Location	Type	Tri-state Control Cell
168			Internal	
169			Internal	
170			Internal	
171	PORTGOOD_L[2]	E12	Output3	172
172			Control	
173			Internal	
174			Internal	
175			Internal	
176			Internal	
177			Internal	
178			Internal	
179			Internal	
180			Internal	
181			Internal	
182			Internal	
183			Internal	
184			Internal	
185			Internal	
186			Internal	
187			Internal	
188			Internal	
189			Internal	
190			Internal	
191			Internal	
192			Internal	
193	EECK	D12	Birdir	194
194			Control	
195	EECS_L	C12	Output3	196
196			Control	
197			Internal	
198			Internal	
199	PLL_BYPASS_L	B14	Input	
200			Internal	
201	INTA_L	A14	Output3	202
202			Control	
203	PERST_L	A13	Input	
204			Internal	
205			Internal	
206			Internal	
207			Internal	
208			Internal	
209			Internal	
210			Internal	
211			Internal	
212	DEBUG_SEL[0]	B12	Input	
213			Internal	
214	EEDO	C11	Input	
215			Internal	
216	EEDI	B11	Birdir	217
217			Control	
218	I2C_ADDR[2]	A11	Input	
219			Internal	
220	I2C_ADDR[1]	A10	Input	
221			Internal	
222			Internal	
223			Internal	
224			Internal	
225			Internal	
226			Internal	
227			Internal	
228			Internal	
229			Internal	
230			Internal	

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Boundary Scan Register Number	Pin Name	Ball Location	Type	Tri-state Control Cell
231			Internal	
232			Internal	
233			Internal	
234			Internal	
235			Internal	
236	I2C_ADDR[0]	A9	Input	
237			Internal	
238	SCL_I2C	B10	Output3	239
239			Control	
240			Internal	
241			Internal	
242	SHDA_I2C	B9	Output3	243
243			Control	
244			Internal	
245			Internal	
246			Internal	
247			Internal	
248	SHCL_I2C	B8	Output3	249
249			Control	
250	SDA_I2C	C10	Output3	251
251			Control	
252	SHPCINT_L	A8	Input	
253			Internal	
254			Internal	
255			Internal	
256			Internal	
257			Internal	
258			Internal	
259			Internal	
260			Internal	
261			Internal	
262			Internal	

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13 ELECTRICAL AND TIMING SPECIFICATIONS

13.1 ABSOLUTE MAXIMUM RATINGS

Table 13-1 Absolute Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Item	Absolute Max. Rating
Storage Temperature	-65°C to 150°C
Junction Temperature, Tj	125 °C
Digital core and analog supply voltage to ground potential (VDDC and AVDD)	-0.3v to 1.2v
Digital I/O and analog high supply voltage to ground potential (VDDR and AVDDH)	-0.3v to 3.8v
DC input voltage for Digital I/O signals	-0.3v to 3.8v
ESD Rating Human Body Model (JEDEC Class 2) Charge Device Model (JEDEC Class 3)	 2kv 500v

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

13.2 DC SPECIFICATIONS

Table 13-2 DC Electrical Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
VDDC	Digital Core Power	1.0		1.1	V
VDDR	Digital I/O Power	2.25	2.5	2.75	
AVDD	PCI Express Analog Power	1.0		1.1	
AVDDH	PCI Express Analog High Voltage Power	2.25	2.5	2.75	
V_{IH}	Input High Voltage	2.0		3.6	
V_{IL}	Input Low Voltage	-0.3		0.8	
V_{OH}	Output High Voltage	2.4	-	-	
V_{OL}	Output Low Voltage	-	-	0.4	
R_{PU}	Pull-up Resistor	63K	92K	142K	Ω
R_{PD}	Pull-down Resistor	57K	91K	159K	
$RST\#_{Slew}$ [1]	PERST_L Slew Rate	50			mV/ns

Note:
1. The min. value for PERST_L Slew Rate is 50 mV/ns, which translates to the requirement that the time for PERST_L from 0V to 2.5V should be less than 50 ns.

13.3 AC SPECIFICATIONS

Table 13-3 PCI Express Interface - Differential Transmitter (TX) Output (5.0 Gbps) Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Unit Interval	UI	199.94	200.0	200.06	ps
Differential p-p TX voltage swing	$V_{TX-DIFF-P-P}$	800	-	-	mV ppd
Low power differential p-p TX voltage swing	$V_{TX-DIFF-P-P-LOW}$	400	-	-	mV ppd
TX de-emphasis level ratio	$V_{TX-DE-RATIO-3.5dB}$	-3.0	-	-4.0	dB
TX de-emphasis level ratio	$V_{TX-DE-RATIO-6dB}$	-5.5		-6.5	dB
Transmitter Eye including all jitter sources	T_{TX-EYE}	0.75	-	-	UI

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Parameter	Symbol	Min	Typ	Max	Unit
TX deterministic jitter > 1.5 MHz	$T_{TX-HF-DJ-DD}$	-	-	0.15	UI
TX RMS jitter < 1.5 MHz	$T_{TX-LF-RMS}$	-	-	3.0	Ps RMS
Transmitter rise and fall time	$T_{TX-RISE-FALL}$	0.15	-	-	UI
TX rise/fall mismatch	$T_{RF-MISMATCH}$	-	-	0.1	UI
Maximum TX PLL Bandwidth	BW_{TX-PLL}	-	-	16	MHz
Minimum TX PLL BW for 3dB peaking	$BW_{TX-PLL-LO-3DB}$	8	-	-	MHz
TX PLL peaking with 8 MHz min BW	$PKG_{TX-PLL1}$	-	-	3.0	dB
DC Differential TX Impedance	$Z_{TX-DIFF-DC}$	80	-	120	Ω
Transmitter Short-Circuit Current Limit	$I_{TX-SHORT}$	-	-	90	mA
TX DC Common Mode Voltage	$V_{TX-DC-CM}$	0	-	3.6	V
Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	0	-	100	mV
Absolute Delta of DC Common Mode Voltage between D+ and D–	$V_{TX-CM-DC-LINE-DELTA}$	0	-	25	mV
Electrical Idle Differential Peak Output Voltage	$V_{TX-IDLE-DIFF-AC-p}$	0	-	20	mV
DC Electrical Idle Differential Output Voltage	$V_{TX-IDLE-DIFF-DC}$	0	-	5	mV
The Amount of Voltage Change Allowed During Receiver Detection	$V_{TX-RCV-DETECT}$	-	-	600	mV
Lane-to-Lane Output Skew	$L_{TX-SKEW}$	-	-	500 ps + 4 UI	ps

Table 13-4 PCI Express Interface - Differential Transmitter (TX) Output (2.5 Gbps) Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Unit Interval	UI	399.88	400.0	400.12	ps
Differential p-p TX voltage swing	$V_{TX-DIFF-P-P}$	800	-	-	mV ppd
Low power differential p-p TX voltage swing	$V_{TX-DIFF-P-P-LOW}$	400	-	-	mV ppd
TX de-emphasis level ratio	$V_{TX-DE-RATIO}$	-3.0	-	-4.0	dB
Minimum TX eye width	T_{TX-EYE}	0.75	-	-	UI
Maximum time between the jitter median and max deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.125	UI
Transmitter rise and fall time	$T_{TX-RISE-FALL}$	0.125	-	-	UI
Maximum TX PLL Bandwidth	BW_{TX-PLL}	-	-	22	MHz
Maximum TX PLL BW for 3dB peaking	$BW_{TX-PLL-LO-3DB}$	1.5	-	-	MHz
Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	0	-	100	mV
Absolute Delta of DC Common Mode Voltage between D+ and D–	$V_{TX-CM-DC-LINE-DELTA}$	0	-	25	mV
Electrical Idle Differential Peak Output Voltage	$V_{TX-IDLE-DIFF-AC-p}$	0	-	20	mV
The Amount of Voltage Change Allowed During Receiver Detection	$V_{TX-RCV-DETECT}$	-	-	600	mV
Transmitter DC Common Mode Voltage	$V_{TX-DC-CM}$	0	-	3.6	V
Transmitter Short-Circuit Current Limit	$I_{TX-SHORT}$	-	-	90	mA
DC Differential TX Impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω
Lane-to-Lane Output Skew	$L_{TX-SKEW}$	-	-	500 ps + 2 UI	ps

Table 13-5 PCI Express Interface - Differential Receiver (RX) Input (5.0 Gbps) Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Unit Interval	UI	199.94	200.0	200.06	ps
Differential RX Peak-to-Peak Voltage	$V_{RX-DIFF-PP-CC}$	120	-	1200	mV
Total jitter tolerance	TJ_{RX}	0.68	-	-	UI
Receiver DC common mode impedance	Z_{RX-DC}	40	-	60	Ω
RX AC Common Mode Voltage	$V_{RX-CM-AC-P}$	-	-	150	mV
Electrical Idle Detect Threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	-	175	mV

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Table 13-6 PCI Express Interface - Differential Receiver (RX) Input (2.5 Gbps) Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Unit Interval	UI	399.88	400.0	400.12	ps
Differential RX Peak-to-Peak Voltage	$V_{RX-DIFF-PP-CC}$	175	-	1200	mV
Receiver eye time opening	T_{RX-EYE}	0.4	-	-	UI
Maximum time delta between median and deviation from median	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.3	UI
Receiver DC common mode impedance	Z_{RX-DC}	40	-	60	Ω
DC differential impedance	$Z_{RX-DIFF-DC}$	80	-	120	Ω
RX AC Common Mode Voltage	$V_{RX-CM-AC-P}$	-	-	150	mV
DC input CM input impedance during reset or power down	$Z_{RX-HIGH-IMP-DC}$	200	-	-	kΩ
Electrical Idle Detect Threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	-	175	mV
Lane to Lane skew	$L_{RX-SKEW}$	-	-	20	ns

13.4 OPERATING AMBIENT TEMPERATURE

Table 13-7 Operating Ambient Temperature

(The Operating Ambient Temperature be associated with Chapter 14.)

Item	Low	High	Unit
Ambient Temperature with power applied	-40	85	°C

Note: Exposure to high temperature conditions for extended periods of time may affect reliability.

13.5 POWER CONSUMPTION

Table 13-8 Power Consumption

Active Lane per Port	1.0VDDC		1.0VDDA		2.5AVDDH		2.5VDDR		Total		Unit
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	
4/ 8 x1	0.55	1.355	0.535	1.044	0.09	0.102	0.02	0.041	1.20	2.54	W
4/ 4 x 2	0.627	1.194	0.534	1.042	0.09	0.102	0.02	0.030	1.27	2.37	W

Test Conditions:

- Typical power measured under the conditions of 1.0V/ 2.5V power rail without device usage on all downstream ports.
- Maximum power measured under the conditions of 1.1V/ 2.75V with PCIe2 devices usage on all downstream ports
- Ambient Temperature at 25°C
- Power consumption in the table is a reference, be affected by various environment, bus traffic and power supply etc.

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14 THERMAL DATA

The information described in this section is provided for reference only.

Table 14-1 Thermal Data

Power (Watt)	T_a (℃)	JEDEC Board	Airflow (m/s)	Θ_{JA} (℃/W)	T_j (℃)	Θ_{JC} (℃/W)
2.3	85	4-Layer	0	26.65	146.30	8.96
			1	23.71	139.53	
			2	22.57	136.91	
		8-Layer	0	17.75	125.83	8.44
			1	16.65	123.30	
			2	16.33	122.56	

Note:
1. T_a: Ambient Temperature
2. T_J: Junction Temperature
3. Maximum allowable junction temperature = 125℃
4. Θ_{JA}: Thermal Resistance, Junction-to-Ambient
5. Θ_{JC}: Thermal Resistance, Junction-to-Case
6. Power measured under the conditions of 1.0V/ 2.5V with PCIe2 devices usage on all downstream ports in 912 mode
7. The shaded fields provide a recommendation that allows PI7C9X2G912GP to support Industrial Temperature Range

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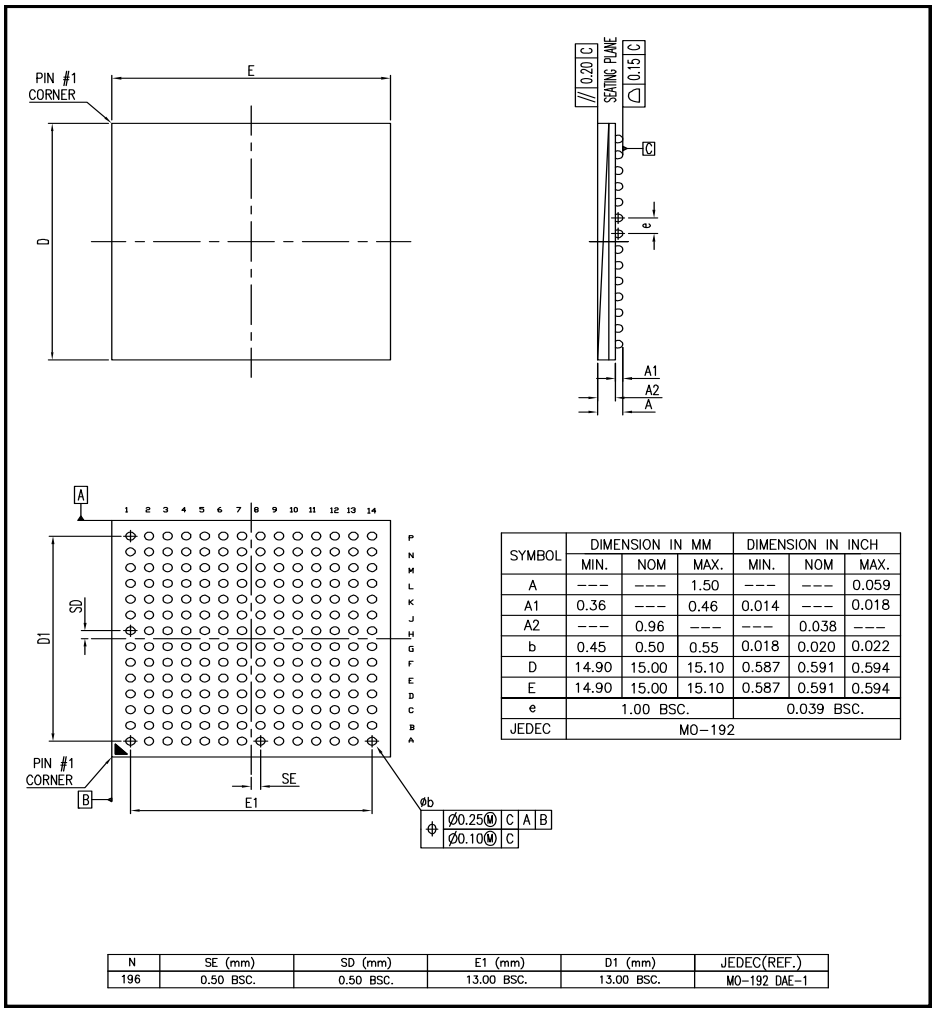
15 PACKAGE INFORMATION

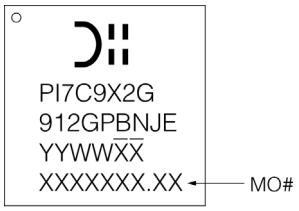
The package of PI7C9X2G912GP is a 15mm x 15mm LBGA (196 Ball) package. The following are the package information and mechanical dimension:



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	---	---	1.50	---	---	0.059
A1	0.36	---	0.46	0.014	---	0.018
A2	---	0.96	---	---	0.038	---
b	0.45	0.50	0.55	0.018	0.020	0.022
D	14.90	15.00	15.10	0.587	0.591	0.594
E	14.90	15.00	15.10	0.587	0.591	0.594
e	1.00 BSC.			0.039 BSC.		
JEDEC	MO-192					

N	SE (mm)	SD (mm)	E1 (mm)	D1 (mm)	JEDEC(REF.)
196	0.50 BSC.	0.50 BSC.	13.00 BSC.	13.00 BSC.	MO-192 DAE-1

Figure 15-1 Package Outline Drawing



YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code
Bar above fab code means Cu wire
Bar above assy code means ULA BOM

Figure 15-2 Part Marking

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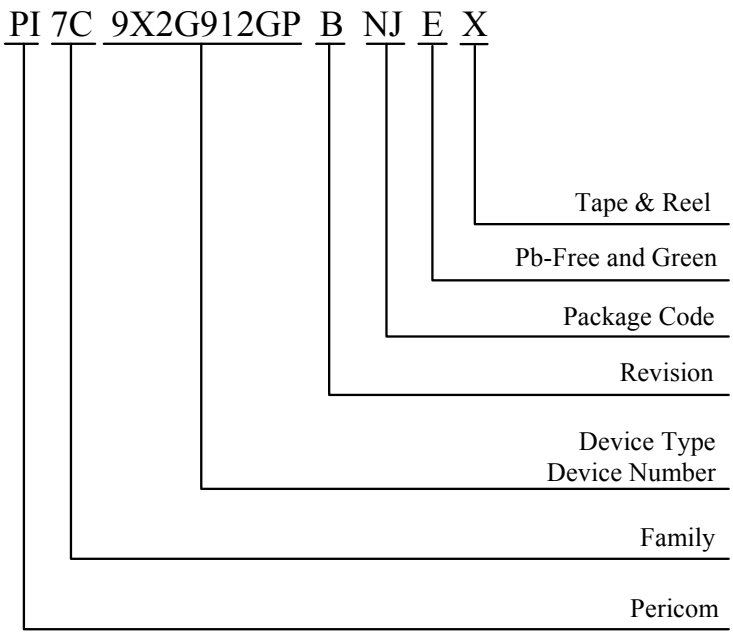
16 ORDERING INFORMATION

Part Number	Operating Temperature	Package Code	Package Description
PI7C9X2G912GPBNJEX	-40° to 85°C (Industrial Temperature)	NJ	196-pin 15mmx15mm LBGA

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.



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