International
IOR Rectifier

IR3522

DATA SHEET

XPHASE3™ DDR & VTT CONTROL IC

DESCRIPTION

The IR3522 Control IC combined with IR3506 *xPHASE3*™ Phase ICs implements a full featured DDR3 power solution. The IR3522 provides control functions for both the VTT (single phase) and VDDR (multiphase) power rails which can interfaces with any number of IR3506 ICs each driving and monitoring a single phase to power any number of DDR3 DIMMs. The *xPHASE3*™ architecture delivers a power supply that is smaller, more flexible, and easier to design while providing higher efficiency than conventional approaches.

FEATURES

- I^2C interface programs 1.025V< VREF1<1.612V, the VDD output voltage reference
- I^2C also programs the VTT tracking ratio ± 25 %, and provides digital ON/OFF control
- Four different I^2C addresses are selectible using 2 ADDR pins
- Four different VREF1 voltages are selectible using 2 VID pins if I^2C communication is not available
- VTT tracking defaults to ½ the VDD Remote Sense Amp output voltage
- Power Good output driven by an external bias input
- VDD to VTT overvoltage protection
- Soft-Stop turn-off to ensure VDDR and Vtt tracking
- Fault activated Crowbar pin to drive external NMOS devices for external output voltage protection
- Pin programmable slew rate of I^2C programmed VREF1 voltage transitions
- 0.5% overall VDD system set point accuracy
- Remote sense amplifiers provide differential sensing and requires less than 50uA bias current
- Pin programmable per phase switching frequency of 250kHz to 1.5MHz
- Complete protection including over-current, over-voltage, open remote sense, and open control

APPLICATION CIRCUIT

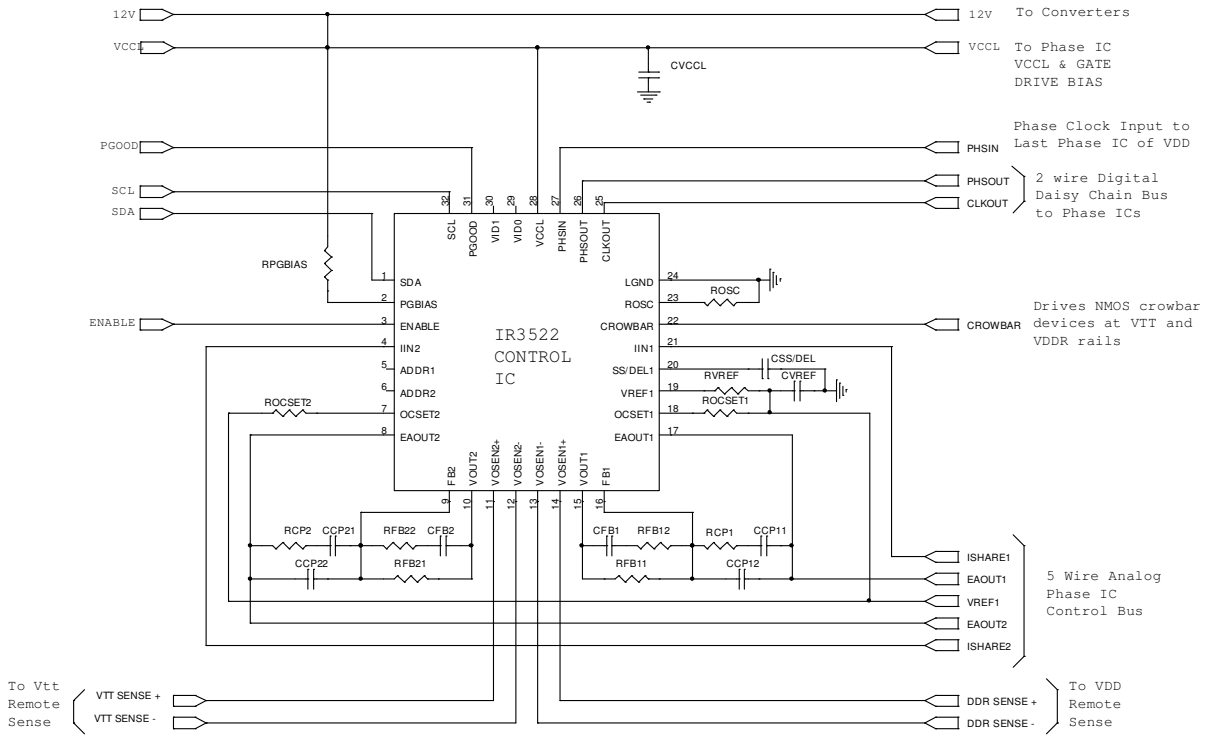


Figure 1 – IR3522 Application Circuit

ORDERING INFORMATION

Device	Package	Order Quantity
IR3522MTRPBF	32 Lead MLPQ (5 x 5 mm body)	3000 per reel
* IR3522MPBF	32 Lead MLPQ (5 x 5 mm body)	100 piece strips

* Samples only

PIN DESCRIPTION

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	SDA	SDA (Serial Data) is a bidirectional signal that is an input and open drain output for both master (I^2C controller) and slave (IR3522). SDA requires a pull resistor to a bias voltage and should not be floated.
2	PGBIAS	Input to provide bias to the Power Good output transistor directly from the converter input voltage. Enables the Power Good output to assert even if there is no bias supplied to the VCCL pin. Internal voltage clamp protects the pin. Do not exceed 100 uA of pull-up current.
3	ENABLE	Enable input. A logic low applied to this pin puts the IC into fault mode. A logic high on the pin resets and enables the converter. Do not float this pin as the logic state will be undefined.
4	IIN2	Output 2 average current input from the output 2 phase IC(s).
5	ADDR1	Digital input to program bit 1 of the 2 bit address code with internal pull-up. Connect to LGND for logic “0”, float for logic “1”
6	ADDR2	Digital input to program bit 2 of the 2 bit address code with internal pull-up. Connect to LGND for logic “0”, float for logic “1”
7	OCSET2	Programs the output 2 constant converter output current limit through an external resistor tied to VREF1 and an internal current source from this pin. Over-current protection can be disabled by over sizing the resistor value to program the threshold higher than IIN2 pin possible signal amplitude, but no greater than 5V (do not float this pin as improper operation will occur).
8	EAOUT2	Output of the output 2 error amplifier.
9	FB2	Inverting input to the output 2 error amplifier.
10	VOUT2	Output 2 remote sense amplifier output.
11	VOSEN2+	Output 2 remote sense amplifier input. Connect to output at the load.
12	VOSEN2-	Output 2 remote sense amplifier input. Connect to ground at the load.
13	VOSEN1-	Output 1 remote sense amplifier input. Connect to ground at the load.
14	VOSEN1+	Output 1 remote sense amplifier input. Connect to output at the load.
15	VOUT1	Output 1 remote sense amplifier output. Provides reference to Error Amp2.
16	FB1	Inverting input to the output 1 error amplifier.
17	EAOUT1	Output of the output 1 error amplifier.
18	OCSET1	Programs the output 1 constant converter output current limit through an external resistor tied to VREF1 and an internal current source from this pin. Over-current protection can be disabled by over sizing the resistor value to program the threshold higher than IIN2 pin possible signal amplitude, but no greater than 5V (do not float this pin as improper operation will occur).
19	VREF1	Reference voltage programmed by the I^2C inputs and error amplifier non-inverting input. Connect an external RC network to LGND to program dynamic VID slew rate and provide compensation for the internal buffer amplifier.
20	SS/DEL1	Connect an external capacitor to LGND to program startup and Fault delay timing

PIN#	PIN SYMBOL	PIN DESCRIPTION
21	IIN1	Output 1 average current input from the output 1 phase IC(s). This pin is also used to initialize Diode Emulation Mode in the phase IC(s).
22	CROWBAR	Drives NMOS crowbar devices at VTT and VDDR rails.
23	ROSC	Connect a resistor to LGND to program oscillator frequency and OCSET1, OCSET2, and VREF bias currents. Oscillator frequency equals switching frequency per phase. The pin voltage is 0.6V during normal operation.
24	LGND	Local Ground for internal circuitry and IC substrate connection.
25	CLKOUT	Clock output at switching frequency multiplied by phase number. Connect to CLKIN pins of phase ICs.
26	PHSOUT	Phase clock output at switching frequency per phase. Connect to PHSIN pin of the first phase IC.
27	PHSIN	Feedback input of phase clock. Connect to PHSOUT pin of the last phase IC.
28	VCCL	Output of the voltage regulator, and power input for clock oscillator circuitry. Connect a decoupling capacitor to LGND.
29	VID0	Digital input to program one of four power-up VREF1 VDD reference values. Connect to LGND for logic “0”, float for logic “1”
30	VID1	Digital input to program one of four power-up VREF1 VDD reference values. Connect to LGND for logic “0”, float for logic “1”
31	PGOOD	Open collector output that drives low during startup and under any external fault condition. The Power Good function also monitors output voltages and this pin will drive low if any of the voltage planes are outside of the specified limits. Connect external pull-up.
32	SCL	SCL (Serial Clock) is an open drain output of the I^2C controller and input to IR3522. This pin requires an external bias voltage and should not be floated.

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed below may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. All voltages are absolute voltages referenced to the LGND pin.

Operating Junction Temperature……..0 to 150°C
Storage Temperature Range…….-65°C to 150°C
ESD Rating……HBM Class 1C JEDEC Standard
MSL Rating……2
Reflow Temperature…….260°C

PIN #	PIN NAME	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
1	SDA	8V	-0.3V	1mA	10mA
2	PGBIAS	8V	-0.3V	1mA	1mA
3	ENABLE	3.5V	-0.3V	1mA	1mA
4	IIN2	8V	-0.3V	5mA	1mA
5	ADDR1	3.5V	-0.3V	1mA	1mA
6	ADDR2	3.5V	-0.3V	1mA	1mA
7	OCSET2	8V	-0.3V	1mA	1mA
8	EAOUT2	8V	-0.3V	25mA	10mA
9	FB2	8V	-0.3V	1mA	1mA
10	VOUT2	8V	-0.3V	5mA	25mA
11	VOSEN2+	8V	-0.5V	5mA	1mA
12	VOSEN2-	1.0V	-0.5V	5mA	1mA
13	VOSEN1-	1.0V	-0.5V	5mA	1mA
14	VOSEN1+	8V	-0.5V	5mA	1mA
15	VOUT1	8V	-0.3V	5mA	25mA
16	FB1	8V	-0.3V	1mA	1mA
17	EAOUT1	8V	-0.3V	25mA	10mA
18	OCSET1	8V	-0.3V	1mA	1mA
19	VREF1	3.5V	-0.3V	1mA	1mA
20	SS/DEL1	8V	-0.3V	1mA	1mA
21	IIN1	V(VCCL) + 1.1 V	-0.3V	5mA	1mA
22	CROWBAR	8V	-0.3V	35mA	1mA
23	ROSC	8V	-0.3V	1mA	1mA
24	LGND	n/a	n/a	20mA	1mA
25	CLKOUT	8V	-0.3V	100mA	100mA
26	PHSOUT	8V	-0.3V	10mA	10mA
27	PHSIN	8V	-0.3V	1mA	1mA
28	VCCL	8V	-0.3V	1mA	20mA
29	VID0	8V	-0.3V	1mA	1mA
30	VID1	8V	-0.3V	1mA	1mA
31	PGOOD	VCCL + 0.3V	-0.3V	1mA	20mA
32	SCL	8V	-0.3V	1mA	1mA

RECOMMENDED OPERATING CONDITIONS FOR RELIABLE OPERATION WITH MARGIN
4.75V ≤ VCCL ≤ 7.5V, -0.3V ≤ VOSEN-x ≤ 0.3V, 0 °C ≤ T_J ≤ 100 °C, 7.75 kΩ ≤ R_{OSC} ≤ 50 kΩ, $C_{SS/DEL1}$ = 0.1uF

ELECTRICAL CHARACTERISTICS

The electrical characteristics table list the spread of critical values that are guaranteed to be within the recommended operating conditions (unless otherwise specified). Typical values represent the median values, which are related to 25°C.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
SVID Interface					
SCL & SDA Input Thresholds	Threshold Increasing	**1.265**	**1.325**	**1.385**	V
	Threshold Decreasing	**1.04**	**1.1**	**1.16**	V
	Threshold Hysteresis	150	225	300	mV
Bias Current	0V ≤ V(x) ≤ 3.5V, SDA not asserted	-5	0	5	uA
SDA Low Voltage	I(SDA)= 3mA		20	300	mV
SDA Output Fall Time	0.7 x VDD to 0.3 x VDD, 1.425V ≤ VDD ≤ 1.9V, 10 pF ≤ Cb ≤ 400 pF, Cb=capacitance of one bus line (Note 1)	20+ 0.1 xCb(pF)		250	ns
Pulse width of spikes suppressed by the input filter	Note 1	85	260	550	ns
ADDRx Internal Pull-up	Pull-up to 3.3 V typical	50	100	250	kΩ
ADDRx Threshold Voltage		1.38	1.65	1.94	V
ADDRx Float Voltage		3.1	3.3	3.5	V
Oscillator					
PHSOUT Frequency		**-10%**	**See Figure 2**	**+10%**	kHz
ROSC Voltage		0.57	0.600	0.630	V
CLKOUT High Voltage	I(CLKOUT)= -10 mA, measure V(VCCL) – V(CLKOUT).			1	V
CLKOUT Low Voltage	I(CLKOUT)= 10 mA			1	V
PHSOUT High Voltage	I(PHSOUT)= -1 mA, measure V(VCCL) – V(PHSOUT)			1	V
PHSOUT Low Voltage	I(PHSOUT)= 1 mA			1	V
PHSIN Threshold Voltage	Compare to V(VCCL)	30	50	70	%
Remote Sense Differential Amplifiers					
Unity Gain Bandwidth	Note 1	3.0	6.4	9.0	MHz
Input Offset Voltage	1.025 V ≤ V(VOSEN1+) - V(VOSEN1-) ≤ 1.6125 V, 385mV ≤ V(VOSEN2+) - V(VOSEN2-) ≤ 1.021 V, Note 2	**-3**	**0**	**3**	mV
Source Current	1.025 V ≤ V(VOSEN1+) - V(VOSEN1-) ≤ 1.6125 V, 385mV ≤ V(VOSEN2+) - V(VOSEN2-) ≤ 1.021 V	3	7	15	mA
Sink Current	1.025 V ≤ V(VOSEN1+) - V(VOSEN1-) ≤ 1.6125 V, 385mV ≤ V(VOSEN2+) - V(VOSEN2-) ≤ 1.021 V	300	450	650	uA
Slew Rate	1.025 V ≤ V(VOSEN1+) - V(VOSEN1-) ≤ 1.6125 V, 385mV ≤ V(VOSEN2+) - V(VOSEN2-) ≤ 1.021 V Note 1.	2	4	8	V/us
VOSEN+ Bias Current	1.025 V ≤ V(VOSEN1+) - V(VOSEN1-) ≤ 1.6125 V, 385mV ≤ V(VOSEN2+) - V(VOSEN2-) ≤ 1.021 V		30	50	uA
VOSEN- Bias Current	1.025 V ≤ V(VOSEN1+) - V(VOSEN1-) ≤ 1.6125 V, 385mV ≤ V(VOSEN2+) - V(VOSEN2-) ≤ 1.021 V, All VID Codes		30	50	uA
Low Voltage	V(VCCL) =7V			40	mV
High Voltage	V(VCCL) – V(VOUTx)	1.2	1.8	2.3	V

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Soft Start and Soft Stop					
Start Delay	Measure Enable to EAOUT1 activation	1	2.9	3.5	ms
Start-up Time	Measure Enable activation to PGOOD	3	8	13	ms
SS/DEL1 to FB1 Input Offset Voltage	With FB1 = 0V, adjust V(SS/DEL1) until EAOUT1 drives high	0.7	1.4	1.9	V
Charge Current		-20	-45	-90	µA
Soft Stop Discharge Currents		25	55	105	µA
Charge Voltage		3.7	4	4.2	V
Discharge Comp. Threshold		150	220	300	mV
Delay Comparator Threshold	Relative to Charge Voltage, SS/DELx rising Note 1		80		mV
Delay Comparator Threshold	Relative to Charge Voltage, SS/DELx falling Note 1		120		mV
Delay Comparator Hysteresis	Note 1		40		mV
IINx Bias Current		-1	0	1	uA
SRD Comp. Rise Threshold		330	390	440	mV
SRD Comp. Fall Threshold		310	360	425	mV
SRD Comp Hysteresis		15	30	50	mV
IIN1 High Voltage	Measure V(VCCL)-V(IIN1)	0		1.2	V
Error Amplifiers					
VOUT1 System Set-Point Accuracy	(Deviation from Table 2 and per test circuit in Figures 2A)	**-0.5**		**0.5**	%
VOUT2 Tracking Accuracy	(Deviation from Table 2, and 3 per test circuit in Figures 2B)	**-1.0**		**1.0**	%
Input Offset Voltage	Measure V(FB1) – V(VREF1). Measure V(FB2) – V(VOUT1)/2. Note 2	**-1**	**0**	**1**	mV
FB1, FB2 Bias Currents		-1	0	1	µA
DC Gain	Note 1	**100**	**110**	**135**	dB
Bandwidth	Note 1	**20**	30	40	MHz
Slew Rate	Note 1	**5.5**	12	20	V/µs
Sink Current		0.4	0.85	1.2	mA
Source Current		5.0	8.5	12.0	mA
Maximum Voltage	Measure V(VCCL) – V(EAOUTx)	500	780	950	mV
Minimum Voltage			120	250	mV
Open Control Loop Detection Threshold	Measure V(VCCL) - V(EAOUTx), Relative to Error Amplifier maximum voltage.	125	300	600	mV
Open Control Loop Detection Delay	Measure PHSOUT pulse numbers from V(EAOUTx)=V(VCCL) to PGOOD = low.		8		Pulses
FB2 Activation Voltage	With FB2 grounded, V(VOUT1)/2 when EAOUT2 drives high	40	70	100	mV
VREF1 Reference					
Source and Sink Currents	Includes I(OCSET1) and I(OCSET2)	**-8%**	**2000*Vrosc(V) / ROSC(kΩ)**	**+8%**	µA
POWER GOOD (PGOOD) Output					
Under Voltage Threshold - Voutx Decreasing	VOUT1 referenced to VREF1 VOUT2 referenced to VOUT1/2	-365	-315	-265	mV
Under Voltage Threshold - Voutx Increasing	VOUT1 referenced to VREF1 VOUT2 referenced to VOUT1/2	-325	-275	-225	mV
Under Voltage Threshold Hysteresis		5	53	110	mV
Output Voltage	I(PGOOD) = 3mA		150	300	mV
Leakage Current	V(PGOOD) = 5.5V		0	10	µA
PGBIAS Activation Threshold	I(PGOOD)=2mA, V(PGOOD) = 300mV		2	3.5	V
PGBIAS Clamp Voltage	I(PGBIAS) = 100uA	3	4.5	6.5	V
I(PGBIAS)max				100	uA

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Over Voltage Protection (OVP) Comparators					
VOUT1 Threshold Voltage	Compare to V(VREF1)	230	260	300	mV
VOUT2 Threshold Voltage	Compare to V(VREF1)	-20	0	20	mV
CROWBAR					
VOUT1 Propagation Delay to CROWBAR	Measure time from V(VOUT1) > V(VREF1) (500 mV overdrive) to V(CROWBAR) transition to > 2 V with 1nF.		40	100	ns
VOUT2 Propagation Delay to CROWBAR	Measure time from V(VOUT2) > V(VREF1) (250 mV overdrive) to V(CROWBAR) transition to > 2 V with 1nF.		40	100	ns
CROWBAR Pull-up Resistance, Active	To VCCL		5	15	Ω
CROWBAR Passive Pull Down Resistance		12	25	65	kΩ
CROWBAR Active Pull Down Resistance to LGND			20	60	Ω
Track Fault Comparator					
Threshold Voltage	Compare VOUT1 to VOUT2	**0.99**	**1.06**	**1.13**	V
Propagation Delay to CROWBAR	Measure time from V(VOUT1) > V(VOUT1) (1.2V overdrive) to V(CROWBAR) transition to > 0.9 * V(VCCL).		90	180	ns
Open Sense Line Detection					
Sense Line Detection Active Comparator Threshold Voltage		150	200	250	mV
Sense Line Detection Active Comparator Offset Voltage	V(VOUTx) < [V(VOSENx+) – V(LGND)] / 2	35	62.5	90	mV
VOSEN+ Open Sense Line Comparator Threshold	Compare to V(VCCL)	86.5	89.0	91.5	%
VOSEN- Open Sense Line Comparator Threshold		0.36	0.40	0.44	V
Sense Line Detection Source Currents	V(VOUTx) = 100mV	200	500	700	uA
VIDx					
VID0 & VID1 Input Thresholds		1.38	1.65	1.94	V
Internal Pull-up	Pull-up to 3.3 V typical	50	100	250	kΩ
Float Voltage		3.1	3.3	3.5	V
ENABLE					
Threshold Increasing		1.38	1.65	**1.94**	V
Threshold Decreasing		**0.8**	0.99	1.2	V
Threshold Hysteresis		470	620	770	mV
Bias Current	0V ≤ V(x) ≤ 3.5V	-5	0	5	uA
Blanking Time	Noise Pulse < 100ns will not register an ENABLE state change. Note 1	75	250	400	ns
Over-Current Comparators					
Input Offset Voltage	1V ≤ V(OCSETx) ≤ 3.3V	-35	0	35	mV
OCSET Bias Current		**-5%**	**Vrosc(V)*1000/ Rosc(KΩ)**	**+5 %**	µA
2048-4096 Count Threshold	ROSC value, Note 1	11.3	16	23.1	kΩ
1024-2048 Count Threshold	ROSC value, Note 1	14.4	20	29.1	kΩ

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
VCCL					
Supply Current		**3.5**	**7**	**15**	mA
UVLO Start Threshold		4.20	4.43	**4.7**	V
UVLO Stop Threshold		**3.8**	3.99	4.3	V
Hysteresis		0.36	0.42	0.46	V

Note 1: Guaranteed by design, but not tested in production
Note 2: VDACx Outputs are trimmed to compensate for Error & Amp Remote Sense Amp input offsets
Bold Letters: Critical specs

SYSTEM SET POINT TEST

Converter output voltage is determined by the system set point voltage which is the voltage that appears at the FBx pins when the converter is in regulation. The set point voltage includes error terms for the VDAC digital-to-analog converters, the Error Amp input offsets, and the Remote Sense input offsets. The voltage appearing at the VDACx pins is not the system set point voltage. System set point voltage test circuits for Outputs 1 and 2 are shown in Figures 2A and 2B.

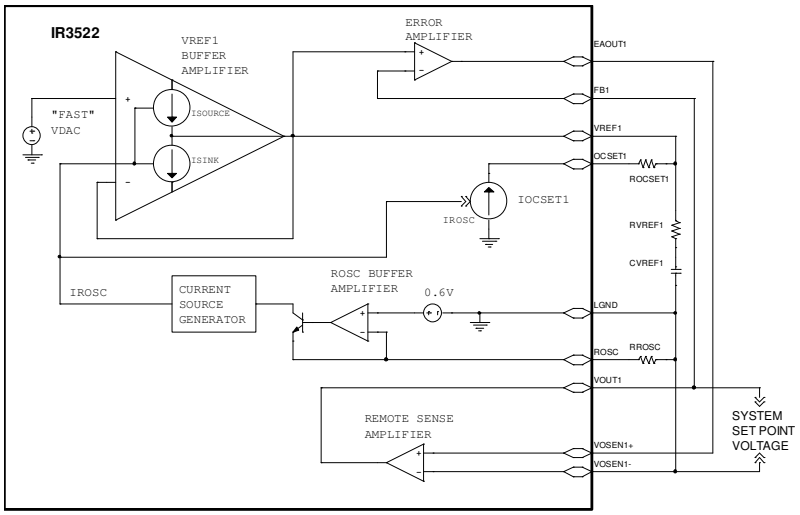


Figure 2A - Output 1 System Set Point Test Circuit

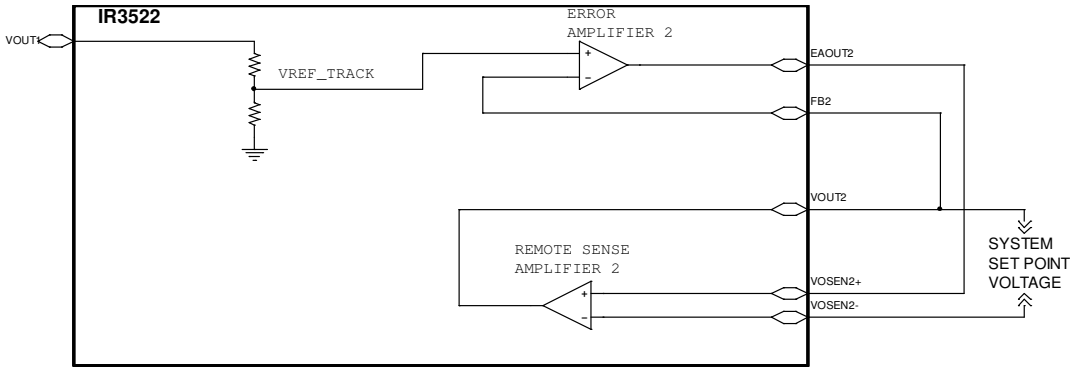


Figure 2B - Output 2 System Set Point Test Circuit

SYSTEM THEORY OF OPERATION

PWM Control Method

The PWM block diagram of the *xPHASE3*™ architecture is shown in Figure 3. Feed-forward voltage mode control with trailing edge modulation is used to provide system control. A voltage type error amplifier with high-gain and wide-bandwidth, located in the Control IC, is used for the voltage control loop. The feed-forward control is performed by the phase ICs as a result of sensing the Input voltage (FET's drain voltage). The PWM ramp slope will change with the input voltage and automatically compensate for changes in the input voltage. The input voltage can change due to variations in the silver box output voltage or due to the wire and PCB-trace voltage drop related to changes in load current.

.

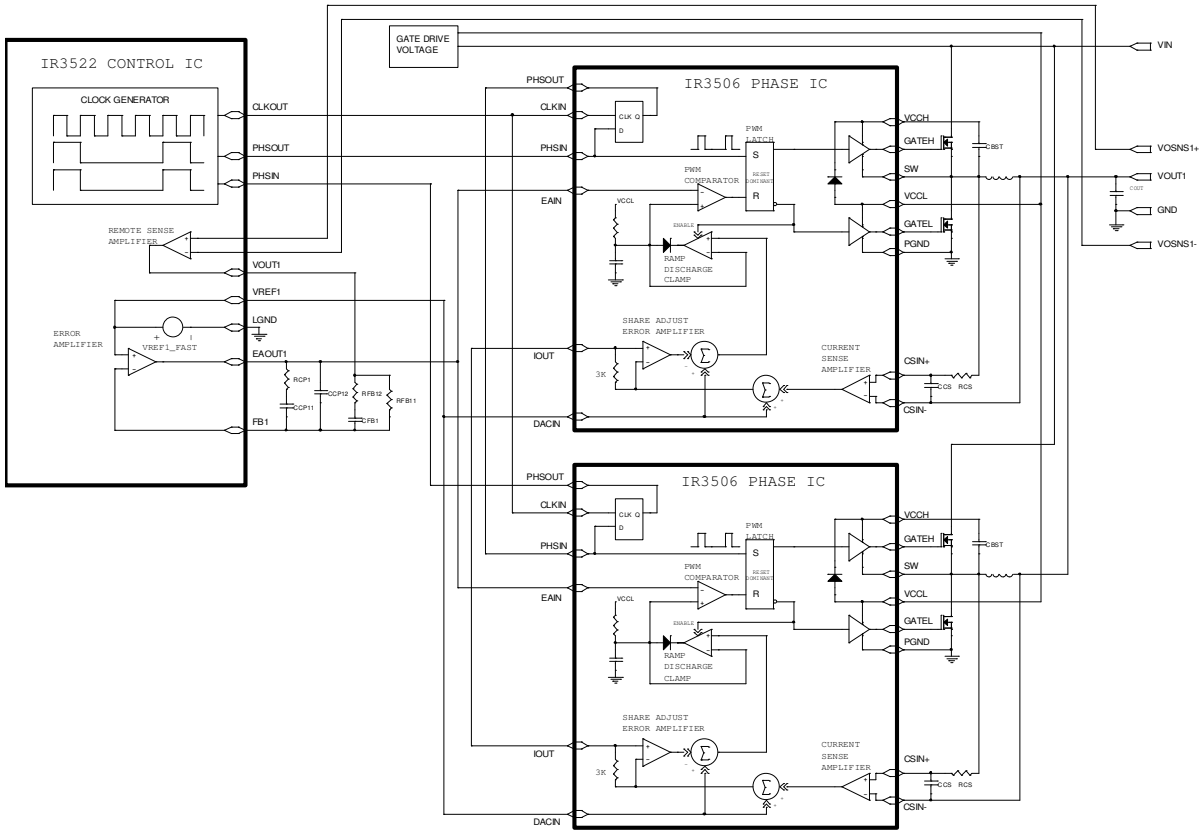


Figure 3 - PWM Block Diagram

Frequency and Phase Timing Control

The system oscillator is located in the Control IC and is programmable from 250 kHz to 9 MHZ by an external resistor. The control IC clock signal (CLKOUT) is connected to CLKIN of all the phase ICs. The phase timing of the phase ICs is controlled by a daisy chain loop. The control IC phase clock output (PHSOUT) is connected to the phase clock input (PHSIN) of the first phase IC, and PHSOUT of the first phase IC is connected to PHSIN of the second phase IC, etc. The last phase IC (PHSOUT) is connected back to PHSIN of the control IC to complete the loop. During power up, the control IC sends out clock signals from both CLKOUT and PHSOUT pins and detects the feedback at PHSIN pin to determine the phase number and monitor any fault in the daisy chain loop. Figure 4 shows the phase timing for a four phase converter.

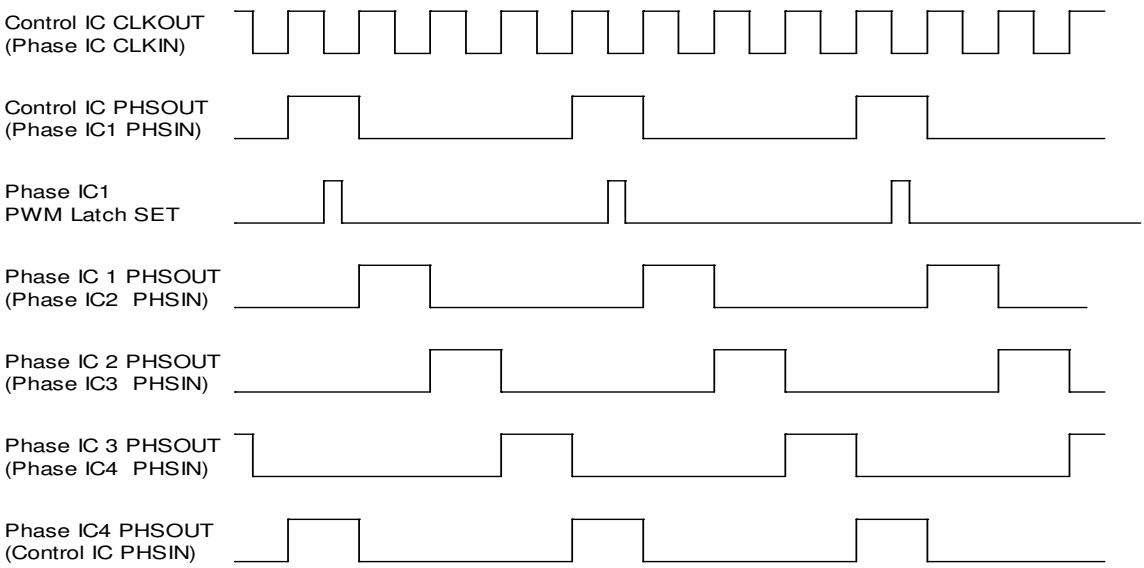


Figure 4 Four Phase Oscillator Waveforms

PWM Operation

The PWM comparator is located in the phase IC. Upon receiving a clock falling edge and PHSIN high, the PWM latch is set and the PWM ramp voltage begins to increase and turning off the low side driver The high side driver is then turned on once GATEL falls below 1.0V (non-overlap time). When the PWM ramp voltage exceeds the error amplifier's output voltage, the PWM latch is reset and the internal ramp capacitor is quickly discharged to the output voltage of share adjust amplifier. And, the ramp will remains discharged until the next clock pulse. This reset turns off the high side driver and enables the low side driver after the non-overlap time ((GATEH-SW) < 1.0V).

The PWM latch is reset dominant allowing all phases to go to zero duty cycle within a few tens of nanoseconds in response to a load step decrease. Phases can overlap and go up to 100% duty cycle in response to a load step increase with turn-on gated by the clock pulses. An error amplifier output voltage greater than the common mode input range of the PWM comparator results in 100% duty cycle regardless of the voltage of the PWM ramp. This arrangement guarantees the error amplifier is always in control and can demand 0 to 100% duty cycle as required. It also favors response to a load step decrease which is appropriate given the low output to input voltage ratio of most systems. The inductor current will increase much more rapidly than decrease in response to load transients.

This control method is designed to provide "single cycle transient response" where the inductor current changes in response to load transients within a single switching cycle maximizing the effectiveness of the power train and minimizing the output capacitor requirements. An additional advantage of this architecture is that differences in ground or input voltage at the phases have no effect on operation since the PWM ramps are referenced to VDAC.

Figure 5 depicts PWM operating waveforms under various conditions.

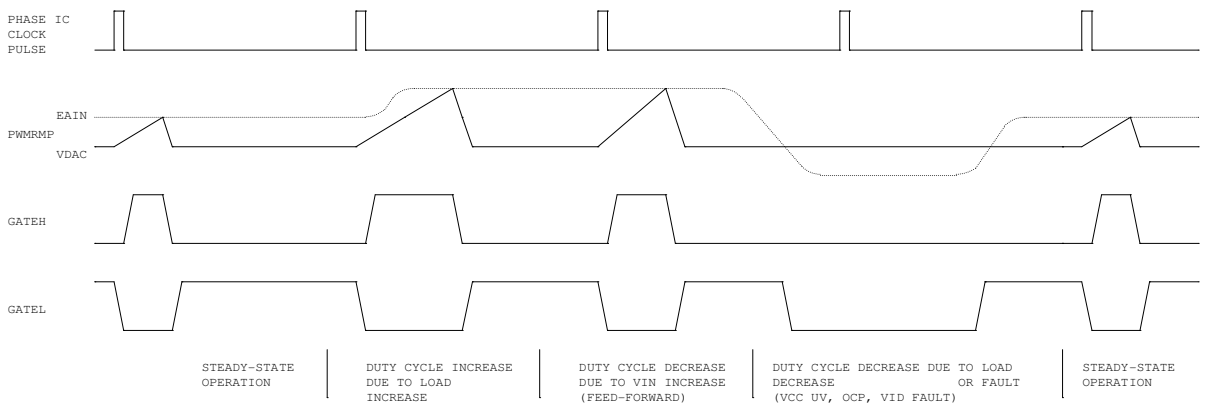


Figure 5 PWM Operating Waveforms

Lossless Average Inductor Current Sensing

Inductor current can be sensed by connecting a series RC network in parallel with the inductor and measuring the voltage across the capacitor, as shown in Figure 6. The equation of this sensing network is,

$$v_C(s) = v_L(s)\frac{1}{1+sR_{CS}C_{CS}} = i_L(s)R_L\frac{1+s(L/R_L)}{1+sR_{CS}C_{CS}}.$$

Usually, the resistor Rcs and capacitor Ccs are chosen so that the RC time constant equals the time constant of the inductor which is the inductance L divided by the inductor's DCR (RL). If the two time constants match, the voltage across Ccs is proportional to the current through L, and the sense circuit can be treated as if only a sense resistor with the value of RL was used. The mismatch of the time constants does not affect the measurement of inductor DC current, but affects the AC component of the inductor current.

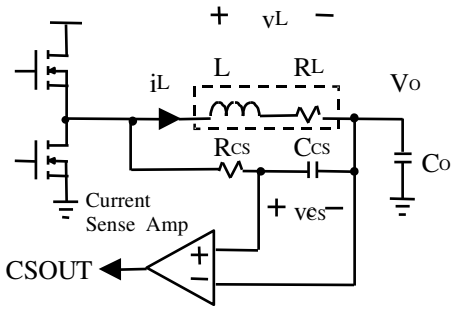


Figure 6 Inductor Current Sensing and Current Sense Amplifier

The advantage of sensing the inductor current versus high side or low side sensing is that actual output current being delivered to the load is obtained rather than peak or sampled information about the switch currents. The output voltage can be positioned to meet a load line based on real time information. Except for a sense resistor in series with the inductor, this is the only sense method that can support a single cycle transient response. Other methods provide no information during either load increase (low side sensing) or load decrease (high side sensing).

An additional problem associated with peak or valley current mode control for voltage positioning is that they suffer from peak-to-average errors. These errors will show in many ways but one example is the effect of frequency variation. If the frequency of a particular unit is 10% low, the peak to peak inductor current will be 10% larger and the output impedance of the converter will drop by about 10%. Variations in inductance, current sense amplifier bandwidth, PWM prop delay, any added slope compensation, input voltage, and output voltage are all additional sources of peak-to-average errors.

Current Sense Amplifier

A high speed differential current sense amplifier is located in the IR3506 phase IC, as shown in Figure 7. Its gain is nominally 32.5 at 25ºC, and the 3850 ppm/ºC increase in inductor DCR should be considered when setting the controller's current limit.

The current sense amplifier can accept positive differential input up to 50 mV and negative up to -10 mV before clipping. The output of the current sense amplifier is summed with the DAC voltage and sent to the control IC and other phases through an on-chip 3KΩ resistor connected to the ISHARE pin. The ISHARE pins of all the phases are tied together and the voltage on the share bus represents the average current through all the inductors and is used by the control IC for current limit protection.

Average Current Share Loop

Current sharing between phases of the converter is achieved by the average current share loop in each phase IC. The output of the current sense amplifier is compared with average current at the share bus. If a single phase current is smaller than the average current, the phase IC share adjust amplifier will pull down the starting point of the PWM ramp thereby increasing its duty cycle and output current. Conversely, a phase current larger than the average current will pull up the PWM starting point decreasing its duty cycle and output current. The current share amplifier is internally compensated so that the crossover frequency, of the current share loop, is much slower than that of the voltage loop and the two loops do not interact.

IR3522 THEORY OF OPERATION

Block Diagram

The Block diagram of the IR3522 is shown in Figure 7. The following discussions are applicable to either output plane unless otherwise specified.

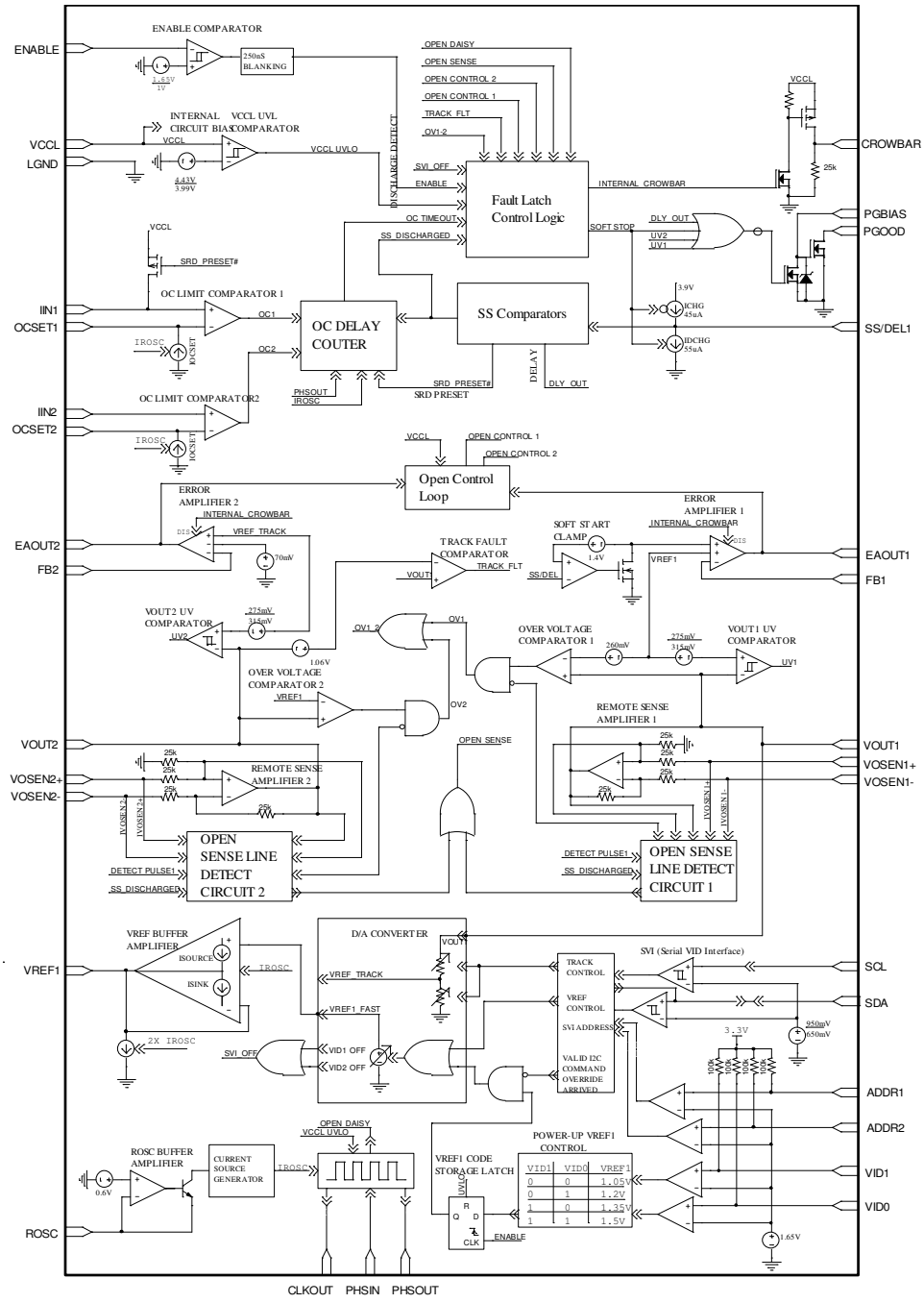


Figure 7 Block Diagram

Serial VID Control

The IR3522 outputs can be controlled via a serial VID Interface (SVID) which employs a Fast Mode I^2C protocol. VREF1, which is the reference for VOUT1, can also be programmed to boot-up to one of four codes through pins VID0 and VID1 prior to ENABLE rising if SVID communication is not available prior to power-up. Refer to Table 4. Pins VID0 and VID1 have internal 100K pull-up resistors to an internal 3.3V. The SVID controls both the VOUT1 and VOUT2 margining (see Table 2 or 3) depending on which serial address precedes the data string. See Table 1 for proper address codes. If the top address is used, then both outputs will coincide with the values in Table 2 depending on data code used, where VOUT2 is always half the value of VOUT1. The second address will only have an effect on VOUT2's amplitude (margining +26.67 % and -25 %) as defined in Table 3. Since there is no internal compensation for Vref_track (VOUT2 reference), **It is recommended that VOUT2 be incremented to its final value** to prevent possible output overshoot. If no serial command is received before an enable event (ENABLE pin going high), the controller's VOUT1 will startup in a default state as indicated in Table 4 and VOUT2 to 0.75 V (half of VDAC).

Addresses and data are serially transmitted in 8-bit words. The first data bit of the SVID data word represents the PSI_L bit and will be ignored by the IR3522 therefore this system will never enter a power-saving mode. The remaining data bits SVID[6:0] select the desired VOUTx regulation voltage as defined in Table 2 or Table 3 depending address chosen. VOUT1 is divided in half by an internal resistor divider to provide a reference voltage (Vref_track) for VOUT2. This allows VOUT2 to track VOUT1 maintaining a desired differential voltage. SVID [6:0] are the inputs to the Digital-to-Analog Converter (VREF) which then provides an analog reference voltage to the transconductance type buffer amplifier. This VREF buffer provides a system reference on the VREF1 pin. The VREF1 voltage along with error amplifier and remote sense differential amplifier input offsets are post-package trimmed to provide a 0.5% system set-point accuracy, as measured in Figures 2A and 2B. VREF1 slew rates are programmable by properly selecting external series RC compensation networks located between the VREF1 and the LGND pins. The VREF1 source and sink currents are derived off the external oscillator frequency setting resistor, R_{ROSC}. The programmable slew rate enables the IR3522 to smoothly transition the regulated output voltage throughout VID transitions resulting in a power supply input and output capacitor inrush currents, along with output voltage overshoot, to be well controlled.

The ADDR1 and ADDR2 pins (5, 6) are reserved for controller addressing. These pins have internal 100K pull-up resistors to an internal 3.3V. By floating or shorting to ground these two pins, four different controller identification address states can be made. By setting bit 2 and 3 of the SVI address codes (see Figure 8) to the desired controller address, a CPU can communicate with one controller while ignoring other controllers sharing the same SVID bus.

SVI Address [6:0] + Wr

6	5	4	ADDR1	ADDR2	1	0	WR

Figure 8 Bit 2 and 3 are use for Controller addressing

The SCL and SDA pins require external pull-up biasing and should not be floated. Biasing of pins SDA, SCL, VID0, VID1, ADDR1 and ADDR2 prior to applying VCCL is acceptable. For Write, WR=0.

SVI Address	
SVI Address [6:0] + Wr	**Description**
[bit6 :bit5 : bit4 : ADDR1 _ ADDR2 : bit1 : bit0 : WR]	
110**1**_**1**100 in binary or D_C in hex if ADDR1 and ADDR2 pins are high	Set VID only Output 1
110**1**_**1**010 in binary or D_A in hex if ADDR1 and ADDR2 pins are high	Set VID only Output 2
BOLD indicates the pin states of ADDR1 and ADDR2, in this case high or floating.	

Table 1 – SVI Address

VDDR (VREF1) SVID Codes and Resulting VTT Default (50%) Voltage			
Hex	**VDDR SVID Codes**	**VDDR, VREF1, VOUT1 Typical Target**	**VOUT2**
00	X000_0000	1.6125	0.80625
01	X000_0001	1.6	0.8
02	X000_0010	1.5875	0.79375
03	X000_0011	1.575	0.7875
04	X000_0100	1.5625	0.78125
05	X000_0101	1.55	0.775
06	X000_0110	1.5375	0.76875
07	X000_0111	1.525	0.7625
08	X000_1000	1.5125	0.75625
09	X000_1001	1.5	0.75
0A	X000_1010	1.4875	0.74375
0B	X000_1011	1.475	0.7375
0C	X000_1100	1.4625	0.73125
0D	X000_1101	1.45	0.725
0E	X000_1110	1.4375	0.71875
0F	X000_1111	1.425	0.7125
10	X001_0000	1.4125	0.70625
11	X001_0001	1.4	0.7
12	X001_0010	1.3875	0.69375
13	X001_0011	1.375	0.6875
14	X001_0100	1.3625	0.68125
15	X001_0101	1.35	0.675
16	X001_0110	1.3375	0.66875
17	X001_0111	1.325	0.6625
18	X001_1000	1.3125	0.65625
19	X001_1001	1.3	0.65
1A	X001_1010	1.2875	0.64375
1B	X001_1011	1.275	0.6375
1C	X001_1100	1.2625	0.63125
1D	X001_1101	1.25	0.625
1E	X001_1110	1.2375	0.61875
1F	X001_1111	1.225	0.6125
20	X010_0000	1.2125	0.60625
21	X010_0001	1.2	0.6
22	X010_0010	1.1875	0.59375
23	X010_0011	1.175	0.5875
24	X010_0100	1.1625	0.58125
25	X010_0101	1.15	0.575
26	X010_0110	1.1375	0.56875
27	X010_0111	1.125	0.5625
28	X010_1000	1.1125	0.55625
29	X010_1001	1.1	0.55
2A	X010_1010	1.0875	0.54375
2B	X010_1011	1.075	0.5375
2C	X010_1100	1.0625	0.53125
2D	X010_1101	1.05	0.525
2E	X010_1110	1.0375	0.51875
2F	X010_1111	1.025	0.5125
	x1xx_xxxx	VID OFF, no change in VREF or VTT	

Table 2: VDDR Margin Codes and resulting 50% Vtt Tracking
(VIDX pin controlled codes are in Gray)

VTT Margining Range Codes			
Hex	**VTT SVID Codes**	**% Change from Default**	**% Change from VOUT1**
0	x000_0000	26.67	63.16
1	x000_0001	25	62.35
2	x000_0010	23.33	61.52
3	x000_0011	21.67	60.70
4	x000_0100	20	59.87
5	x000_0101	18.33	59.06
6	x000_0110	16.67	58.23
7	x000_0111	15	57.40
8	x000_1000	13.33	56.59
9	x000_1001	11.67	55.78
0A	x000_1010	10	54.94
0B	x000_1011	8.33	54.12
0C	x000_1100	6.67	53.28
0D	x000_1101	5	52.46
0E	x000_1110	3.33	51.64
0F	x000_1111	1.67	50.82
10	x001_0000	0	50
11	x001_0001	-1.67	49.16
12	x001_0010	-3.33	48.31
13	x001_0011	-5	47.46
14	x001_0100	-6.67	46.61
15	x001_0101	-8.33	45.78
16	x001_0110	-10	44.93
17	x001_0111	-11.67	44.08
18	x001_1000	-13.33	43.25
19	x001_1001	-15	42.42
1A	x001_1010	-16.67	41.58
1B	x001_1011	-18.33	40.74
1C	x001_1100	-20	39.90
1D	x001_1101	-21.67	39.08
1E	x001_1110	-23.33	38.21
1F	x001_1111	-25	37.44
	x1xx_xxxx	VID OFF	VID OFF

Table 3 – Vtt Margining (Default in Gray)

Pre-ENABLE VREF1 Codes		
VID1	VID0	VDDR
0	0	1.05
0	1	1.2
1	0	1.35
1	1	1.5

Table 4 – Pre-Enable VDDR program Codes

Response	Open Daisy	Open Sense	Open Control	Tracking Fault	UVLO (VCCL)	OC	Over Voltage	Disable	VID_OFF SVID	UVLO (Vout)
Latch	UVLO CLEARED Latch			ENABLE CLEARED Latch				SS Latch		No
Reset	Recycle VCCL			Recycle EN or Cycle VID_OFF through SVID				SS discharge below 0.22V		No
Outputs Affected	Both									none
Disables EA	Yes							No		No
Soft Stop	No							Yes		No
CROWBAR	Yes							No		
Flags PGood	Yes									
Delays	32 Clock Pulses	No	8 PHSOUT Pulses	No	No	Delay Counter	No	250ns Blanking Time	No	No
Additional Flagged Response	Yes, IIN1 pin is pulled-up to VCCL when SS discharge below 0.35V. This action latches on the Phase IC(s) Diode Emulation Mode which insure proper current sharing during soft start**.									No

*Pulse number range depends on Rosc value selected (See Specifications Table)
** IIN1 is pulled low when SS charges above 0.4V.

Table 5 – IR3522 Fault protocol

.

Serial VID Interface Protocol and VID-on-the-fly Transition

The IR3522 supports the SVI bus protocol which is based on Fast-mode I^2C. SVID commands from a processor are communicated through SVID bus pins SCL and SDA.

The SMBus *send byte* protocol is used by the IR3522 VID-on-the-fly transactions. The IR3522 will wait until it detects a start bit which is defined as an SDA falling edge while SCL is high. A 7bit address code plus one write bit (low) should then follow the start bit. This address code will be compared against an internal address table and the IR3522 will reply with an acknowledge ACK bit if the address is one of the two stored addresses otherwise the ACK bit will not be sent out. The SDA pin is pulled low by the IR3522 to generate the ACK bit. Table 1 has the list of addresses recognized by the IR3522.

The processor should then transmit the 8-bit data word immediately following the ACK bit. The first bit is ignored (bit 7). The IR3522 replies again with an ACK bit once the data is received. If the received data is not a VID-OFF command, the IR3522 immediately changes the VREF1 analog outputs to the new target. VOUT1 and VOUT2 then slew to the new VID voltages. See Figure 9 for a send byte example.

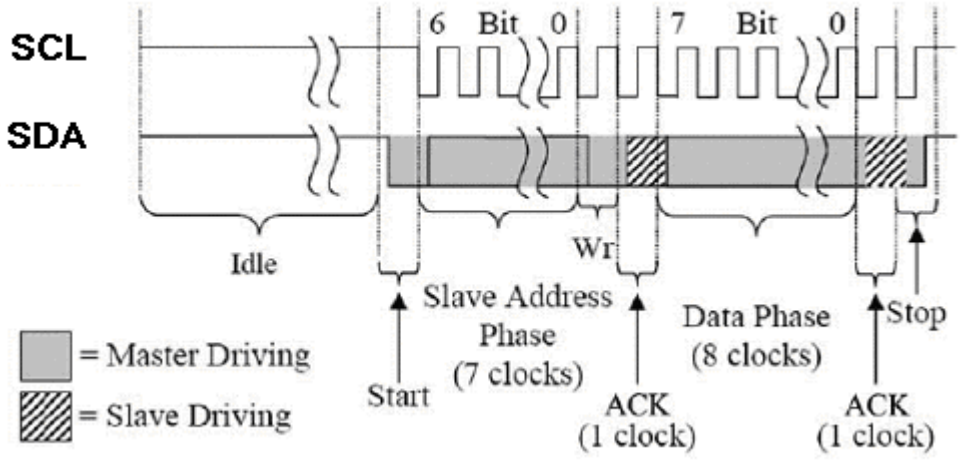


Figure 9 Send Byte Example

Remote Voltage Sensing

$VOSEN_X+$ and $VOSEN_X-$ are used for remote sensing and are connected directly to the load. The remote sense differential amplifiers are high speed, have low input offset and low input bias currents to ensure accurate voltage sensing and fast transient response.

Start-up Sequence

The IR3522 is designed as a chipset with the IR3506 Phase IC to achieve output voltage tracking. VOUT2's internal reference (VREF_TRACK) is generated by a divided-by-half internal resistor divider. This will ensure VOUT2 remains half the value of VOUT1 preventing possible damage to some DDR system's microprocessors. In addition, a track-fault comparator is implemented to monitor both outputs which will further guarantee the outputs remain at least 1.0 V apart and will generate a fault if this limit is surpassed, further protecting the DDR system.

When VCCL is applied to the IC and the SS/DEL is below 0.3V, IIN1 (only) is pulled up to VCCL through an internal PFET enabling a diode emulation preset latch on the IR3506 phase IC. Diode emulation mode ensures proper current sharing during system soft-start by turning off the bottom sync FET when negative inductor current is sensed via the CSIN- and CSIN+ pins. The IIN1 pin is release once SS/DEL charges above 0.3 V. Once VOUT1 reaches 75% of its final operating value, the diode emulation mode is reset allowing the phase ICs to sink current.

The IR3522 has a programmable soft-start and soft-stop function. The soft-start helps limit the surge current during the converter start-up, whereas the soft-stop is needed to maintain output tracking during system turn-off. A capacitor connected between the SS/DEL and LGND pins controls timing. A constant source and sink current control the charge and discharge rates of the SS/DEL.

Figure 10 depicts the SVID start-up sequence. When the ENABLE input is asserted and there are no faults, the SS/DEL pin will begin charging. If the IC receives a SVID communication prior to the ENABLE pin going high, the output ramps up to the program value listed in Table 2, otherwise the VOUT1 and VOUT2 default to 1.5 V and 0.75 V, respectively. The error amplifier output, $EAOUT_x$, is clamped low until SS/DEL reaches 1.4V. The error amplifier will then regulate the converter's output voltage to match the V(SS/DEL)-1.4V offset until the converter output reaches the SVID code or default state. The SS/DEL voltage continues to increase until it rises above the threshold of Delay Comparator where the PGOOD output is allowed to go high.

A low signal on the ENABLE or VID_OFF input immediately sets the fault latch, which causes the EAOUT pin to drive low, thereby turning off the phase IC drivers. The PGOOD pin also drives low and SS/DEL discharges to 0.2V. If the fault has cleared, the fault latch will be reset by the SS/DEL discharge comparator allowing another soft start charge cycle to occur.

All other faults (See Table 5) will set a different fault latch that can only be reset by cycling ENABLE or the VID_OFF SVID command. These faults discharge SS/DEL, pull down $EAOUT_X$, pull up CROWBAR to VCCLDRV and drive PGOOD low. The CROWBAR circuit is design to drive an external NMOS device to pull the output voltage to ground. This feature minimizes negative voltage undershoots at the output by reducing sync FET current during fault events.

The converter can be disabled by pulling the SS/DEL pins below 0.6V

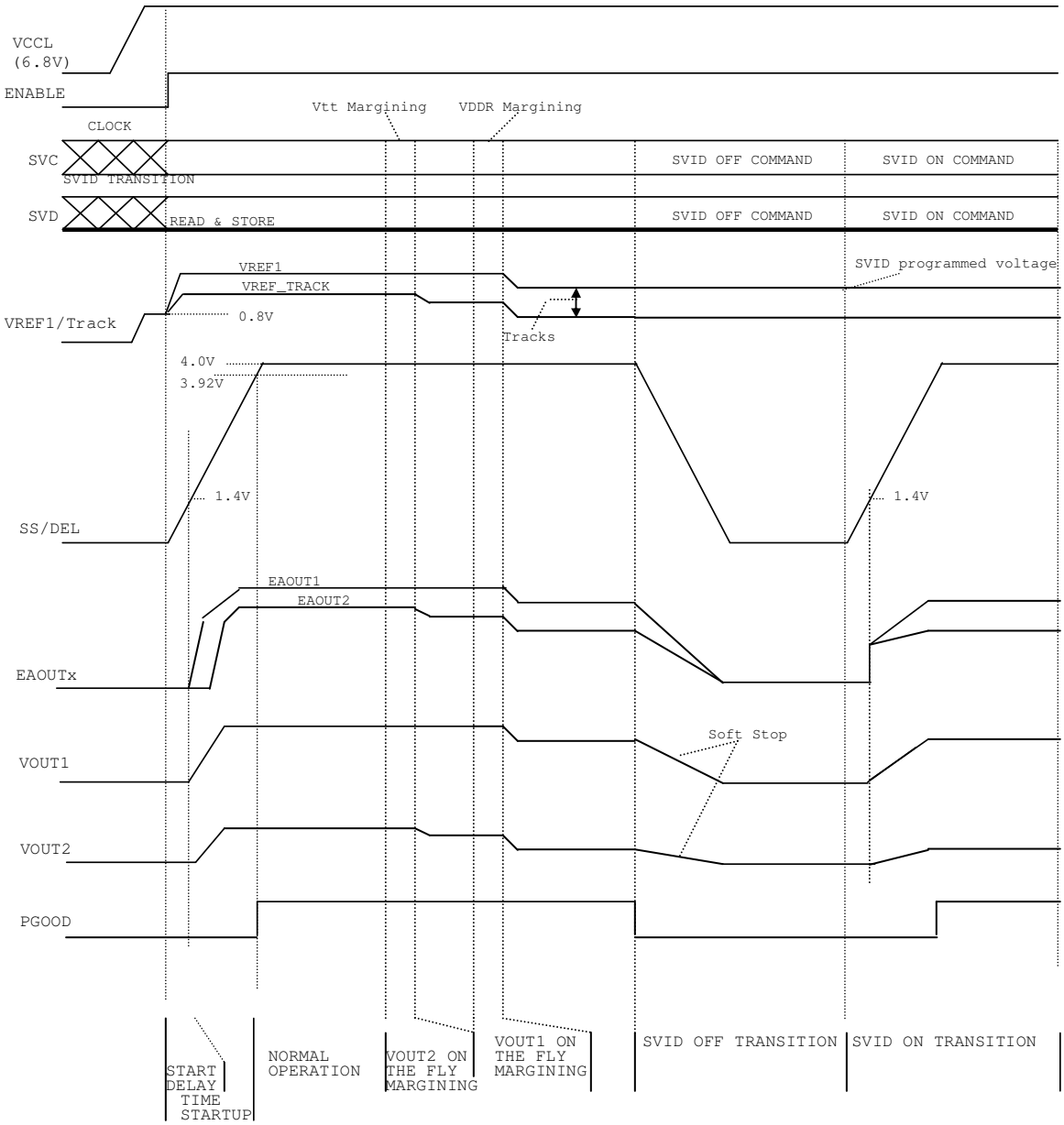


Figure 10 SVID Start-up Sequence Transitions

Over-Current Protection

The over current limit threshold is set by a resistor connected between $OCSET_X$ and VREF1 pin. An over current fault is flagged after a delay programmed by Rocs (see Electrical Specification). The delay is required since over-current conditions can occur as part of normal operation due to load transients or VID transitions.

If the IIN_X pin voltage, which is proportional to the average current plus VREF1 voltage, exceeds the OCSETx voltage, the OCDELAY counter starts counting the PHSOUT pulses. If the over-current condition persists long enough for the counter to reach the program number, the fault latch will be set which will then pull the error amplifier's output low to stop phase IC switching and will also de-assert the PGOOD signal. The SS/DEL capacitor will then discharge by a 55 uA current. The output current is not controlled during the delay time. This latch can only reset by either recycling the ENABLE pin or VID_OFF command.

VCCL Under Voltage Lockout (UVLO)

The IR3522 monitors the VCCL supply voltage to determine if the amplitude is proper to adequately drive the top and bottom gates. As VCCL begins to rise during power up, the IC is allowed to power up when VCCL reaches 4.43 V (Typical). The ENABLE CLEARED fault latches will be released. If VCCL voltage drops below 3.99V (Typical) of the set value, the ENABLE CLEARED fault latch will be set.

VID OFF Codes

SVID OFF codes will turn off the converter keeping the error amplifiers active and discharging SS/DEL through the 50uA discharge current allowing the outputs to discharge in a control manner (soft-stop). Upon receipt of a non-off SVID code the converter will turn on and transition to the voltage represented by the SVID as shown in Figure 10.

Power Good (PGOOD)

The PGOOD pin is an open-drain output and should have an external pull-up resistor. During soft start, PGOOD remains low until the output voltage is in regulation and SS/DEL is above 3.9V. The PGOOD pin becomes low if any fault is registered (see TABLE 5 for details). A high level at the PGOOD pin indicates that the converter is in operation with no fault and ensures the output voltage is within regulation.

PGOOD monitors the output voltage. If any of the voltage planes fall out of regulation, PGOOD will become low, but the VR continues to regulate its output voltages. Output voltage out-of-spec is defined as 315mV to 275mV below nominal voltage. VID on-the-fly transition which is a voltage plane transitioning between one voltage associated with one VID code and a voltage associated with another VID code is not considered to be out of specification.

Open Voltage Loop Detection

The output voltage range of error amplifier is continuously monitored to ensure the voltage loop is in regulation. If any fault condition forces the error amplifier output above VCCL-1.08V for 8 PHSOUT switching cycles, the fault latch is set. The fault latch can only be cleared by cycling the ENABLE or the VID_OFF command.

Enable Input

Pulling the ENABLE pin below 0.8V sets the Fault Latch. Forcing ENABLE to a voltage above 1.65V allows the SS/DEL pin to begin a power-up cycle.

Over Voltage Protection (OVP)

Output over-voltage might occur due to a high side MOSFET short or if the output voltage sense path is compromised. If the over-voltage protection comparators sense that either VOUT1 pin voltage exceeds VREF1 by 260mV or VOUT2 exceeds VREF1, the over voltage fault latch is set which pulls the error amplifier output low to turn off the converter power stage. The IR3522 communicates an OVP condition to the system by raising the CROWBAR pin voltage to within V(VCCL) – 0.2 V. With the error amplifiers outputs low, the low-side MOSFET

turn-on within approximately 150ns. The low side MOSFET will remain low until the over voltage fault condition latch cleared. This latch is cleared by cycling the ENABLE pin or the VID_OFF command.

The overall system must be considered when designing for OVP. In many cases the over-current protection of the AC-DC or DC-DC converter supplying the multiphase converter will be triggered thus providing effective protection without damage as long as all PCB traces and components are sized to handle the worst-case maximum current. If this is not possible, a fuse can be added in the input supply to the multiphase converter.

Open Remote Sense Line Protection

If either remote sense line $VOSEN_X+$ or $VOSEN_X-$ is open, the output of Remote Sense Amplifier ($VOUT_X$) drops. The IR3522 continuously monitors the $VOUT_X$ pin and if $VOUT_X$ is lower than 200 mV, two separate pulse currents are applied to the $VOSEN_X+$ and $VOSEN_X-$ pins to check if the sense lines are open. If $VOSEN_X+$ is open, a voltage higher than 90% of V(VCCL) will be present at $VOSEN_X+$ pin and the output of Open Line Detect Comparator will be high. If $VOSEN_X-$ is open, a voltage higher than 400mV will be present at $VOSEN_X-$ pin and the Open Line Detect Comparator output will be high. With either sense line open, the Open Sense Line Fault Latch will be set to force the error amplifier output low and immediately shut down the converter. SS/DEL will be discharged and the Open Sense Fault Latch can only be reset by cycling the ENABLE pin or the VID_OFF command.

Open Daisy Chain Protection

The IR3522 checks the daisy chain every time it powers up. It starts a daisy chain pulse on the PHSOUT pin and detects the feedback at PHSIN pin. If no pulse comes back after 30 CLKOUT pulses, the pulse is restarted again. If the pulse fails to come back the second time, the Open Daisy Chain fault is registered, and SS/DEL_X is not allowed to charge. The fault latch can only be reset by cycling the ENABLE pin or the VID_OFF command.

After powering up, the IR3522 monitors PHSIN pin for a phase input pulse equal or less than the number of phases detected. If PHSIN pulse does not return within the number of phases in the converter, another pulse is started on PHSOUT pin. If the second started PHSOUT pulse does not return on PHSIN, an Open Daisy Chain fault is registered.

Phase Number Determination

After a daisy chain pulse is started, the IR3522 checks the timing of the input pulse at PHSIN pin to determine the phase number.

DESIGN PROCEDURES - IR3522 AND IR3506 CHIPSET

IR3522 EXTERNAL COMPONENTS

All the output components are selected using one output but suitable for both unless otherwise specified.

Oscillator Resistor *RROSC*

The only one oscillator of IR3522 generates square-wave pulses to synchronize the phase ICs. The switching frequency of the each phase converter equals the PHSOUT frequency, which is set by the external resistor RROSC, use Figure 11 to determine the RROSC value. The CLKOUT frequency equals the switching frequency multiplied by the phase number.

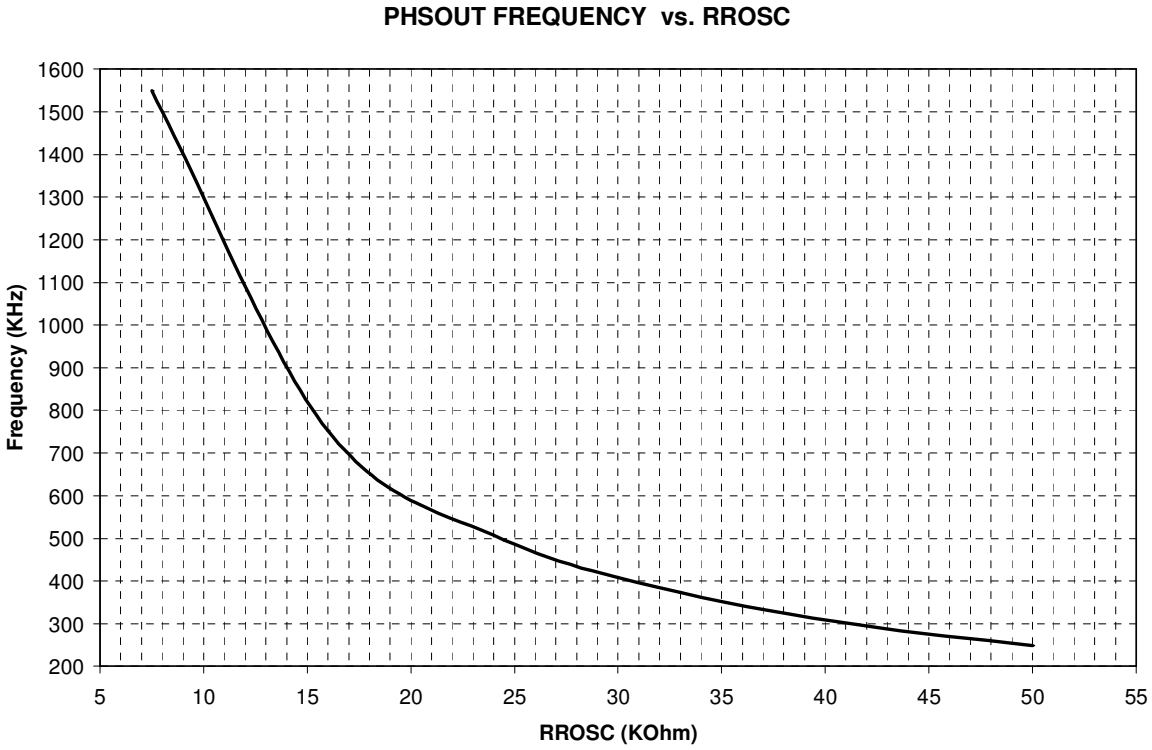


Figure 11 - PHSOUT Frequency vs. RROSC chart

Soft Start Capacitor *CSS/DEL*

The Soft Start capacitor CSS/DEL programs three different time parameters, soft start delay time, soft start time, and soft stop time.

SS/DEL pin voltage controls the slew rate of the converter output voltage, as shown in Figure 10. Once the ENABLE pin rises above 1.65V, there is a soft-start delay time TD1 during which SS/DEL pin is charged from zero to 1.4V. Once SS/DEL reaches 1.4V the error amplifier output is released to allow the soft start. The soft start time TD2 represents the time during which converter voltage rises from zero to SVID voltage (or default voltage) and the SS/DEL pin voltage rises from 1.4V to SVID voltage plus 1.4V. Power good time, TD3, is the time period from VR reaching the SVID voltage to the PGOOD signal being issued.

Calculate CSS/DEL based on the required soft start time TD2.

$$C_{SS/DEL} = \frac{TD2 * I_{CHG}}{SVID} = \frac{TD2 * 45 * 10^{-6}}{SVID} \quad (1)$$

The soft start delay time TD1, power good time TD3, and soft stop time are determined by equation (2), (3) and (4) respectively.

$$TD1 = \frac{C_{SS/DEL} * 1.4}{I_{CHG}} = \frac{C_{SS/DEL} * 1.4}{45 * 10^{-6}} \quad (2)$$

$$TD3 = \frac{C_{SS/DEL} * (3.92 - SVIC - 1.4)}{I_{CHG}} = \frac{C_{SS/DEL} * (3.92 - SVID - 1.4)}{45 * 10^{-6}} \quad (3)$$

$$TD4 = \frac{C_{SS/DEL} * SVIS}{I_{CHG}} = \frac{C_{SS/DEL} * SVID}{55 * 10^{-6}} \quad (4)$$

VDAC Slew Rate Programming Capacitor *CVDAC* and Resistor *RVDAC*

The slew rate of VREF1 down-slope SRDOWN can be programmed by the external capacitor CVDAC as defined in (5), where ISINK is the sink current of VREF1 pin. The resistor RVDAC is used to compensate VDAC circuit and is determined by (6)

$$C_{VDAC} = \frac{I_{SINK}}{SR_{DOWN}} \quad (5)$$

$$R_{VDAC} = 0.5 + \frac{3.2 * 10^{-15}}{C_{VDAC}^{\ 2}} \quad (6)$$

Over Current Setting Resistor *ROCSET*

The total input offset voltage (VCS_TOFST) of current sense amplifier in phase ICs is the sum of input offset (VCS_OFST) of the amplifier itself and that created by the amplifier input bias current flowing through the current sense resistor RCS.

$$V_{CS\_TOFST} = V_{CS\_OFST} + I_{CSIN+} * R_{CS} \quad (7)$$

The inductor DC resistance is utilized to sense the inductor current. RL is the inductor DCR.

The over-current limit is set by the external resistor, ROCSET, as defined in (9). ILIMIT is the required over current limit. IOCSET is the bias current of OCSET pin and can be calculated with the equation in the ELECTRICAL CHARACTERISTICS Table. GCS is the gain of the current sense amplifier of the IR3506 phase IC. KP is the ratio of inductor peak current over average current in each phase and can be calculated from (10).

$$R_{OCSET} = [\frac{I_{LIMIT}}{n} * R_L * (1 + K_P) + V_{CS\_TOFST}] * G_{CS} / I_{OCSET} \quad (9)$$

$$K_P = \frac{(V_I - V_O) * V_O / (L * V_I * f_{SW} * 2)}{I_O / n} \quad (10)$$

IR3506 EXTERNAL COMPONENTS

Inductor Current Sensing Capacitor *Ccs* and Resistor *Rcs*

The DC resistance of the inductor is utilized to sense the inductor current. Usually the resistor Rcs and capacitor Ccs in parallel with the inductor are chosen to match the time constant of the inductor, and therefore the voltage across the capacitor Ccs represents the inductor current. If the two time constants are not the same, the AC component of the capacitor voltage is different from that of the real inductor current. The time constant mismatch does not affect the average current sharing among the multiple phases, but affect the current signal ISHARE as well as the output voltage during the load current transient if adaptive voltage positioning is adopted.

Measure the inductance L and the inductor DC resistance RL. Pre-select the capacitor Ccs and calculate Rcs as follows.

$$R_{CS} = \frac{L/R_L}{C_{CS}} \quad (11)$$

Bootstrap Capacitor *CBST*

Depending on the duty cycle and gate drive current of the phase IC, a capacitor in the range of 0.1uF to 1uF is needed for the bootstrap circuit.

Decoupling Capacitors for Phase IC

0.1uF-1uF decoupling capacitors are required at VCC and VCCL pins of phase ICs.

Type III Compensation

Choose the crossover frequency fc between 1/10 and 1/5 of the switching frequency per phase, the desired phase margin θc and Rfb1 (see Figure 12). Determine the component values based on the equations below. wc is 2*π*fc (the crossover angular frequency), Le is the equivalent inductance of the converter, C is the output capacitance, Rst is the total equivalent resistance in series with the inductor, Rc is the output capacitance ESR and R is the load resistance.

$$Ccp = \frac{1}{K \cdot Rfb1} \quad (12)$$

$$Rcp = \frac{1}{Ccp \cdot wz1} \quad (13)$$

$$Cfb = \frac{1}{wz2 \cdot Rfb1} \quad (14)$$

$$Ccp1 = \frac{1}{wp2 \cdot Rcp} \quad (15)$$

$$Rfb2 = \frac{1}{wp1 \cdot Cfb} \quad (16)$$

where,

$$wz1 = \frac{wc}{10} \quad (17)$$

$$wz2 = wc \cdot \sqrt{\frac{1-\sin(\theta c)}{1+\sin(\theta c)}} \quad (18)$$

$$wp1 = wc \cdot \sqrt{\frac{1+\sin(\theta c)}{1-\sin(\theta c)}} \quad (19)$$

$$wp2 = 1.4 \cdot wp1 \quad (20)$$

$$K = \frac{(wc^4 \cdot t_4^2 + wc^2 \cdot t_2^2)((1 - b \cdot wc^2)^2 + a^2 \cdot wc^2)(R + Rst)}{Gpwm \cdot H \cdot t_5 \cdot t_6 \cdot R} \quad (21)$$

where, Gpwm is the gain of the PWM generator, H is the gain of the feedback filter and

$$a = \frac{Le + C(R \cdot Rst + R \cdot Rc + Rst \cdot Rc)}{R + Rst} \quad (22)$$

$$b = Le \cdot C \frac{R + Rc}{R + Rst} \quad (23)$$

$$t_1 = 1 - \frac{wc^2}{wz1 \cdot wz2} \quad (24)$$

$$t_2 = 1 - \frac{wc^2}{wp1 \cdot wp2} \quad (25)$$

$$t_3 = \frac{1}{wz1} + \frac{1}{wz2} \quad (26)$$

$$t_4 = \frac{1}{wp1} + \frac{1}{wp2} \quad (27)$$

$$t_5 = \sqrt{(1 - b \cdot wc^2 + wc^2 \cdot Rc \cdot C \cdot a)^2 + wc^2 (Rc \cdot C(1 - b \cdot wc^2) - a)^2} \quad (28)$$

$$t_6 = \sqrt{wc^4 (t_2 \cdot t_3 - t_1 \cdot t_4)^2 + wc^2 (t_1 \cdot t_2 + wc^2 \cdot t_3 \cdot t_4)^2} \quad (29)$$

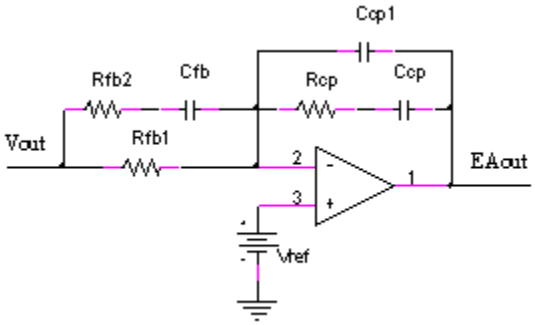


Figure 12 Voltage Loop Compensation Network

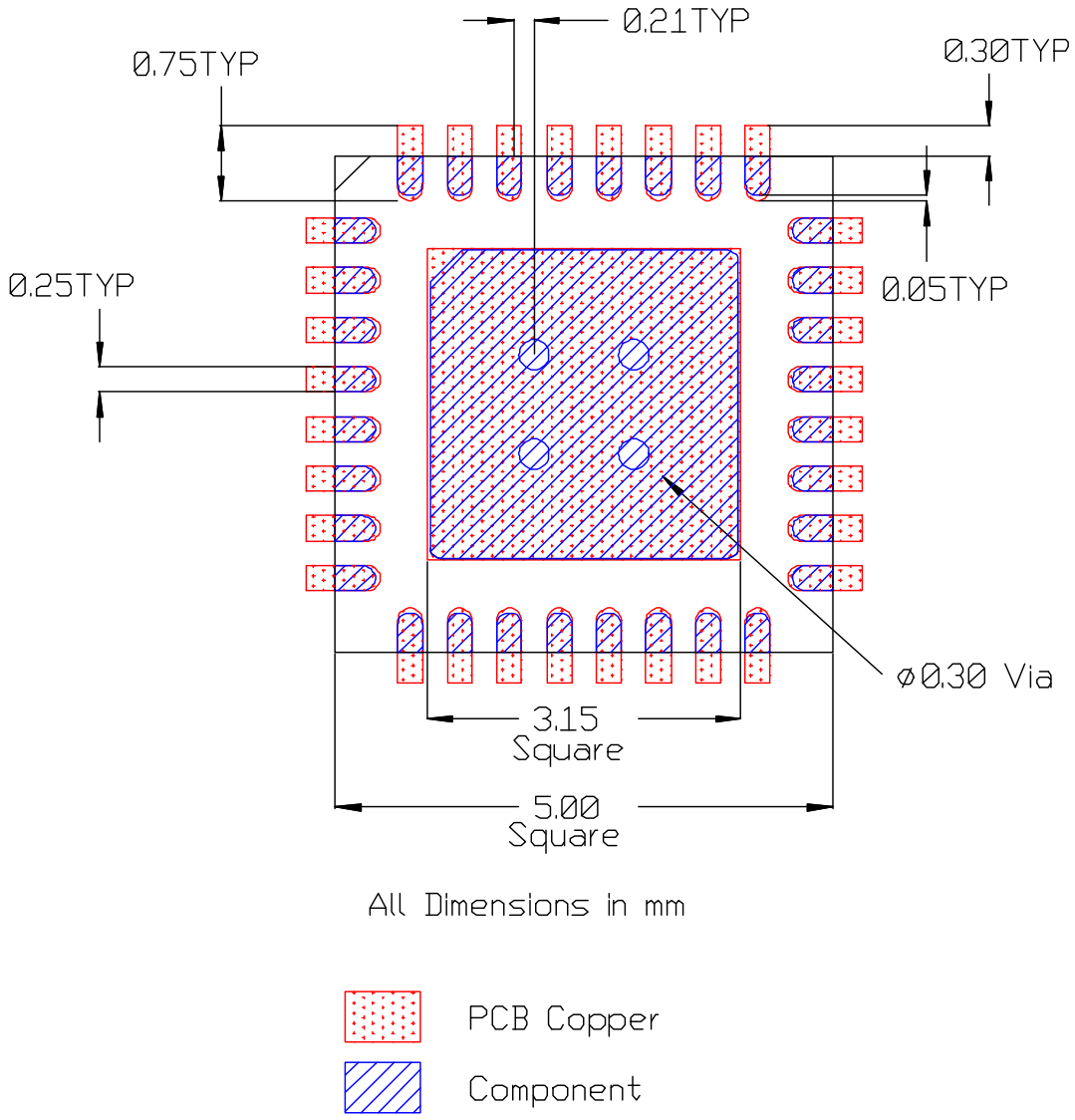
LAYOUT GUIDELINES

The following layout guidelines are recommended to reduce the parasitic inductance and resistance of the PCB layout, therefore minimizing the noise coupled to the IC.

- Dedicate at least one middle layer for a ground plane LGND.
- Connect the ground tab under the control IC to LGND plane through a via.
- Separate analog bus (EAIN, DACIN and ISHARE) from digital bus (CLKIN, PHSIN, and PHSOUT) to reduce the noise coupling.
- Place VCCL decoupling capacitor VCCL as close as possible to VCCL and LGND pins.
- Place the following critical components on the same layer as control IC and position them as close as possible to the respective pins, ROSC, ROCSET, RVDAC, CVDAC, and CSS/DEL. Avoid using any via for the connection.
- Place the compensation components on the same layer as control IC and position them as close as possible to EAOUT, FB, VO and VDRP pins. Avoid using any via for the connection.
- Use Kelvin connections for the remote voltage sense signals, VOSNS+ and VOSNS-, and avoid crossing over the fast transition nodes, i.e. switching nodes, gate drive signals and bootstrap nodes.
- Avoid analog control bus signals, VDAC, IIN, and especially EAOUT, crossing over the fast transition nodes.
- Separate digital bus, CLKOUT, PHSOUT and PHSIN from the analog control bus and other compensation components.

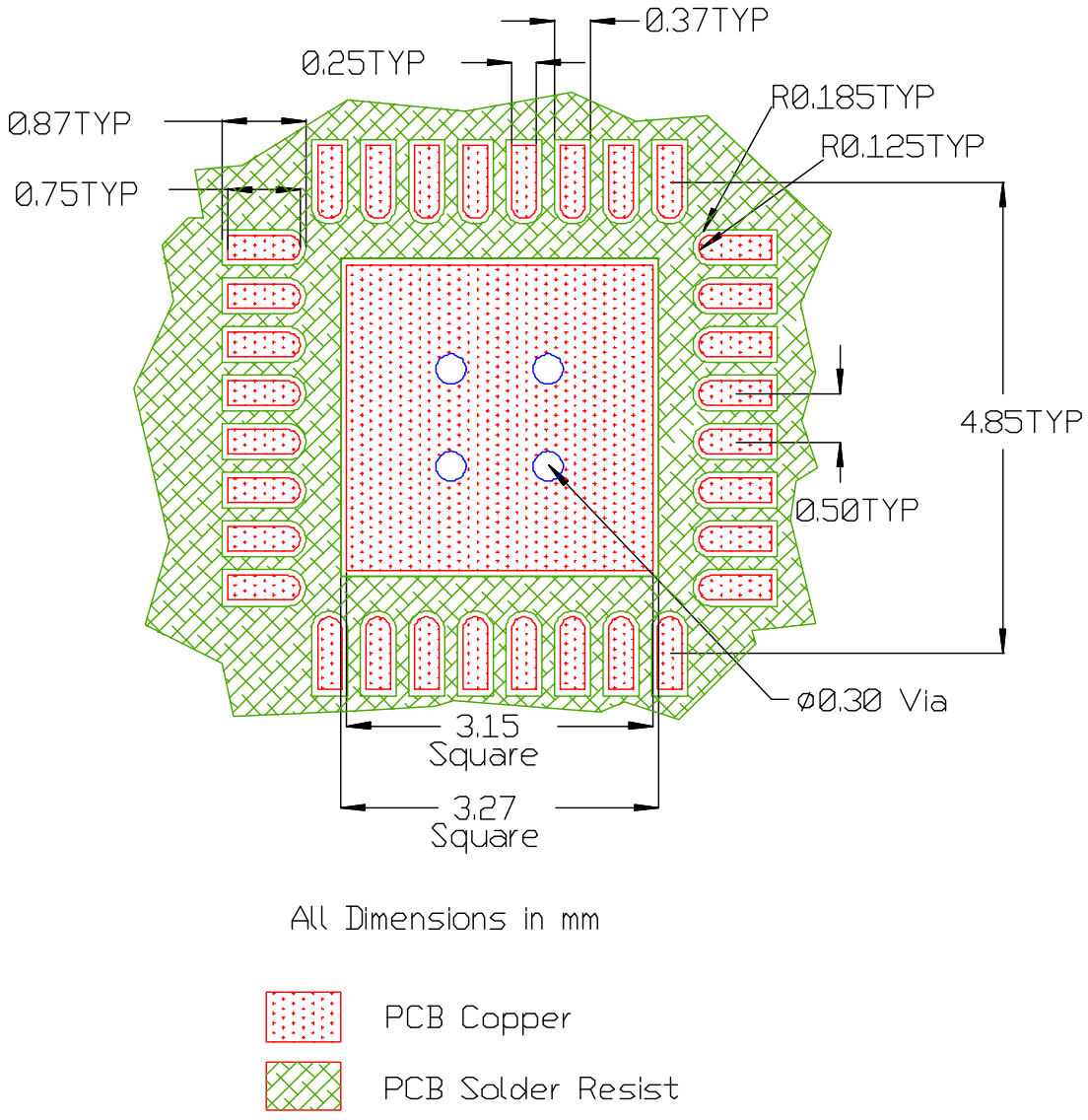
PCB METAL AND COMPONENT PLACEMENT

- Lead land width should be equal to nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to prevent shorting.
- Lead land length should be equal to maximum part lead length + 0.3 mm outboard extension + 0.05mm inboard extension. The outboard extension ensures a large and inspectable toe fillet, and the inboard extension will accommodate any part misalignment and ensure a fillet.
- Center pad land length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be ≥ 0.17mm for 2 oz. Copper (≥ 0.1mm for 1 oz. Copper and ≥ 0.23mm for 3 oz. Copper)
- A single 0.30mm diameter via shall be placed in the center of the pad land and connected to ground to minimize the noise effect on the IC.
- No pcb traces should be routed nor vias placed under any of the 4 corners of the IC package. Doing so can cause the IC to rise up from the pcb resulting in poor solder joints to the IC leads.



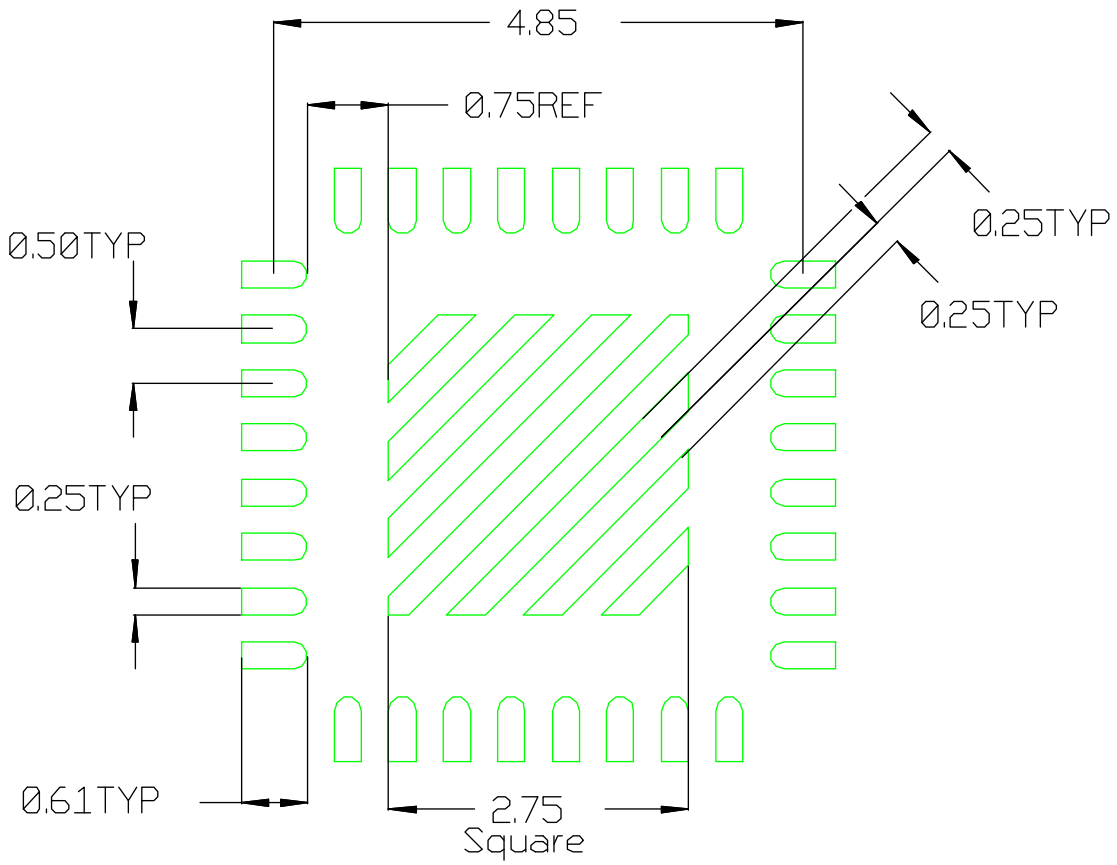
SOLDER RESIST

- The solder resist should be pulled away from the metal lead lands by a minimum of 0.06mm. The solder resist mis-alignment is a maximum of 0.05mm and it is recommended that the lead lands are all Non Solder Mask Defined (NSMD). Therefore pulling the S/R 0.06mm will always ensure NSMD pads.
- The minimum solder resist width is 0.13mm.
- At the inside corner of the solder resist where the lead land groups meet, it is recommended to provide a fillet so a solder resist width of ≥ 0.17mm remains.
- The land pad should be Solder Mask Defined (SMD), with a minimum overlap of the solder resist onto the copper of 0.06mm to accommodate solder resist mis-alignment. In 0.5mm pitch cases it is allowable to have the solder resist opening for the land pad to be smaller than the part pad.
- Ensure that the solder resist in-between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.
- The single via in the land pad should be tented or plugged from bottom boardside with solder resist.



STENCIL DESIGN

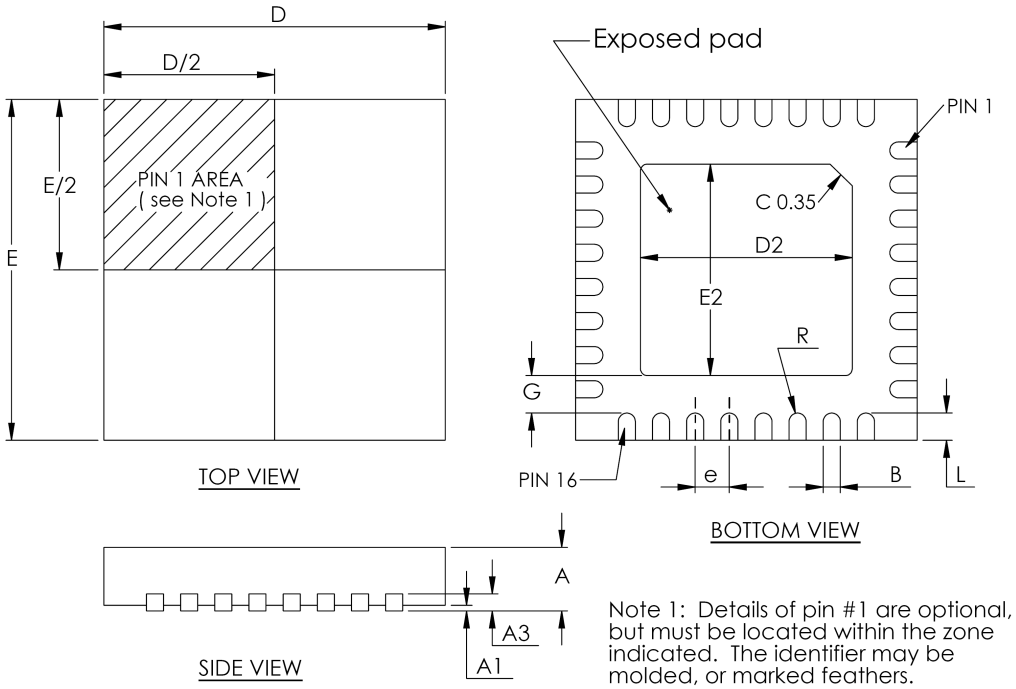
- The stencil apertures for the lead lands should be approximately 80% of the area of the lead lands. Reducing the amount of solder deposited will minimize the occurrence of lead shorts. Since for 0.5mm pitch devices the leads are only 0.25mm wide, the stencil apertures should not be made narrower; openings in stencils < 0.25mm wide are difficult to maintain repeatable solder release.
- The stencil lead land apertures should therefore be shortened in length by 80% and centered on the lead land.
- The land pad aperture should be striped with 0.25mm wide openings and spaces to deposit approximately 50% area of solder on the center pad. If too much solder is deposited on the center pad the part will float and the lead lands will be open.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.



Stencil Aperture
All Dimensions in mm

PACKAGE INFORMATION

32L MLPQ (5 x 5 mm Body) θ_{JA} =24.4 °C/W, θ_{JC} =0.86 °C/W



Note 1: Details of pin #1 are optional, but must be located within the zone indicated. The identifier may be molded, or marked feathers.

32-PIN 5x5 (unit: MM)			
DIM	MIN	NOM	MAX
A	0.8	0.85	0.9
A1	0.00		0.05
A3	0.20 REF		
B	0.20	0.25	0.30
D	4.95	5.00	5.05
D2	3.00	3.10	3.20
E	4.95	5.00	5.05
E2	3.00	3.10	3.20
e	0.5 REF		
G	0.55 REF		
L	0.30	0.40	0.50
R	0.125 TYP		

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.
www.irf.com