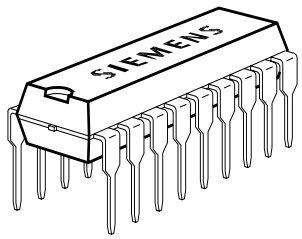
SIEMENS

Control IC for Single-Ended and Push-Pull Switched-Mode Power Supplies (SMPS)

TDA 4718 A

Features

- Feed-forward control (line hum suppression)
- Push-pull outputs
- Dynamic output current limitation
- Overvoltage protection
- Undervoltage protection
- Soft start
- Double pulse suppression



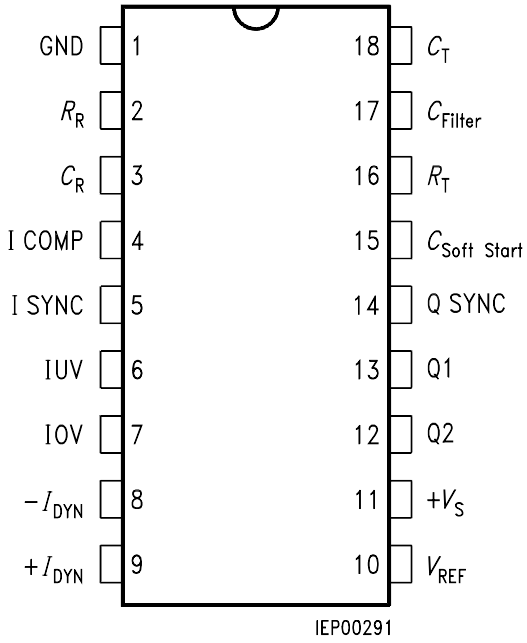
P-DIP-18-1

Type	Ordering Code	Package	Temp.-Range
▼ TDA 4718 A	Q67000-Y639	P-DIP-18-1	– 25 to 85 °C

▼ Not for new design

These versatile SMPS control ICs comprise digital and analog functions which are required to design high-quality flyback, single-ended and push-pull converters in normal, half-bridge and full-bridge configurations. The component can also be used in single-ended voltage multipliers and speed-controlled motors. Malfunctions in electrical operation are recognized by the integrated operational amplifiers, which activate protective functions.

Pin Configuration
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	GND	Ground 0 V
2 3	R_R C_R	Ramp generator R_R Ramp generator C_R
4 5	I COMP I SYNC	+ Input comparator K2 Sync. input
6 7	IUV IOV	Input undervoltage, ON/OFF Input overvoltage
8 9	$-I_{DYN}$ $+I_{DYN}$	Input dynamic current limitation (–) Input dynamic current limitation (+)
10 11	$+V_{REF}$ $+V_S$	Reference voltage Supply voltage
12 13	Q 2 Q 1	Output Q2 Output Q1
14 15	Q SYNC $C_{soft\ start}$	Sync. output Soft start
16 17 18	R_T C_{filter} C_T	VCO R_T Capacitance VCO C_T

Circuit Description

Voltage Controlled Oscillator (VCO)

The VCO generates a sawtooth voltage. The duration of the falling edge is determined by the value of C_T. The duration of the rising edge of the waveform and, therefore, approximately the frequency, is determined by the value of R_T. By varying the voltage at C_{filter}, the oscillator frequency can be changed by its rated value. During the fall time, the VCO provides a trigger signal for the ramp generator, as well as an L signal for a number of IC parts to be controlled.

Ramp Generator

The ramp generator is triggered by the VCO and oscillates at the same frequency. The duration of the falling edge of the ramp generator waveform is to be shorter than the fall time of the VCO. To control the pulse width at the output, the voltage of the rising edge of the ramp generator signal is compared with a DC voltage at comparator K2. The slope of the rising edge of the ramp generator signal is controlled by the current through R_R. This offers the possibility of an additional, superimposed control of the output duty cycle. This additional control capability, called “feed-forward control”, is utilized to compensate for known interference such as ripple on the input voltage.

Phase Comparator

If the component is operated without external synchronization, the sync input must be connected to the sync output for the phase comparator to set the rated voltage at C_{filter}. The VCO then oscillates with rated frequency. In the case of external synchronization, other components can be synchronized with the sync output. The component can be frequency-synchronized, but not phase-synchronized, with the sync input. The duty cycle of the squarewave voltage at the sync input is arbitrary. The best stability as to small phase and frequency interference deviation is achieved with a duty cycle as offered by the sync output.

Push-Pull Flipflop

The push-pull flipflop is switched by the falling edge of the VCO. This ensures that only one output of the two push-pull outputs is enabled at a time.

Comparator K2

The two plus inputs of the comparator are switched such that the lower plus level is always compared with the level of the minus input. As soon as the voltage of the rising sawtooth edge exceeds the lower of the two plus levels, both outputs are disabled via the pulse turn-off flipflop. The period during which the respective, active outputs is low can be infinitely varied. As the frequency remains constant, this process corresponds to a change in duty cycle.

Pulse-Turn-OFF Flipflop

The pulse turn-OFF flipflop enables the outputs at the start of each half cycle. If an error signal from comparator K7 or a turn-off signal from K2 is present, the outputs will immediately be switched off.

Comparator K3

Comparator K3 limits the voltage at capacitance $C_{\text{soft start}}$ (and also at K2) to a maximum of + 5 V. The voltage at the ramp generator output may, however rise to 5.5 V. With a corresponding slope of the rising ramp generator edge, the duty cycle can be limited to a desired maximum value.

Comparator K4

The comparator has its switching threshold at 1.5 V and sets the error flipflop with its output if the voltage at capacitance $C_{\text{soft start}}$ is below 1.5 V. However, the error flipflop accepts the set signal only if no reset pulse (error) is applied. In this way the outputs cannot be turned on again as long as an error signal is present.

Soft Start

The lower one of the two voltages at the plus inputs of K2 is a measure for the duty cycle at the output. At the instant of turning on the component, the voltage at capacitor $C_{\text{soft start}}$ equals 0 V. As long as no error is present, this capacitor is charged with a current of 6 µA to the maximum value of 5 V. In case of an error, $C_{\text{soft start}}$ is discharged with a current of 2 µA. A set signal is pending at the error flipflop below a charge of 1.5 V and the outputs are enabled if no reset signal is pending simultaneously. As the minimum ramp generator voltage, however, is 1.8 V, the duty cycle at the outputs is actually increased slowly and continuously not before the voltage at $C_{\text{soft start}}$ exceeds 1.8 V.

Error Flipflop

Error signals, which are led to input $\overline{\text{R}}$ of the error flipflop cause an immediate disabling of the outputs, and after the error has been eliminated, cause the component to switch on again by the soft start.

Comparator K5, K6, K8, V_{REF} Overcurrent Load

These are error detectors which cause immediate disabling of the outputs via the error flipflop when an error occurs. After elimination of the error, the component switches on again using the soft start. The output of K5 can be fed back to the input. This causes the IC output stage to remain disabled even after elimination of the overvoltage. However, it requires high-ohmic overvoltage coupling.

Comparator K7

K7 serves to recognize overcurrents. This is the reason why both inputs of the op amp have been brought out. Turning on is resumed after error recovery at the beginning of the next half period but without using the soft start.

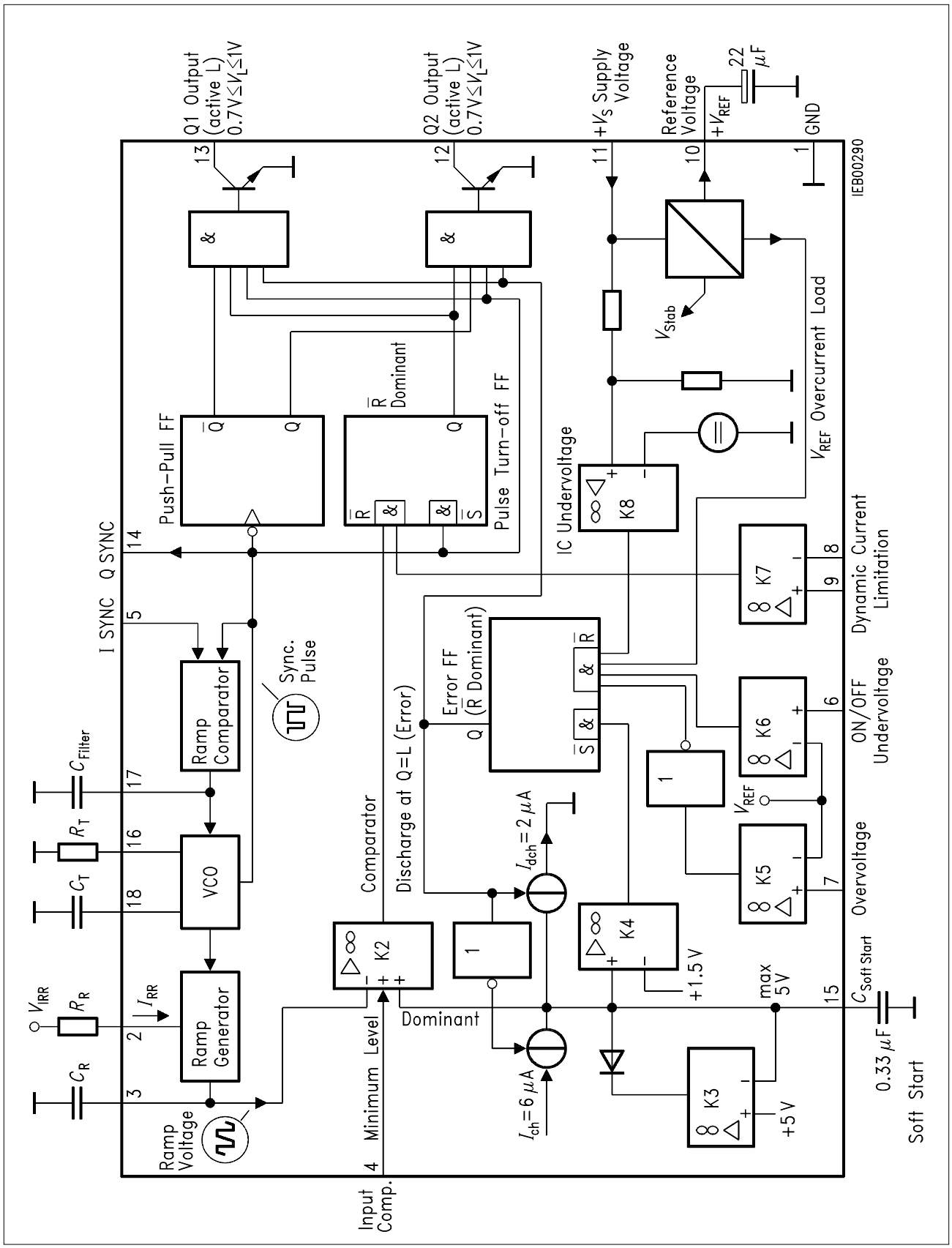
K7 has a common-mode range covers 0 V and + 4 V. The delay time between occurrence of an error and disabling of the outputs is only 250 ns.

Outputs

Both outputs are transistors with open collectors and operate in a push-pull arrangement. They are active low. The time in which only one of the two outputs is conductive can be varied infinitely. The length of the falling edge at VCO is equal to the minimum time during which both outputs are disabled simultaneously. The minimum L voltage is 0.7 V.

Reference Voltage

The reference voltage source is a highly constant source with regard to its temperature behavior. It can be utilized in the external wiring of the op amp, the error comparators, the ramp generator, or other external components.



Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Supply voltage	V_S	– 0.3	33	V	
Voltage at Q1, Q2	V_Q	– 0.3	33	V	Q1, Q2 high
Current at Q1, Q2	I_Q		70	mA	Q1, Q2 low
Sync output	$V_{SYNC\ Q}$	– 0.3	7	V	SYNC Q high
	$I_{SYNC\ Q}$	0	10	mA	SYNC Q low
Sync input	$V_{SYNC\ I}$	– 0.3	33	V	
Input C_{filter}	$V_{I\ Cf}$	– 0.3	7	V	
Input R_T	$V_{I\ RT}$	– 0.3	7	V	
Input C_T	$V_{I\ CT}$	– 0.3	7	V	
Input R_R	$V_{I\ RR}$	– 0.3	7	V	
Input C_R	$I_{I\ CR}$	– 10	10	mA	
Input comparator K2, K5, K6, K7	$V_{I\ K}$	– 0.3	33	V	
Output K5	$V_{Q\ K5}$	– 0.3	33	V	
Reference voltage	V_{REF}	– 0.3	V_{REF}	V	
Input $C_{soft\ start}$	$V_{I\ soft\ start}$	– 0.3	7	V	
Junction temperature	T_j		150	°C	
Storage temperature	T_{stg}	– 55	125	°C	
Thermal resistance system-air	$R_{th\ SA}$		60	K/W	

Operating Range

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Supply voltage	V_S	10.5	30	V	
Ambient temperature	T_A	– 25	85	°C	
VCO frequency Ramp generator frequency	f f_{RG}	40 40	250 000 250 000	Hz Hz	

Characteristics

V_S = 11 to 30 V; T_A = – 25 to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply current	I_S	8		20	mA	C_T = 1 nF f_{VCO} = 100 kHz
Reference						
Reference voltage	V_{REF}	2.35 2.45	2.5 2.5	2.65 2.55	V V	0 mA < I_{REF} < 5 mA 0 < T_A < 70 °C
Reference voltage change	ΔV_{REF}		8		mV	14 V ± 20 %
Reference voltage change	ΔV_{REF}		15		mV	25 V ± 20 %
Reference voltage change	ΔV_{REF}			15	mV	0 mA < I_{REF} < 5 mA
Temperature coefficient	TC		0.25	0.4	mV/K	
Response threshold of I_{REF} overcurrent	I_{REF}		10		mA	

Characteristics (cont'd)
V_S = 11 to 30 V; T_A = – 25 to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Oscillator (VCO)						
Frequency range	f_{VCO}	40		100 000	Hz	
Frequency change	$\Delta f/f_{VCO}$		0.5		%	14 V ± 20 %
Frequency change	$\Delta f/f_{VCO}$	– 1		1	%	25 V ± 20 %
Tolerance	$\Delta f/f_{VCO}$	– 7		7	%	$\Delta R_T = 0$; $\Delta C_T = 0$
Fall time sawtooth	t		1		µs	C_T = 1 nF
	t		10		µs	C_T = 10 nF
RC combination	C_T	0.82		47	nF	
VCO	R_T	5		700	kΩ	
Ramp Generator						
Frequency range	f	40		100 000	Hz	
Maximum voltage at C_R	V_H		5.5		V	
Minimum voltage at C_R	V_L		1.8		V	
Input current through R_R	I_{RR}	0		400	µA	
Current transformation ratio	I_{RR}/I_{CR}		1/4			
Synchronization						
Sync output	$V_{Q\,H}$	4			V	$I_{Q\,H}$ = – 200 µA
	$V_{Q\,L}$			0.4	V	$I_{Q\,L}$ = 1.6 mA
Sync input	$V_{I\,H}$	2			V	
	$V_{I\,L}$			0.8	V	
Input current	$-I_I$			5	µA	

Characteristics (cont'd)
V_S = 11 to 30 V; T_A = – 25 to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Comparator K2						
Input current	$-I_{I\,K2}$			2	µA	
Turn-OFF delay [1]	$t_{D\,OFF}$			500	ns	
Input voltage	$V_{I\,K2}$					for duty cycle
			1.8		V	D = 0
			5		V	D = max.
Common-mode input voltage range	$V_{I\,C}$	0		5.5	V	
Soft Start K3, K4						
Charge current for $C_{soft\ start}$	I_{ch}		6		µA	
Discharge current for $C_{soft\ start}$	I_{dch}		2		µA	
Upper limiting voltage	V_{lim}		5		V	
Switching voltage K4	V_{K4}		1.5		V	
Output Stages Q1, Q2						
Output voltage	$V_{Q\,H}$			30	V	
	$V_{Q\,L}$			1.1	V	I_Q = 20 mA
Output leakage current	I_Q			2	µA	$V_{Q\,H}$ = 30 V
ON, OFF, Undervoltage K6						
Switching voltage	V	V_{REF} – 0.03		V_{REF} + 0.03	V	
Input current	$-I_I$			2	µA	
Turn-OFF delay time [2]	$t_{D\,OFF}$		250		ns	
Error detection time [2]	t		50		ns	

[1] At the input: step function ΔV = – 100 mV ⌐→ ΔV = + 100 mV
[2] At the input: step function $\Delta V = V_{REF}$ – 100 mV ⌐→ V_{REF} + 100 mV

Characteristics (cont'd)
V_S = 11 to 30 V; T_A = – 25 to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Dynamic Current Limitation K7						
Common-mode input voltage range	V_{IC}	0		4	V	
Input offset voltage	V_{IO}	– 10		10	mV	
Input current	$-I_I$			2	µA	
Turn-OFF delay time [1]	$t_{D\ OFF}$		250		ns	
Error detection time [1]	t		50		ns	
Overvoltage K5						
Switching voltage	V	V_{REF} – 0.03		V_{REF} + 0.03	V	
Input current	$-I_I$			2	µA	
Output current	$-I_Q$	0		200	µA	$V_{QH\ min}$ = 5 V
Turn-OFF delay time [2]	$t_{D\ OFF}$		250		ns	
Error detection time [2]	t		50		ns	
Supply Undervoltage						
Turn-ON threshold for V_S rising	V_S	8.8		11	V	
Turn-OFF threshold for V_S falling	V_S	8.5		10.5	V	
Input C_{filter}						
Rated voltage for rated frequency	V_R		4		V	
Frequency approx. proportional to voltage within the range	V_R	3		5	V	
Voltage at open sync input	$V_{C\ filter}$		1.6		V	

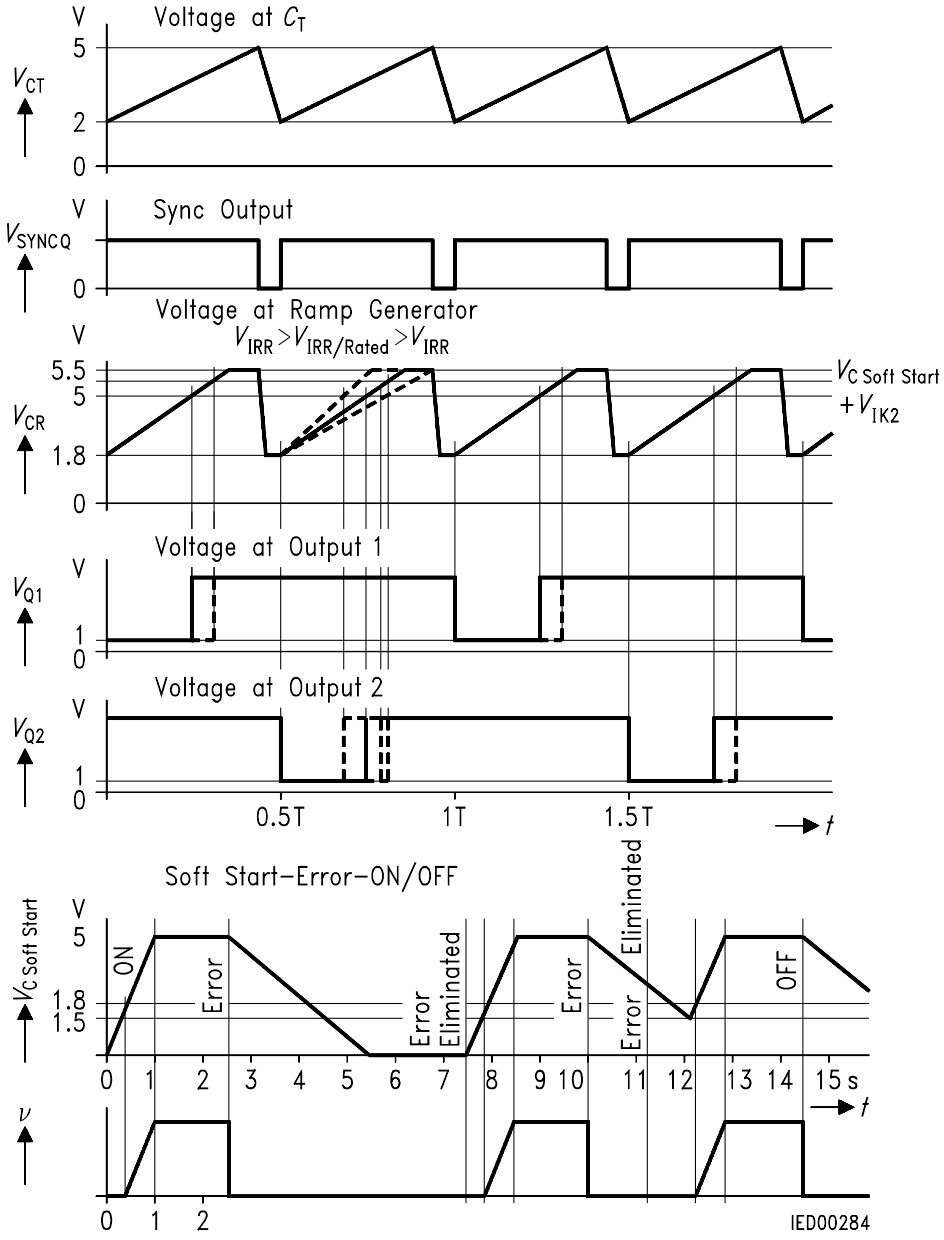
[1] At the input: step function ΔV = – 100 mV ⌐→ ΔV = + 100 mV
[2] At the input: step function $\Delta V = V_{REF}$ – 100 mV ⌐→ V_{REF} + 100 mV

Dimensioning Notes for RC Network

1. Determination of the minimum time during which both outputs must be disabled
   → selection of C_T; selection of $C_R \leq C_T$.
2. Determination of the VCO frequency = 2 x output frequency
   → selection of R_T.
3. Determination of the rated slope of the rising ramp generator voltage, which the maximum possible turn-on period per half wave depends on
   → selection of R_R.
4. Duration of the soft start process
   → selection of $C_{soft\ start}$.
5. In the case of a free-running VCO: connect sync output with sync input.
6. Capacitance C_{filter} is not required in the free-running operation (sync input connected with sync output).

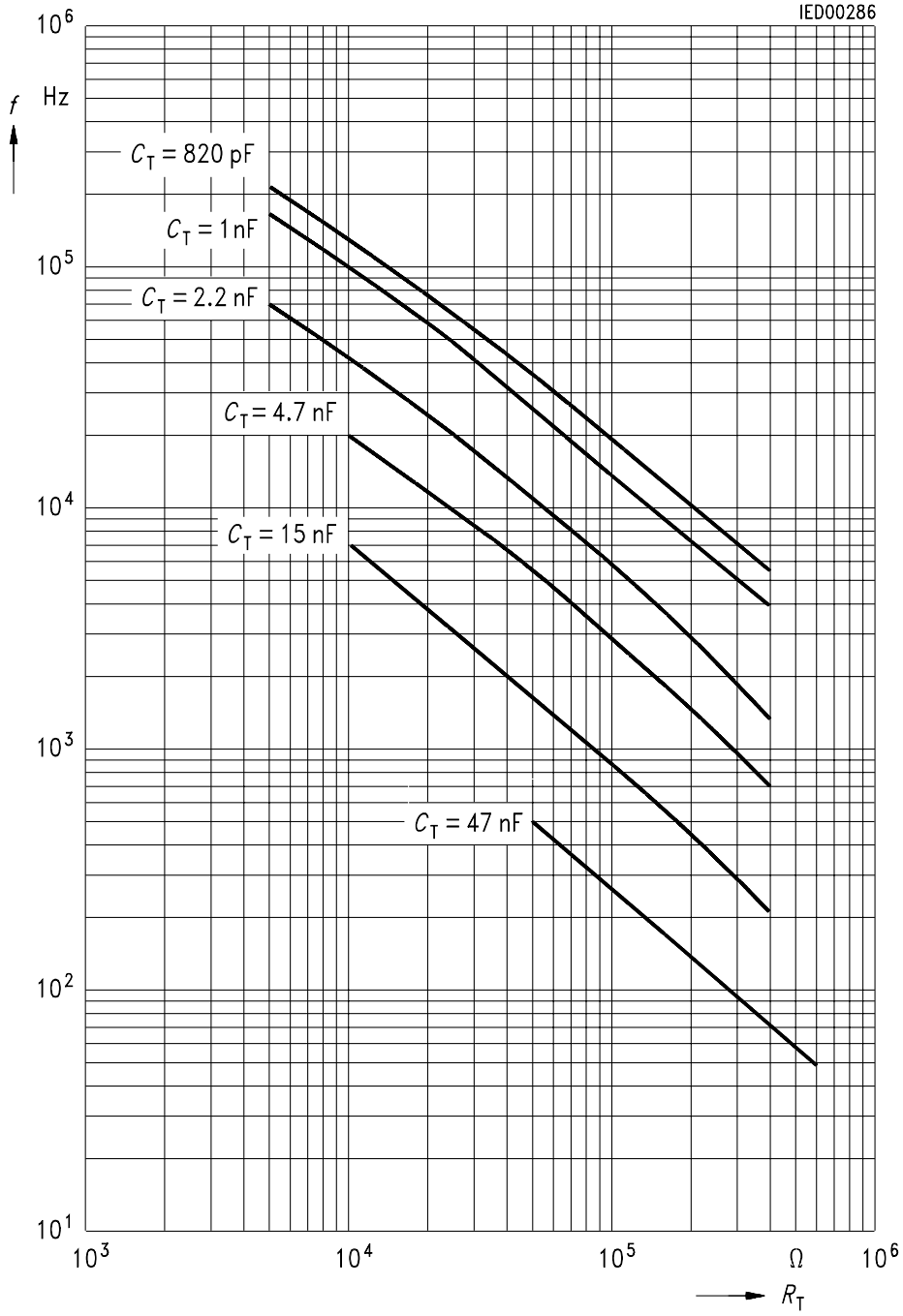
   In the case of external synchronization, that value depends on the selected operating frequency and the required maximum phase interference deviation.

Rated VCO frequency:	100 kHz	50 Hz
C_{filter} favourable:	10 nF	1µF



Pulse Diagram

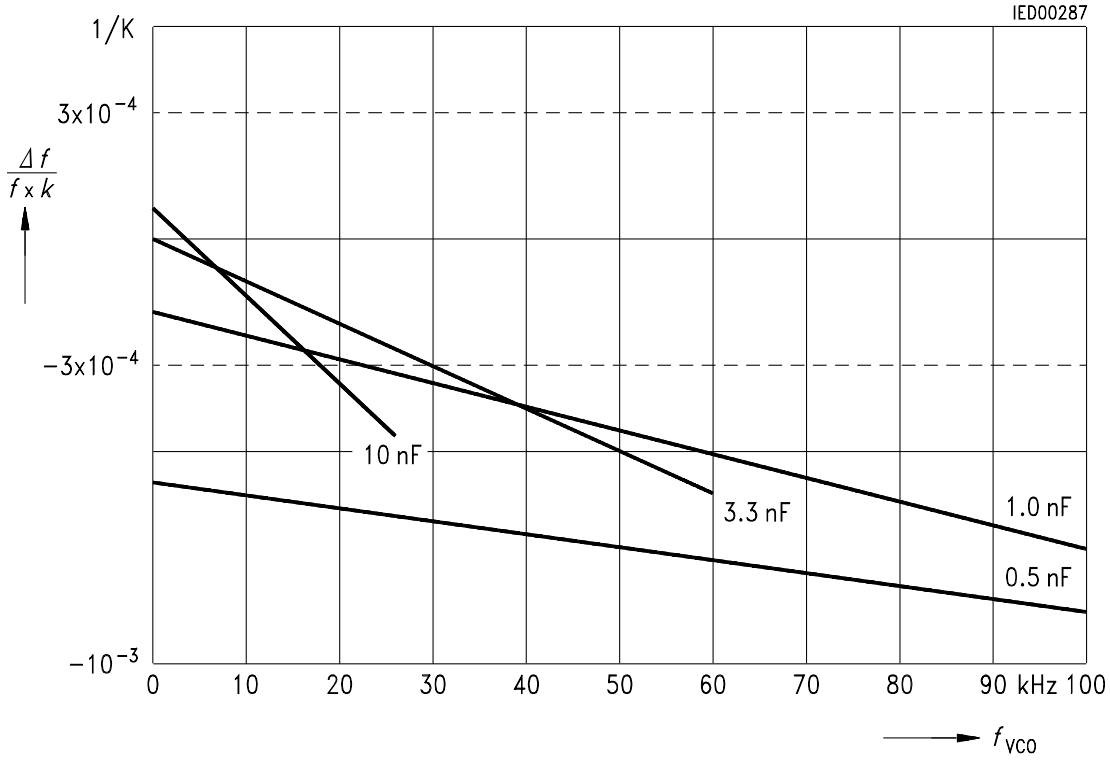
VCO Frequency versus R_T and C_T



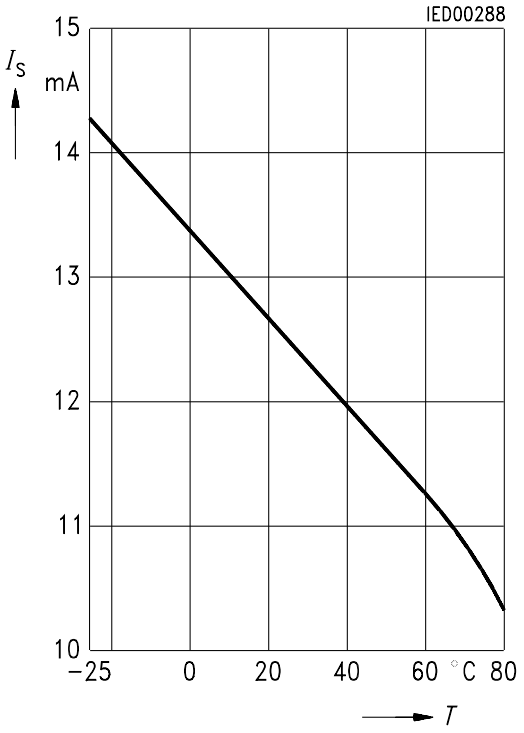
VCO Temperature Response

V_S = 12 V; D = max.

$\frac{\Delta f_{VCO}}{f_K \times K}[1/K]$ with C_T as parameter



Current Consumption versus Temperature



Output Current versus Output Voltage