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Features

➔ 3.3V ±10% supply voltage

➔ 25MHz XTAL or reference clock input

➔ Five PCIe® 2.0 Compliant 100MHz selectable HCSL outputs with -0.5% spread
  – default is spread off

➔ Two 25MHz LVCMOS output

➔ Industrial temperature range: -40°C to 85°C

➔ Packaging (Pb free and Green)
  ▫ TSSOP 28 (L)

Description

The PI6C49015 is a high performance networking clock generator which generates PCIe 2.0 Compliant 100MHz HCSL clock signals along with two LVCMOS 25MHz clock from either 25MHz crystal or reference input. This integrated solution is ideal for Networking, Embedded systems and other systems that require PCIe 1.0 and 2.0 HCSL signals and 25MHz clocks yet small foot print.
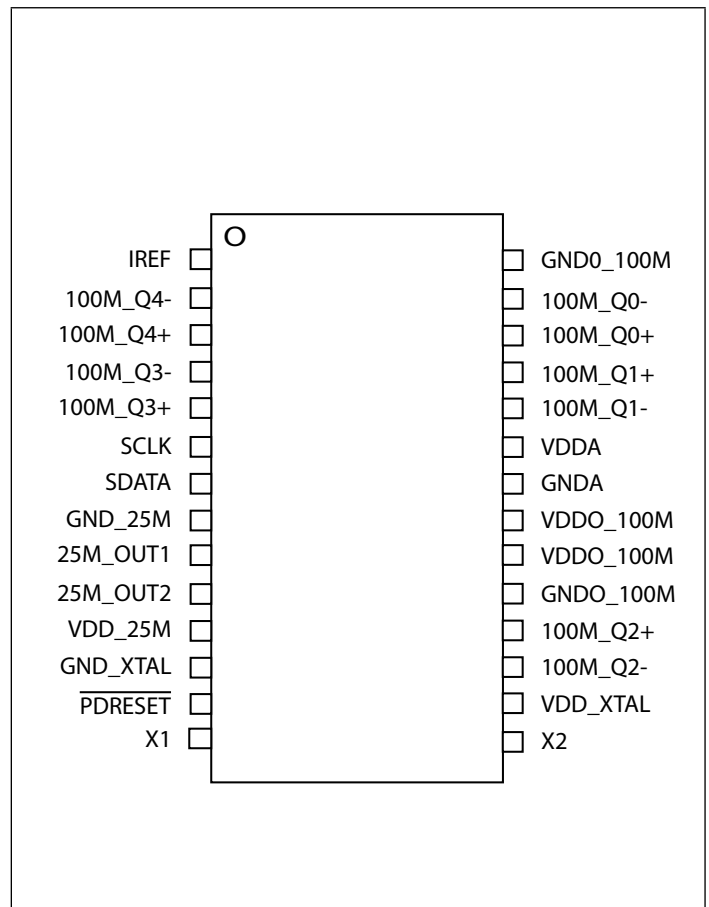
Applications

➔ Networking systems

➔ Embedded systems

➔ Other systems

Block Diagram
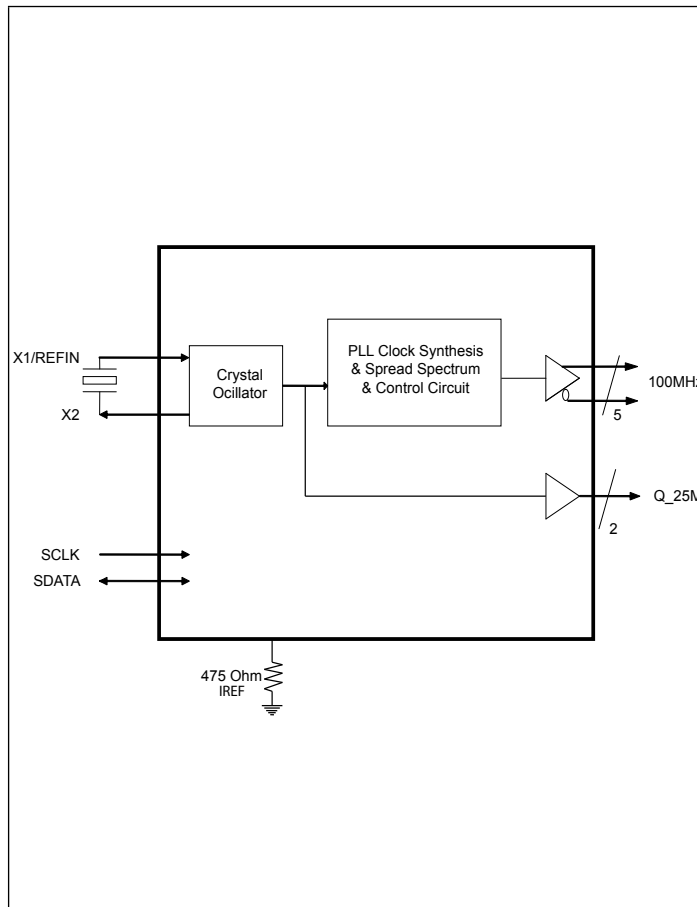
Pin Configuration

Pin Description

Pin #	Pin Name	Pin Type	Pin Description
1	IREF	Output	Connect to 475-Ohm resistor to set HCSL output drive current
2	100M_Q4-	Output	100MHz HCSL output
3	100M_Q4+	Output	100MHz HCSL output
4	100M_Q3-	Output	100MHz HCSL output
5	100M_Q3+	Output	100MHz HCSL output
6	SCLK	Input	SMBus compatible input clock. Supports fast mode 400 kHz input clock
7	SDATA	I/O	SMBus compatible data line
8	GND_25M	Power	Ground for 25MHz output
9	25M_OUT1	Output	25MHz LVCMOS output. When disabled, output is trisated and has a normal 110kOhm pull-down
10	25M_OUT2	Output	25MHz LVCMOS output. When disabled, output is trisated and has a normal 110kOhm pull-down
11	VDD_25M	Power	3.3V supply for 25MHz output
12	GND_XTAL	Power	Ground for XTAL
13	$\overline{\text{PDRESET}}$	Input	Power on reset, when low all PLLs are powered down and output trisated. SMBus registers are reset to default values
14	X1	Input	Crystal input. Integrated 6pf capacitance
15	X2	Output	Crystal output. Integrated 6pf capacitance
16	VDD_XTAL	Power	3.3V supply for XTAL
17	100M_Q2-	Output	100MHz HCSL output
18	100M_Q2+	Output	100MHz HCSL output
19	GNDO_100M	Output	Ground for 100MHz output buffer
20	VDDO_100M	Power	3.3V supply for 100MHz output buffer
21	VDDO_100M	Power	3.3V supply for 100MHz output buffer
22	GNDA	Power	Ground for 100MHz related PLL
23	VDDA	Power	3.3V supply for 100MHz related PLL
24	100M_Q1-	Output	100MHz HCSL output
25	100M_Q1+	Output	100MHz HCSL output
26	100M_Q0+	Output	100MHz HCSL output
27	100M_Q0-	Output	100MHz HCSL output
28	GNDO_100M	Power	Ground for 100MHz output buffer

Serial Data Interface (SMBus)

PI6C49015 is a slave only SMBus device that supports indexed block read and indexed block write protocol using a single 7-bit address and read/write bit as shown below.

Address Assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	0/1

How to Write

1 bit	8 bits	1	8 bits	1	8 bits	1	8 bits	1		8 bits	1	1 bit
Start bit	d2H	Ack	Register offset	Ack	Byte Count = N	Ack	Data Byte 0	Ack	…	Data Byte N - 1	Ack	Stop bit

Note:
1.   Register offset for indicating the starting register for indexed block write and indexed block read. Byte Count in write mode cannot be 0.

How to Read (M: abbreviation for Master or Controller; S: abbreviation for slave/clock)

1 bit	8 bits	1 bit	8 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	8 bits	1 bit	…	8 bits	1 bit	1 bit
M: Start bit	M: Send "D2h"	S: sends Ack	M: send starting data-byte location: N	S: sends Ack	M: Start bit	M: Send "D3h"	S: sends Ack	S: sends # of data bytes that will be sent: X	M: sends Ack	S: sends starting data byte N	M: sends Ack	…	S: sends data byte N+X-1	M: Not Ac-knowl-edge	M: Stop bit

Byte 0: Spread Spectrum Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	Spread Spectrum Selection for 100 MHz HCSL PCI-Express clocks	RW	0	All 100MHz HCSL PCI Express output	0=spread off 1 = -0.5% down spread
6	Enables hardware or software control of OE bits (see Byte 0–Bit 6 and Bit 5 Functionality table)	RW	0	$\overline{PD\_RESET}$ pin, bit 5	0 = hardware cntl 1 = software ctrl
5	Software $\overline{PD\_RESET}$ bit. Enables or disables all outputs (see Byte 0–Bit 6 and Bit 5 Functionality table)	RW	1	All outputs	0 = disabled 1 = enabled
4 to 1	Reserved	RW	Undefined	Not Applicable	
0	OE for 25M_Out2	RW	1	25M_Out2	0 = disabled 1 = enabled

Byte 0 - Bit 6 and Bit 5 Functionality

Bit 6	Bit 5	Description
0	X	$\overline{PD\_RESET}$ HW pin/signal = enabled
1	0	Disables all outputs and tri-states the outputs, $\overline{PD\_RESET}$ HW pin/signal = DO NOT CARE
1	1	Enable all outputs, $\overline{PD\_RESET}$ HW pin/signal = DON'T CARE

Byte 1: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	Reserved	RW	Undefined	Not Applicable	
6	OE for 25M_Out1	RW	1	25M_Out1	0 = disabled 1 = enabled
5	Reserved	RW	Undefined	Not Applicable	
4	OE for 100M_Q4 HCSL output	RW	1	100M_Q4	0=disable 1 = enabled
3	Reserved	RW	Undefined	Not Applicable	
2	OE for 100M_Q3 HCSL output	RW	1	100M_Q3	0=disable 1 = enabled
1 to 0	Reserved	RW	Undefined	Not Applicable	

Byte 2: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7 to 5	Reserved	RW	Undefined	Not Applicable	
4 to 0	Reserved	R	Undefined	Not Applicable	

Byte 3: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	OE for 100M_Q2 HCSL Output	RW	1	100M_Q2	0 = disabled 1 = enabled
6 to 3	Reserved	RW	Undefined	Not Applicable	
2	OE for 100M_Q1 HCSL Output	RW	1	100M_Q1	0 = disabled 1 = enabled
1	OE for 100M_Q0 HCSL Output	RW	1	100M_Q0	0 = disabled 1 = enabled
0	Reserved	R	Undefined	Not Applicable	

Byte 4 & 5: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7 to 0	Reserved	R	Undefined	Not Applicable	

Byte 6: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	Revision ID bit 3	R	1	Not Applicable	
6	Revision ID bit 2	R	0	Not Applicable	
5	Revision ID bit 1	R	0	Not Applicable	
4	Revision ID bit 0	R	0	Not Applicable	
3	Vendor ID bit 3	R	0	Not Applicable	
2	Vendor ID bit 2	R	0	Not Applicable	
1	Vendor ID bit 1	R	1	Not Applicable	
0	Vendor ID bit 0	R	1	Not Applicable	

Absolute Maximum Ratings[1] (Over operating free-air temperature range)

Parameters	Min.	Max.	Units
Storage Temperature	-65	150	°C
Ambient Temperature with Power Applied	-40	85	
3.3V Analog Supply Voltage	-0.5	4.6	V
ESD Protection (HBM)		2000	

Note:
1. Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions

Symbol	Parameters	Test Condition	Min.	Typ.	Max.	Units
V_{DD}	Power supply		3.0	-	3.6	V
I_{DD}	Total Power Supply Current	All outputs unloaded	-	-	65	mA
$I_{DD\_Output\ Tri-stated}$	Total power supply current with tri-stated outputs	OE = "0", no load	-	-	42	mA
$I_{DD\ Power-Down}$	Total power supply current in power down mode	$\overline{PD\_RESET}$= "0", no load	-	-	3.8	mA
T_A	Operating temperature		-40	-	+85	°C

LVCMOS DC Electrical Characteristics
Over Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage		2	-	V_{DD}+0.3	V
V_{IL}	Input Low Voltage		-0.3	-	0.8	
V_{OH}	Output High Voltage	I_{OH} = -8mA	V_{DD}-0.4	-	-	
V_{OL}	Output Low Voltage	I_{OL} = 8mA	-	-	0.4	
I_{IH}	Input High Current	$V_{IN} = V_{DD}$ -0.1V	-	-	45	µA
I_{IL}	Input Low Current	$V_{IN} = 0V$	-45	-	-	
R_{PU}	Internal Pull-Up Resistance	$\overline{PDRESET}$	-	216	-	kOhm
R_{DN}	Internal Pull-Down Resistance	25M_OUT1, 25M_OUT2	-	110	-	

HCSL DC Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	Output High Voltage		660	-	950	
V_{OL}	Output Low Voltage		-	-	150	
V_{CROSS}	Absolute Crossing Point Voltages		250	-	550	mV
ΔV_{CROSS}	Total variation of V_{CROSS} overall edges		-	-	140	
I_{OH}	Input High Current	With 475-Ohm resistor connected between I_{REF} pin and GND	-	12	-	mA

LVCMOS AC Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_{in}	Input Frequency		-	25	-	MHz
F_{OUT}	Output Frequency	C_{LOAD} = 15pF	-	25	-	
T_r/T_f	Output Rise/Fall time	20% of V_{DD} to 80% of V_{DD}	-	-	1.2	ns
T_{DC}	Output Duty Cycle		45	-	55	%
T_j	Period Jitter	25 MHz clock output	-	-	30	ps

HCSL AC Switching Characteristics[1,2,3]

Over Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_{OUT}	Output Frequency	HCSL termination	-	-	100	MHz
T_r/T_f	Output Rise/Fall time	Between 0.175V and 0.525V	175	-	700	ps
$\Delta T_r/\Delta T_f$	Rise and Fall Time Variation[2]		-	-	125	ps
T_{DC}	Output Duty Cycle[3]		47	-	53	%
T_{cj}	Cycle-to-Cycle Jitter[3]	Differential waveform	-	-	70	ps
T_{PJ}	Peak-to-Peak Phase Jitter	Using PCIe jitter measurement method			86	ps
$J_{RMS2.0}$	PCIe 2.0 RMS Phase Jitter	PCIe 2.0 Test Method @ 100MHz Output			3.1	ps

Notes:

1. Test configuration is Rs=33Ω, Rp=49.9Ω, and 2pF

2. Measurement taken from a single-ended waveform.

3. Measurement taken from a differential waveform.
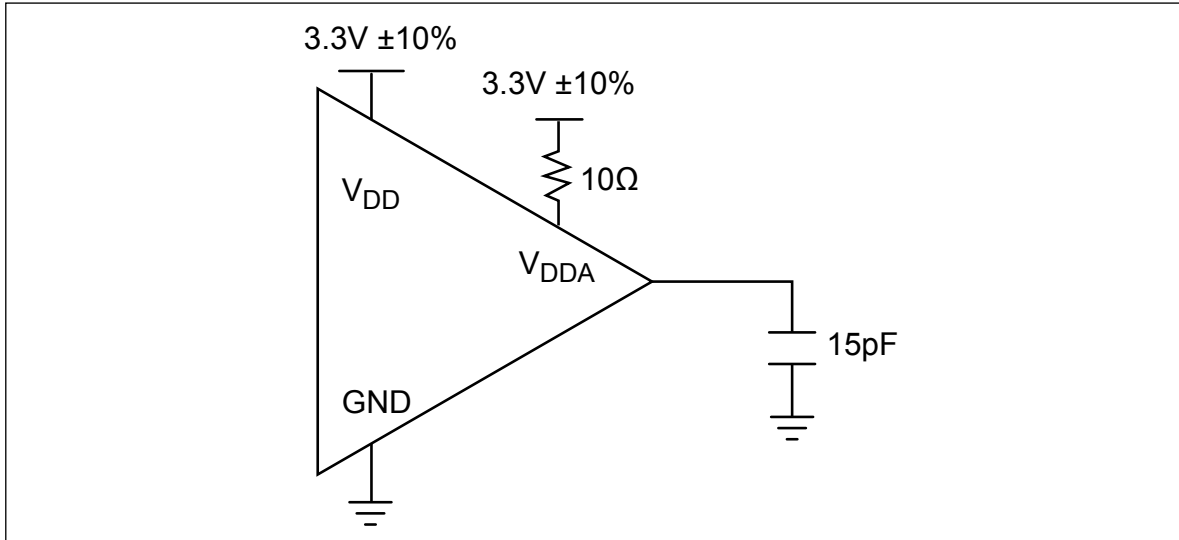
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HCSL Output Buffer Characteristics

V_{DD}
(3.3V ± 10%)

R_O

R_{OS}

↓ Iout

V_{OUT} = 0.85V max

Slope ~ 1/Rs

I_{OUT}

0V   0.85V
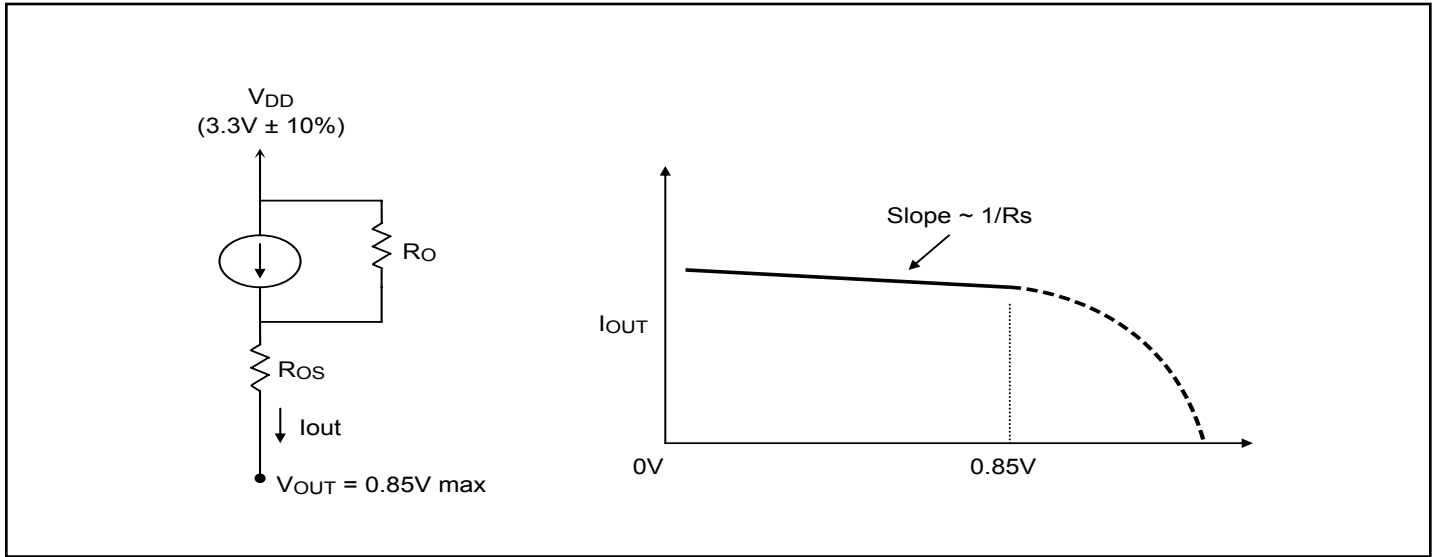
HCSL Output Buffer Characteristics

Symbol	Minimum	Maximum
R_O	3000Ω	N/A
R_{OS}	unspecified	unspecified
V_{OUT}	N/A	950mV

Configuration Test Load Board Termination for HCSL Outputs

PI6C49015

Rs
33Ω
5%

Rs
33Ω
5%

TLA

TLB

Clock

Clock#

475Ω
1%

Rp
49.9Ω
1%

Rp
49.9Ω
1%

2pF
5%

2pF
5%
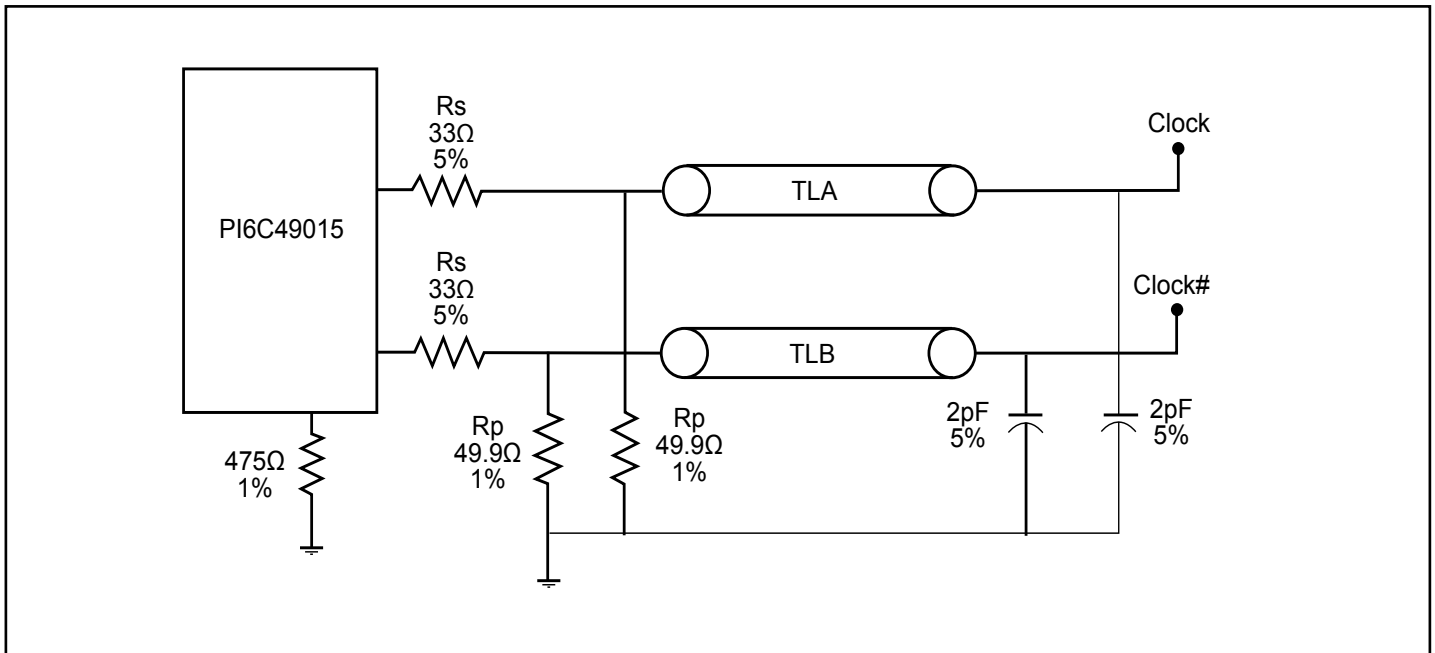
LVCMOS Test Circuit

Application Notes

Crystal circuit connection

The following diagram shows PI6C49015 crystal circuit connection with a parallel crystal. For the CL=18pF crystal, it is suggested to use C1= 18pF, C2= 18pF. C1 and C2 can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts.
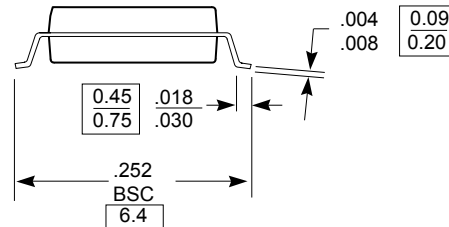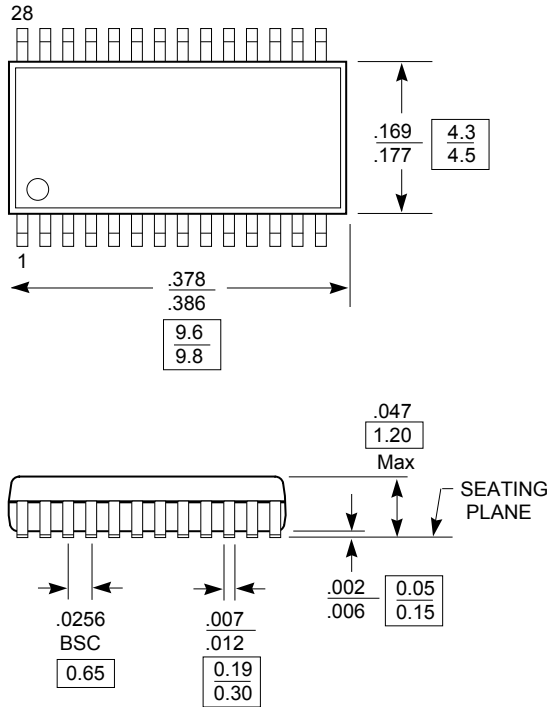
Crystal Oscillator Circuit
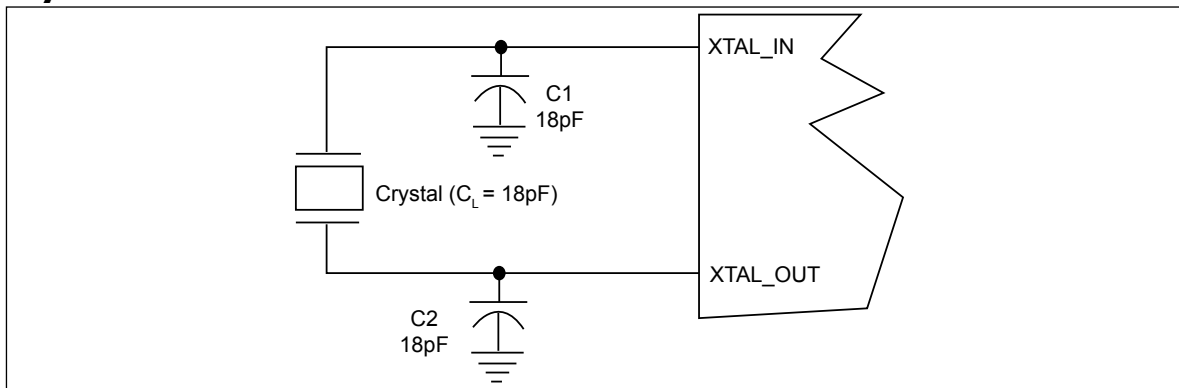
Recommended Crystal Specification

Pericom recommends:

a) GC2500003 XTAL 49S/SMD(4.0 mm), 25M, CL=18pF, +/-30ppm, http://www.pericom.com/pdf/datasheets/se/GC_GF.pdf

b) FY2500081, SMD 5x3.2(4P), 25M, CL=18pF, +/-30ppm, http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf

c) FL2500047, SMD 3.2x2.5(4P), 25M, CL=18pF, +/-20ppm, http://www.pericom.com/pdf/datasheets/se/FL.pdf

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REVISION: D
DATE: 03/09/05

28

1

.169 / .177 | 4.3 / 4.5

.378 / .386 | 9.6 / 9.8

.004 / .008 | 0.09 / 0.20

0.45 / 0.75 | .018 / .030

.252 BSC | 6.4

.047 | 1.20 | Max

SEATING PLANE

.0256 BSC | 0.65

.007 / .012 | 0.19 / 0.30

.002 / .006 | 0.05 / 0.15

Note:
1. Package Outline Exclusive of Mold Flash and Metal Burr
2. Controlling dimentions in millimeters
3. Ref: JEDEC MO-153F/AE

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DESCRIPTION: 28-Pin, 173-Mil Wide, TSSOP

PACKAGE CODE: L

Note:
• For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information[(1-3)]

Ordering Code	Package Code	Package Description
PI6C49015LIE	L	28 pin, Pb-free & Green, TSSOP (L28)

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/

2. E = Pb-free and Green

3. Adding an X suffix = Tape/Reel

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