TVS Diodes

Transient Voltage Suppressor Diodes

ESD103-B1-02Series

Bi-directional Femto Farad Capacitance TVS Diode

ESD103-B1-02ELS
ESD103-B1-02EL

Data Sheet

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Final

Power Management & Multimarket

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Revision History: Revision 0.2, 2012-09-20	
Page or Item	**Subjects (major changes since previous revision)**
Revision 1.0, 2013-05.07	
All	New type ESD103-B1-02EL inserted

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Last Trademarks Update 2010-06-09

1 Bi-directional Femto Farad Capacitance TVS Diode

1.1 Features

- ESD/Transient protection of RF and ultra-high speed signal lines according to:
  – **IEC61000-4-2: ±10 kV** (contact)
- Extremely low capacitance C_L **= 0.09 pF** (typical) at f = 1 GHz
- Maximum working voltage: V_{RWM} **= ±15 V**
- Very low reverse current: I_R **< 0.1 nA** (typ.)
- Very low series inductance down to 0.2 nH typical (TSSLP-2-4)
- Extremely small form factor down to 0.62 x 0.32 x 0.31 mm²
- Pb-free package (RoHS compliant)

RoHS

1.2 Application Examples

- ESD protection in RF applications
- Tailored for connectivity applications
- WLAN, GPS antenna, DVB T/H, Bluetooth Class 1 and 2
- Automated Meter Reading

1.3 Product Description

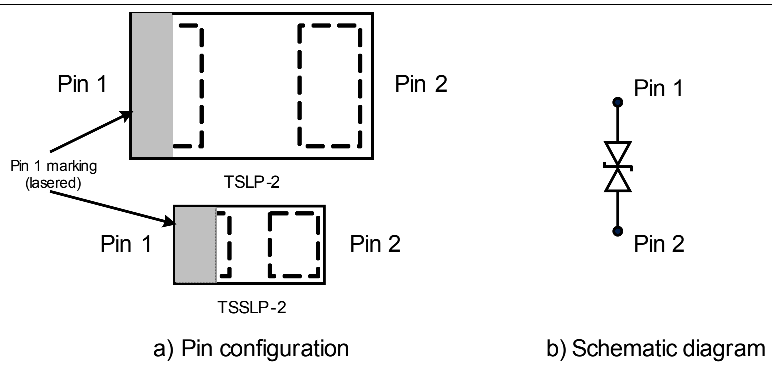


Figure 1 Pin configuration and Schematic diagram

Table 1 Ordering Information

Type	Package	Configuration	Marking code
ESD103-B1-02ELS	TSSLP-2-4	1 line, bi-directional	V
ESD103-B1-02EL[1)]	TSLP-2-20	1 line, bi-directional	V

1) Product not available yet, target data

2 Characteristics

Table 2 Maximum Ratings at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
ESD contact discharge[1]	V_{ESD}	-10	–	10	kV
Operating temperature	T_{OP}	-55	–	125	°C
Storage temperature	T_{stg}	-65	–	150	°C

1) V_{ESD} according to IEC61000-4-2 (R = 330 Ω, C = 150 pF discharge network)

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

2.1 Electrical Characteristics at T_A = 25 °C, unless otherwise specified

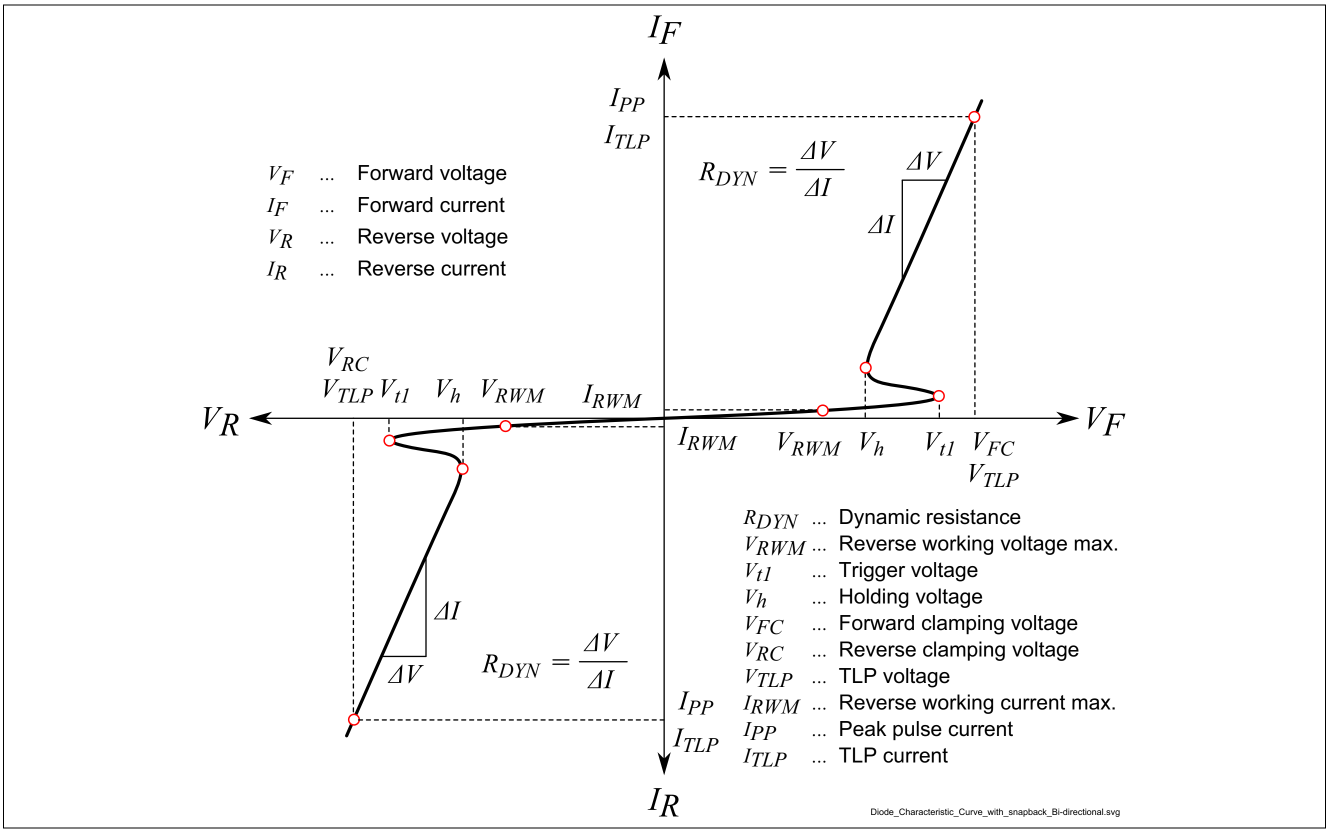


Figure 2 Definitions of electrical characteristics

Table 3 **DC Characteristics** at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	V_{RWM}	-15	–	15	V	
Trigger voltage	V_{Trig}	–	21	–	V	I_{BR} = 1 mA, from Pin 1 to Pin 2
		–	21	–		I_{BR} = 1 mA, from Pin 2 to Pin 1
Reverse current	I_R	–	<0.1	50	nA	V_R = 15 V

Table 4 **RF Characteristics** at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance	C_L	–	0.13	0.2	pF	V_R = 0 V, f = 1 MHz
		–	0.09	–		V_R = 0 V, f = 1 GHz
Series inductance	L_S	–	0.2	–	nH	ESD103-B1-02ELS
		–	0.4	–		ESD103-B1-02EL

Table 5 **ESD Characteristics** at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage[1)]	V_{CL}	–	36	–	V	I_{TLP} = 8 A
		–	48	–		I_{TLP} = 16 A
Dynamic resistance[1)]	R_{DYN}	–	1.8	–	Ω	t_p = 100 ns

1) ANSI/ESD STM5.5.1 - Electrostatic Discharge Sensitive Testing using Transmission Line Pulse (TLP) Model. TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 0.6 ns, I_{TLP} and V_{TLP} averaging window: t_1 = 30 ns to t_2 = 60 ns, extraction of dynamic resistance using least squares fit of TLP characteristic between I_{TLP1} = 2 A and I_{TLP2} = 14.1 A. Please refer to Application Note AN210[1].

3 Typical Characteristics

At T_A = 25 °C, unless otherwise specified

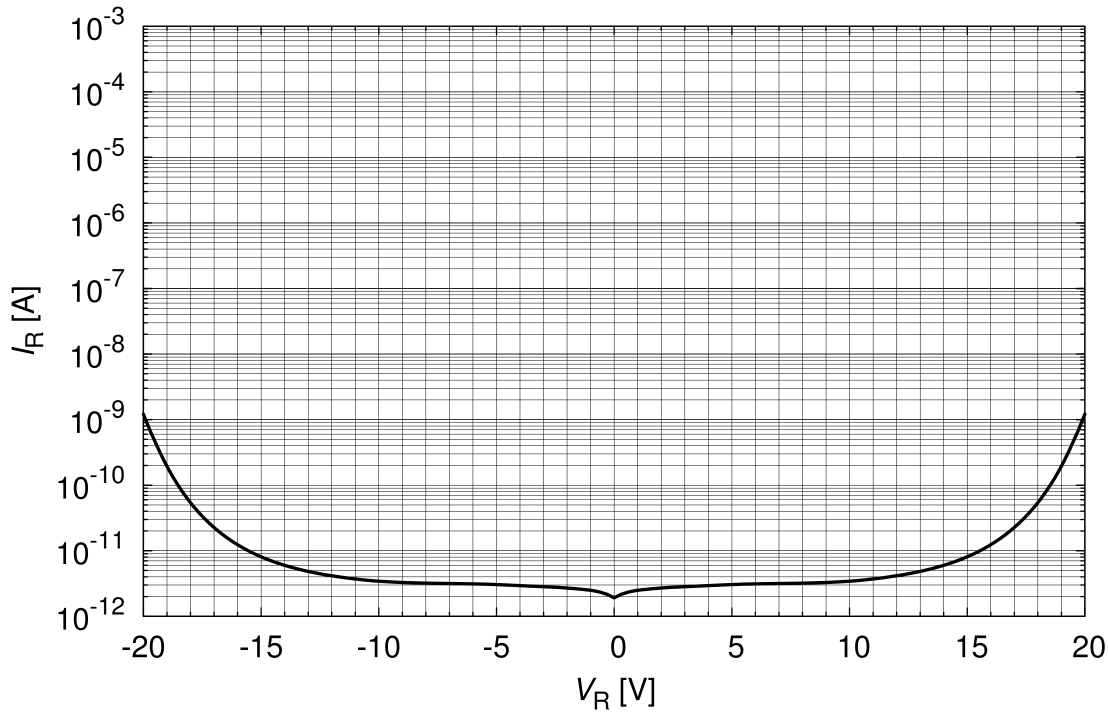


Figure 3 Reverse current $I_R = f(V_R)$

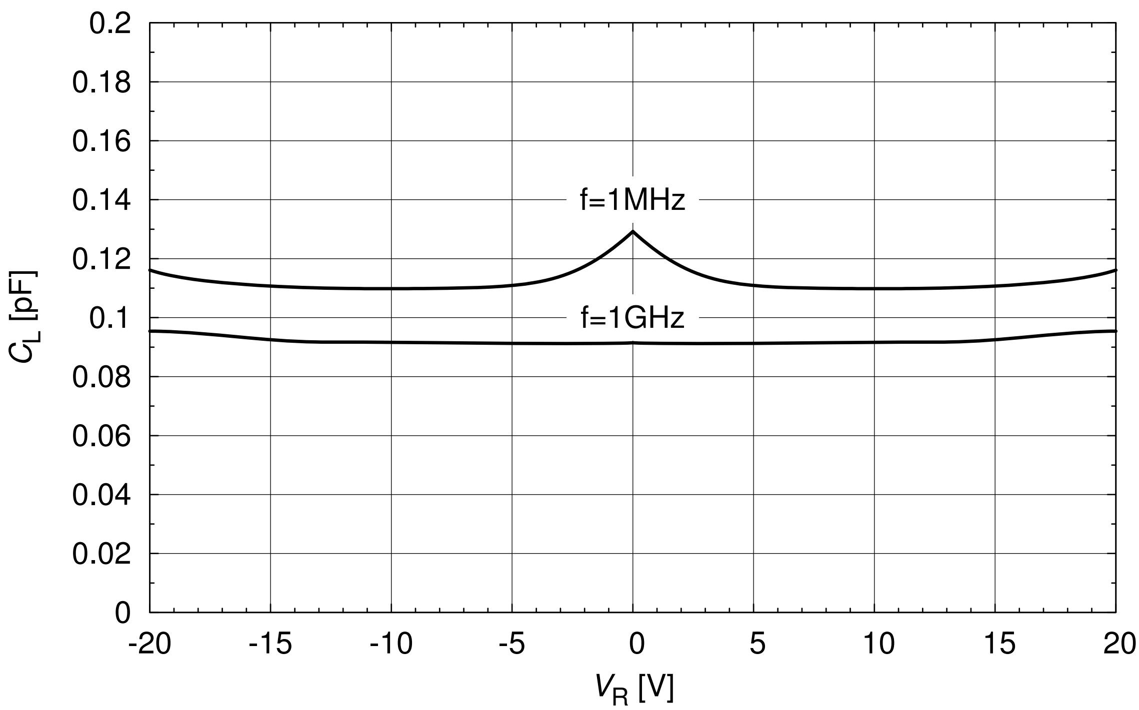


Figure 4 Line capacitance $C_L = f(V_R)$, f = 1 MHz

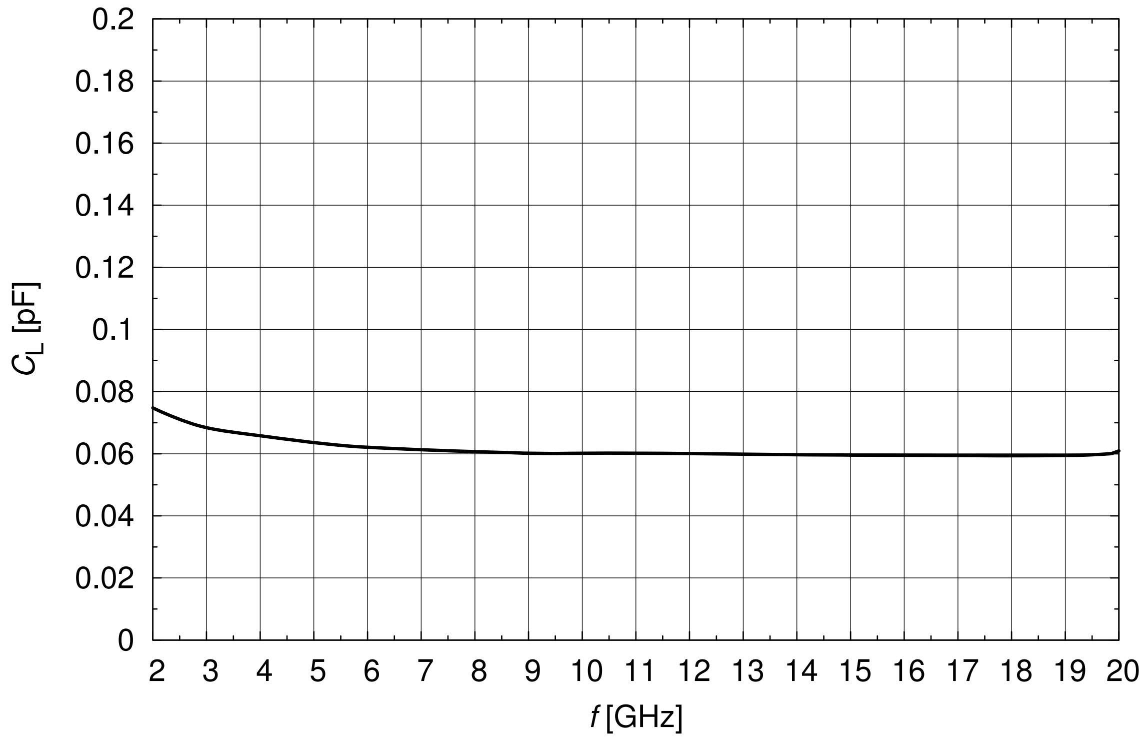


Figure 5 Line capacitance: $C_L = f(f)$, V_R = 0 V

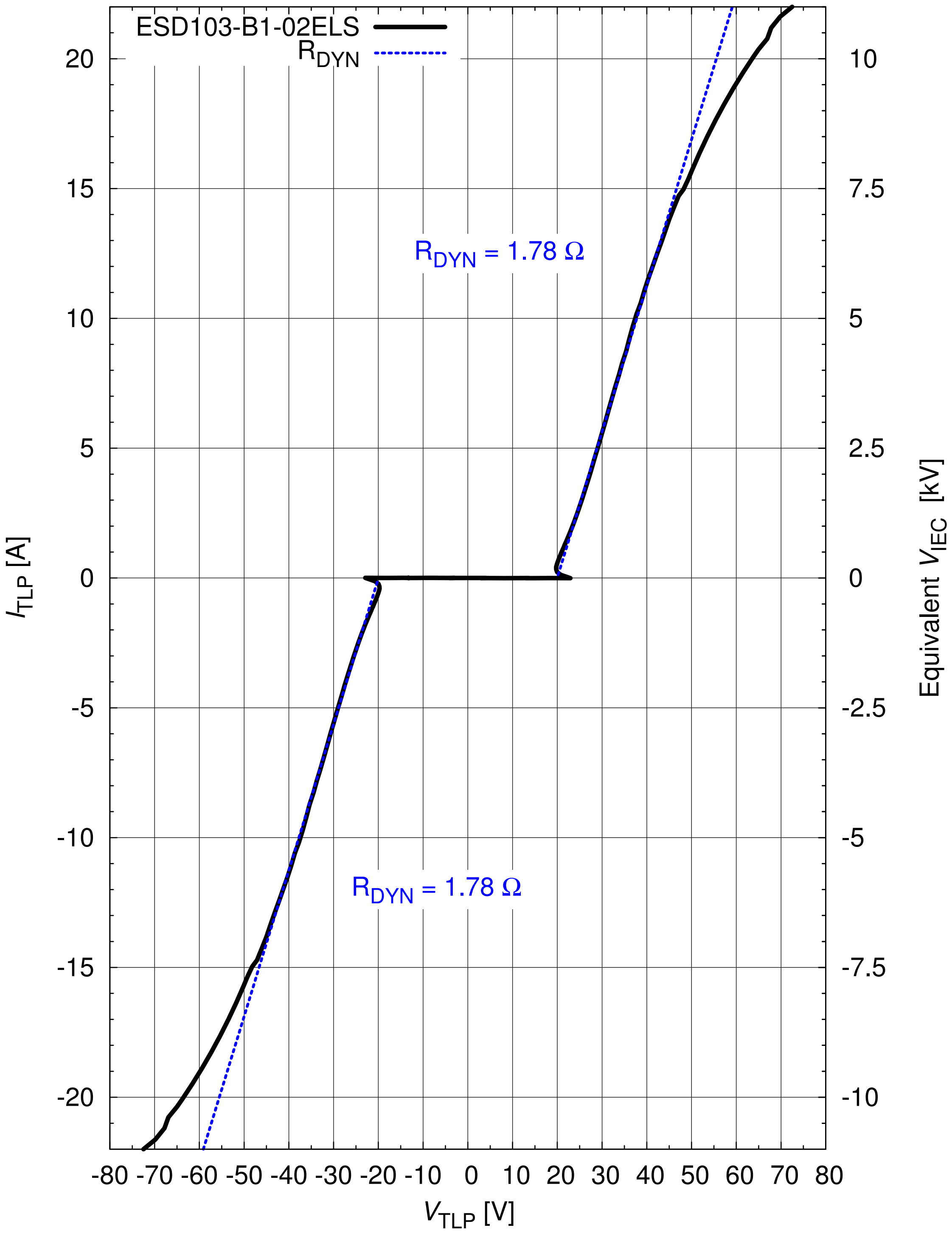


Figure 6 **Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ according ANSI/ESDSTM5.5.1-Electrostatistic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: $Z_0 = 50\ \Omega$, t_p = 100 ns, t_r = 0.6 ns, I_{TLP} and V_{TLP} average window: t_1 = 30 ns to t_2 = 60 ns, extraction of dynamic resistance using squares fit to TLP characteristics between I_{TLP1} = 2 A and I_{TLP2} = 14.1 A. Please refer to Application Note AN210[1]**

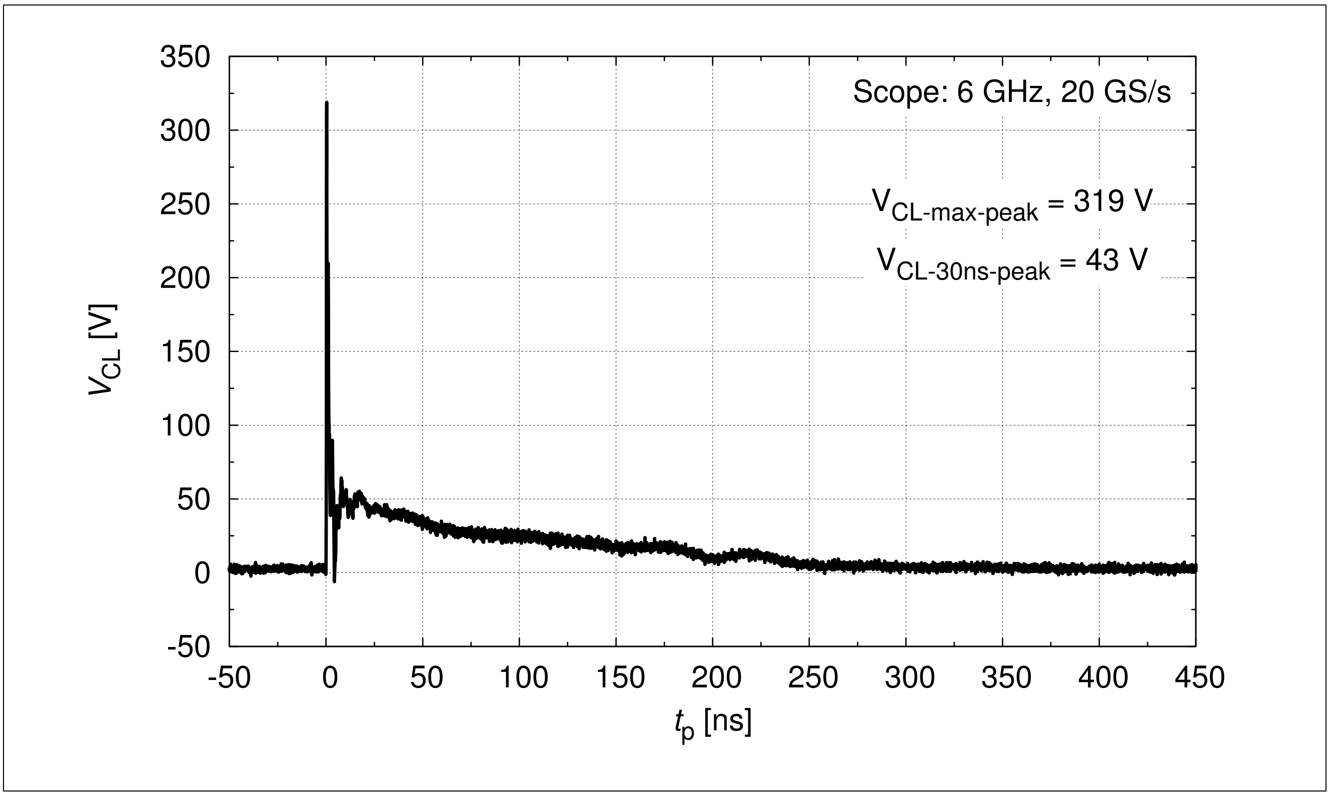


Figure 7 Clamping voltage at +8 kV discharge according IEC61000-4-2 (*R* = 330 Ω, *C* = 150 pF)

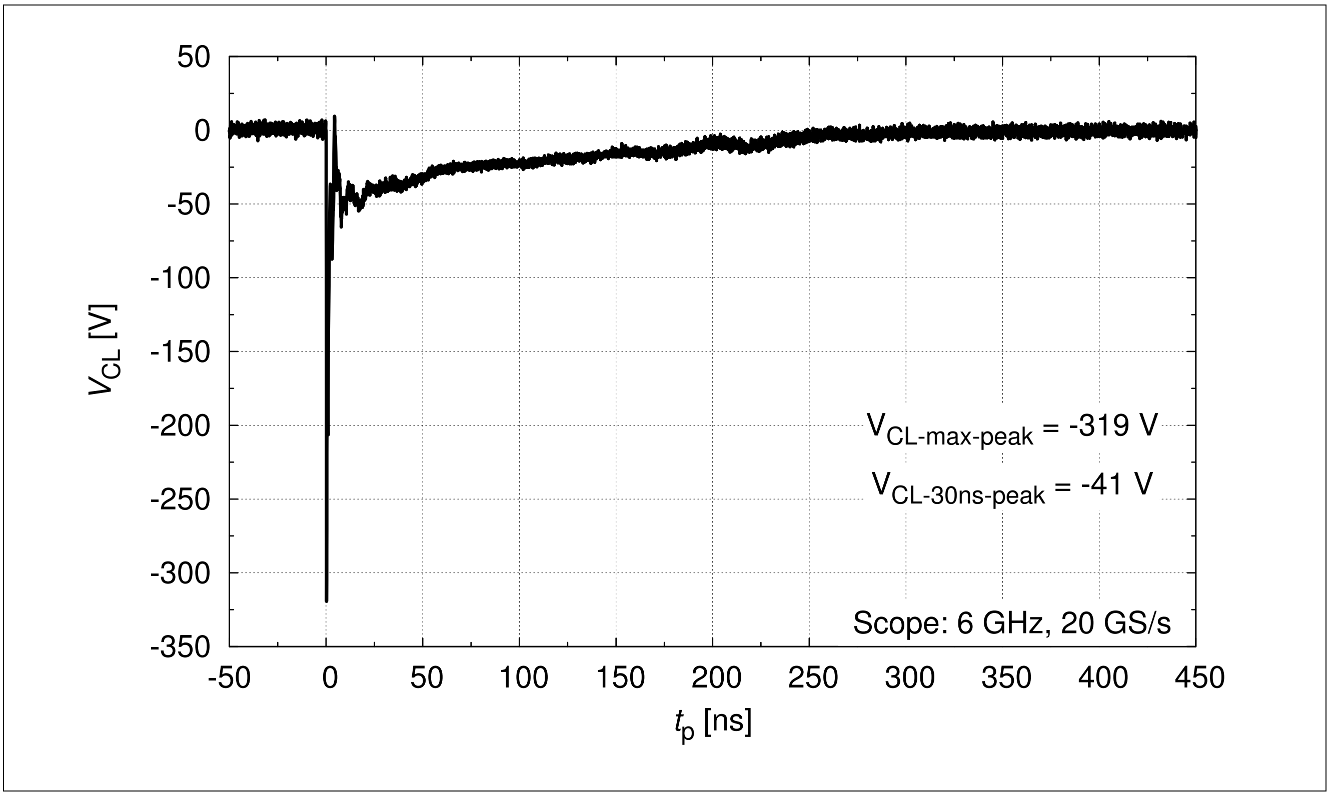
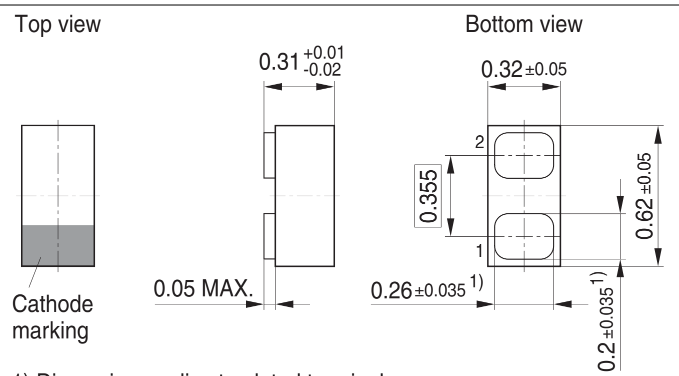


Figure 8 Clamping voltage at -8 kV discharge according IEC61000-4-2 (*R* = 330 Ω, *C* = 150 pF)

4 Package Information

4.1 TSSLP-2-4



1) Dimension applies to plated terminals

Figure 9 TSSLP-2-4 Package outline

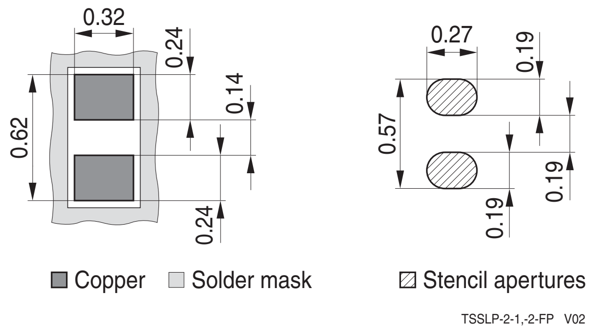
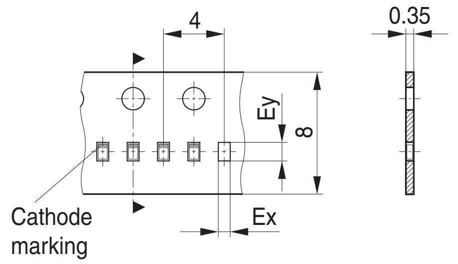


Figure 10 TSSLP-2-4 Footprint



Tape type	Ex	Ey
Punched Tape	0.43	0.73
Embossed Tape	0.37	0.67

Deliveries can be both tape types (no selection possible).
Specification allows identical processing (pick & place) by users.

TSSLP-2-1,-2-TP V03

Figure 11 TSSLP-2-4 Packing

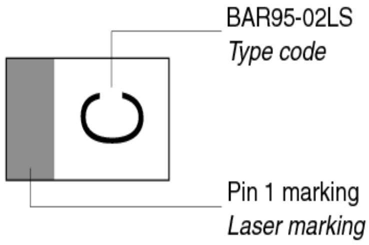


Figure 12 TSSLP-2-4 Marking (example)

4.2 TSLP-2-20

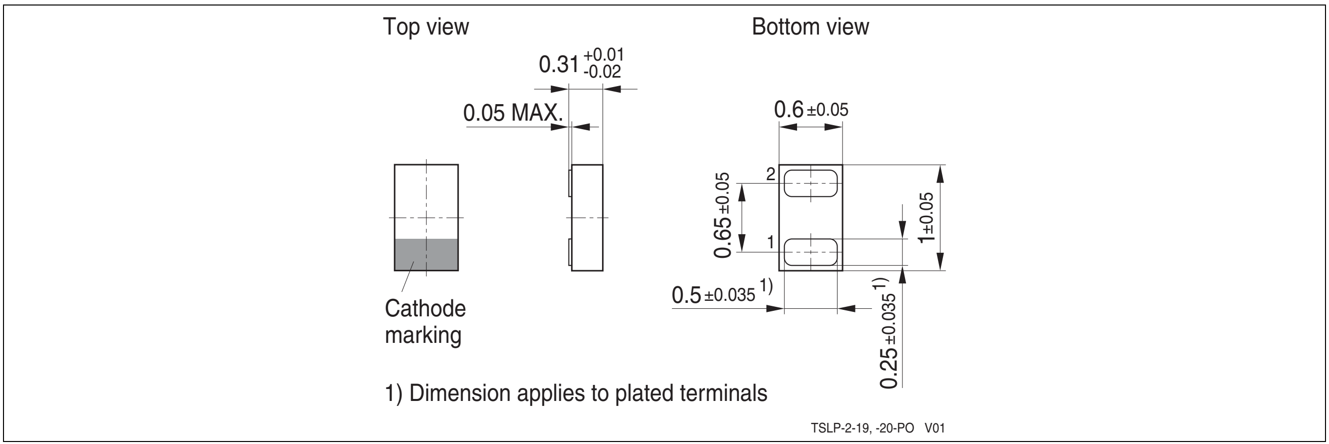


Figure 13 TSLP-2-20 Package outline

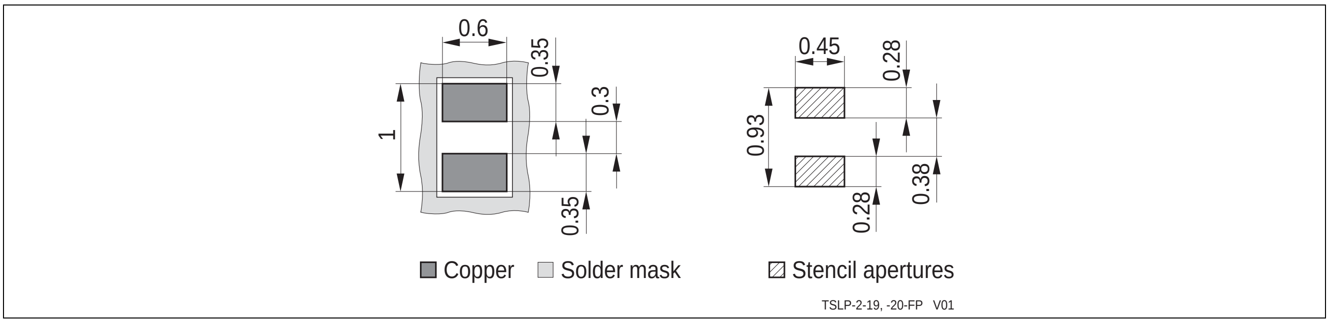


Figure 14 TSLP-2-20 Footprint

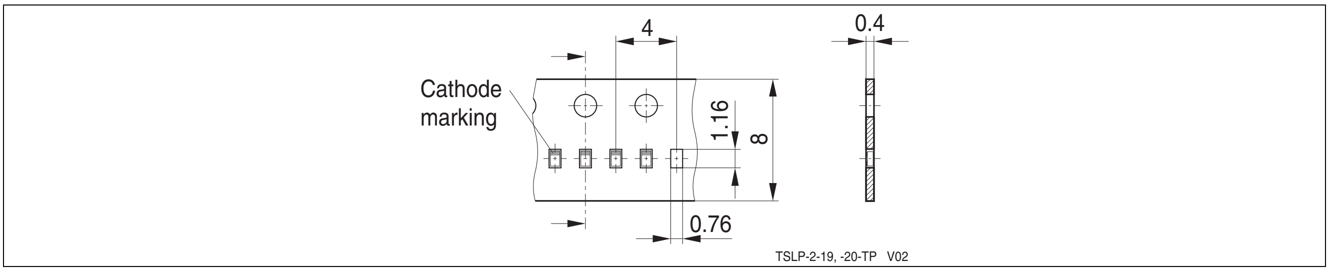


Figure 15 TSLP-2-20 Packing

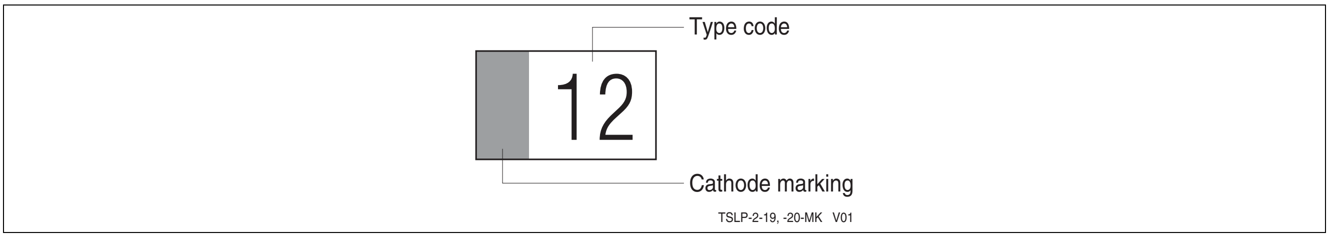


Figure 16 TSLP-2-20 Marking (example)

References

[1] Infineon AG - **Application Note AN210**: Effective ESD Protection Design at System Level using VF-TLP Characterization Methodology

[2] Infineon AG - Recommendations for PCB Assembly of Infineon TSLP and TSSLP Packages

[3] Tero, Ranta, Juha Ellä, Helena Pohjonen: Antenna Switch Linearity Requirements for GSM/WCDMA Mobile Phone Front-Ends. Nokia Technology Platforms, P.O.Box 86, FIN-24101 SALO.

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