ICL5102 resonant controller IC 2nd generation with PFC for power supply and lighting drivers

Features

- 1.3MHz Maximum Soft Start Frequency
- 500kHz adjustable RUN Frequency
- Integrated PFC and HB controllers
- Supports universal input ($90V_{AC}$ to $305V_{AC}$) and wide output range
- Low count of external components supporting small form factors and a cost efficient design
- All parameters set by simple resistors only
- Junction temperature Range -40℃ to +150℃
- Fast startup < 300ms, $I_{Startup}$ < 100µA
- Power Factor Correction > 99%, THD < 5%
- High efficiency up to 94%
- Active BURST Mode with Power Limitation / low Standby < 300mW / can be disabled
- 3 Phase self-adapting Soft Start
- Brownout Detection
- Boundary mode operation during nominal load and WCM[1] mode during low load down to 0.1%
- Improved THD compensation
- Adjustable PFC current limitation
- Fully integrated 650V high-side driver
- Self-adaptive dead time 250ns – 750ns
- Detection of capacitive operation, overload, short circuit, output over voltage OVP & hot spot over temperature via NTC, Surge protection using in all cases Auto Restart

Potential Applications

- Offline AC-DC Power Supply, LCD TV, Adapter
- LED driver, e.g. commercial or residential lighting systems
- Integrated electronic control gear for LED luminaires

Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

[1] WCM = Wait Cycle Mode = THD optimized DCM

Product Type	Package
ICL5102 51 – 100	PG-DSO-16

Datasheet
www.infineon.com

Please read the Important Notice and Warnings at the end of this document
page 1 of 53

V 1.0
2018-05-18

Description

The resonant controller ICL5102 is designed to control resonant converter topologies. The PFC stage operates in Boundary Mode and WCM mode, supporting low load conditions. Integrated high and low side drivers assure a low count of external components, enabling small form factor designs.

ICL5102 parameters are adjusted by simple resistors only, this being the ideal choice to ease the design-in process. A comprehensive set of protection features using auto restart ensures that the controller detects fault conditions, protecting both drivers and load. Figure 1 shows a typical application.
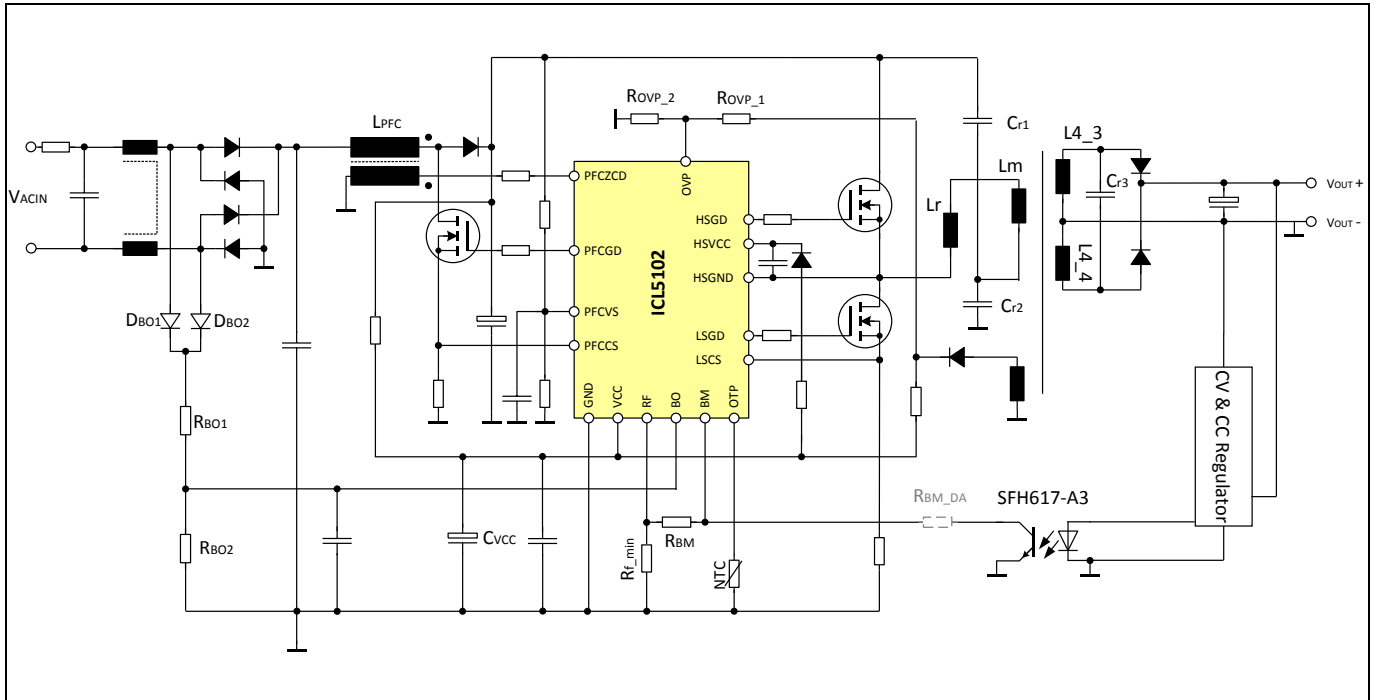

Figure 1   Generic LCC Application

Datasheet
www.infineon.com
Please read the Important Notice and Warnings at the end of this document
page 2 of 53
V 1.0
2018-05-18

Table of Contents

Table of Contents

Datasheet

www.infineon.com

Please read the Important Notice and Warnings at the end of this document

page 4 of 53

V 1.0

2018-05-18

1 Pin Configuration and Description

The pin configuration is shown in Figure 2 PG-DSO-16 Package

LSGD	1		16	HSGD
LSCS	2		15	HSVCC
VCC	3	ICL5102	14	HSGND
GND	4		13	OVP
PFCGD	5		12	BO
PFCCS	6		11	OTP
PFCZCD	7		10	BM
PFCVS	8		9	RF

PG-DSO-16 (150mil)
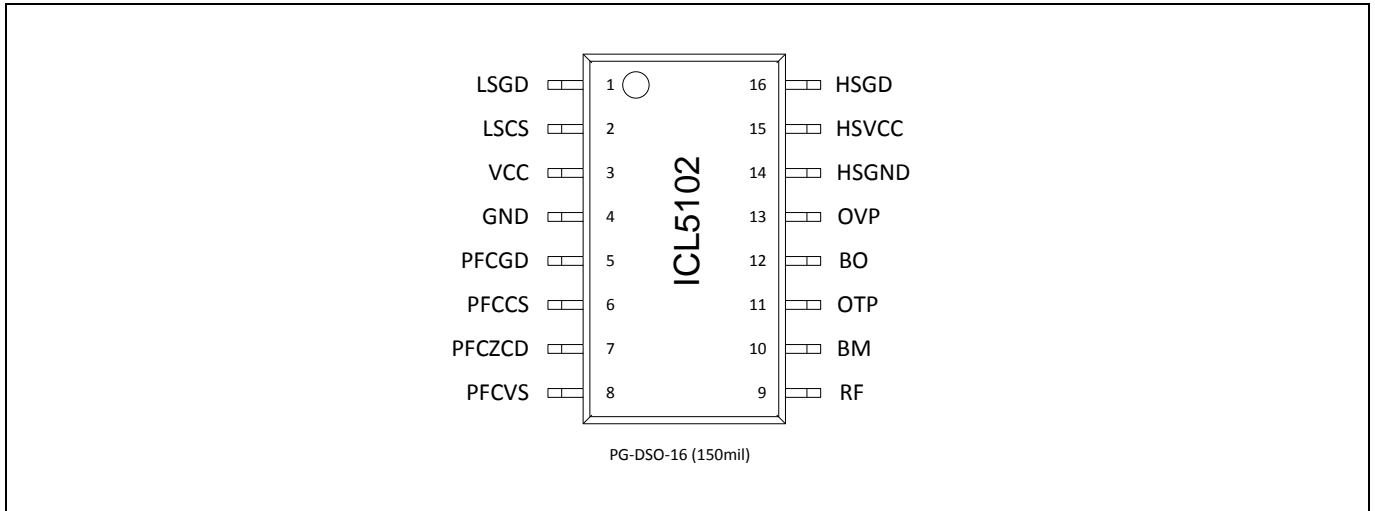
Figure 2 Pin Configuration

1.1 PIN Configuration for PG-DSO-16

Table 1

Symbol	Pin	Function
LSGD	1	Low-side gate drive
LSCS	2	Low-side current sense signal
VCC	3	Low-side chip supply voltage
GND	4	IC GND
PFCGD	5	PFC gate drive
PFCCS	6	PFC current sense signal
PFCZCD	7	PFC zero crossing detection / THD Optimzation
PFCVS	8	PFC voltage sensing
RF	9	RUN frequency setting
BM	10	Burst mode setting
OTP	11	Over Temperature protection
BO	12	Brown out detection
OVP	13	Overvoltage protection
HSGND	14	High-side GND
HSVCC	15	High-side supply voltage
HSGD	16	High-side gate drive

Datasheet
www.infineon.com

Please read the Important Notice and Warnings at the end of this document
page 5 of 53

V 1.0
2018-05-18

1.2 PIN Set-Up

The PIN set-up of ICL5102 for a typical PFC / LLC converter is shown in Figure 3.

Figure 3 PIN Set-Up

Datasheet
www.infineon.com
Please read the Important Notice and Warnings at the end of this document
page 6 of 53
V 1.0
2018-05-18
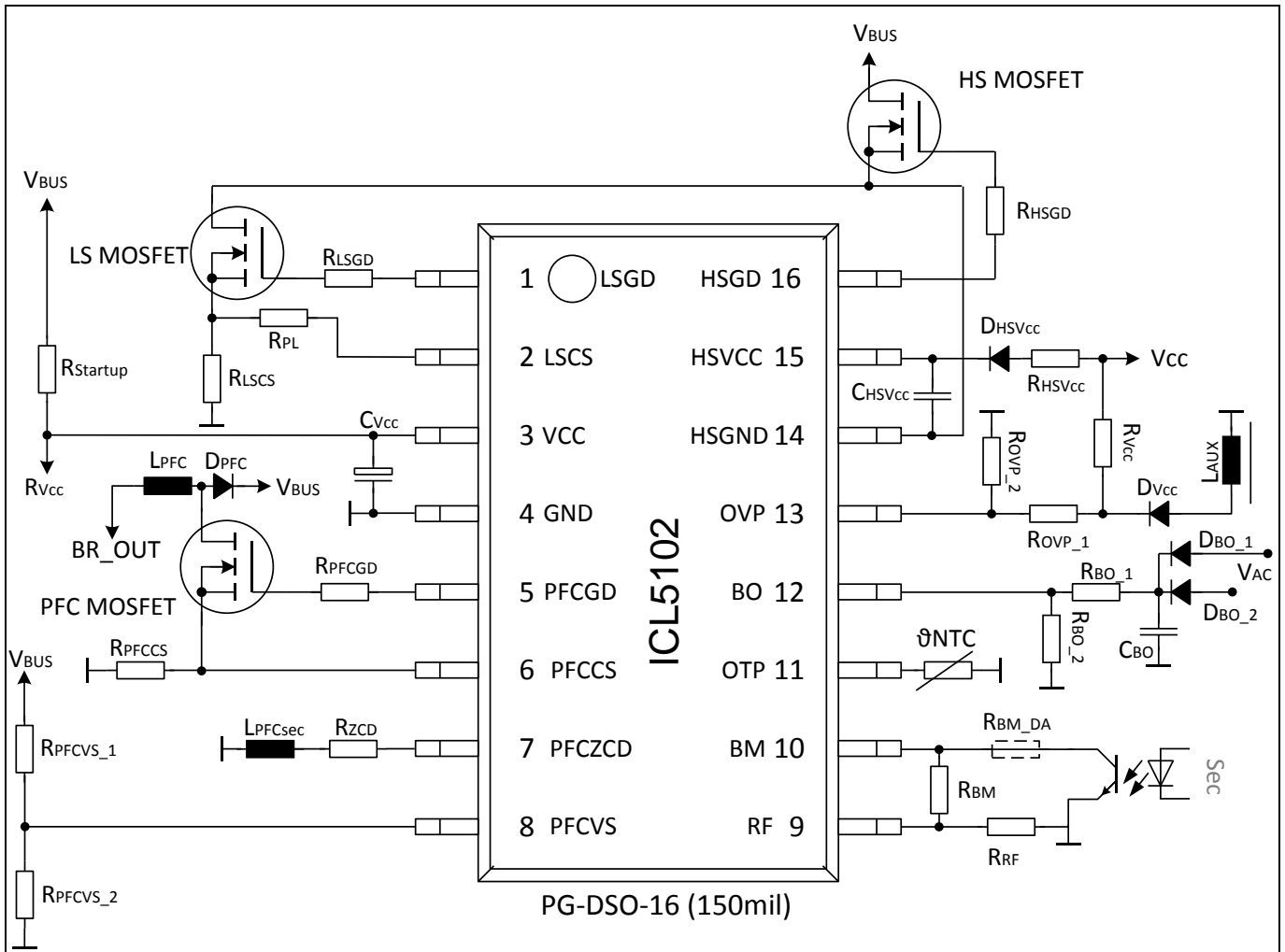
1.3 PIN Functionality

Table 2   Pin Definitions and Function

Symbol	Pin	Function
LSGD	1	**Low-Side Gate Drive** The gate of the low-side MOSFET in a resonant inverter topology is controlled by this pin. The drivers of the ICL5102 are in voltage mode. There is an active low level during UVLO (under voltage lockout) and a limitation of the max high level at 11.0V during normal operation. In order to turn on the MOSFET softly (with a reduced di_{DRAIN}/dt), the gate voltage rises typically within 275ns from low level to high level. The rising time limits the driver current. The source current (here negative) and the maximum high level defining the MOSFET capacitance The fall time of the gate voltage is less than 50 ns in order to turn off quickly. This measure produces different switching speeds during turn-on and turn-off as it is usually achieved with a diode parallel to a resistor in the gate drive loop. It is recommended to use a resistor of typically 22Ω between the drive pin and gate in order to avoid oscillations.The maximum gate capacitance should not exceed Cg = 1.8nF. The dead time between the LSGD signal and HSGD signal is self-adapting between 250ns and 750ns. The pin is protected against negative voltage when switched to low.
LSCS	2	**Low-Side Current Sense Signal** This pin is connected via a serial resistor to the shunt, which is located between the source terminal of the low-side MOSFET of the inverter and ground. Internal clamping structures and filtering measures allow sensing of the source current for the low side inverter MOSFET without additional filter components. There is a first threshold of 0.8V sensed during each ½ cycle. If this threshold is reached, the over current control increases the frequency until the signal is below 0.8V. If this signal is present for longer than 50ms, the controller powers down and auto restarts the system. If the sensed current signal exceeds a second threshold of 1.6V for longer than 500ns, the IC stops the half bridge MOSFETs. There are further thresholds active at this pin to detect capacitive mode operation. A voltage level below -50mV in the second half of the LSGD ON indicates faulty operation (operation below resonance). The 1.6V threshold senses even short over currents during turn-on of the high-side MOSFET as typical for reverse recovery currents of a diode. If one of these comparator thresholds indicates incorrect operating conditions for longer than 620µs the IC turns off the gates and changes to fault mode due to detected capacitive mode operation. See chapter 2.6 The threshold of -50mV is also used to adjust the dead time between turn-off and turn-on of the resonant drivers in a range of 250ns to 750ns during all operating modes. See chapter 2.8 The capacitive load regulation will be active if the threshold of +50mV is reached within the first 7 % of the period. In order to prevent a capacitive switching operation, the controller increases the frequency until the area of capacitive switching is left. See chapter 2.6

VCC	3	**Low-Side Chip Supply Voltage**
		This pin provides the power supply of the ground-related section of the IC. There is a turn-on threshold at typ. 16.0V and an UVLO threshold at typ. 9.0V. The upper supply voltage limit is $V_{CCabsmax}$ = 18.5V. There is an internal VCC clamping at 16.3V (at I_{VCC} = 2mA typically). The maximum Zener current is internally limited to 5mA. The clamping is only active after startup; this ensures a safe start up. An external Zener diode is required for higher current levels. Current consumption during UVLO and during fault mode is less than typ. 80 µA. A ceramic capacitor close to the supply and GND pin is required in order to act as a low-impedance power source for gate drive and logic signal currents. For external Vcc supply make sure, that UVLO is possible. Due to the extended V_{CC} = 18.5V, for the initial Start Up, a 17V Zener diode can be used due to the very low start up current see chapter 2.1
GND	4	**IC GND** This pin is connected to ground and represents the ground level of the IC for the supply voltage, gate drive and sense signals.
PFCGD	5	**PFC Gate Drive** The gate of the MOSFET in the PFC pre-converter designed in boost topology is controlled by this pin. There is an active low level during UVLO and a limitation of the max high level at 11.0V during normal operation. In order to turn on the MOSFET softly (with a reduced di_{DRAIN}/dt), the gate drive voltage rises within 245ns from low level to high level. The rising time limits the driver current. The source current (here negative) and the maximum high level defining the MOSFET capacitance The fall time of the gate voltage is less than 50ns in order to turn off quickly. The maximum gate capacitance should not exceed Cg = 4nFThe PFC section of the IC controls a boost converter as a PFC pre-converter in wait cycle mode (WCM) and critical conduction mode (CrCM). Typically, the control starts with an initial on-time depending on the line input voltage sensed by the BO PIN. Gate drive pulses with a fixed on-time of typically 6.0µs at V_{BO} = 2.0V, increasing up to 24µs and with an off-time of 47µs. As soon as sufficient zero current detector (ZCD) signals are available, the operation mode changes from fixed frequency operation to operation with variable frequency. The PFC works in critical conduction mode operation (CrCM) when rated and/or medium load conditions are present. That means triangular-shaped currents in the boost converter choke without gaps and variable operating frequency. During very low load the operation mode switches into the wait cycle mode (WCM) – that means triangular-shaped currents in the boost converter choke with gaps when reaching the zero current level and variable operating frequency in order to avoid steps in the consumed line current. The Brown Out voltage sets the on-time depending on the line input voltage. The pin is protected against negative voltage when switched to low.
PFCCS	6	**PFC Current Sense Signal** The voltage drop across a shunt resistor located between the source of the PFC MOSFET and GND is sensed with this pin. If the level exceeds a threshold of 1.0V for longer than 200ns, the PFC gate drive is turned off until the zero current detector (ZCD) enables a new cycle.

Datasheet
www.infineon.com

Please read the Important Notice and Warnings at the end of this document
page 8 of 53

V 1.0
2018-05-18

PFCZCD	7	**PFC Zero Crossing Detection**
		This pin senses the current through the boost inductor. If this current becomes zero during the off-time of the PFC MOSFET, the controller initiates a new cycle. A resistor connected between the ZCD winding and PIN 7 limits the sink and source current of the sense pin when the voltage of the ZCD winding exceeds the internal clamping levels (typically 4.6V and -1.4V @ 2mA) of the IC. If the sensed voltage level of the ZCD winding is not sufficient (e.g. during start-up), an internal start-up timer will initiate a new cycle every 52µs after the turn-off of the PFC gate drive. The clamping current out of this pin during the on-time of the PFC MOSFET gives a measure for the momentary input voltage. When the latter is low i.e. close to line zero crossing, the on-time of the PFC MOSFET is enlarged. This helps to minimize gaps in the line current close to zero crossing of the line voltage and improves the THD (Total Harmonic Distortion) of the line current. Optimization of the THD is possible by adjusting the resistor between this pin and the ZCD winding to adapt the THD correction to the boost inductance and PFC MOSFET. In order to calculate this resistor use a zero crossing current in a range of I_{ZCD} = 500µA – 1.2mA depending on design.
PFCVS	8	**PFC Voltage Sensing**
		The intermediate circuit voltage (bus voltage) at the smoothing capacitor is sensed by a resistive divider at this pin. The internal reference voltage for the rated bus voltage is 2.5V. There are further thresholds at < 12.5% of the rated bus voltage for detection of open control loop, < 75% for detection of under voltage during start up. An over voltage is detected during power up if V_{BUS} is > 105%, > 109% and > 115%. The over voltage threshold operates with a hysteresis of 100mV (4% of the rated bus voltage). It is recommended to use a small capacitor between this pin and GND as a spike suppression filter.
		In run mode, PFC over voltage higher than 109% of rated level stops the PFC gate drive within 5µs. As soon as the bus voltage is less than 105% of the rated level, the gate drives are enabled again. If the PFC over voltage 115% lasts for longer than 50ms, an inverter over voltage is detected and turns off the inverter gate drives, too.
RF	9	**Set minimum RUN Frequency**
		A resistor from this pin to ground sets the minimum operating frequency of the LLC / LCC inverter. This frequency limits the maximum output power. The combination of RRF and RBM sets the nominal frequency. This frequency must be lower than the expected run frequency during nominal load condition. The run frequency range is 20kHz to 500kHz. How to calculate the resistors see chapter 2.3.
BM	10	**Burst Mode**
		In order to achieve very low standby power consumption the ICL5102 has an integrated active burst mode. Active burst mode means, that the IC can leave the burst mode any time based on 4 different burst mode exit conditions. A resistor R_{BM} from pin 10 (BM) to RF (PIN 9) sets the max operating frequency when the IC should enter the burst mode depending on the load situation. Furthermore, it is possible disable burst mode by setting a resistor R_{BM_DA} from the opto coupler to BM PIN 10. How to calculate the resistor R_{RF} and R_{BM} see chapter 2.3 and 2.4. **During burst mode** the IC drives the BM pin as an output to generate the soft start ramp and soft on / soft off.

Datasheet

www.infineon.com

Please read the Important Notice and Warnings at the end of this document

page 9 of 53

V 1.0

2018-05-18

OTP	11	**Over Temperature Protection**
		The Over Temperature protection detects the temperature via an external NTC temperature sensor located on the PCB. If the voltage VOTP1 is < 703mV during start-up, the controller prevents a power up. If the voltage at pin 11 drops below VOTP2 < 625mV during RUN or Burst Mode, the IC powers down and auto restarts when VOTP > 703mV. Delay in both cases is 620 µs, the typical current at this pin is IOTP = 100µA. In case of using OTP, set a parallel capacitor from the NTC to GND of max. 1nF. If this function is not in use, a 20k resistance can be connected from PIN 11 to GND.
BO	12	**Brown Out Detection**
		AC line lnput voltage feedforward to set the initial pulse time for the PFC during the very first START UP and the max on-time – depending on the line input voltage. Furthermore, the brown out pin sets the fixed PFC gate pulse width during Burst Mode depending on line input voltage. The voltage at this pin must be above $V_{BO} = 1.4V$ during monitoring to enable a brown in. If the voltage at this pin drops below $V_{BO} = 1.2V$ for longer than 50ms during operation, a brown out is detected and the controller powers down and auto restarts the internal system. Use a double rectifier and high ohm resistors for the voltage divider.
OVP	13	**Over Voltage Protection**
		The ICL5102 has an integrated precise and fast reacting output overvoltage protection by sensing the secondary side output at the transformer supply AUX winding after the rectifier diode. This protection can be enabled or disabled. If the voltage at this pin exceeds $V_{OVP} = 2.5V$ for longer than 5µs during the start-up phase, the controller prevents a power up. In case the voltage at pin 13 exceeds during RUN or Burst Mode the $V_{OVP} = 2.5V$ threshold for longer than 5µs, the IC powers down and restarts automatically. To disable this function, set this pin to IC GND.
HSGND	14	**High-Side GND**
		This pin is connected to the source terminal of the high-side MOSFET, which is also the output of the half bridge. This pin represents the floating ground level of the high-side driver and the high-side supply.
HSVCC	15	**High-Side Supply Voltage**
		This pin provides the power supply of the high-side section of the IC. An external capacitor between pins 14 and 15 acts as bootstrap capacitor, which has to be recharged cycle by cycle via a high-voltage diode from the low-side supply voltage during the on-time of the low-side MOSFET. An UVLO threshold with hysteresis enables the high-side section at 10.4V and disables it at 8.6V.
HSGD	16	**High Side Gate Drive**
		The gate of the high-side MOSFET in a resonant inverter topology is controlled by this pin. There is an active low level during UVLO and a limitation of the max high level at 11.0V during normal operation. The switching characteristics are the same as described for LSGD (pin 1). The rising time limits the driver current. The source current (here negative) and the maximum high level defining the MOSFET capacitance The maximum gate capacitance should not exceed Cg = 1.8nF. The dead time between the LSGD signal and HSGD signal is self-adapting between 250ns and 750ns (typically).

Datasheet
www.infineon.com

Please read the Important Notice and Warnings at the end of this document
page 10 of 53

V 1.0
2018-05-18

2 Feature Description

2.1 Start Up

The sequence of the start-up: the ICL5102 starts with PFC first (see Figure 4). After the PFC BUS voltage is exceeding the V_{PFCVS} = 75% threshold, the half bridge starts working. The time from the IC start-up is depending how fast the PFC BUS voltage is reaching the 75 % level (see Figure 31).
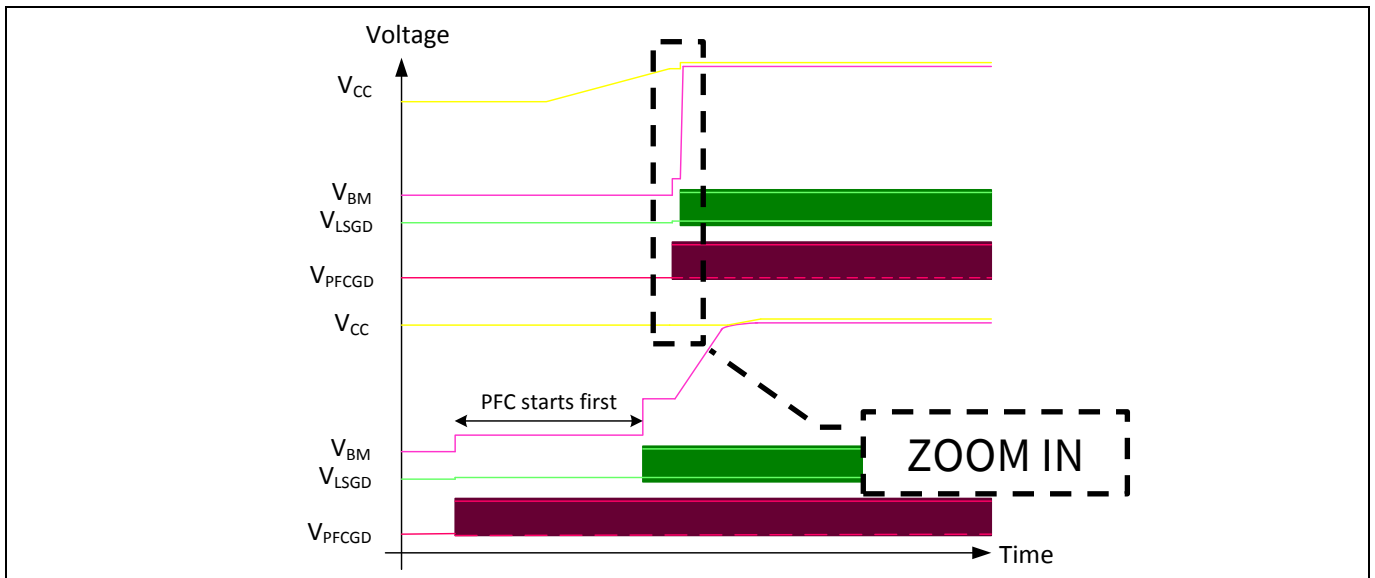
Figure 4   **Start Up Sequence**

Datasheet

www.infineon.com

Please read the Important Notice and Warnings at the end of this document

page 11 of 53

V 1.0

2018-05-18

2.2 Soft Start

The soft start consists of 3 subsequent states within a piecewise linear frequency ramp with a total minimum duration of t < 7ms. In case the LSCS peak voltage $V_{LSCSpeak} > 0.8V$, the ICL5102 stops at the frequency of the frequency ramp and continues the frequency shift when $V_{LSCSpeak} < 0.8V$.

The initial soft start frequency at line voltage first ON or at auto restart is:

$$f_{SoftStart} = 4*(f_{MAX} - f_{MIN}) + f_{MIN}$$

Equation 1: Initial Soft Start Frequency

During state 1 the frequency drops down within 624µs as in the followed equation:

$$f_{SS\_1} = 2.6*(f_{MAX} - f_{MIN}) + f_{MIN}$$

Equation 2: Soft Start Frequency in State 1

During state 2 the frequency ramps down to f_{MAX} within 2.5ms

$$f_{SS\_2} = f_{MAX}$$

Equation 3: Soft Start Frequency in State 2

During state 3 the frequency ramps down to f_{MIN} within 3.75ms

$$f_{SS\_3} = f_{MIN}$$

Equation 4: Soft Start Frequency in State 3

During state 1 and 2, the voltage at the BM pin is driven internally to $V_{BM} = 0.75V$. During state 3, the voltage at the BM pin ramps up from 0.75V up to 2.25V.

During soft start the voltage at the BM pin is driven by an internal ramp generator. This ramp generator can only sink current. Once the external opto-coupler takes away all current through the R_{BM} resistor from the ramp generator the soft start ends. The operational range for the maximum initial soft start frequency f_{InSS} is 1300kHz.

Datasheet
www.infineon.com

Please read the Important Notice and Warnings at the end of this document
page 12 of 53

V 1.0
2018-05-18

2.3 Frequency Setting

A Resonant Converter changes the frequency from a given minimum frequency fmin (full load, maximum power delivery) to a certain maximum frequency fmax that is reached at light load. The minimum frequency has to be chosen such that the converter doesn't enter capacitive switching under any load condition. The maximum frequency must not be too high in order to reduce switching losses and not compromise EMI.

In ICL5102 PIN RF delivers a constant voltage of V_{RF} = 2.5V. The current out of this pin defines the operating frequency, with a frequency to current ratio C_{FC} (typically 4.0 * 10^8 Hz/A). PIN BM is internally clamped to V_{BMmax} = 2.25V. The minimum and maximum frequencies f_{min} and f_{max} are set by the resistors R_{RF} and R_{BM} shown in the block diagram in Figure 6.

2.3.1 Maximum Frequency f_{MAX} of the ICL5102

The maximum RUN frequency f_{MAX} should not exceed the f_{RF5_MAX} as shown in chapter 5.5.3. The correlation between the user defined minimal frequency f_{MIN} and the absolute maximum working frequency f_{MAX} is given by:

$$f_{MAX} < 7 * f_{MIN}$$

Equation 5: Calculation of the maximum Frequency

2.3.2 Minimum Frequency f_{MIN} @ maximum Load

f_{MIN} is reached when the collector current of opto-coupler OC1 is 0µA and the whole current through R_{BM} flows into PIN BM. That means $V_{BM} = V_{BMmax}$ = 2.25V in this operating point.

$$f_{MIN} = C_{FC} * (I_{RF} + I_{RBM}) = C_{FC} * (\frac{2.5V}{R_{RF}} + \frac{2.5V - 2.25V}{R_{BM}})$$

Equation 6: Calculation of the minimum Frequency

2.3.3 Maximum Frequency f_{MAX} Before Entering Burst Mode

f_{MAX} is reached when the opto-coupler current is high enough to lower the voltage @ BM to 0.75V.

$$f_{MAX} = C_{FC} * (I_{RF} + I_{RBM}) = C_{FC} * (\frac{2.5V}{R_{RF}} + \frac{2.5V - 0.75V}{R_{BM}})$$

Equation 7: Calculation of the maximum Frequency

2.3.4 Calculation of R_{RF} and R_{BM}

In order to determine the values for R_{RF} and R_{BM} the frequencies fmin and fmax must be defined as mentioned above. Equations I and II can then be solved for R_{BM} and R_{RF}:

Datasheet
www.infineon.com
Please read the Important Notice and Warnings at the end of this document
page 13 of 53
V 1.0
2018-05-18

$$R_{BM} = C_{FC} * \frac{1.5V}{(f_{MAX} - f_{MIN})} = 4.0*10^8 \frac{Hz}{A} * \frac{1.5V}{(f_{MAX} - f_{MIN})}$$

$$R_{RF} = C_{FC} * \frac{15V}{(7*f_{MIN} - f_{MAX})} = 4.0*10^8 \frac{Hz}{A} * \frac{15V}{(7*f_{MIN} - f_{MAX})}$$

Equation 8: Calculation of R_{BM} and R_{RF}

Datasheet

www.infineon.com

Please read the Important Notice and Warnings at the end of this document

page 14 of 53

V 1.0

2018-05-18

2.3.5 Minimum typical Frequency versus Resistance

Figure 5 shows how to set the minimum RUN frequency via resistance from the RF pin to GND. Valid if no resistor to BM pin.

Typical Minimum RUN Frequency vs Resistance @ Tj = 25°C
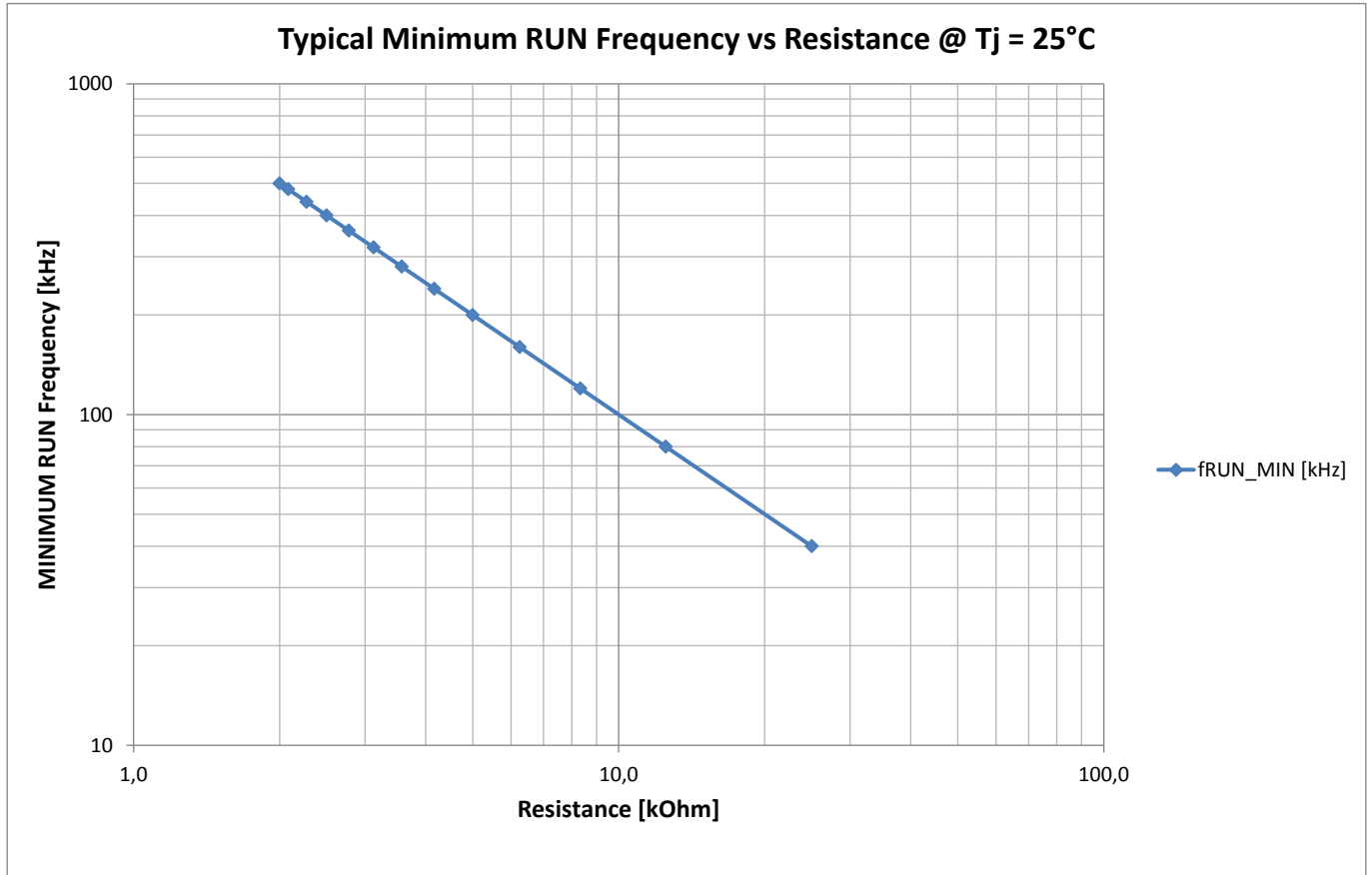
Figure 5 Typical Minimum RUN Frequency vs. Resistance @ Tj = 25°C

2.4 Burst Mode

2.4.1 Burst Mode Introduction

The ICL5102 burst mode is a one PIN concept made for lowest standby power during dimming, no load or µC to reach a STB < 300mW in an ultra-wide range design. The burst mode is self-adapting with an immediate response and covers each kind of load steps. The chip current consumption during Burst Mode is $I_{VCC} \sim 1.5mA$.

Dependent on the voltage at the BM PIN 10, the ICL5102 enters the Burst Mode, starts a burst pulse train, stops the pulse train or exits the burst mode operation in 4 different ways. The block diagram below shows the internal functionality of the burst mode operation. In order to regulate the power during the burst pulse train, a serial resistor R_{PL} from PIN 2 LSCS (see Figure 7) to the shunt resistor can be adjusted experimentally from 200Ω up to 1k depending on the application. Figure 6 shows the block diagram of the burst mode.
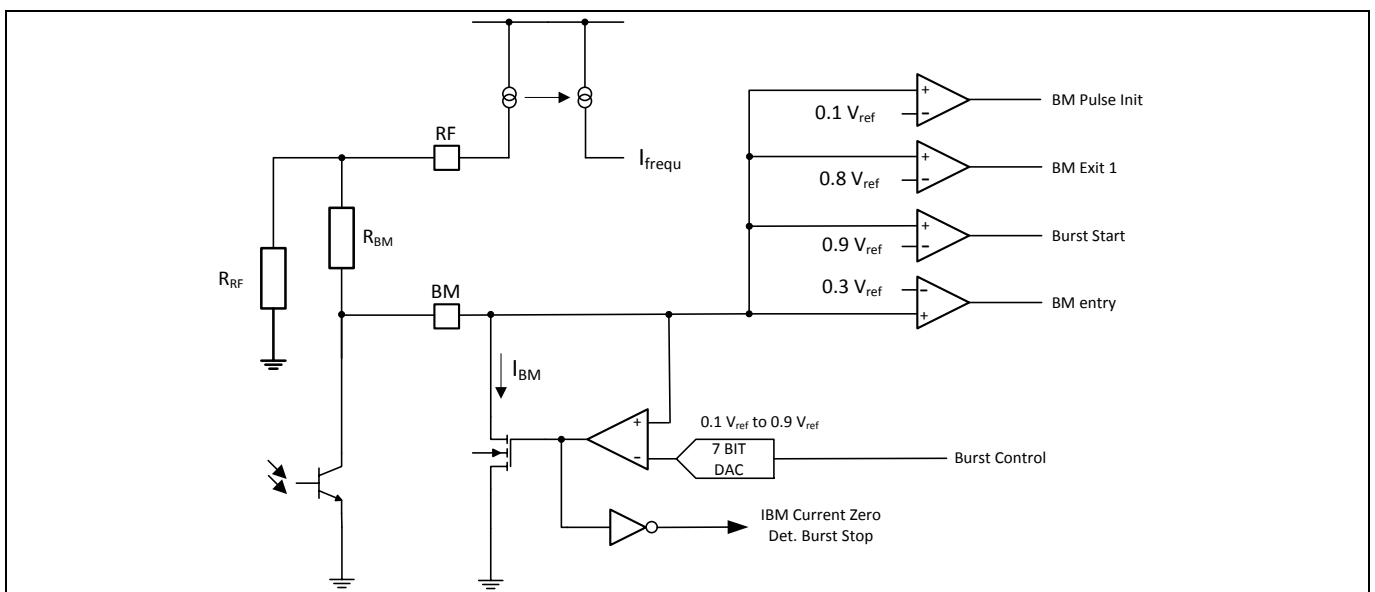
Figure 6 Burst Mode Block Diagram

Furthermore, a ceramic capacitor C_{Opt} at the opto-coupler should not exceed 2.2nF see Figure 7.
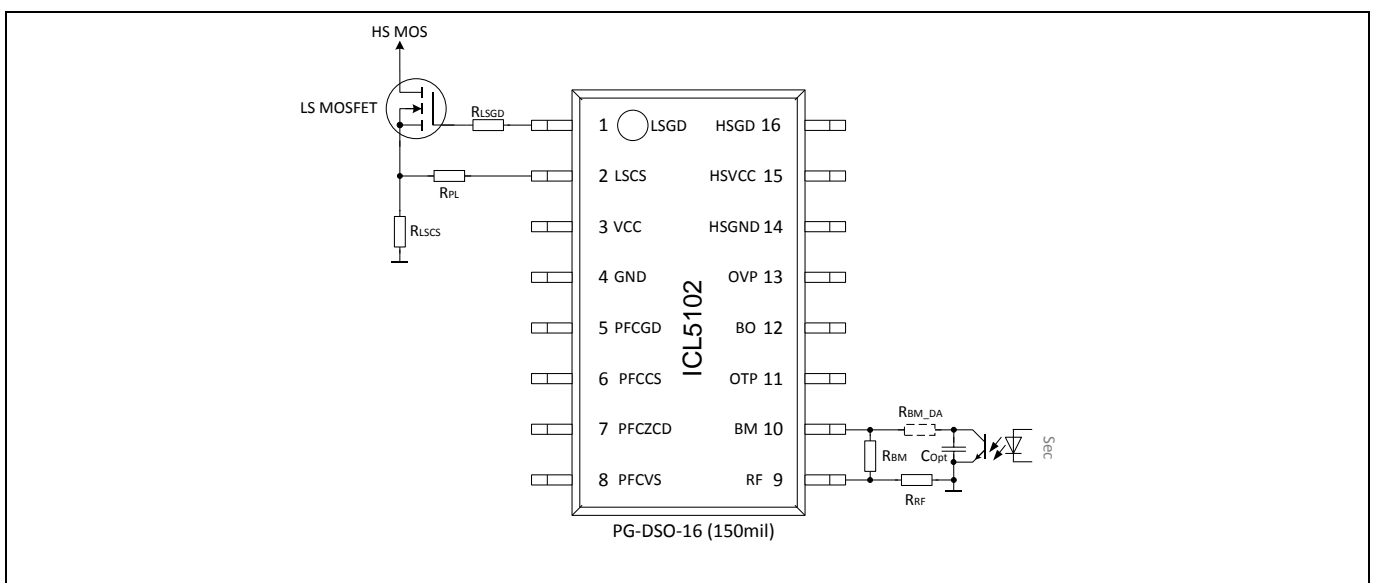
Figure 7 PIN Setup for Burst Mode Operation and Power Limitation during Burst Mode

Datasheet
www.infineon.com
Please read the Important Notice and Warnings at the end of this document
page 16 of 53
V 1.0
2018-05-18

2.4.2 Disable Burst Mode

If the voltage at the BM PIN 10 drops below V_{BM} = 0.75V for longer than 10ms, the burst mode will be entered. A serial resistor resistor R_{BM_DA} (see Figure 7 / calculated via Equation 9) between opto-coupler and BM PIN 10 prevents V_{BM} from going below 0.75V and the ICL5102 from entering burst mode – the burst mode function is disabled.

$$R_{BM\_DA} = \frac{3}{7} * R_{BM}$$

Equation 9: Calculation of R_{BM_DA}

2.4.3 Power Limitation during Burst Pulse

In order to help to prevent audible noise, the ICL5102 limits the power during burst pulse. Figure 8 shows the limitation of power during burst pulse. This can be easily adjusted by the resistor RPL connected to PIN 2 LSCS. This resistor also varies the burst mode pulse frequency.
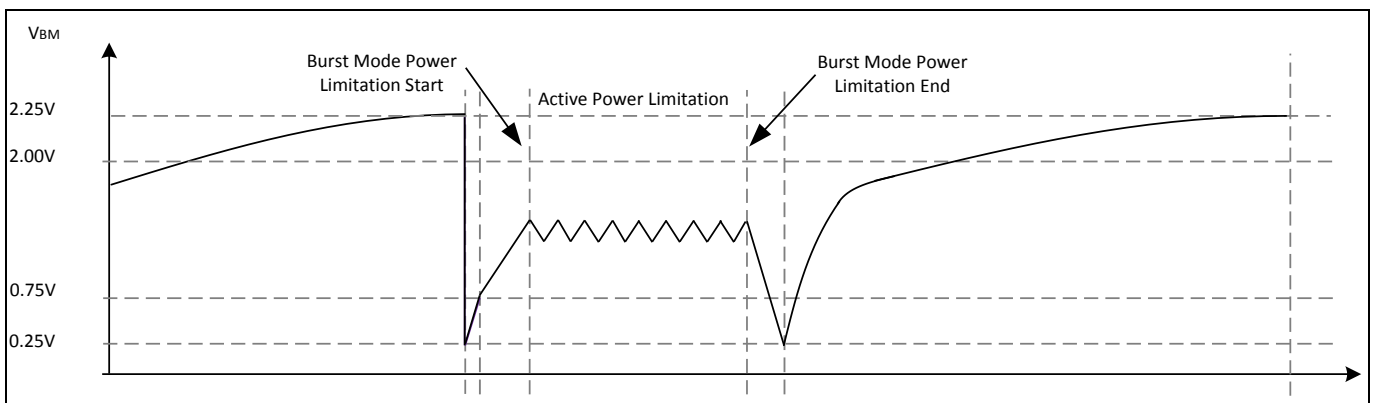
Figure 8   Active Power Limitation during Burst Pulse

2.4.4 Burst Mode Entry

In case of a low load condition, the ICL5102 increases the run frequency until reaching f_{MAX} see Equation 10, the burst mode voltage at the BM PIN 10 will drop below $V_{BM} = 0.75V$.

$$f_{MAX} = C_{FC} * (I_{RF} + I_{RBM}) = C_{FC} * (\frac{2.5V}{R_{RF}} + \frac{2.5V - 0.75V}{R_{BM}})$$

Equation 10: Calculation of the Maximum Frequency before entering the Burst Mode

If the voltage at the BM PIN 10 stays below $V_{BM} = 0.75V$ for longer than $t = 10ms$, the ICL5102 enters the burst mode see Figure 9 (top). In this corridor, the IC increases further the frequency from f_{MAX} up to the soft off frequency $f_{SoftOFF}$ ($f_{SoftOFF} \geq f_{max}$) shown in Equation 11. This guarantees a smooth entry into the burst mode.

$$f_{SoftOFF} = \frac{4}{3} * (f_{MAX} - f_{MIN}) + f_{MIN}$$

Equation 11: Calculation of the Soft OFF Frequency

The ICL5102 starts with a burst sleep phase - all gate drives are off.
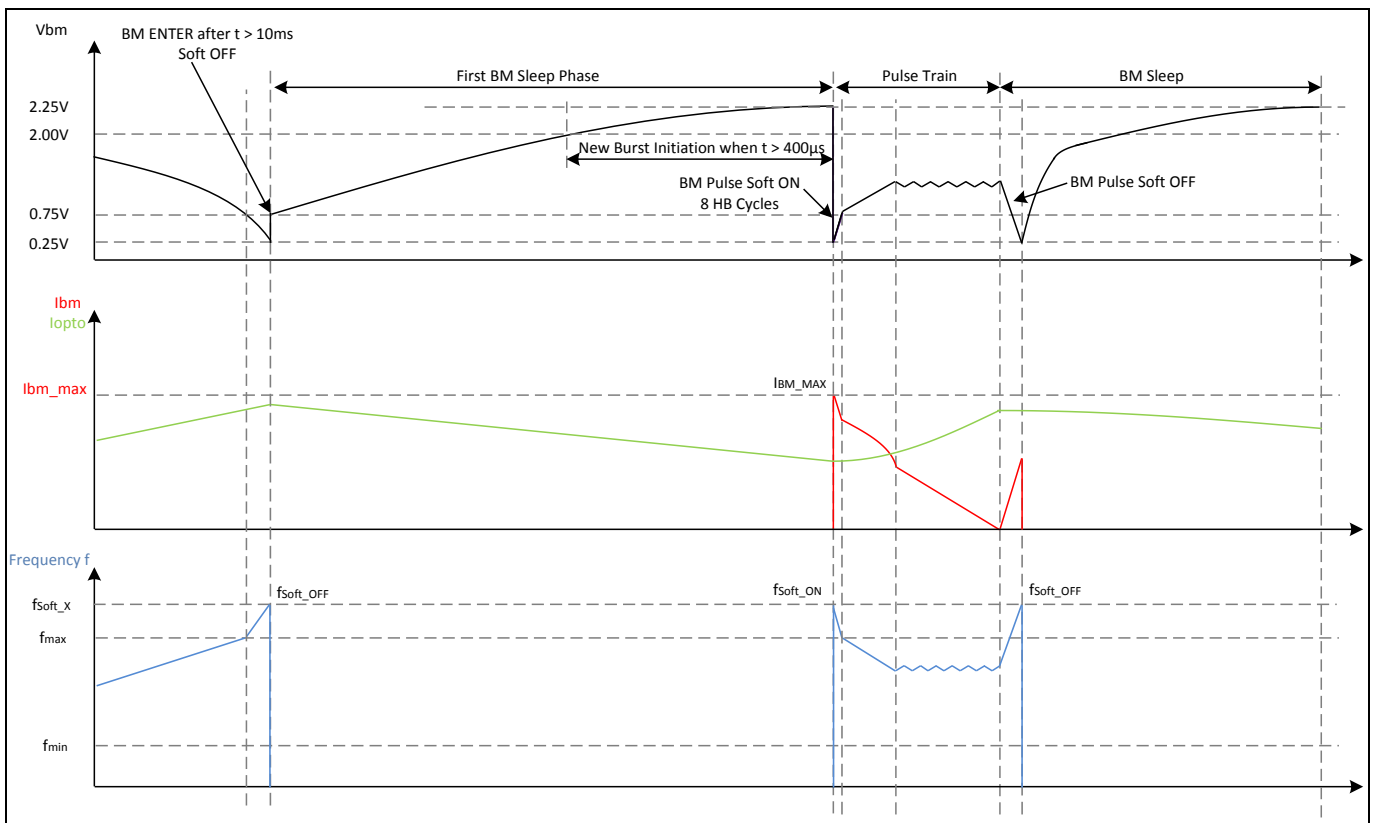
Figure 9   Burst Mode Entry

Datasheet
www.infineon.com
Please read the Important Notice and Warnings at the end of this document
page 18 of 53
V 1.0
2018-05-18

2.4.5 Burst ON (Pulse Train) – Voltage Mode Design

The burst pulse train starts with a higher frequency $f_{SoftON} > f_{max}$ in order to prevent noise or capacitive load operation. Determined by an internal counter, the frequency quickly ramps down to f_{max}. At the end of this ramp a second frequency ramp is reached and decreases the frequency to a stable value. The power will be controlled by the power limitation function of the burst mode. At the same time the current through the opto-coupler is monitored and when it reaches an internally defined value, a soft-off is initiated and the pulse train ends.

Figure 10   Pulse Train

Datasheet
www.infineon.com
Please read the Important Notice and Warnings at the end of this document
page 19 of 53
V 1.0
2018-05-18
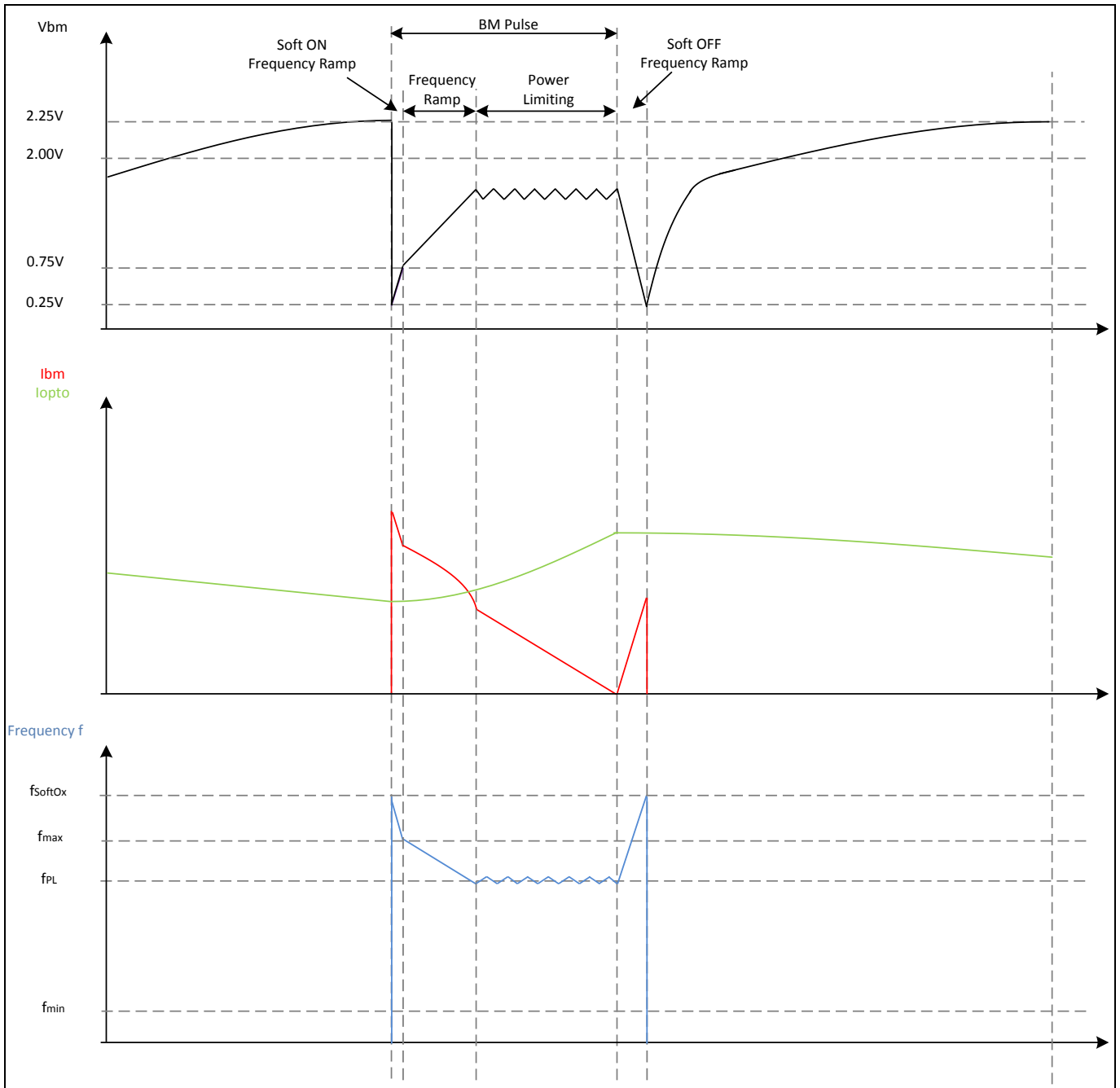
2.4.6 Burst ON (Pulse Train) Phase I: SOFT ON (fixed)

Soft ON Start:

Soft ON will be activated when the voltage at the BM PIN drops to $V_{BM} = 0.25V$. During Soft ON Start, the frequency is internally set to:

$$f_{SoftON} = \frac{4}{3} * (f_{MAX} - f_{MIN}) + f_{MIN}$$

Equation 12: Calculation of the Soft ON Frequency

The internal burst mode current I_{BM} is at the highest level: I_{BM_MAX}.

Soft ON Phase:

During Soft ON phase, an internal Counter reduces the frequency from f_{SoftON} down to f_{MAX}. Also, the internal burst mode current decreases to a certain level.

Soft ON END

The end of soft on is initiated, when the voltage at the BM PIN reaches $V_{BM} = 0.75V$ again.
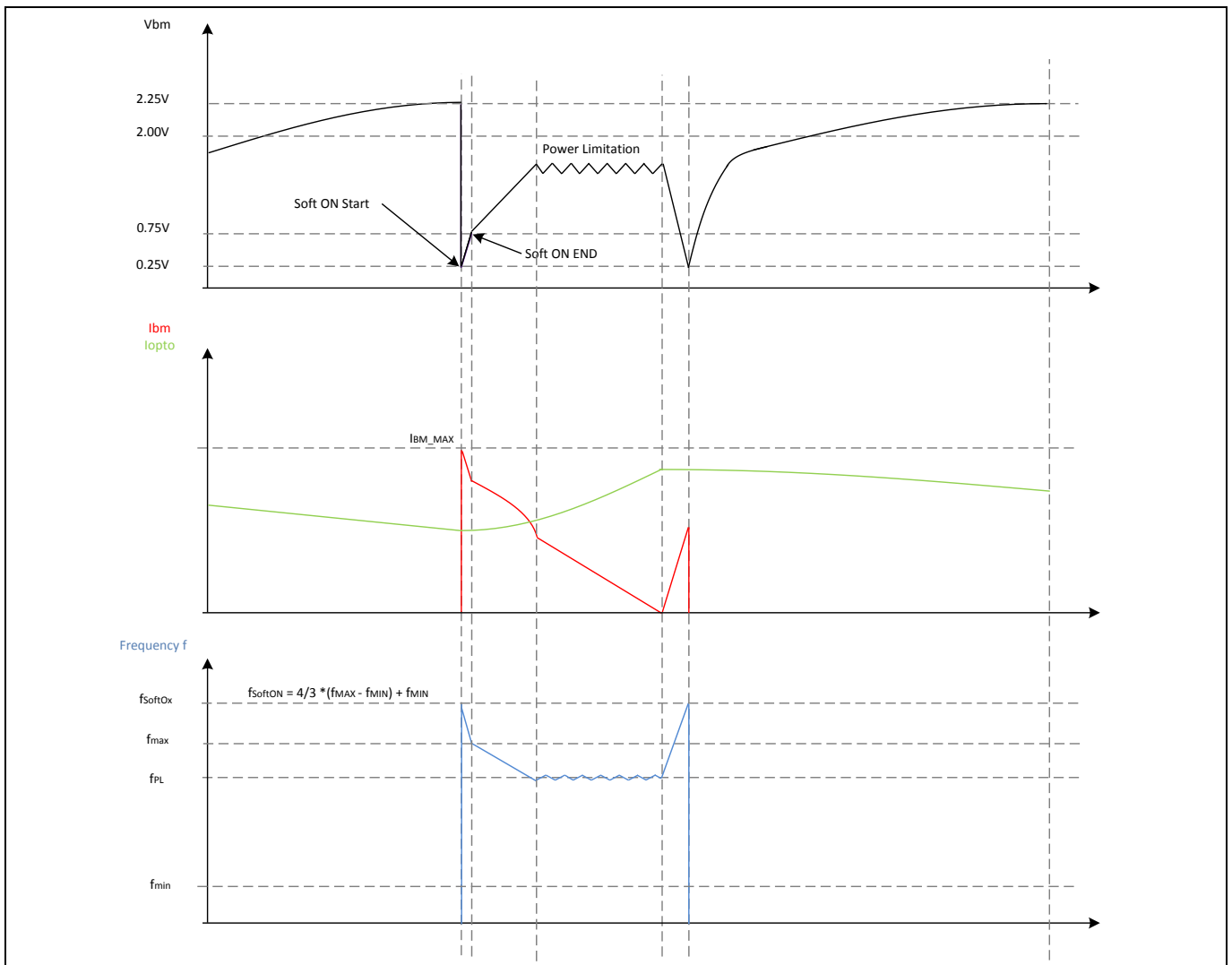
Figure 11   Pulse Train Soft ON

Datasheet
www.infineon.com

Please read the Important Notice and Warnings at the end of this document
page 20 of 53

V 1.0
2018-05-18

2.4.7 Burst ON (Pulse Train) Phase II: Frequency Ramp

The frequency reduces in order to reach the maximum power; the burst mode current I_{BM} decreases also from I_{BM_HIGH} to I_{BM}. Depending on an internal comparator result (see chapter 2.4.8), the frequency will decrease from f_{MAX} to f_{PL} and enters the next phase III (2.4.8).
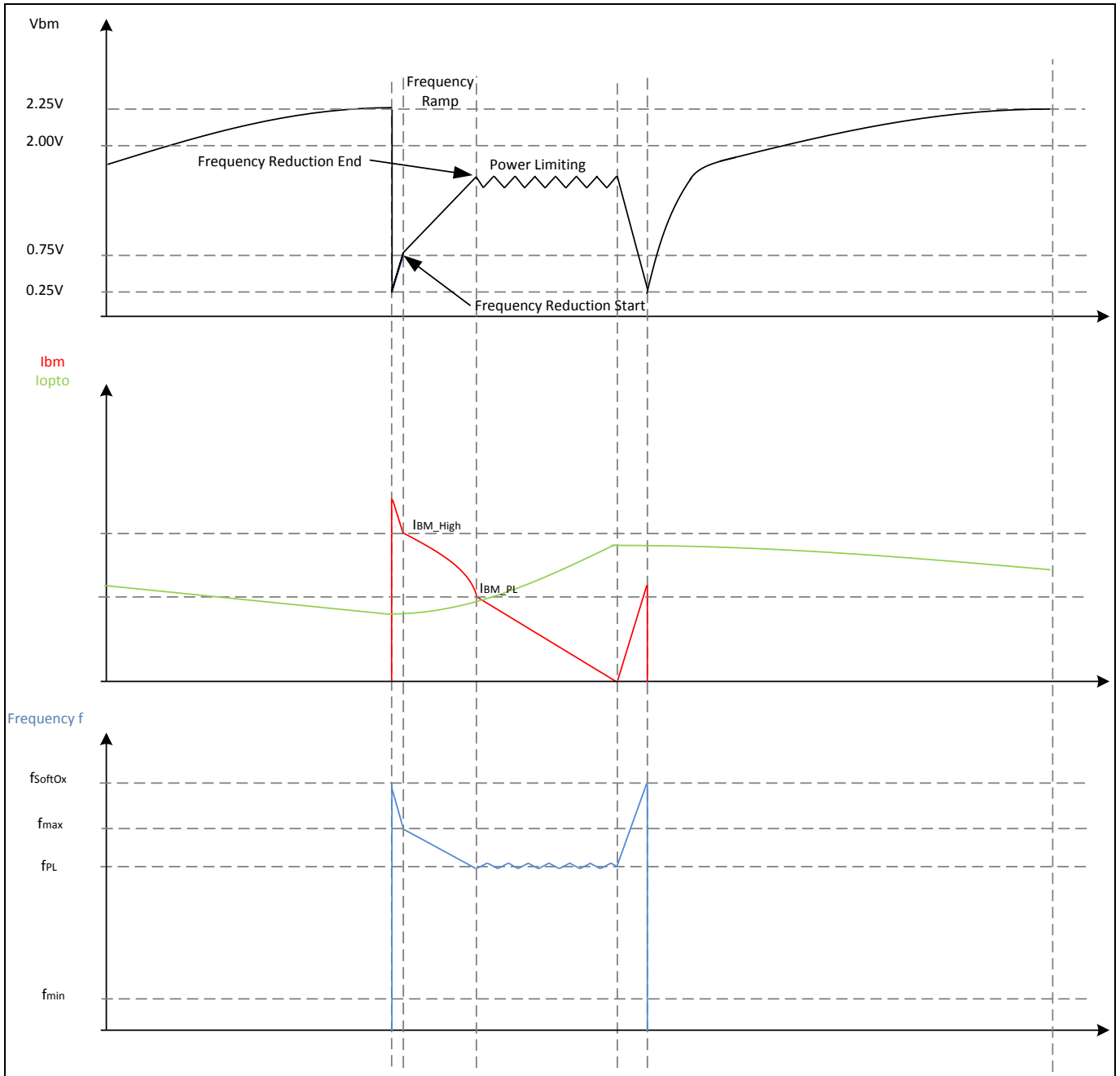
Figure 12   Pulse Train Frequency Ramp

Datasheet
www.infineon.com

Please read the Important Notice and Warnings at the end of this document
page 21 of 53

V 1.0
2018-05-18

2.4.8 Burst ON (Pulse Train) Phase III: Burst Pulse Power Limitation

After adjusting the frequency to the max power in phase II, the controller will hold a constant frequency with a regulation of the power shown in 2.4.7. The opto-coupler current increases, depending on the status of the output stage, and the burst mode sink current decreases from I_{BM_Low} to $I_{BM} = 0\mu A$. In the moment of $I_{BM} = 0\mu A$, the Pulse Train ends after a soft off frequency ramp back to f_{SoftON}.
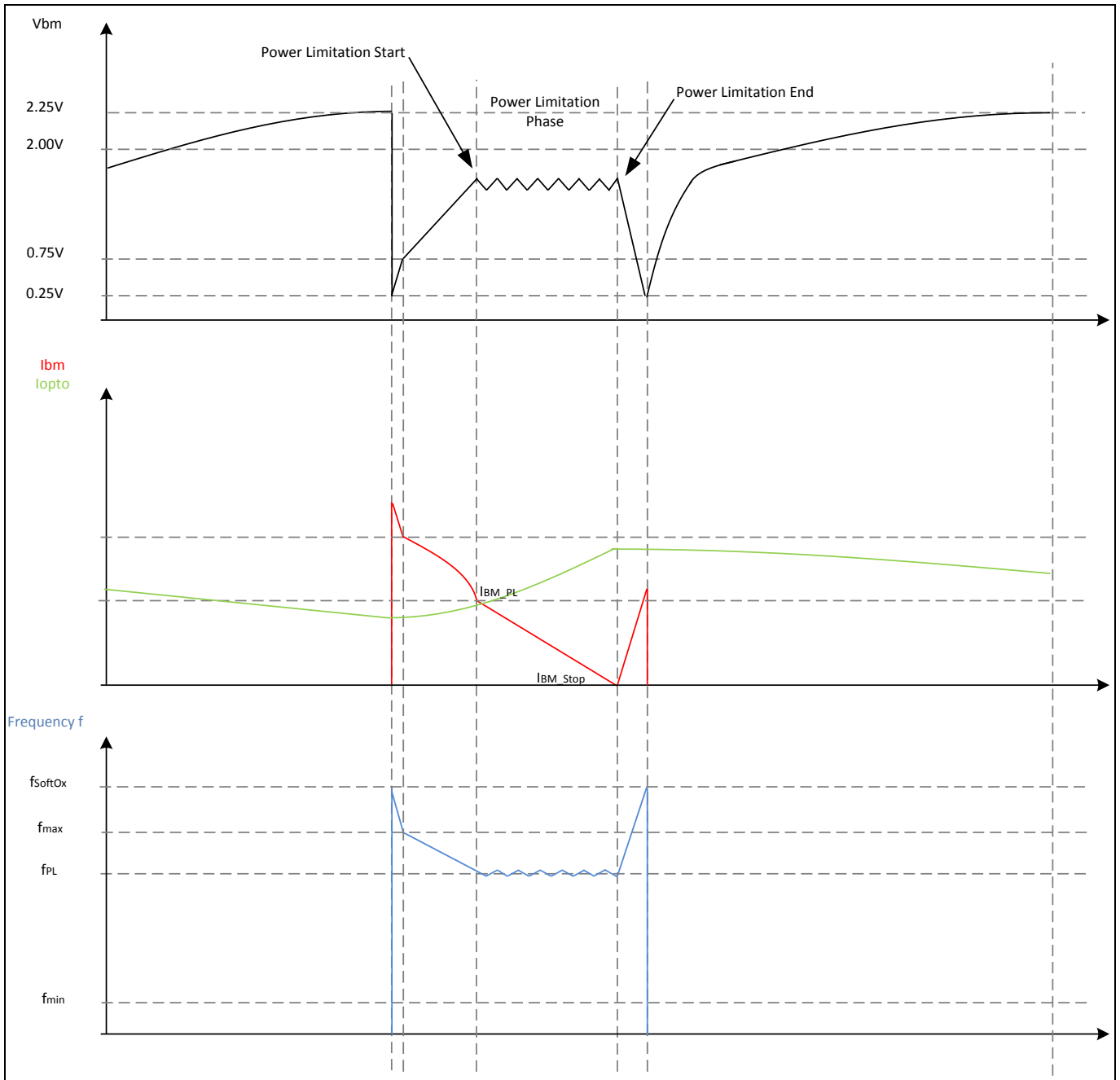
Figure 13   Pulse Train Power Limitation

In Phase III, a serial resistor R_{PL} (see Figure 14) from LSCS to the shunt will set the power limit during burst pulse. The value of this resistor should be between R_{PL} = 200Ω and 1k.
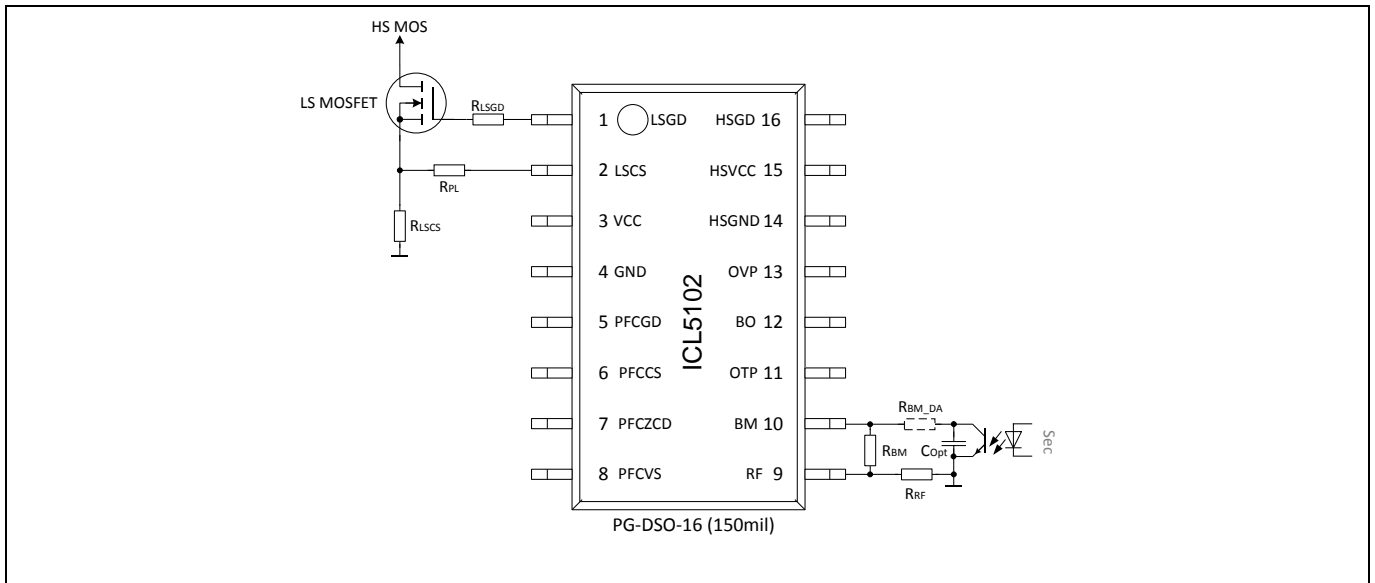
Figure 14   Power Limitation Resistance Setting R_{PL}

During burst pulse power regulation phase, an internal power limitation is active. The threshold of the power limitation can be set by the value of R_{PL} as shown in Figure 14. The voltage at the LSCS PIN will be integrated and compared internally with a 100µA signal see Figure 15.
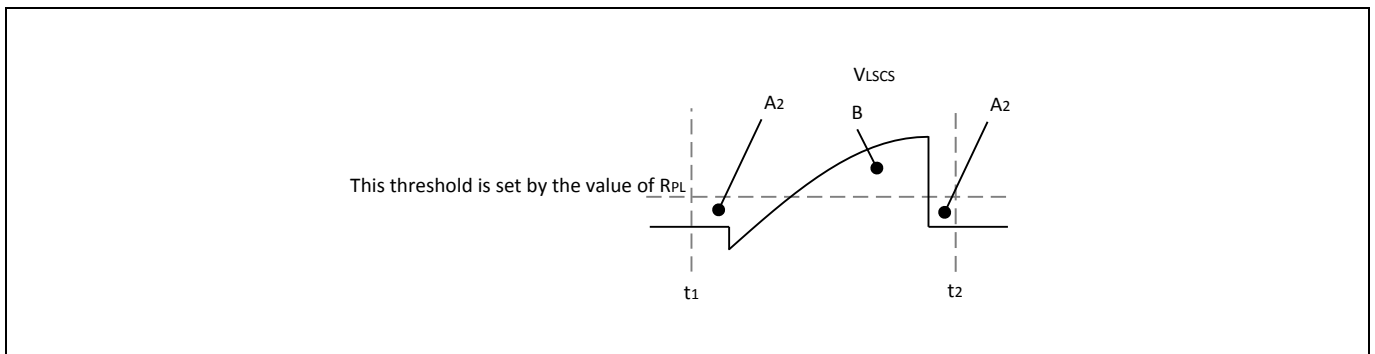
Figure 15   Low Side Current Sense Threshold for Power Limitation

If the area B is greater / less than the areas A1+A2 zero the power limiter increases / decreases the frequency at the same slope as the frequency ramp described in 2.4.7

Datasheet

www.infineon.com

Please read the Important Notice and Warnings at the end of this document

page 23 of 53

V 1.0

2018-05-18

2.5 Burst Mode EXIT

The ICL5102 Burst Mode Concept has 4 different EXIT conditions to jump out of the burst mode operation. The ICL5102 differentiates between 4 load steps conditions during: burst pulse, burst sleep, burst pulse timeout and high static load.

2.5.1 EXIT 1: Load Step during Burst OFF (Sleep)

The condition of exit 1 is a voltage increase from V_{BM} = 2.0V up to V_{BM} = 2.25V within t < 400µs caused due to a load step on the output stage.
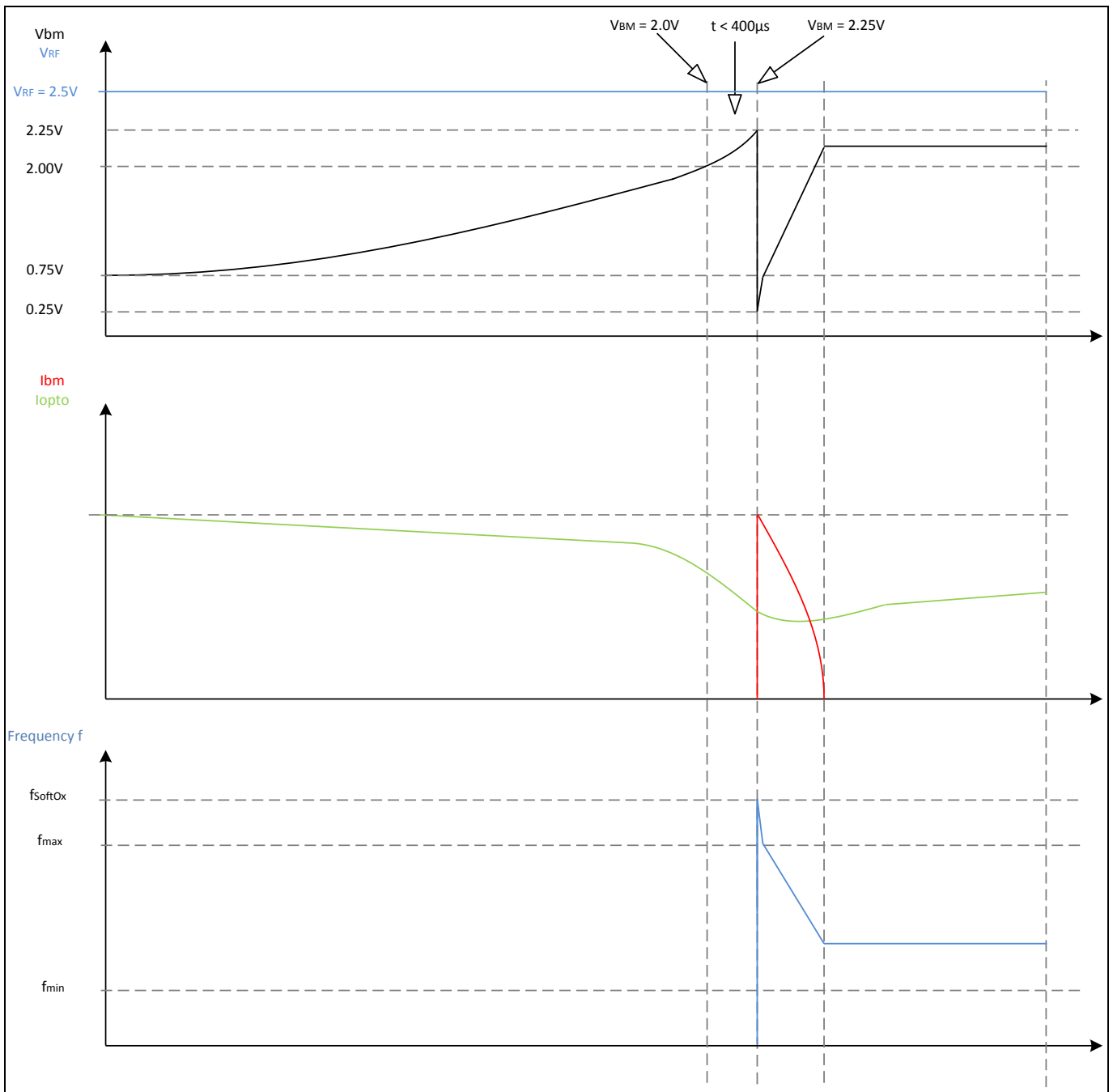
Figure 16 Burst Mode EXIT 1

Datasheet
www.infineon.com

Please read the Important Notice and Warnings at the end of this document
page 24 of 53

V 1.0
2018-05-18

2.5.2 EXIT 2: Load Step during Burst Pulse (Train)

If the BM – voltage increases ΔV_{BM} = + 100mV within 8 cycles, the ICL5102 detects a load step during burst pulse and exits the burst mode operation into normal mode. Background: in case of a load jump, the secondary voltage drops and changes the converters transfer ratio. In order to hold a constant power, the IC reduces the frequency.
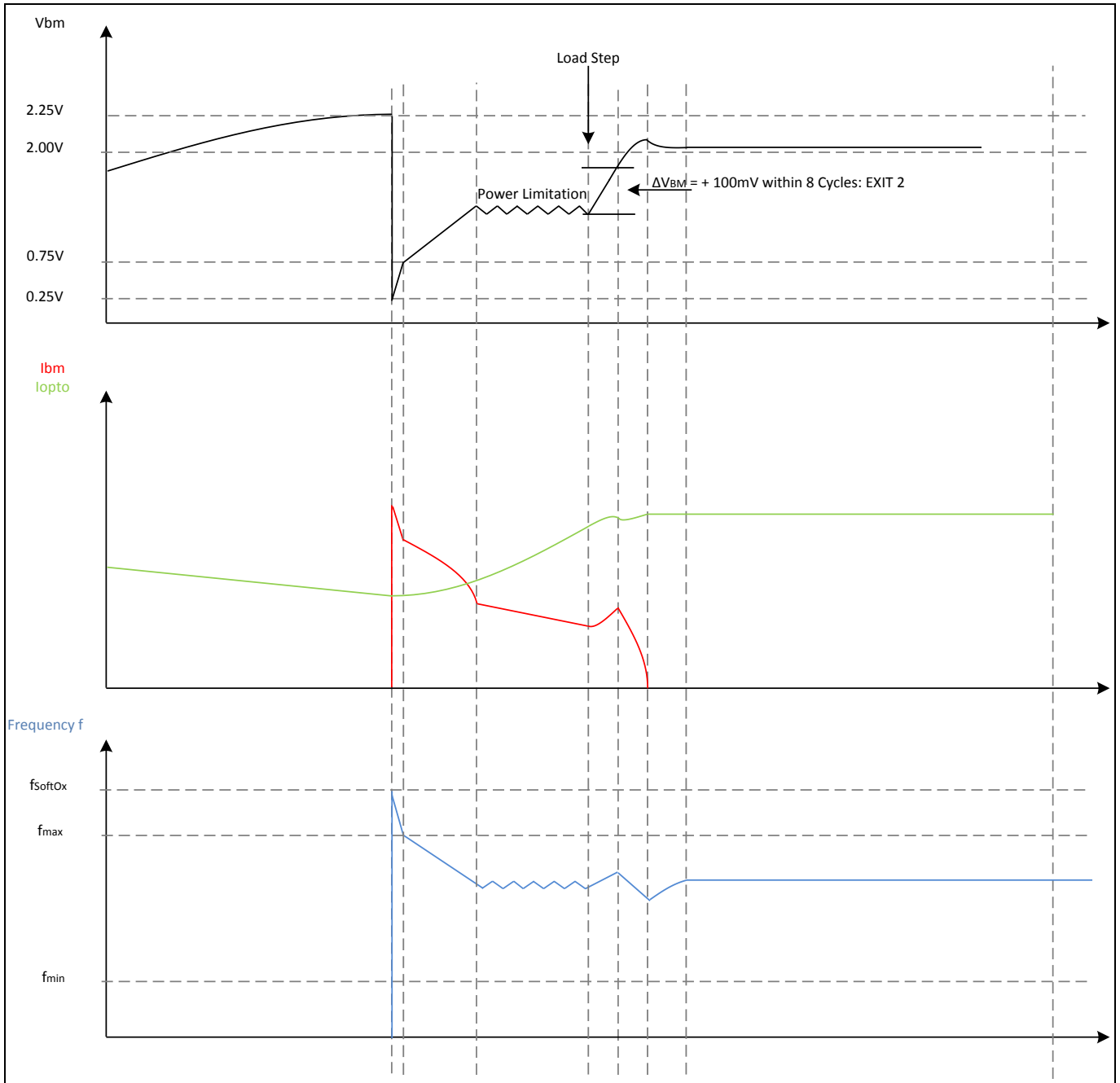
Figure 17 Burst Mode EXIT 2

2.5.3 EXIT 3: Time OUT due to high Static Load while Burst Pulse

As long as the opto-coupler does not take over the whole burst mode current (I_{BM} = 0µA), the ICL5102 stays in the burst train (see Figure 10). If the burst train lasts for longer than 10ms, the ICL5102 detects a high static load and exits the burst train operation (see Figure 18).

Vbm

2.25V
2.00V

0.75V

0.25V

Time OUT: maximum Burst Pulse 10ms

Ibm
Iopto

The Opto-Coupler does NOT take over the whole Burst Mode Current after t > 10ms.

I_{Opto}

$I_{BM} > 0µA$

Frequency f

f_{SoftOx}

f_{max}

f_{min}
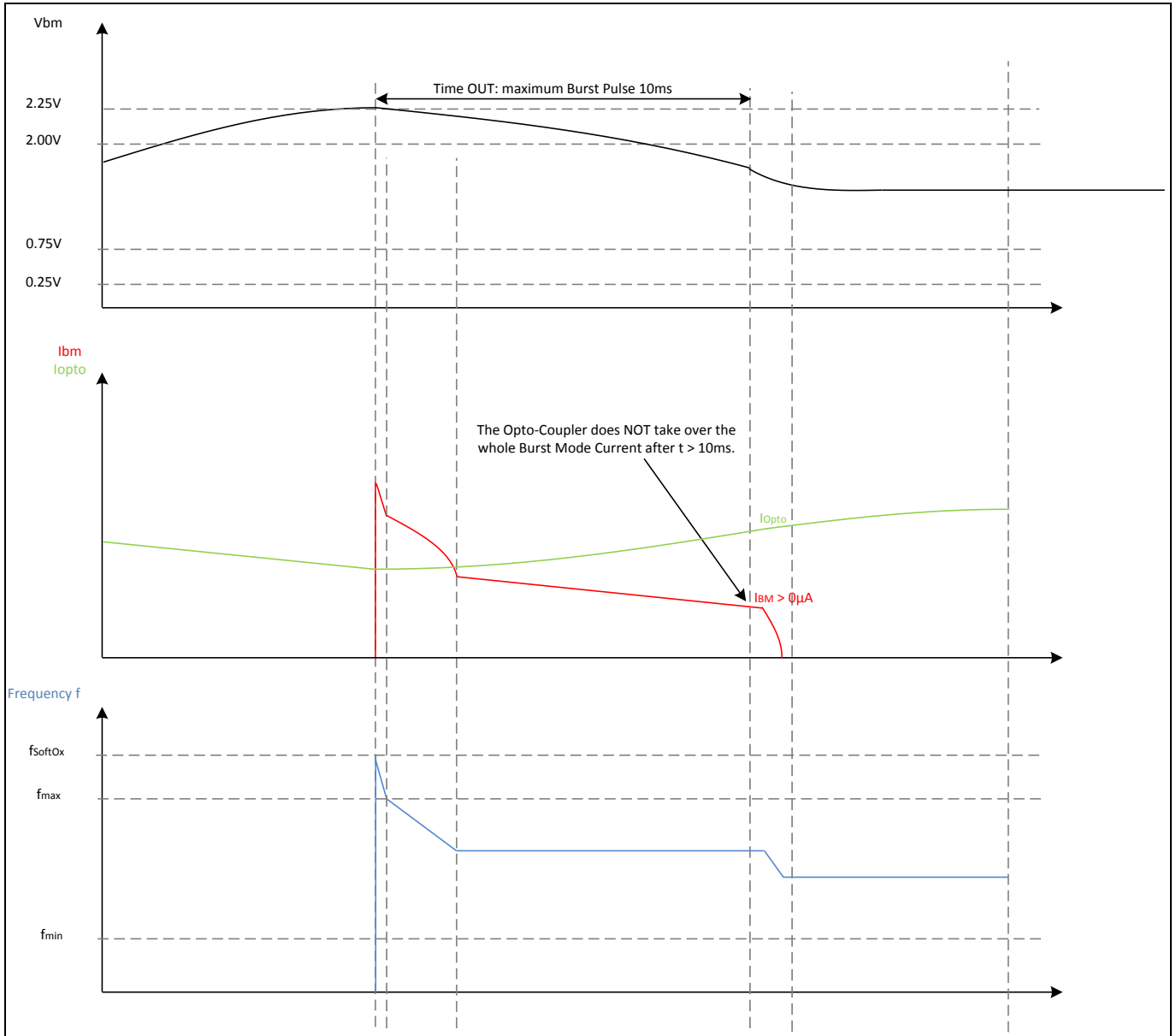
Figure 18 Burst Mode EXIT 3

Datasheet
www.infineon.com

Please read the Important Notice and Warnings at the end of this document
page 26 of 53

V 1.0
2018-05-18

2.5.4 EXIT 4: Duty Cycle of Burst Pulses due to high Static Load

In case a high static load is present, the ICL5102 senses the time of the burst pulse and burst sleep duration. If the burst sleep phase is less than 2 times longer than the burst pulse duration, the ICL5102 detects a high static load and will leave the burst mode operation.

Exit 4 condition:

$t_{BurstPause} < 2 \times t_{BurstPulse}$
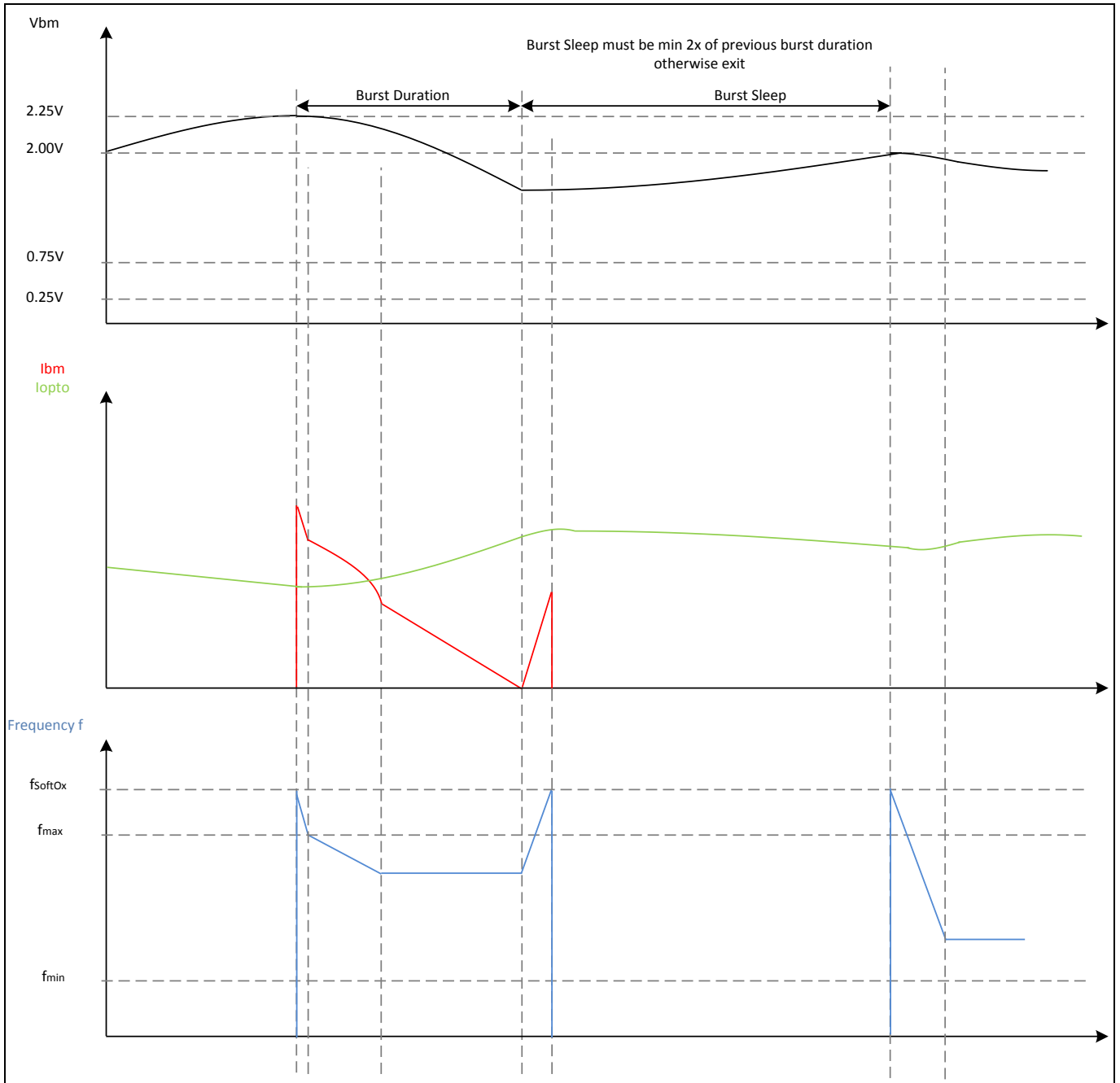
Figure 19 Burst Mode EXIT 4

Datasheet
www.infineon.com
Please read the Important Notice and Warnings at the end of this document
page 27 of 53
V 1.0
2018-05-18

2.6 Capacitive Load Detection and Control

The ICL5102 has 2 different ways to detect a capacitive load operation. Capacitive load detection and capacitive load control.

2.6.1 Capacitive Load Detection

Resonant converter designs should avoid working in capacitive mode operation – not even under abnormal conditions. ICL5102 provides capacitive mode operation detection with Auto Restart. Resonant converters work in capacitive mode when their switching frequency falls below a critical value. This depends on the loading condition and the input-to-output ratio. They are especially prone to enter capacitive mode when the input voltage is lower than the minimum specified and/or the output is overloaded or shorted

Capacitive load operation is detected, if the voltage at the LSCS pin exceeds a first threshold of $V_{LSCSCap1}$ = 1.6V during ON switching of the high-side MOSFET see Figure 24. Or a voltage at the LSCS pin below a second threshold of $V_{LSCSCap2}$ = – 50mV – during the second half of the low side MOSFET ON or directly before the high-side MOSFET is turned on – detects also a capacitive load operation. If this overcurrent is present for longer than 620µs, the IC results a power down into an auto restart.
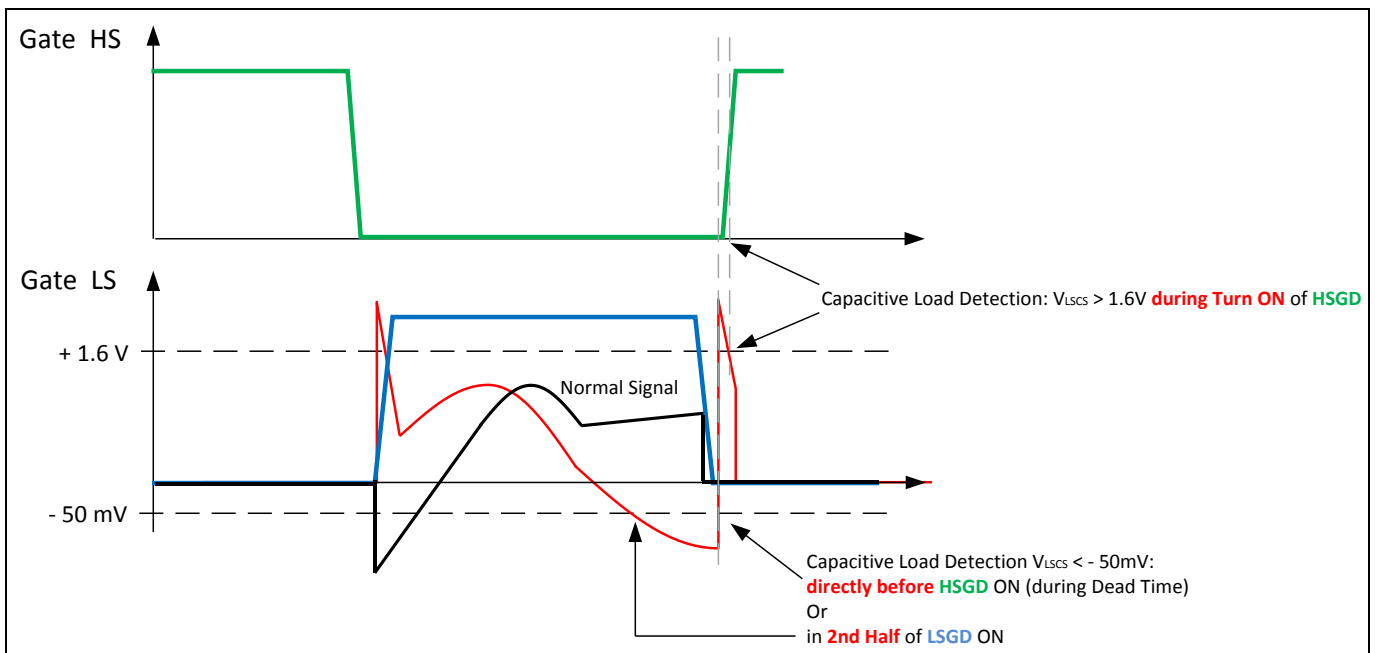
Figure 20   Capacitive Load Detection

Datasheet
www.infineon.com

Please read the Important Notice and Warnings at the end of this document
page 28 of 53

V 1.0
2018-05-18

2.6.2 Capacitive Switching Control

The capacitive load control is activated if the LSCS crosses a +50mV threshold within the first 7% of a cycle.

Each cycle the position where the LSCS voltage crosses a +50mV threshold is sensed. If this crossing occurs within the first 7% of a switching cycle measured from the high side turn off, the ICL5102 increases the frequency until the crossing shifts back behind the first 7% of a period.
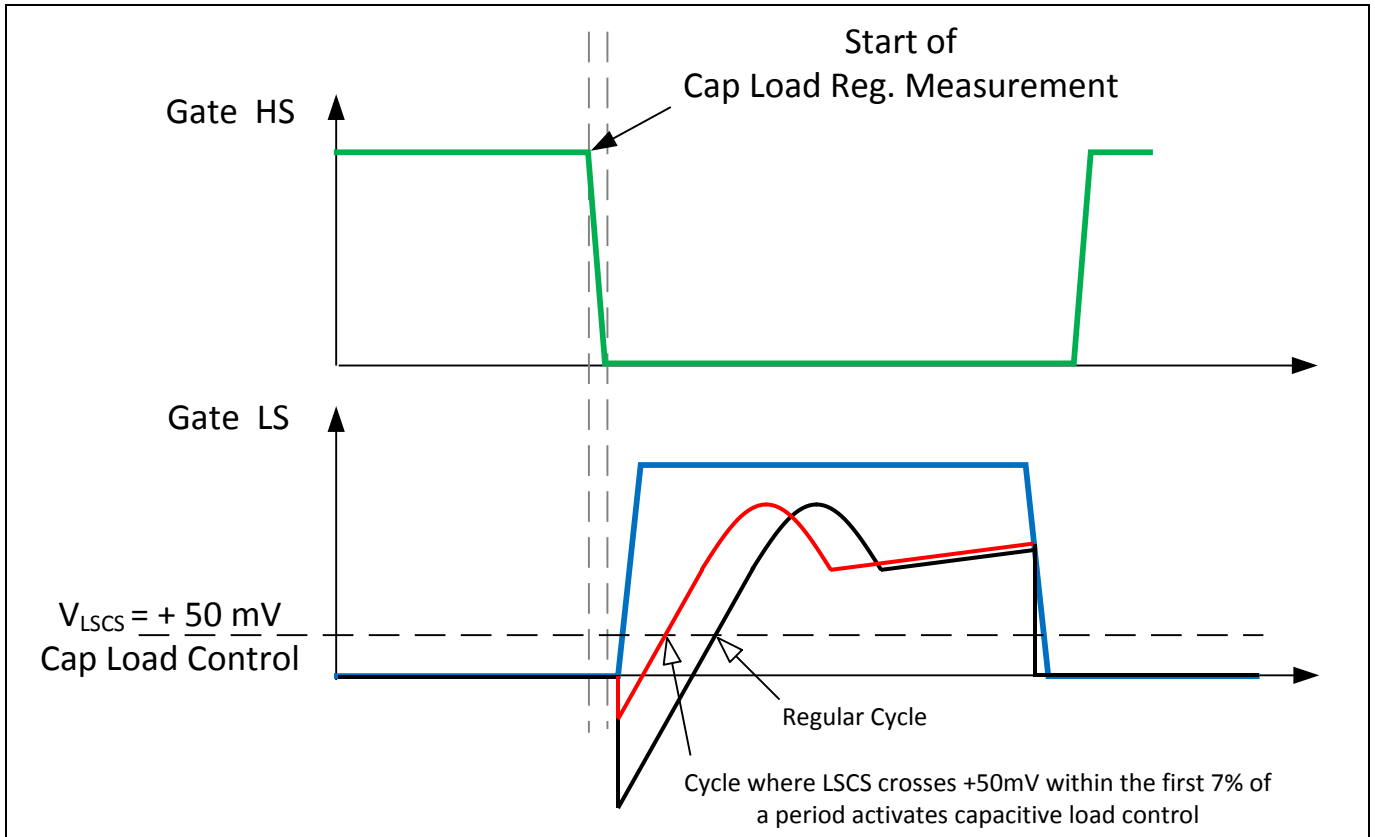
Figure 22   Capacitive Switching Control

V 1.0
2018-05-18

2.7 Over Current Control and Inverter Over Current Detection

The ICL5102 has 2 different ways to detect a over current. Over current control and an inverter over current shut down.

2.7.1 Over Current Control

There is a first threshold of 0.8V sensed by each ½ cycle. If this threshold is reached, the over current control increases the frequency until the signal is below 0.8V. If this signal is present for longer than 50ms, the controller powers down and auto restarts the system.

Gate HS

Gate LS

+ 0.8 V

LSCS Signal

Over Current Control:
the internal over current control increases the RUN Frequency until a maximum set frequency and Shut DOWN after 50ms
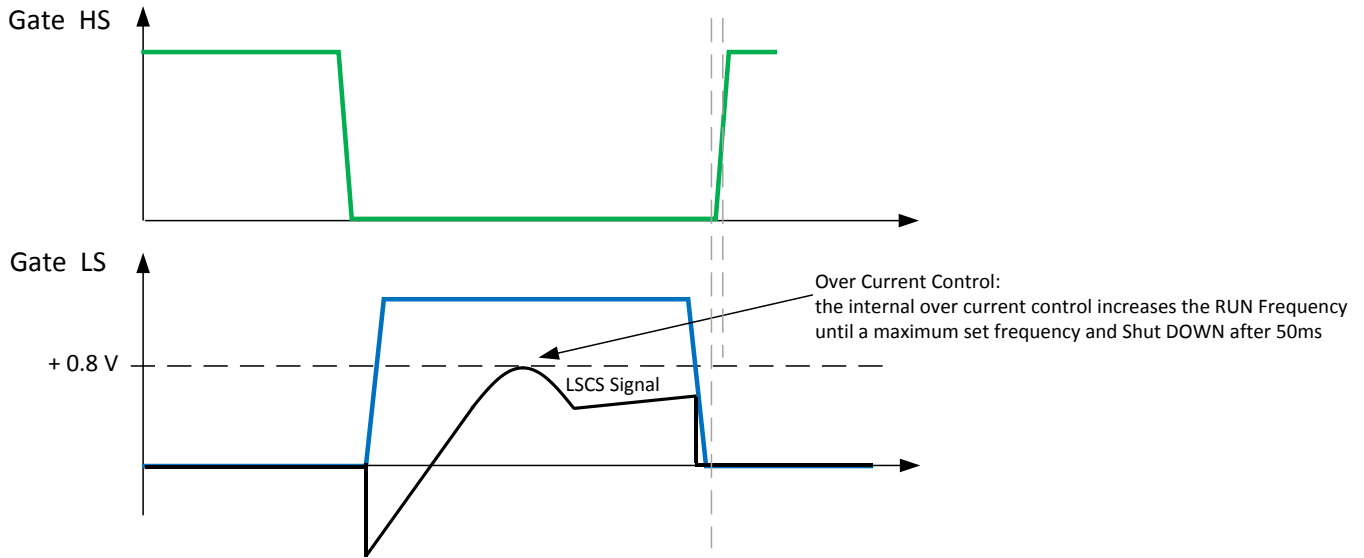
Figure 23   Over Current Control

2.7.2 Inverter Over Current Detection

If the sensed current signal exceeds a second threshold of 1.6V for longer than 500ns, the IC stops the half bridge MOSFETs.

Gate HS

Gate LS

+ 01.6 V

LSCS Signal

Inverter Over Current Detection:
Shut OFF when V_{LSCS} > 1.6 V for longer than 500 ns
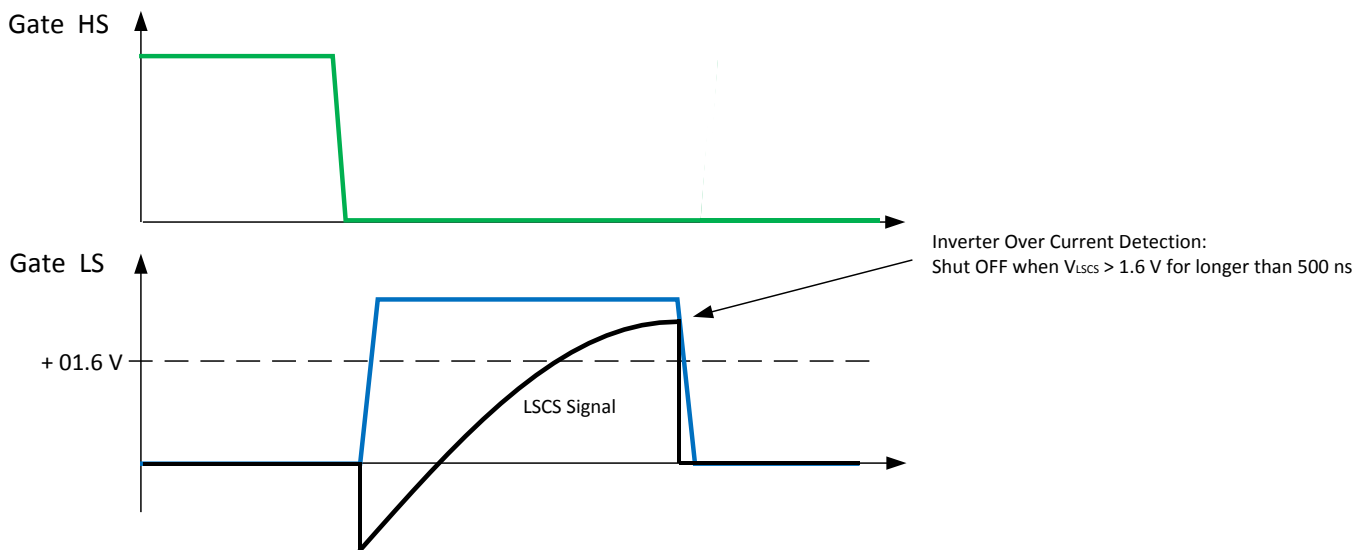
Figure 24   Inverter Over Current Detection

Datasheet
www.infineon.com

Please read the Important Notice and Warnings at the end of this document
page 30 of 53

V 1.0
2018-05-18

2.8 Self-Adaptive Dead Time

The dead time between the turn OFF and turn ON of the resonant drivers is self-adapting and is detected by means of switch-off of the high-side MOSFET and the -50mV threshold of the LSCS voltage. The typical range of the dead time adjustment is 250ns up to 750ns. The start of the dead time measurement is the OFF switching of the high-side MOSFET. The dead time measurement finishes when V_{LSCS} drops below -50mV for longer than typically 300ns (internally fixed propagation delay). This time will be stored; the low-side gate driver switches ON. The high-side gate driver turns ON again after OFF switching of the low-side switch and the stored dead time.
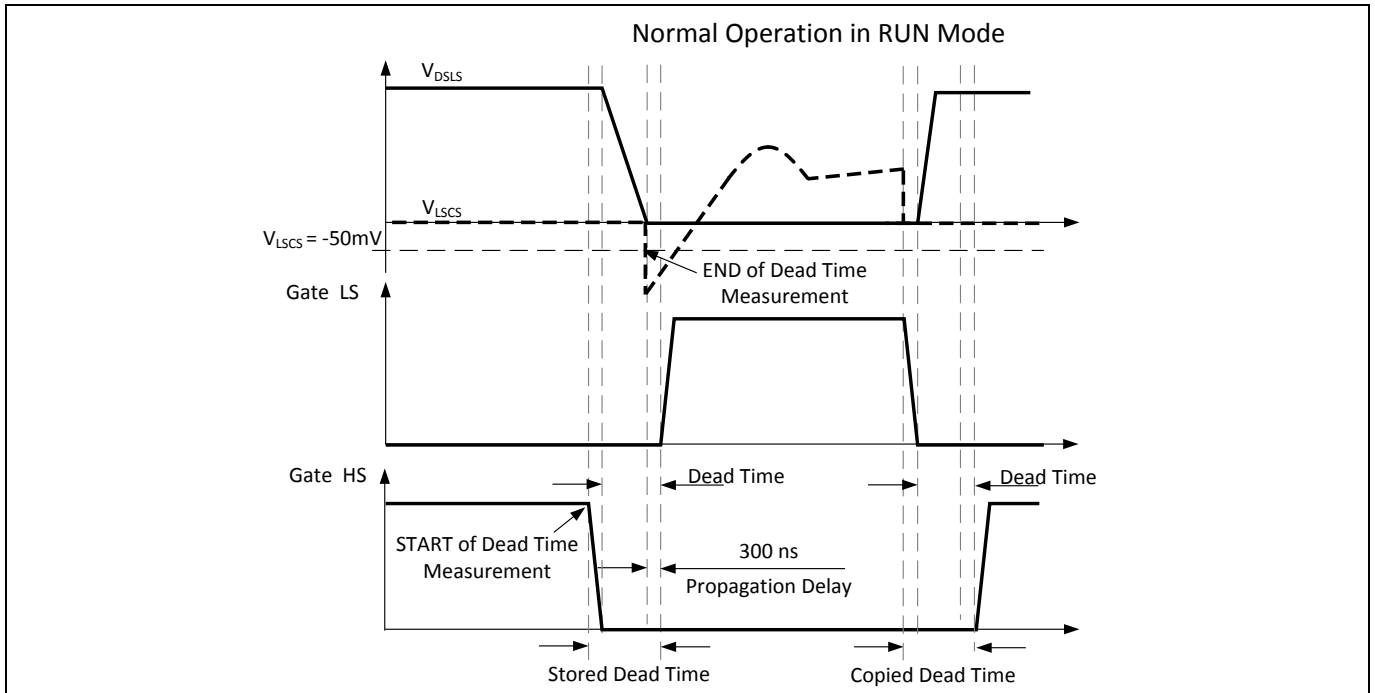
Figure 25   Self-Adaptive Dead Time

Datasheet
www.infineon.com
Please read the Important Notice and Warnings at the end of this document
page 31 of 53
V 1.0
2018-05-18

2.9 PFC Preconverter

The PFC Pre Converter starts at the initial start-up before half bridge starts working what can be seen in chapter 1.

2.9.1 PFC Current Limitation

The PFC current limitation at pin PFCCS terminates the ON – time of the PFC MOSFET cycle by cycle. If the voltage drop at the shunt resistors exceeds V_{PFCCS} = 1.0V, the IC regulates the PFC current.

2.9.2 Wait Cycle (WCM) and Critical Conduction Mode Operation (CritCM)

The digitally controlled PFC pre converter starts with a defined on-time depending on the AC line input voltage sensed via the brown out detection PIN 12. The on- time is enlarged every 280µs (typical) up to a maximum on-time of typical 22.0µs. As soon as a sufficient ZCD signal is available, the controller operates in the critical conduction mode (CritCM) also called boundary mode. At light load condition, the controller switches over into the wait cycle mode (WCM), a THD optimized DCM; patented by INFINEON Technologies.

During Wait Cycle Mode (WCM), the duration of the gap between two on-cycles of the PFC gate drive is proportionally generated to the magnetization period – that means, the time from ON of the PFC FET until the detection of the demagnetization via the zero crossing pin will be measured and multiplied with an internal factor depending on the relative output power see Figure 26.
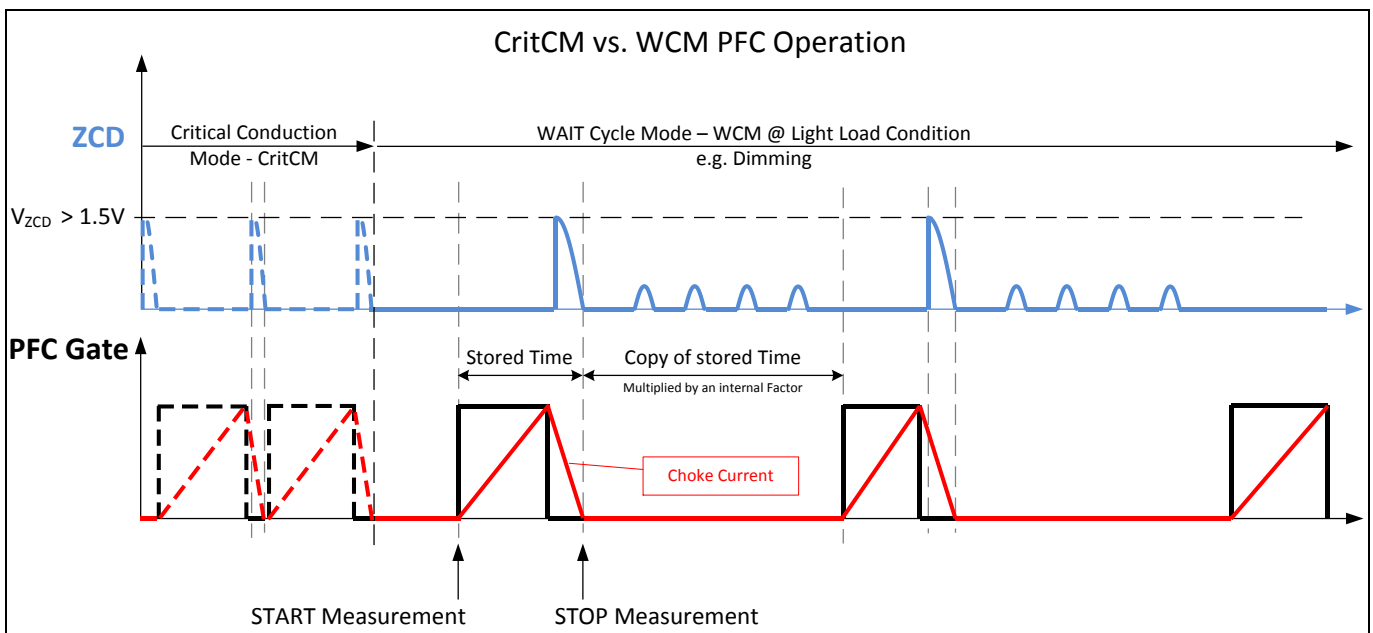
Figure 26   CritCM vs. WCM Operation

Datasheet
www.infineon.com

Please read the Important Notice and Warnings at the end of this document
page 32 of 53

V 1.0
2018-05-18

Figure 27 shows an example how the internal mechanism reacts. The CrCM works in a frequency range of 22kHz up to 250kHz.
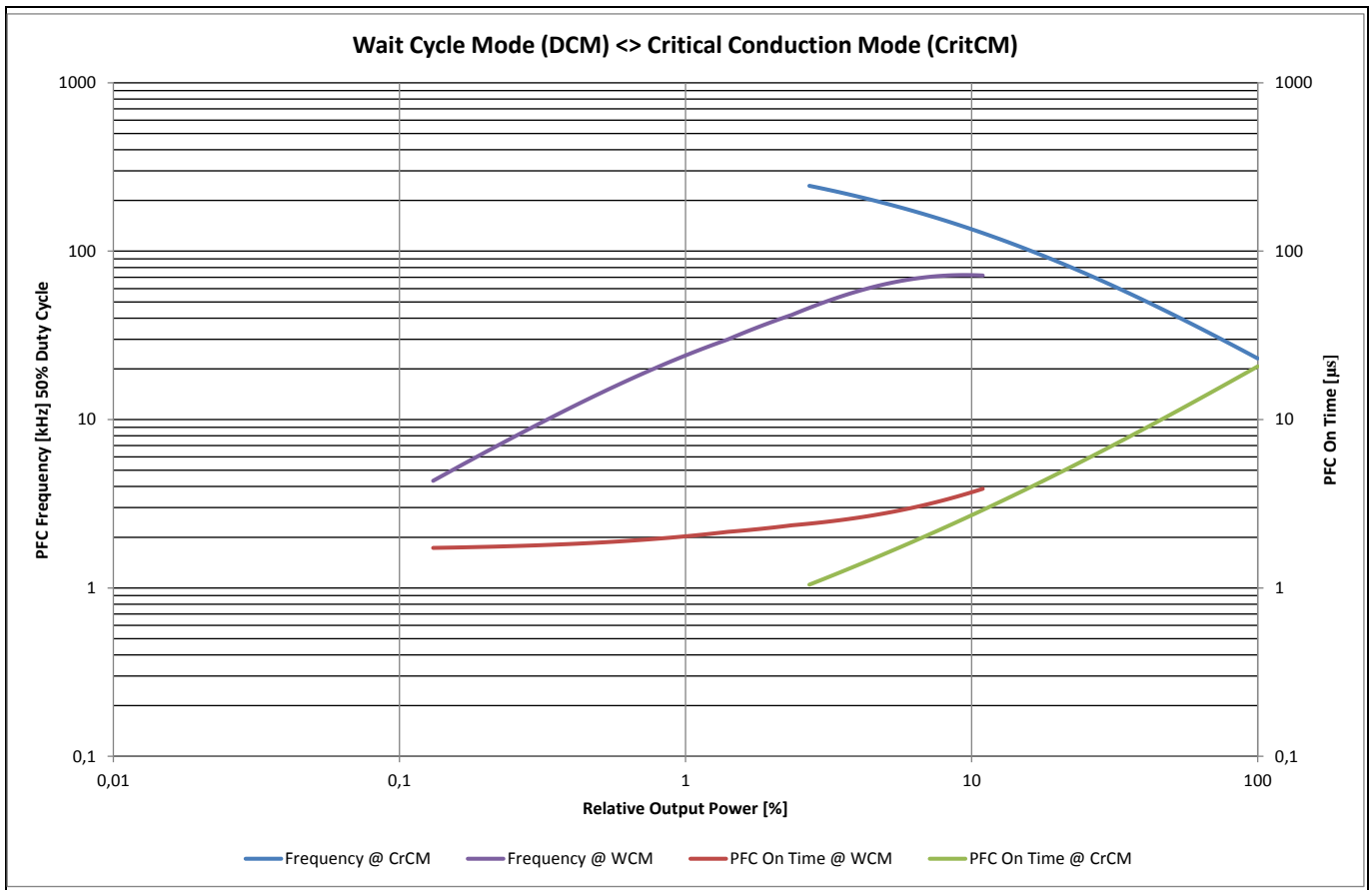
Figure 27   Operating Frequency and ON Time versus Power in WCM and CritCM Operation

For lower loads e.g. dimming, the control operates in the wait cycle mode (WCM) with an on-time from 4.0μs and increasing off- time. The frequency during WCM is variable in a range from 70kHz down to typically 4.0kHz @ 0.1 % Load (Figure 27). Figure 27 shows the on-time range in WCM (Wait Cycle Mode) and CritCM (Critical Conduction Mode) operation. The mode changes within the overlapping area with some hysteresis and with a partial compensation of the line voltage, as detected by the BO input. At a mode change the on-time is corrected to minimize the control loop step.

Datasheet
www.infineon.com

Please read the Important Notice and Warnings at the end of this document
page 33 of 53

V 1.0
2018-05-18

2.9.3 THD Correction via ZCD Signal

An additional feature is the improved THD correction. In order to optimize THD (especially at the areas A with a weak AC line signal shown in Figure 28), there is a possibility to extend pulse width of the PFC gate signal. The PFC gate signal is controlled by the V_{PFCVS} signal with a maximum on-time of typical 22.0µs (see the gray part of the PFC gate signal in Figure 28). By placing a resistor from the ZCD PIN 7 to the AUX winding of the PFC choke, the PFC gate on-time can be extended by factor 2 of t_{ONMax} = 22.0µs depending on line input voltage (see blue part of the PFC gate signal in Figure 28).
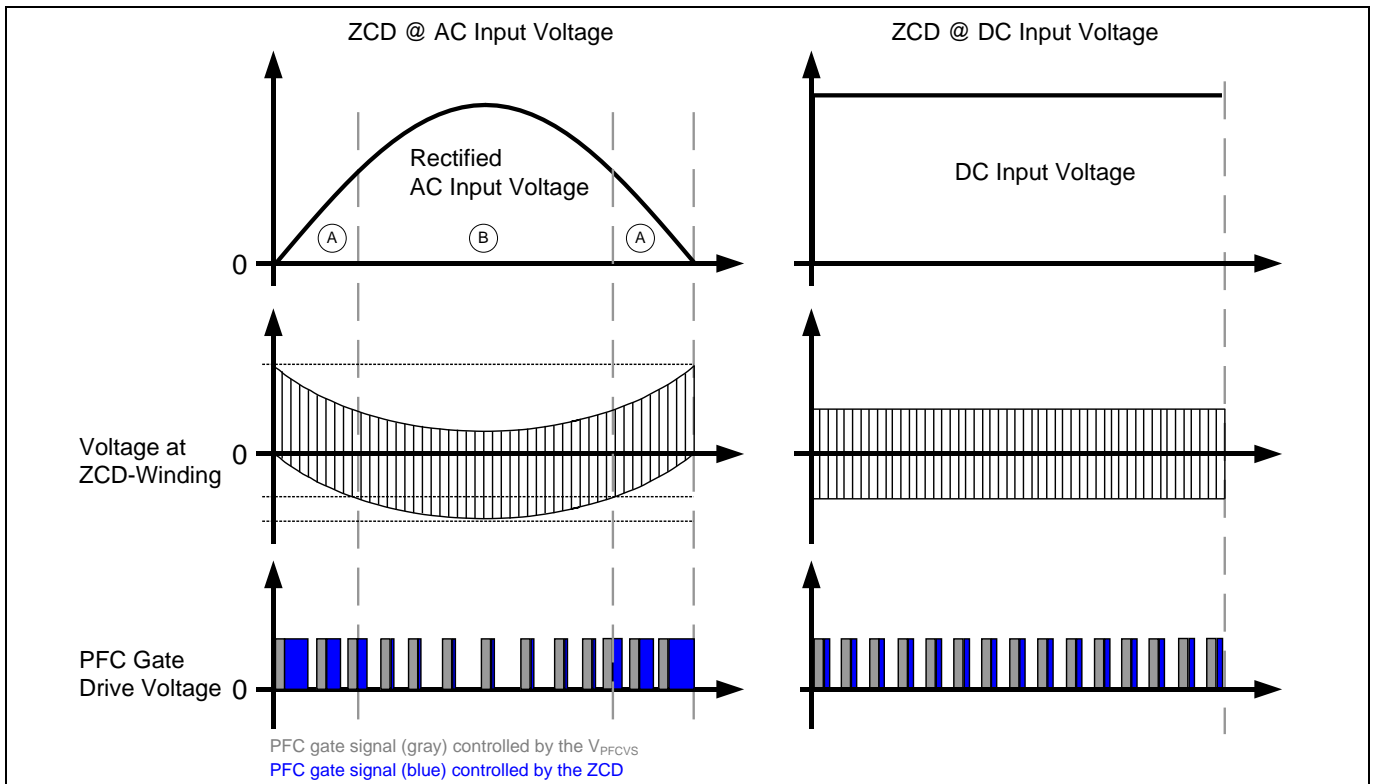
Figure 28 THD Optimization using adjustable Pulse Width Extension

The value of the resistor can be calculated by the ratio of the PFC mains choke and ZCD winding the bus voltage and a current of typically 1.5mA (see equation below). An adjustment of the ZCD resistor causes an optimized THD.

$$R_{ZCD} = \frac{\frac{N_{ZCD}}{N_{PFC}} * V_{BUS}}{1.5mA}$$

Equation 13: R_ZCD a good practical value

Datasheet
www.infineon.com
Please read the Important Notice and Warnings at the end of this document
page 34 of 53
V 1.0
2018-05-18

2.9.4 PFC Bus Voltage Sensing

Bus over voltage, open loop and under voltage states (Figure 29) of the PFC bus voltage are sensed at the PFCVS pin via the voltage divider R_{PFCVS_1} and R_{PFCVS_2} shown in Figure 3.

The bus voltage loop control is completely integrated (Figure 30). After leaving monitoring, the IC starts the power up (V_{CC} > 16.0V). During power up all gates are off, the IC senses the PFC bus voltage below 12.5% (open loop) or above 105% (bus over voltage) both cases will prevent entering the start-up phase. If the condition during power up is valid means NO open loop or bus over voltage, the IC enters the start-up phase. In start-up phase, the IC checks two additional bus voltage levels, V_{BUS} > 109% and VBUS < 75%. In case of V_{BUS} > 75%, below 109% and no open loop the PFC, the PFC gate drive will be active (the inverter gates still off), the IC enters the half bridge soft start phase. During the soft start phase and in run mode, another additional threshold of 115% will be checked. In case of a bus over voltage ($V_{BUSrated}$ > 109%) or an open loop ($V_{BUSrated}$ < 12.5%) in phases power up, soft start, run mode the IC shuts off the gate drives of the PFC within 5µs respective in 1µs. The PFC restarts automatically when the bus voltage is within the corridor (12.5% < $V_{BUSrated}$ < 105%) again. An inverter over voltage will be detected when the rated bus voltage exceeds $V_{BUSrated}$ > 115% for longer than 50ms – this stops the inverter gates, all gates (HS / LS / PFC) are off.
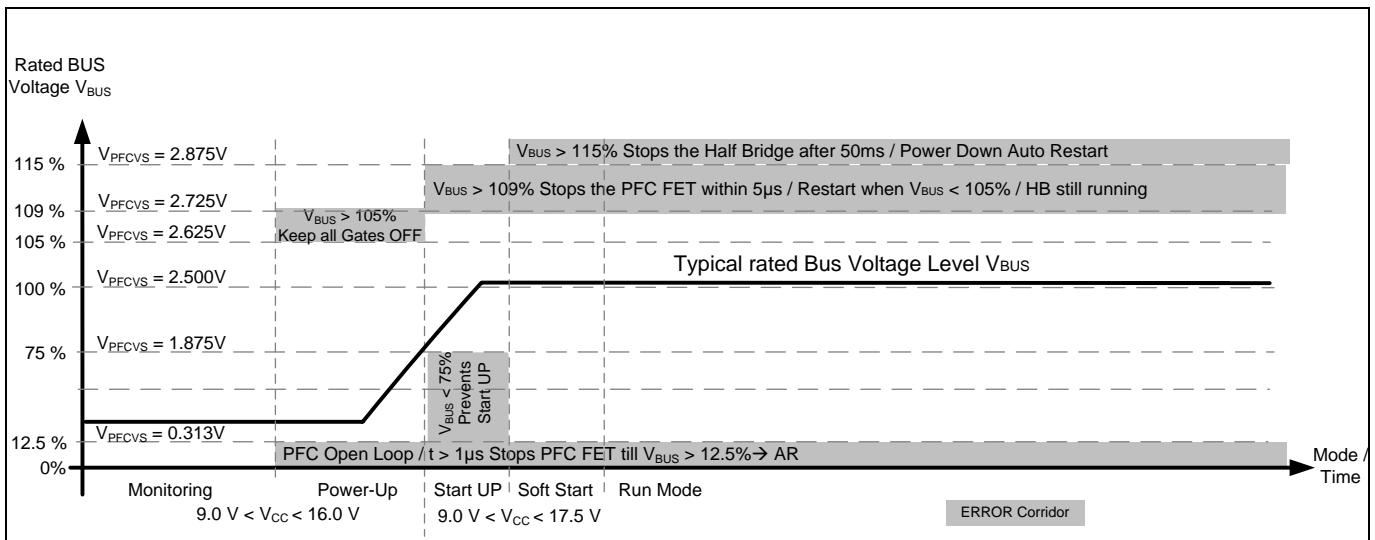
Figure 29 PFC Bus Voltage Operating Level and Error Detection

Datasheet
www.infineon.com

Please read the Important Notice and Warnings at the end of this document
page 35 of 53

V 1.0
2018-05-18

2.9.5 PFC Structure of Mixed Signal

A digital NOTCH filter eliminates the input voltage ripple. It auto-tunes to the mains frequency within 48Hz to 63Hz. A subsequent error amplifier with PI characteristic cares for a stable operation of the PFC pre converter (Figure 30).
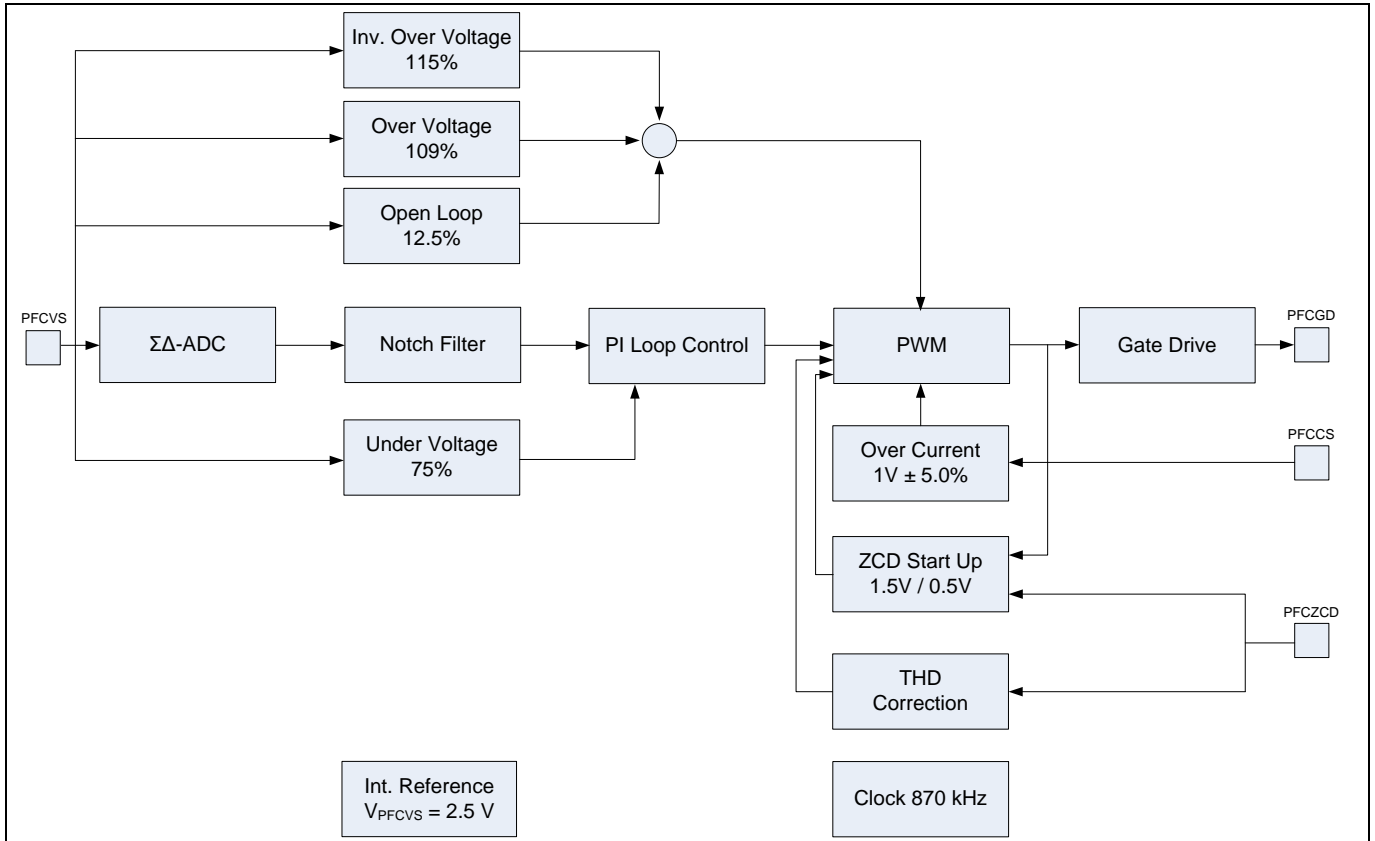
Figure 30 Structure of the mixed digital and analog control of the PFC pre converter

The zero current detection (ZCD) is sensed by the PFCZCD pin via R_{ZCD} shown in Figure 3. The information of finished current flow during demagnetization is required in CritCM and in WCM as well. The input is equipped with a special filtering including a blanking of typically 500ns and a large hysteresis of typically 0.5V and 1.5V V_{PFCZCD} (Figure 30).

Datasheet
www.infineon.com
Please read the Important Notice and Warnings at the end of this document
page 36 of 53
V 1.0
2018-05-18

3 Bubble Chart

Operating FLOW Chart ICL5102
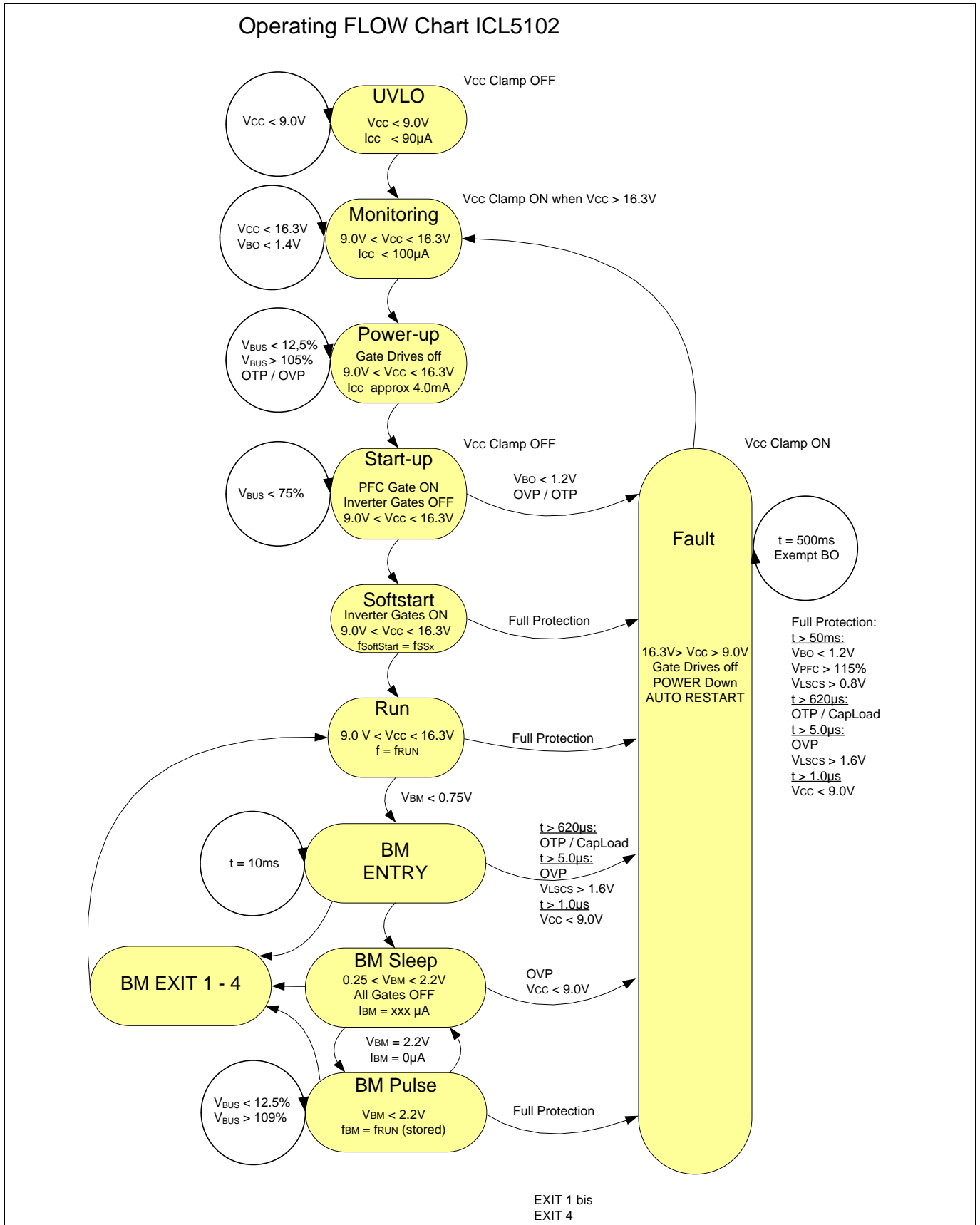
Figure 31 Bubble Chart of internal Processes

Datasheet
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Please read the Important Notice and Warnings at the end of this document
page 37 of 53

V 1.0
2018-05-18

4 FAULT Matrix

Table 3

Description of Fault	Characteristics of Fault			Operating Mode Detection is active							Consequence
	Definition of Fault	Action	Minimum Duration of effect	Monitoring	Power-up 130µs	Start-up	Soft start	Rune Mode	Burst PULSE	Burst SLEEP	Reaction
Supply voltage V_{CC} < 16.0V before power up	Below start-up threshold	W	1µs	X							Prevents Power up
Supply voltage Vcc < 9.0V after power up	Below UVLO threshold	A	1µs	X	X	X	X	X	X	X	Power Down AUTO RESTART
Brown OUT Detection V_{BO} < 1.2V	BO	A	50ms			X	X	X	X		Power Down AUTO RESTART when V_{BO} > 1.4V
Brown IN Control V_{BO} < 1.4V	BI	W	1µs	X							Prevents Power up
Over Temperature Detection V_{OTP1} < 703mV	OTP	W	620µs		X						Prevents Power up
Over Temperature Detection V_{OTP2} < 625mV	OTP	A	620µs			X	X	X	X		Power Down AUTO RESTART when V_{OTP} > 703mV
Bus voltage < 12.5% of rated level	Open Loop detection	W	1µs		X						Keep ALL gate drives off, RESTART when V_{BUS} > 12.5%
Bus voltage < 12.5% of rated level	Open Loop detection	W	1µs			X	X	X	X		Stops PFC FET RESTART when V_{BUS} > 12.5%
Bus voltage < 75% of rated level	PFC Under voltage	W	1µs				X				Prevents Start Up until V_{BUS} > 75% Keep HB Gate Drives OFF
Bus voltage > 105% of rated level	PFC Overvoltage	W	5µs		X						Keep ALL Gate drives off AUTO RESTART after V_{BUS} < 105%
Bus voltage > 109% of rated level	PFC Overvoltage	W	5µs			X	X	X	X		Stops PFC FET RESTART when V_{BUS} < 105%
Bus voltage > 115% of rated level	Inverter Overvoltage	A	50ms				X	X	X		Power Down AUTO RESTART
Output Over Voltage V_{OVP} > 2.5V	OVP	W	5µs		X						Prevents Power up
Output Over Voltage V_{OVP} > 2.5V	OVP	A	5µs			X	X	X	X	X	Stops ALL FETs RESTART when V_{OVP} < 2.5V
Capacitive Load operation below resonance	Cap Load	A	620µs				X	X	X		Power Down AUTO RESTART
Capacitive Load Control	Capacitive Load Control	N	1/2 cycle				X	X			Increase HB frequency
N = Handled during Normal Operation	W = Wait while Condition is present										A = Auto-Restart

Datasheet
www.infineon.com

Please read the Important Notice and Warnings at the end of this document
page 38 of 53

V 1.0
2018-05-18

FAULT Matrix

Description of Fault	Characteristics of Fault			Operating Mode Detection is active							Consequence
	Definition of Fault	Action	Minimum Duration of effect	Monitoring	Power-up 130µs	Start-up	Soft start	Rune Mode	Burst PULSE	Burst SLEEP	Reaction
Voltage at PFCCS pin V_{PFCCS} > 1.0V	PFC Over Current cont.	N	200ns			X	X	X	X		Stops on-time of PFC FET immediately
Voltage at LSCS pin V_{LSCS} > 0.8V	Overcurrent control	N	1/2 cycle				X	X	X		Increase HB frequency
Voltage at LSCS pin V_{LSCS} > 0.8V	Overcurrent Shut down	A	50ms				X	X			Power Down AUTO RESTART
Voltage at LSCS pin V_{LSCS} > 1.6V	Inverter overcurrent	A	500ns				X	X	X		Power Down AUTO RESTART
N = Handled during Normal Operation	W = Wait while Condition is present										A = Auto-Restart

Datasheet
www.infineon.com

Please read the Important Notice and Warnings at the end of this document
page 39 of 53

V 1.0
2018-05-18

5 Electrical Characteristics

Note: *All voltages except the high-side signals are measured with respect to GND (pin 4). The high-side voltages are measured with respect to HSGND (pin 14). The voltage levels are valid of other ratings are not violated. All driver source currents or currents out of the IC are per definition negative.*

5.1 Absolute Maximum Ratings

Note: *Absolute maximum ratings are defined as ratings, which if exceeded may lead to destruction of the integrated circuit. For the same reason make sure that any capacitor connected to VCC (pin 3) and HSVCC (pin 15) is discharged before assembling the application circuit.*

Table 4 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
LSCS Voltage	V_{LSCS}	- 5	6	V	
LSCS Current	I_{LSCS}	- 3	3	mA	
LSGD Voltage	V_{LSGD}	- 0.3	V_{cc}+0.3	V	Internally clamped to 11V
LSGD Peak Source Current	$I_{LSGDsomax}$	- 75	5	mA	< 500 ns
LSGD Peak Sink Current	$I_{LSGDsimax}$	- 50	400	mA	< 100 ns
VCC Voltage	V_{VCC}	- 0.3	18.5	V	Use max. 18V Zener Diode
VCC Zener Clamp Current	$I_{VCCzener}$	- 5	5	mA	
PFCGD Voltage	V_{PFCGD}	- 0.3	V_{cc}+0.3	V	Internally clamped to 11V
PFCGD Peak Source Current	$I_{PFCGDsomax}$	- 150	5	mA	< 500 ns
PFCGD Peak Sink Current	$I_{PFCGDsimax}$	- 100	700	mA	< 100 ns
PFCCS Voltage	V_{PFCCS}	- 5	6	V	
PFCCS Current	I_{PFCCS}	- 3	3	mA	
PFCZCD Voltage	V_{PFCZCD}	- 3	6	V	
PFCZCD Current	I_{PFCZCD}	- 5	5	mA	
PFCVS Voltage	V_{PFCVS}	- 0.3	5.3	V	
RFM Voltage	V_{RFM}	- 0.3	5.3	V	
OTP Voltage	V_{OTP}	- 0.3	5.3	V	
OVP Voltage	V_{OVP}	- 0.3	5.3	V	
Burst Mode Voltage	V_{BM}	- 0.3	5.3	V	
Brown Out Voltage	V_{BO}	- 0.3	5.3	V	
HSGND Voltage	V_{HSGND}	- 650	650	V	Referring to GND[1]
HSGND Voltage Transient	dV_{HSGND}/dt	- 40	40	V/ns	
HSVCC Voltage	V_{HSVCC}	- 0.3	18.0	V	Referring to HSGND
HSGD Voltage	V_{HSGD}	- 0.3	V_{HSVCC}+0.3	V	Internally clamped to 11V

---

[1] Limitation due to creeping distance between the HS & LS Pins (CTT 900V inside)

Datasheet
www.infineon.com

Please read the Important Notice and Warnings at the end of this document
page 40 of 53

V 1.0
2018-05-18

Electrical Characteristics

Parameter	Symbol	Limit Values		Unit	Remarks
HSGD Peak Source Current	$I_{HSGDsomax}$	- 75	0	mA	< 500ns
HSGD Peak Sink Current	$I_{HSGDsimax}$	0	400	mA	< 100ns
Junction Temperature	T_J	- 40	150	°C	
Storage Temperature	T_S	- 55	150	°C	
Maximum Power Dissipation	P_{TOT}	—	1	W	PG-DSO-16 / T_{amb}=25°C
Thermal Resistance (2 Chips) Junction - Ambient	R_{thJA}	—	125	K/W	PG-DSO-16 @ T_A = 85°C & PCB Area > 30x20mm
Soldering Temperature Wave		—	260	°C	Wave Soldering[1]
Soldering Temperature Reflow		—	2)	°C	Reflow Soldering[2]
ESD Capability HBM	V_{ESD_HBM}	—	2	kV	Human Body Model[3]
ESD Capability CDM	V_{ESD_CDM}	—	500	V	Charged Device Model[4]

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[1] According to JESD22A111

[2] According to J-STD-020D

[3] According to EIA/JESD22-A114-B

[4] According to JESD22-C101

Datasheet

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page 41 of 53

V 1.0

2018-05-18

5.2 Operating Range

The IC operates as described in the functional description once the values listed here lie within the operating range.

Table 5   Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
HSVCC Supply Voltage	V_{HSVCC}	7.9	17.5	V	Referring to HSGND
HSGND Voltage	V_{HSGND}	- 650	650	V	Referring to GND[1]
VCC Voltage @ 25°C	V_{VCC}	8.5	17.5	V	T_J = 25°C
VCC Voltage @ 125°C	V_{VCC}	8.5	18.0	V	T_J = 125°C
LSCS Voltage Range	V_{LSCS}	- 4	5	V	In active mode
PFCVS Voltage Range	V_{PFCVS}	0	4	V	
PFCCS Voltage Range	V_{PFCCS}	- 4	5	V	In active mode
PFZCD Current Range	I_{PFCZCD}	- 3	3	mA	In active mode
OVP Voltage Range	V_{OVP}	0	2.5	V	
Junction Temperature	T_J	- 40	125	°C	
Adjustable Run Frequency	f_{RF}	20	500	kHz	@ Tj_{max} = 125°C / Ta = - 40°C
Soft Start Frequency max	f_{SSmax}	-	1300	kHz	@ Soft Start
Mains Frequency	f_{Mains}	45	65	Hz	NOTCH Filter Operation

5.3 Characteristics Power Supply Section

Note: *The electrical characteristics involve the spread of values given within the specified supply voltage and junction temperature range T_J from -40 °C to 125 °C. Typical values represent the median values, which are given in reference to 25 °C. If not otherwise stated, a supply voltage of 15 V and V_{HSVCC} = 15 V is assumed and the IC operates in active mode. Furthermore, all voltages refer to GND if not otherwise mentioned.*

Table 6   Characteristics of Power Supply Section

Parameter	Symbol	Limit Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
VCC Quiescent Current	I_{VCCqu1}	—	70	120	µA	V_{VCC} = 8.0V
VCC Supply Current 1)	$I_{VCCSupply}$	—	4.0	5.8	mA	V_{PFCVS} > 2.725V
VCC Supply Current in Auto Restart Mode	$I_{VCCLatch}$	—	100	160	µA	
VCC Turn-On Threshold	V_{VCCOn}	15.4	16.0	16.6	V	
VCC Turn-Off Threshold	V_{VCCOff}	8.5	9.0	9.5	V	
VCC Turn-On/Off Hyst.	V_{VCCHys}	6.7	7.0	7.4	V	
VCC Zener Clamp Voltage	$V_{VCCClamp}$	15.4	16.3	16.6	V	IVCC = 2mA

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[1] Limitation due to creeping distance between the HS & LS Pins (CTT 900V inside)

Datasheet

www.infineon.com

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page 42 of 53

V 1.0

2018-05-18

Electrical Characteristics

Parameter	Symbol	Limit Values			Unit	Note or Test Condition
VCC Zener Clamp Current	$I_{VCCZener}$	3	—	6	mA	VVCC = 18V
High Side Leakage Current	$I_{HSGNDleak}$	—	0.01	2.0	µA	V_{HSGND} = 650V, V_{GND} = 0V
HSVCC Quiescent Current	$I_{HSVCCqu1}$[1]	—	190	280	µA	V_{HSVCC} = 8.0V
HSVCC Supply Current[2]	$I_{HSVCCqu2}$[1]	—	0.65	1.2	mA	$V_{HSVCC} > V_{HSVCCOn}$
HSVCC Turn-On Threshold	$V_{HSVCCOn}$[1]	9.55	10.3	11	V	
HSVCC Turn-Off Threshold	$V_{HSVCCOff}$[1]	7.9	8.6	9.3	V	
HSVCC Turn-On/Off Hyst.	$V_{HSVCCHy}$[1]	1.4	1.7	2.1	V	
Low Side Ground	GND					

[1] Refers to high-side ground (HSGND)

[2] With inactive gate

Datasheet
www.infineon.com
Please read the Important Notice and Warnings at the end of this document
page 43 of 53
V 1.0
2018-05-18

5.4 Characteristics of PFC Section

5.4.1 PFC Current Sense (PFCCS)

Table 7   Electrical Characteristics of PFCCS Pin

Parameter	Symbol	Limit Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Turn-off threshold	$V_{PFCCSOff}$	0.95	1.0	1.05	V	
Overcurrent blanking + propagation delay[1]	$t_{PFCCSOff}$	140	200	260	ns	
Leading-edge blanking	$t_{Blanking}$	180	250	320	ns	Pulse width when $V_{PFCCS} > 1.0V$
PFCCS bias current	$I_{PFCCSBias}$	- 0.5	—	0.5	µA	$V_{PFCCS} = 1.5V$

5.4.2 PFC Zero Current Detection (PFCZCD)

Table 8   Electrical Characteristics of PFCZCD Pin

Parameter	Symbol	Limit Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Zero crossing upper thr.[2]	$V_{PFCZCDUp}$	1.4	1.5	1.6	V	
Zero crossing lower thr.[3]	$V_{PFCZCDLow}$	0.4	0.5	0.6	V	
Zero crossing hysteresis	$V_{PFCZCDHys}$	—	1.0	—	V	
Clamping of pos. voltages	$V_{PFCZCDpclp}$	4.1	4.6	5.10	V	$I_{PFCZCDSink} = 2mA$
Clamping of neg. voltages	$V_{PFCZCDnclp}$	- 1.70	- 1.4	- 1.0	V	$I_{PFCZCDSource} = - 2mA$
PFCZCD bias current	$I_{PFCZCDBias}$	- 0.5	—	5.0	µA	$V_{PFCZCD} = 1.5V$
PFCZCD bias current	$I_{PFCZCDBias}$	- 0.5	—	0.5	µA	$V_{PFCZCD} = 0.5V$
PFCZCD ringing supp.[4] time	$t_{Ringsup}$	350	500	650	ns	
Limit value for on-time extension	$\Delta t \times I_{ZCD}$	400	600	670	pC	

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[1] Turn-Off threshold

[2] Turn-Off threshold

[3] Turn-On threshold

[4] Ringing suppression time

Datasheet
www.infineon.com

Please read the Important Notice and Warnings at the end of this document
page 44 of 53

V 1.0
2018-05-18

5.4.3 PFC Voltage Bus Sensing (PFCVS)

Table 9   Electrical Characteristics of PFCVS Pin

Parameter	Symbol	Limit Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Trimmed reference voltage	$V_{PFCVSRef}$	2.46	2.50	2.54	V	
Overvoltage turn-off (115 %)	$V_{PFCVSUp1}$	2.82	2.88	2.93	V	HB Gate OFF
Overvoltage turn-off (109 %)	$V_{PFCVSUp2}$	2.67	2.73	2.78	V	PFC Gate OFF
Overvoltage turn-on (105 %)	$V_{PFCVSLow}$	2.56	2.63	2.68	V	
Overvoltage hysteresis	$V_{PFCVSHys}$	70	100	130	mV	4 % rated bus voltage
Under voltage (75 %)	$V_{PFCVSUV1}$	1.83	1.88	1.92	V	
Under voltage (12.5 %)	$V_{PFCVSUV2}$	0.237	0.31	0.387	V	
PFCVS bias current	$I_{PFCVSBias}$	- 1.0	—	1.0	µA	V_{PFCVS} = 2.5V

5.4.4 PFC PWM Generation

Table 10   Characteristics of PFC PWM

Parameter	Symbol	Limit Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Initial on-time[1]	$t_{PFCON\_initial}$	1.75	6.0	10.64	µs	V_{PFCZCD} = 0V, V_{BO} = 2.0V
Max. on-time[2]	t_{PFCON_max}	17	22	26	µs	@ V_{ACIN} = 90V
Switch threshold from CritCM to WCM	t_{PFCON_min}	100	220	370	ns	
Repetition time[1]	t_{PFCRep}	47	52	60	µs	V_{PFCZCD} = 0V
Off time	t_{PFCOff}	42	47	52.5	µs	

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[1] When missing zero crossing signal

[2] At the maximum of the AC line input voltage in RUN Mode

Datasheet
www.infineon.com
Please read the Important Notice and Warnings at the end of this document
page 45 of 53
V 1.0
2018-05-18

5.4.5 PFC Gate Drive (PFCGD)

Table 11 Electrical Characteristics of PFCGD Pin

Parameter	Symbol	Limit Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
PFCGD Low Voltage	$V_{PFCGDLow}$	0.40	0.70	0.92	V	I_{PFCGD} = 5mA
		0.40	0.75	1.12	V	I_{PFCGD} = 20mA
		- 0.20	0.30	0.62	V	I_{PFCGD} = -20mA
PFCGD High Voltage	$V_{PFCGDHigh}$	10.0	11.0	11.6	V	I_{PFCGD} = -20mA
		7.5	—	—	V	I_{PFCGD} = -1mA / V_{VCC}[1]
		7.0	—	—	V	I_{PFCGD} = -5mA / V_{VCC}[1]
PFCGD active Shut Down	$V_{PFCGASD}$	0.40	0.75	1.12	V	I_{PFCGD} = 20mA / V_{VCC}=5V
PFCGD UVLO Shut Down	$V_{PFCGDuvlo}$	0.30	1.00	1.60	V	I_{PFCGD} = 5mA / V_{VCC}=2V
PFCGD Peak Source Current	$I_{PFCGDSource}$	—	- 100	—	mA	[2+3]
PFCGD Peak Sink Current	$I_{PFCGDSink}$	—	500	—	mA	[2+3]
PFCGD Voltage during sink Current	$V_{PFCGDHigh}$	10.8	11.7	12.3	V	$I_{PFCGDSinkH}$ = 3mA
PFC Rise Time	$t_{PFCGDRise}$	125	275	580	ns	2V > V_{LSGD} < 8V [2]
PFC Fall Time	$t_{PFCGDFall}$	20	45	72	ns	8V > V_{LSGD} > 2V [2]

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[1] V_{VCC} = V_{VCCOff} + 0.3V

[2] R_{Load} = 4Ω and C_{Load} = 3.3nF

[3] This parameter is no subject to production testing – verified by design / characterization

Datasheet
Please read the Important Notice and Warnings at the end of this document
V 1.0
www.infineon.com
page 46 of 53
2018-05-18

5.5 Characteristics of Inverter

5.5.1 Low-Side Current Sense (LSCS)

Table 12   Electrical Characteristics of LSCS Pin

Parameter	Symbol	Limit Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Overcurrent shutdown volt. 1	$V_{LSCSOvC1}$	1.54	1.6	1.66	V	
Duration of overcurrent 1	$t_{LSCSOvC1}$	430	600	670	ns	
Overcurrent shutdown Volt. 2	$V_{LSCSOvC2}$	0.74	0.8	0.86	V	
Duration of overcurrent 2	$t_{LSCSOvC2}$	—	50	—	ms	[1]
Capacitive mode det. Level 1	$V_{LSCSCap1}$	1.54	1.6	1.66	V	during turn-on of the HSGD
Capacitive mode duration 1	$t_{LSCSCap1}$	30	50	90	ns	
Capacitive mode det. Level 2	$V_{LSCSCap2}$	- 70	- 50	- 25	mV	before turn-on of the HSGD
Capacitive mode duration 2	$t_{LSCSCap2}$	300	390	550	ns	
Capacitive load control regulation voltage	$V_{LSCSCapC}$	25	50	70	mV	
Capacitive switching regulation ratio	$R_{LSCSCapC}$	4.5	7.0	9.0	%	
Over Current Control	V_{LSCSCC}	0.74	0.8	0.86	V	
LSCS bias current	$I_{LSCSBias}$	-1.0	—	1.0	µA	@ V_{LSCS} = 1.5 V

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[1] The parameter is not subject to production testing – verified by design/characterization

Datasheet

www.infineon.com

Please read the Important Notice and Warnings at the end of this document

page 47 of 53

V 1.0

2018-05-18

5.5.2 Low-Side Gate Drive (LSGD)

Table 13 Electrical Characteristics of LSGD Pin

Parameter	Symbol	Limit Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
LSGD low voltage	$V_{LSGDLow}$	0.40	0.70	1.00	V	I_{LSGD} = 5 mA
		0.40	0.80	1.20	V	I_{LSGD} = 20 mA
		- 0.30	0.20	0.53	V	I_{LSGD} = - 20 mA
LSGD high voltage	$V_{LSGDHigh}$	10.0	10.8	11.6	V	I_{LSGD} = - 20 mA
		7.5	—	—	V	I_{LSGD} = –1 mA[1]
		7.0	—	—	V	I_{LSGD} = –5 mA[2]
LSGD active shutdown	$V_{LSGDASD}$	0.4	0.75	1.12	V	I_{LSGD} = 20 mA / V_{CC} = 5V
LSGD UVLO shutdown	$V_{LSGDUVLO}$	0.3	1.0	1.6	V	I_{LSGD} = 5 mA / V_{CC} = 2 V
LSGD peak source current	$I_{LSGDSource}$	—	- 50	—	mA	[2+3]
LSGD peak sink current	$I_{LSGDSink}$	—	300	—	mA	[1+2]
LSGD voltage during sink Current	$V_{LSGDHigh}$	—	11.7	—	V	$I_{LSGDsinkH}$ = 3 mA
LSGD rise time	$t_{LSGDRise}$	125	275	580	ns	2 V < V_{LSGD} < 8 V [1]
LSGD fall time	$t_{LSGDFall}$	20	35	60	ns	8 V > V_{LSGD} > 2 V [1]

5.5.3 Inverter Run Frequency (RF)

Table 14 Characteristics of Inverter Run Frequency

Parameter	Symbol	Limit Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
RF voltage in run mode	V_{RF}	2.46	2.5	2.54	V	@ 100µA < I_{RFM} < 800µA
Run frequency	f_{RF}	97.5	100	102.5	kHz	R_{RF} = 10kΩ
Adjustable run frequency	f_{RF1}	37	40	43	kHz	I_{RF} = - 100 µA
	f_{RF2}	76	80	84	kHz	I_{RF} = - 200 µA
	f_{RF3}	190	200	210	kHz	I_{RF} = - 500 µA
	f_{RF4}	220	240	260	kHz	I_{RF} = - 600 µA
	f_{RF5}	290	320	350	kHz	I_{RF} = - 800 µA
	$f_{RFmax-25°C}$	450	500	-	kHz	I_{RF} = - 1.25 mA / @ T_j = - 25°C[4]
	$f_{RFmax-40°C}$	400	500	-	kHz	I_{RF} = - 1.25 mA / @ T_j = - 40°C[4]

[1] V_{CC} = V_{CCOFF} + 0.3 V

[2] Load: R_{Load} = 10 Ω and C_{Load} = 1 nF

[3] The parameter is not subject to production testing – verified by design/characterization

[4] Make sure, that the expected ambient temperature do NOT causes a maximum junction temperature higher than 125°C

Datasheet
www.infineon.com
Please read the Important Notice and Warnings at the end of this document
page 48 of 53
V 1.0
2018-05-18

5.5.4 Burst Mode Operation (BM)

Table 15   Characteristics of Burst Mode

Parameter	Symbol	Limit Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Burst Mode Thresholds	$V_{BMEntry}$	710	750	790	mV	
	$t_{BMEntry}$	8.5	10.0	11.5	ms	
	$V_{BMStart}$	2.13	2.20	2.27	V	
	V_{BMExit}	1.93	2.0	2.07	V	
	I_{BMmax}		800		µA	
	I_{BMStop}	-3	—	14	µA	

5.5.5 Brown Out Detection (BO)

Table 16   Electrical Characteristics of BO Pin

Parameter	Symbol	Limit Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Brownout Detection ON	V_{BOON}	1.14	1.2	1.26	V	
Brownout Detection Leave	$V_{BOLeave}$	1.34	1.4	1.46	V	
BO Bias Current	I_{BOBias}	-0.5	—	0.5	µA	$V_{BO} = 5.0V$

5.5.6 Over Voltage Protection (OVP)

Table 17   Electrical Characteristics of OVP Pin

Parameter	Symbol	Limit Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
OVP Reference Voltage	V_{OVP_Ref}	2.45	2.5	2.55	V	t > 5µs
OVP Bias Current	I_{OVP_Bias}	- 0.5	—	0.5	µA	VOVP = 3.0V

Datasheet
www.infineon.com

Please read the Important Notice and Warnings at the end of this document
page 49 of 53

V 1.0
2018-05-18

5.5.7 Over Temperature Protection (OTP) for NTC

Table 18   Electrical Characteristics of OTP Pin

Parameter	Symbol	Limit Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Over Temperature Protection	V_{OTP1}	670	703	735	mV	
	V_{OTP2}	594	625	665	mV	
Over Temperature Protection Current	I_{OTP}	- 106	- 100	- 94	µA	Voltage at pin is internally limited to typically 5V

5.5.8 High Side Gate Driver (HSGD)

Table 19   Electrical Characteristics of HSGD Pin

Parameter	Symbol	Limit Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
HSGD Low Voltage	$V_{HSGDLow}$	0.018	0.05	0.1	V	I_{HSGD} = 5mA
		0.40	1.10	2.50	V	I_{HSGD} = 100mA
		- 0.40	-0.20	- 0.04	V	I_{LSGD} = - 20mA
HSGD High Voltage	$V_{HSGDHigh}$	9.7	10.5	11.3	V	V_{CCHS}=15V
		7.8	—	—	V	I_{HSGD} = - 20mA
HSGD active Shut Down	$V_{HSGDASD}$	0.04	0.22	0.50	V	$V_{CCHSOFF}$ + 0.3V
HSGD Peak Source Current	$I_{HSGDSource}$	—	- 50	—	mA	I_{HSGD} = - 1mA[1]
HSGD Peak Sink Current	$I_{HSGDSink}$	—	300	—	mA	V_{CCHS}=5V[1]
HSGD Rise Time	$t_{HSGDRise}$	120	220	320	ns	I_{HSGD} = 20mA
HSGD Fall Time	$t_{HSGDFall}$	17	35	70	ns	R_{Load} = 10Ω+C_{Load} = 1nF

5.6 Timing Section

Table 20

Parameter	Symbol	Limit Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Inverter Dead Time max_1	$t_{Deadmax1}$	550	750	930	ns	LSCS > - 50mV / 100kHz
Inverter Dead Time max_2	$t_{Deadmax2}$	350	500	600	ns	LSCS > - 50mV / 500kHz
Inverter Dead Time min	$t_{Deadmin}$	150	250	300	ns	LSCS < - 50mV / 500kHz

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[1] The parameter is not subject to Production Test – verified by Design / Characterization
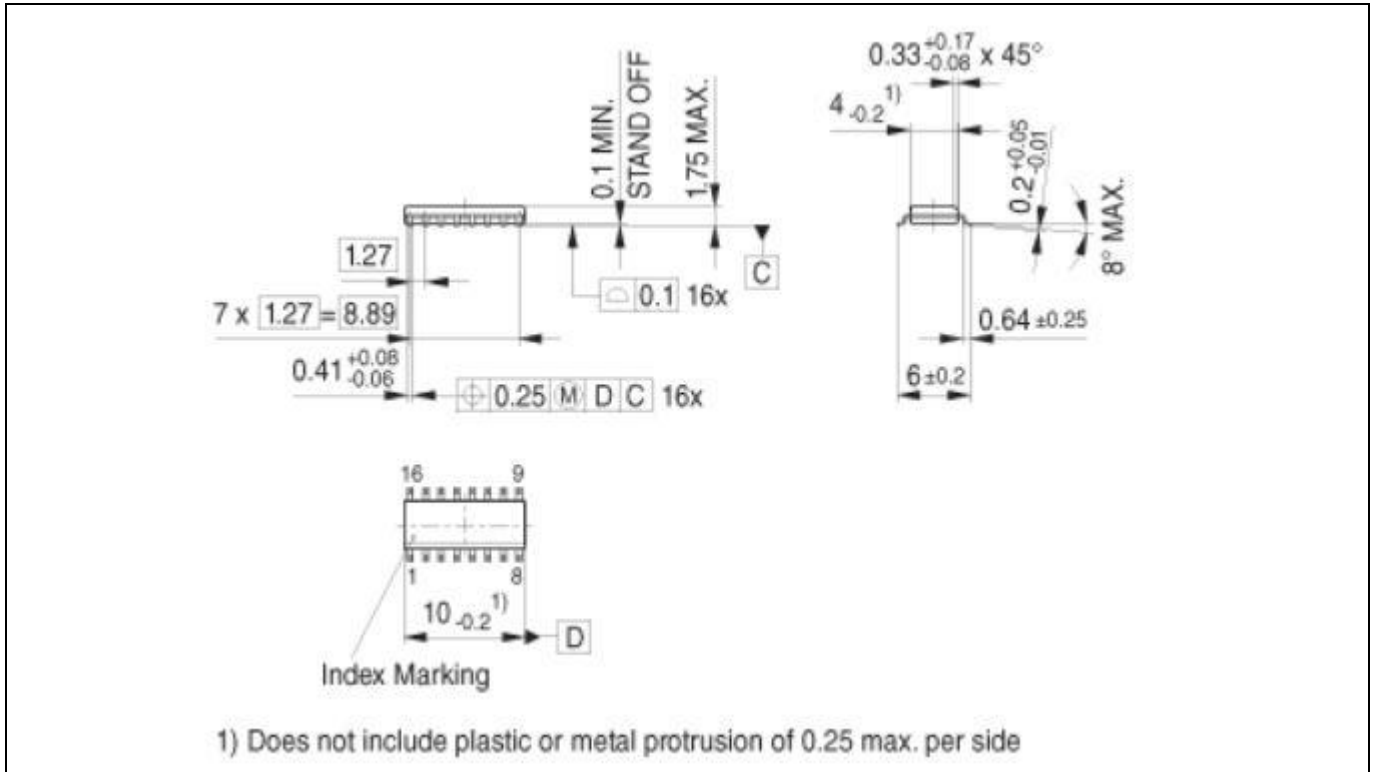
6 Outline Dimension

Figure 32 PG-DSO-16

Note:

1. *You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products":* *http://www.infineon.com/products*
2. *Dimensions in mm.*

Datasheet
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Please read the Important Notice and Warnings at the end of this document
page 51 of 53

V 1.0
2018-05-18

Revision history

Document version	Date of release	Description of changes
V1.0	26.04.2018	

Datasheet

www.infineon.com

Please read the Important Notice and Warnings at the end of this document

page 52 of 53

V 1.0

2018-05-18

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