

BGM15LA12

Low-Band LNA Multiplexer Module

Data Sheet

Revision 3.0 - 2015-07-24

Power Management & Multimarket

Edition 2015-07-24

Published by Infineon Technologies AG 81726 Munich, Germany

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Revision History

Document No.: BGM15LA12_v3.0.pdf

Revision History: Rev. v3.0

Previous Version: Preliminary, Revision v2.4 - 2014-08-21

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Page	Subjects (major changes since last revision)						
all	"Preliminary" status removed						
19	Package Outline Drawing: Minimum package height specified						
19	Marking Specification added						
20	Footprint Recommendation added						

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Contents

1	Features	6
2	Product Description	6
3	Maximum Ratings	7
4	DC Characteristics	8
5	RF Characteristics 5.1 BAND 8 5.2 BAND 12 5.3 BAND 20 5.4 BAND 26 5.5 BAND 28	9 10 11 12 13
6	MIPI RFFE Specification	14
7	Application Information	20
8	Package Information	22

List of Figures

1	BGM15LA12 Block diagram
2	Received clock signal constraints
3	Bus active data receiver timing requirements
4	Bus park cycle timing
5	Bus active data transmission timing specification
6	Requirements for VIO-initiated reset
7	BGM15LA12 Pin Configuration (top view)
8	BGM15LA12 Application Schematic
9	ATSLP-12-1 Package Outline (top, side and bottom views)
10	Marking Specification (top view)
11	Footprint Recommendation
12	ATSI P-12-1 Carrier Tane

Data Sheet 4 Revision 3.0 - 2015-07-24





List of Tables

	Ordering Information
2	Maximum Ratings
4	DC Characteristics
5	RF Characteristics Band 8
6	RF Characteristics Band 12
7	RF Characteristics Band 20
8	RF Characteristics Band 26
9	RF Characteristics Band 28
10	MIPI Features
11	Startup Behavior
12	MIPI RFFE operating timing
13	Register Mapping
14	Truth Table, Register_0 19
15	Pin Definition and Function
16	Bill of Materials



BGM15LA12 Low-Band LNA Multiplexer Module

1 Features

Power gain: 17.5 dBLow noise figure: 1.1 dB

Low current consumption: 4.9 mA
Frequency range from 0.7 to 1.0 GHz

• RF output internally matched to 50 Ω

· Low external component count

• High port-to-port-isolation

• Suitable for LTE / LTE-Advanced and 3G applications

• No decoupling capacitors required if no DC applied on RF lines

• On chip control logic including ESD protection

Supply voltage: 2.2 to 3.3 V

 Integrated MIPI RFFE interface operating in 1.1 to 1.95 V voltage range

Software programmable MIPI RFFE USID

• Small form factor 1.1 mm x 1.9 mm

• High EMI robustness

RoHS and WEEE compliant package



2 Product Description

The BGM15LA12 is a LNA multiplexer module for LTE low-band frequencies that increases the data rate while keeping flexibility and low footprint. It is a perfect solution for multimode handsets based on LTE-Advanced and WCDMA. The BGM15LA12 is controlled via a MIPI RFFE controller. The device configuration is shown in Fig. 12.

Table 1: Ordering Information

Туре	Package	Marking
BGM15LA12	ATSLP-12-1	L1

(a) Infineon



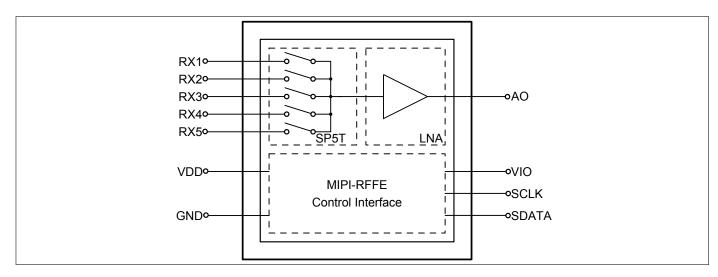


Figure 1: BGM15LA12 Block diagram

3 Maximum Ratings

Table 2: Maximum Ratings

Parameter	Symbol Values				Unit	Note / Test Condition
		Min.	Тур.	Max.		
Supply Voltage VDD	V_{DD}	-0.3	_	3.6	٧	1
Voltage at RF pins Rx	V _{Rx}	-0.3	_	0.9	٧	_
Voltage at RF output pin AO	V _{AO}	-0.3	_	V _{DD} +0.3	٧	_
Voltage at GND pins	V_{GND}	-0.3	_	0.3	٧	_
Current into pin VDD	I _{DD}	_	_	16	mA	_
RF input power	P _{IN}	_	_	0	dBm	_
Total power dissipation	P _{tot}	_	_	60	mW	
Junction temperature	T _J	_	_	150	°C	_
Ambient temperature range	T _A	-40	_	85	°C	_
Storage temperature range	T _{STG}	-65	_	150	°C	_
ESD capability, HBM	V _{ESD_HBM}	_	_	1000	٧	according to JESD22A-114
RFFE Supply Voltage	V _{IO}	-0.5	_	3.6	٧	_
DEEE Cupply Voltage Layele	V _{SCLK} ,	-0.7	_	V _{IO} +0.7	V	_
RFFE Supply Voltage Levels	V _{SDATA}			(max.		
				3.6)		

¹ All voltages refer to GND-Nodes unless otherwise noted

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.



4 DC Characteristics

Table 4: DC Characteristics at $T_{\rm A}$ = 25 °C

Parameter ¹	Symbol	Values			Unit	Note / Test Condition
		Min.	Тур.	Max.		
Supply Voltage	V_{DD}	2.2	_	3.3	٧	_
Supply Current	I _{DD}	_	4.9	5.9	mA	ON-mode
		_	0.1	2	μΑ	OFF-Mode
RFFE supply voltage	V _{IO}	1.1	1.8	1.95	V	_
RFFE input high voltage ²	V _{IH}	0.7*V _{IO}	_	V _{IO}	V	_
RFFE input low voltage ²	V _{IL}	0	_	0.3*V _{IO}	٧	_
RFFE output high voltage ²	V _{OH}	0.8*V _{IO}	_	V _{IO}	٧	_
RFFE output low voltage ²	V _{OL}	0	_	0.2*V _{IO}	٧	_
RFFE control input capaci-	C _{Ctrl}	_	_	2	pF	_
tance						
RFFE supply current	I _{VIO}	_	15	-	μΑ	Idle State

¹Based on the application described in Chapter 7

²SCLK and SDATA



5 RF Characteristics

5.1 BAND 8

Table 5: RF Characteristics Band 8 at $T_{\rm A}$ = 25 °C, $V_{\rm DD}$ = 2.8 V, f = 925 – 960 MHz, with matching described in Chapter 7 (C=1.1 pF, L=11 nH)

Parameter ¹	Symbol		Values		Unit	Note / Test Condition	
		Min.	Тур.	Max.			
Insertion power gain ²	$ S_{21} ^2$	14.3	15.8	17.3	dB	_	
Noise figure ²	NF	_	1.1	1.6	dB	Z _S =50 Ω	
Input return loss ^{2 3}	RLin	8	11	_	dB	-	
Output return loss ^{2 3}	RLout	12	>20	_	dB	-	
Reverse isolation AO to RX port ²	$1/ S_{12} ^2$	19	23	-	dB	-	
Inband input 1dB- compression point ^{2 3}	IP _{1dB}	-11	-8	_	dBm	-	
Inband input 3 rd -order intercept point ^{2 3 4}	IIP ₃	-4	-1	_	dBm	f_1 =937 MHz, f_2 =947 MHz, f_{12} =927 MHz	
Isolation RX to RX port ^{2 5}	ISO	35	40	_	dB		
Isolation RX to AO port ^{2 5}	ISO	24	29	_	dB	forward direction	
Stability ⁵	k	>1	-	_		f=20 MHz-10 GHz	
RF Rise Time RX Port	t _{on/off}	0.5	1	5	μ S	10 % to 90 % ON;	
On/Off ⁵						90 % to 10 % ON	
Power Up Settling Time ⁵	t _{BC}	_	10	25	μ S	After power down mode	

¹The parameter values are valid at any RX port using the matching described in Chapter 7

Data Sheet 9 Revision 3.0 - 2015-07-24

²PCB losses are subtracted

³ Verification based on AQL; not 100% tested in production

 $^{^{4}}$ Input power = $-30 \, dBm$ for each tone

⁵Guaranteed by device design; not tested in production



5.2 BAND 12

Table 6: RF Characteristics Band 12 at $T_{\rm A}$ = 25 °C, $V_{\rm DD}$ = 2.8 V, f = 729 – 746 MHz, with matching described in Chapter 7 (C=2.2 pF, L=16 nH)

Parameter ¹	Symbol	mbol Values			Unit	Note / Test Condition	
		Min.	Тур.	Max.			
Insertion power gain ²	$ S_{21} ^2$	15.2	16.7	18.2	dB	_	
Noise figure ²	NF	_	1.2	1.7	dB	$Z_{\rm S}$ =50 Ω	
Input return loss ^{2 3}	<i>RL</i> _{in}	8	11	_	dB	_	
Output return loss ^{2 3}	RLout	8	12	_	dB	_	
Reverse isolation AO to RX port ^{2 3}	$1/ S_{12} ^2$	19	23	_	dB	_	
Inband input 1dB- compression point ^{2 3}	IP _{1dB}	-14	-11	-	dBm	-	
Inband input 3 rd -order intercept point ^{2 3 4}	IIP ₃	-7	-4	-	dBm	$f_1 = 732 \text{ MHz}, f_2 = 742 \text{ MHz}, $ $f_{12} = 722 \text{ MHz}$	
Isolation RX to RX port ^{2 5}	ISO	34	39	_	dB		
Isolation RX to AO port ^{2 5}	ISO	24	29	_	dB	forward direction	
Stability ⁵	k	>1	_	_		f=20 MHz-10 GHz	
RF Rise Time RX Port On/Off ⁵	t _{on/off}	0.5	1	5	μ S	10 % to 90 % ON; 90 % to 10 % ON	
Power Up Settling Time ⁵	t _{BC}	_	10	25	μs	After power down mode	

 $^{^{\}rm 1}{\rm The}$ parameter values are valid at any RX port using the matching described in Chapter 7 $^{\rm 2}{\rm PCB}$ losses are subtracted

Revision 3.0 - 2015-07-24 **Data Sheet** 10

³Verification based on AQL; not 100% tested in production

 $^{^{4}}$ Input power = $-30 \, dBm$ for each tone

⁵Guaranteed by device design; not tested in production



5.3 BAND 20

Table 7: RF Characteristics Band 20 at $T_{\rm A}$ = 25 °C, $V_{\rm DD}$ = 2.8 V, f = 791 – 821 MHz, with matching described in Chapter 7 (C=1.8 pF, L=15 nH)

Parameter ¹	Symbol	Symbol Values		Unit	Note / Test Condition		
		Min.	Тур.	Max.			
Insertion power gain ²	$ S_{21} ^2$	15	16.5	18	dB	_	
Noise figure ²	NF	_	1.15	1.65	dB	Z _S =50 Ω	
Input return loss ^{2 3}	<i>RL</i> _{in}	8	11	_	dB	_	
Output return loss ^{2 3}	<i>RL</i> _{out}	11	19	_	dB	_	
Reverse isolation AO to RX port ^{2 3}	$1/ S_{12} ^2$	20	24	_	dB	-	
Inband input 1dB- compression point ^{2 3}	IP _{1dB}	-13	-10	_	dBm	-	
Inband input 3 rd -order inter- cept point ^{2 3 4}	IIP ₃	-5	-2	_	dBm	f_1 =801 MHz, f_2 =811 MHz, f_{12} =791 MHz	
Isolation RX to RX port ^{2 5}	ISO	34	39	_	dB		
Isolation RX to AO port ^{2 5}	ISO	24	29	_	dB	forward direction	
Stability ⁵	k	>1	_	_		f=20 MHz-10 GHz	
RF Rise Time RX Port On/Off ⁵	t _{on/off}	0.5	1	5	μ S	10 % to 90 % ON; 90 % to 10 % ON	
Power Up Settling Time ⁵	t _{BC}	_	10	25	μ s	After power down mode	

 $^{^{\}rm 1}{\rm The}$ parameter values are valid at any RX port using the matching described in Chapter 7 $^{\rm 2}{\rm PCB}$ losses are subtracted

Data Sheet Revision 3.0 - 2015-07-24 11

³ Verification based on AQL; not 100% tested in production

 $^{^{4}}$ Input power = $-30 \, dBm$ for each tone

⁵Guaranteed by device design; not tested in production



5.4 BAND 26

Table 8: RF Characteristics Band 26 at $T_{\rm A}$ = 25 °C, $V_{\rm DD}$ = 2.8 V, f = 859 – 894 MHz, with matching described in Chapter 7 (C=1.5 pF, L=13 nH)

Parameter ¹	Symbol		Values		Unit	Note / Test Condition	
		Min.	Тур.	Max.			
Insertion power gain ²	$ S_{21} ^2$	14.8	16.3	17.8	dB	_	
Noise figure ²	NF	_	1.2	1.7	dB	Z _S =50 Ω	
Input return loss ^{2 3}	RL _{in}	8	11	_	dB	_	
Output return loss ^{2 3}	RL _{out}	12	>20	_	dB	_	
Reverse isolation AO to RX port ^{2 3}	$1/ S_{12} ^2$	19	23	_	dB	-	
Inband input 1dB- compression point ^{2 3}	IP _{1dB}	-11	-8	_	dBm	-	
Inband input 3 rd -order inter- cept point ^{2 3 4}	IIP ₃	-4	-1	-	dBm	f_1 =871 MHz, f_2 =881 MHz, f_{12} =861 MHz	
Isolation RX to RX port ^{2 5}	ISO	34	39	_	dB		
Isolation RX to AO port ^{2 5}	ISO	24	29	_	dB	forward direction	
Stability ⁵	k	>1	_	_		f=20 MHz-10 GHz	
RF Rise Time RX Port	t _{on/off}	0.5	1	5	μ S	10 % to 90 % ON;	
On/Off ⁵						90 % to 10 % ON	
Power Up Settling Time ⁵	t _{BC}	_	10	25	μ s	After power down mode	

 $^{^{\}rm 1}{\rm The}$ parameter values are valid at any RX port using the matching described in Chapter 7 $^{\rm 2}{\rm PCB}$ losses are subtracted

Data Sheet 12 Revision 3.0 - 2015-07-24

³ Verification based on AQL; not 100% tested in production

 $^{^{4}}$ Input power = $-30 \, dBm$ for each tone

⁵Guaranteed by device design; not tested in production



5.5 BAND 28

Table 9: RF Characteristics Band 28 at $T_{\rm A}$ = 25 °C, $V_{\rm DD}$ = 2.8 V, f = 758 – 803 MHz, with matching described in Chapter 7 (C=2 pF, L=16 nH)

Parameter ¹	Symbol	Symbol Values			Unit	Note / Test Condition	
		Min.	Тур.	Max.			
Insertion power gain ²	$ S_{21} ^2$	15.1	16.6	18.1	dB	_	
Noise figure ²	NF	_	1.1	1.6	dB	Z _S =50 Ω	
Input return loss ^{2 3}	RL _{in}	8	11	_	dB	_	
Output return loss ^{2 3}	<i>RL</i> _{out}	11	16	_	dB	_	
Reverse isolation AO to RX port ^{2 3}	$1/ S_{12} ^2$	21	25	-	dB	-	
Inband input 1dB- compression point ^{2 3}	IP _{1dB}	-13	-10	_	dBm	-	
Inband input 3 rd -order inter- cept point ^{2 3 4}	IIP ₃	-6	-3	_	dBm	$f_1 = 775 \text{ MHz}, $ $f_2 = 785 \text{ MHz},$ $f_{12} = 765 \text{ MHz}$	
Isolation RX to RX port ^{2 5}	ISO	34	39	_	dB		
Isolation RX to AO port ^{2 5}	ISO	24	29	_	dB	forward direction	
Stability ⁵	k	>1	_	_		f=20 MHz-10 GHz	
RF Rise Time RX Port On/Off ⁵	t _{on/off}	0.5	1	5	μ S	10 % to 90 % ON; 90 % to 10 % ON	
Power Up Settling Time ⁵	t _{BC}	_	10	25	μ S	After power down mode	

 $^{^{\}rm 1}{\rm The}$ parameter values are valid at any RX port using the matching described in Chapter 7 $^{\rm 2}{\rm PCB}$ losses are subtracted

Data Sheet Revision 3.0 - 2015-07-24 13

³ Verification based on AQL; not 100% tested in production

 $^{^{4}}$ Input power = $-30 \, dBm$ for each tone

⁵Guaranteed by device design; not tested in production



6 MIPI RFFE Specification

All sequences are implemented according to the 'MIPI Alliance Specification for RF Front-End Control Interface' document version 1.10 - 26. July 2011.

Table 10: MIPI Features

Feature	Supported	Comment
Register write command sequence	Yes	
Register read command sequence	Yes	
Extended register write command sequence	No	Up to 4 Bytes
Extended register read command sequence	No	Up to 4 Bytes
Register 0 write command sequence	Yes	
Trigger function	Yes	Trigger assignment to each control register is sup-
		ported
Programmable USID	Yes	3 register command sequence and extended regis-
		ter command sequence
Status Register	Yes	Register for debugging
Reset	Yes	By VIO, Power Mode and RFFE_STATUS
Group SID	Yes	
USID_Sel pin	No	External pin for changing USID is not implemented
Full speed write	Yes	
Half speed read	Yes	
Full speed read	Yes	

Table 11: Startup Behavior

Feature	State	Comment
Power status	LOW POWER	The chip is in low power mode after startup
Trigger function	ENABLED	Trigger function is enabled after startup. Trigger function can be dis-
		abled via PM_TRIG register.

Data Sheet 14 Revision 3.0 - 2015-07-24



Table 12: MIPI RFFE Operating Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Тур.	Max.		
CCLK Eroquopov	FSCLK	0.032	_	26	MHz	Full speed
SCLK Frequency	FSCLK	0.032	_	13	MHz	Half speed
SCLK Period	TSCLK	0.038	-	32	μ s	Full speed
SOLIN I GIIOU	TOOLK	0.077	-	32	μ S	Half speed
SCLK Low Period	TSCLKIL	11.25	_	_	ns	Full speed, see Fig. 2
OLIN LOW I GIIOG	TOOLNIL	24	_	_	ns	Half speed, see Fig. 2
SCLK High Period	TSCLKIH	11.25	_	_	ns	Full speed, see Fig. 2
OCEN Flight Fellod	TOOLKIIT	24	_	_	ns	Half speed, see Fig. 2
SDATA Setup Time	TS	1	_	_	ns	Full speed, see Fig. 3
	10	2	_	_	ns	Half speed, see Fig. 3
SDATA Hold Time	TH	5	_	_	ns	Full speed, see Fig. 3
DDATA FIOID TIME	111	5	_	_	ns	Half speed, see Fig. 3
SDATA Release Time	TSDATAZ	_	_	10	ns	Full speed, see Fig. 4
DAIA Helease Time	TODAIAL	_	_	18	ns	Half speed, see Fig. 4
Fime for Data Output	TD	_	_	10.25	ns	Full speed, see Fig. 5
ine ioi bata Output	10	_	_	22	ns	Half speed, see Fig. 5
SDATA Rise/Fall Time	TSDATAOTR	2.1	_	6.5	ns	Full speed, see Fig. 5
DAIA HISE/I dii Hille	IODAIAOIT	2.1	_	10	ns	Half speed, see Fig. 5
IO Rise Time	TVIO-R	10	_	450	μ S	See Fig. 6
/IO Reset Time	TVIO-RST	10	-	_	μ s	See Fig. 6
Reset Delay Time	TSIGOL	0.12	_	_	μ S	See Fig. 6

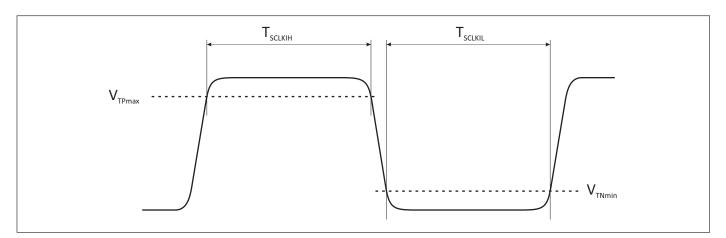


Figure 2: Received clock signal constraints



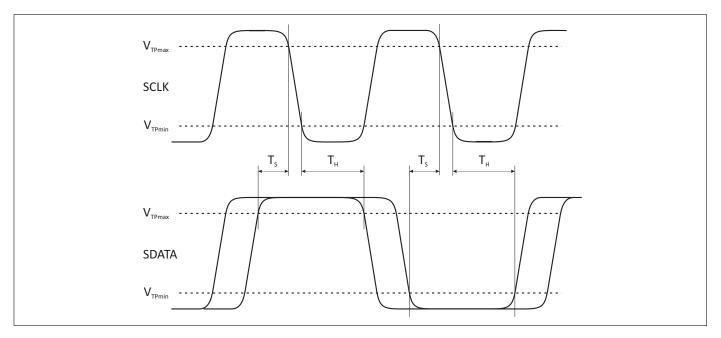


Figure 3: Bus active data receiver timing requirements

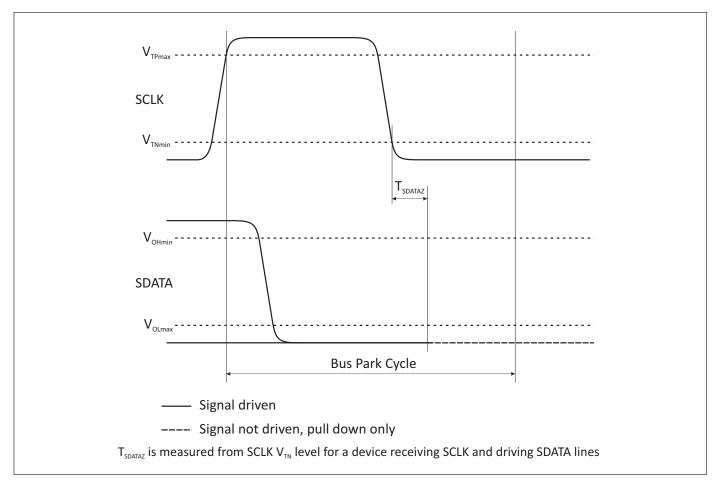


Figure 4: Bus park cycle timing

Data Sheet 16 Revision 3.0 - 2015-07-24



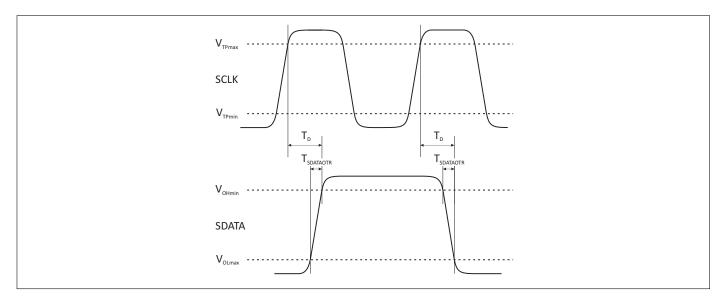


Figure 5: Bus active data transmission timing specification

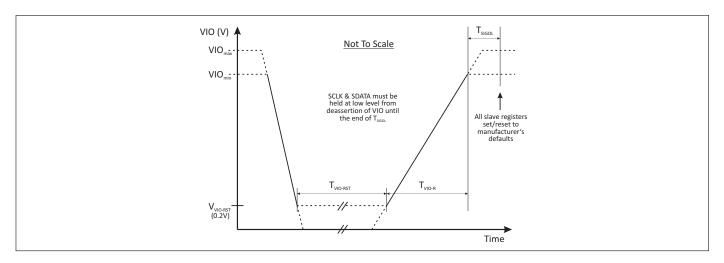


Figure 6: Requirements for VIO-initiated reset

Table 13: Register Mapping

Register	Register Name	Data	Function	Description	Default	Broadcast_ID	Trigger	R/W
Address		Bits				Support	Support	
0x0000	REGISTER_0	7:0	MODE_CTRL	Module control	00000000	No	Yes	R/W
0x001D	PRODUCT_ID	7:0	PRODUCT_ID	This is a read-only register. However,	11010001	No	No	R
				during the programming of the USID				
				a write command sequence is per-				
				formed on this register, even though				
				the write does not change its value.				
0x001E	MANUFACTURER_ID	7:0	MANUFACTURER_ID [7:0]	This is a read-only register. However,	00011010	No	No	R
				during the programming of the USID,				
				a write command sequence is per-				
				formed on this register, even though				
				the write does not change its value.				

Continued on next page



Table 13: Register Mapping - Continued from previous page

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x001C	PM_TRIG	7:6	PWR_MODE	00: Normal operation 01: Default settings (STARTUP) 10: Low power (LOW POWER) 11: Reserved	10	Yes	No	R/W
		5	TRIGGER_MASK_2	If this bit is set, trigger 2 is disabled. When all triggers disabled, if writing to a register that is associated to trigger 2, the data goes directly to the desti- nation register.	0	No	No	
		4	TRIGGER_MASK_1	If this bit is set, trigger 1 is disabled. When all triggers disabled, if writing to a register that is associated to trigger 1, the data goes directly to the desti- nation register.	0	No	No	
		3	TRIGGER_MASK_0	If this bit is set, trigger 0 is disabled. When all triggers disabled, if writing to a register that is associated to trigger 0, the data goes directly to the desti- nation register.	0	No	No	
		2	TRIGGER_2	A write of a one to this bit loads trigger 2's registers.	0	Yes	No	
		1	TRIGGER_1	A write of a one to this bit loads trigger 1's registers.	0	Yes	No	R/W
		0	TRIGGER_0	A write of a one to this bit loads trigger 0's registers.	0	Yes	No	
0x001F	MAN_USID	7:6	SPARE	These are read-only bits that are reserved and yield a value of 0b00 at readback.	00	No	No	R/W
		5:4	MANUFACTURER_ID [9:8]	These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value.	01			
		3:0	USID	Programmable USID. Performing a write to this register using the described programming sequences will program the USID in devices supporting this feature. These bits store the USID of the device.	0001			
0x001A	RFFE_STATUS	7	SOFTWARE RESET	Normal operation Software reset	0	No	No	R/W
		6	COMMAND_FRAME_ PARITY_ERR	Command sequence received with parity error - discard command.	0	No	No	R
		5	COMMAND_LENGTH_ERR	Command length error	0			
		4	ADDRESS_FRAME_ PARITY_ERR	Address frame parity error = 1	0			
		3	DATA_FRAME_ PARITY_ERR	Data frame with parity error	0			
		2	READ_UNUSED_REG	Read command to an invalid address	0]		
		1	WRITE_UNUSED_REG	Write command to an invalid address	0]		
		0	BID_GID_ERR	Read command with a BROAD- CAST_ID or GROUP_SID	0			
0x001B	GROUP_SID	7:4	RESERVED		0	No	No	R/W
		3:0	GROUP_SID	Group slave ID	0			



Table 14: Modes of Operation (Truth Table, Register_0)

		REGISTER_0 Bits							
State	Mode	D7	D6	D5	D4	D3	D2	D1	D0
1	Isolation	х	х	х	0	0	0	0	0
2	RX1-AO	х	х	х	0	0	0	0	1
3	RX2-AO	х	х	х	0	0	0	1	0
4	RX3-AO	х	х	х	0	1	0	0	0
5	RX4-AO	х	х	х	0	0	1	0	0
6	RX5-AO	х	х	х	1	0	0	0	0
7	RX1&RX2-AO	х	х	х	0	0	0	1	1
8	RX2&RX3-AO	х	х	х	0	1	0	1	0
9	RX3&RX4-AO	х	х	х	0	1	1	0	0
10	RX4&RX5-AO	х	х	х	1	0	1	0	0
11	RX1&RX3-AO	х	х	х	0	1	0	0	1
12	RX2&RX4-AO	х	х	х	0	0	1	1	0
13	RX3&RX5-AO	х	х	х	1	1	0	0	0
14	RX1&RX4-AO	х	х	Х	0	0	1	0	1
15	RX2&RX5-AO	х	х	Х	1	0	0	1	0
16	RX1&RX5-AO	x	Х	х	1	0	0	0	1



7 Application Information

Pin Configuration and Function

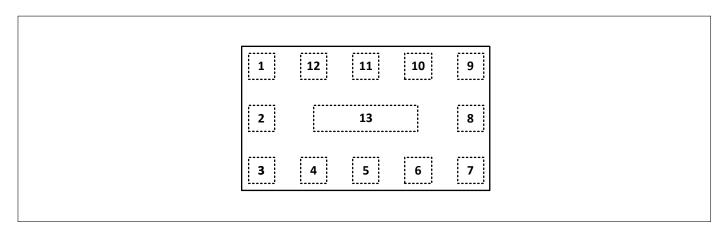


Figure 7: BGM15LA12 Pin Configuration (top view)

Table 15: Pin Definition and Function

Name	Function
SCLK	MIPI RFFE Clock
VIO	MIPI RFFE Power Supply
RX5	RF-Port RX No. 5
RX4	RF-Port RX No. 4
RX3	RF-Port RX No. 3
RX2	RF-Port RX No. 2
RX1	RF-Port RX No. 1
GND	Ground
GND	Ground
AO	RF-Output Port
VDD	Power Supply
SDATA	MIPI RFFE Data IO
GND	Ground
	SCLK VIO RX5 RX4 RX3 RX2 RX1 GND GND AO VDD SDATA



Application Board Configuration

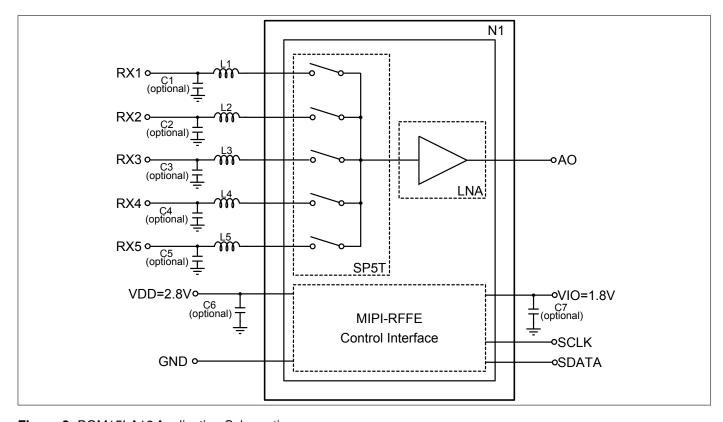


Figure 8: BGM15LA12 Application Schematic

Table 16: Bill of Materials Table

Name -	Value	Daalsana	BA f t	Fation
Name	Value	Package	Manufacturer	Function
C1 (optional)	2 pF	0402	Various	Input matching Band 28 ²⁾
C2 (optional)	1.1 pF	0402	Various	Input matching Band 8 ²⁾
C3 (optional)	1.8 pF	0402	Various	Input matching Band 20 ²⁾
C4 (optional)	2.2 pF	0402	Various	Input matching Band 12 ²⁾
C5 (optional)	1.5 pF	0402	Various	Input matching Band 26 ²⁾
C6 (optional)	1 nF	0402	Various	RF Bypass ¹⁾
C7 (optional)	1 nF	0402	Various	RF Bypass ¹⁾
L1	16 nH	0402	Various	Input matching Band 28 ²⁾
L2	11 nH	0402	Various	Input matching Band 82)
L3	15 nH	0402	Various	Input matching Band 20 ²⁾
L4	18 nH	0402	Various	Input matching Band 12 ²⁾
L5	13 nH	0402	Various	Input matching Band 26 ²⁾
N1	BGM15LA12	ATSLP-12-1	Infineon	LNA Multiplexer Module

¹⁾RF bypass recommended to mitigate power supply noise.

²⁾ The matching elements must be optimized with reference to the frequency band of interest. Each band can be arbiratily assigned to an RF port. The configuration shown in the table is only an example of the port assignment.



8 Package Information

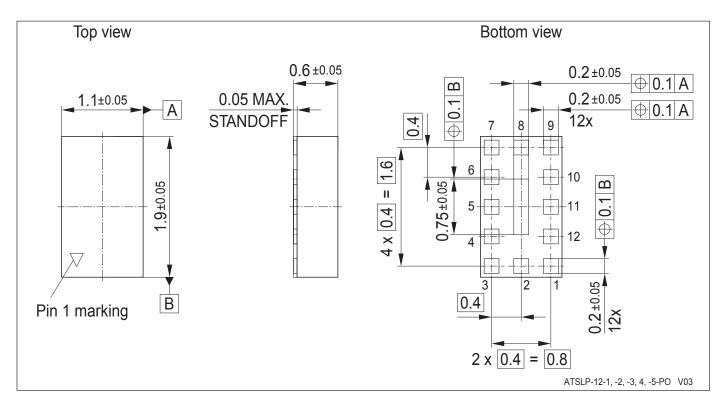


Figure 9: ATSLP-12-1 Package Outline (top, side and bottom views)

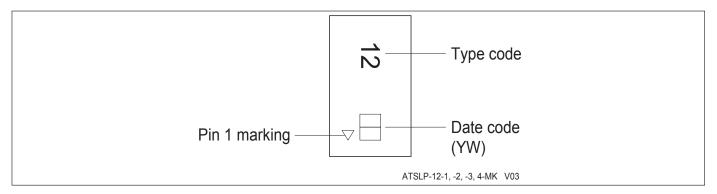


Figure 10: Marking Specification (top view)



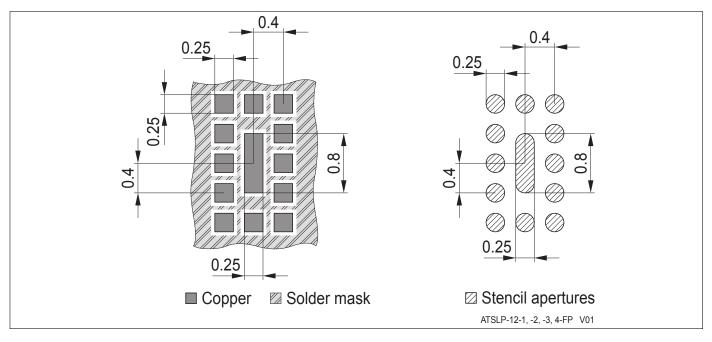


Figure 11: Footprint Recommendation

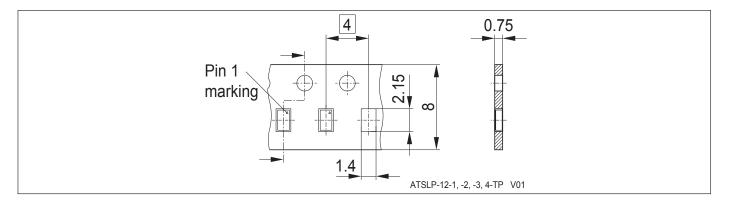


Figure 12: ATSLP-12-1 Carrier Tape

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