

GAN039-650NBBA

650 V, 33 mOhm Gallium Nitride (GaN) FET in a CCPAK1212 package

19 April 2021

Objective data sheet

1. General description

The GAN039-650NBBA is an Automotive qualified 650 V, 33 m Ω Gallium Nitride (GaN) FET in a CCPAK1212 package. It is a normally-off device that combines Nexperia's latest high-voltage GaN HEMT H2 technology and low-voltage silicon MOSFET technologies — offering superior reliability and performance.

This product has been fully designed and qualified to meet AEC-Q101 requirements.

2. Features and benefits

- Fully automotive qualified to AEC-Q101:
 - 175 °C rating suitable for thermally demanding environments
- · Simplified driver design as standard level MOSFET gate drivers can be used:
 - 0 V to 12 V drive voltage
 - Gate threshold voltage V_{GSth} of 4 V
- Robust gate oxide with ±20 V V_{GS} rating
- · High gate threshold voltage of 4 V for gate bounce immunity
- Low body diode V_f for reduced losses and simplified dead-time adjustments
- Transient over-voltage capability for increased robustness
- CCPAK package technology:
 - Improved reliability, with reduced R_{th(i-mb)} for optimal cooling
 - Lower inductances for lower switching losses and EMI
 - 175 °C maximum junction temperature
 - High Board Level Reliability absorbing mechanical stress during thermal cycling, unlike traditional QFN packages
 - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
 - Easy solder wetting for good mechanical solder joints

3. Applications

- Automotive On-Board-Charger systems
- Automotive DC-DC
- · Hard and soft switching converters for industrial and datacom power
- Bridgeless totempole PFC
- PV and UPS inverters
- Servo motor drives

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{DS}	drain-source voltage	-55 °C ≤ T _j ≤ 175 °C	-	-	650	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C	-	-	60	А
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>	-	-	300	W



Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Tj	junction temperature		-55	-	175	°C
Static chara	cteristics					
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 32 \text{ A}; T_j = 25 \text{ °C}$	-	33	39	mΩ
Dynamic cha	aracteristics					
Q_{GD}	gate-drain charge	I _D = 32 A; V _{DS} = 400 V; V _{GS} = 10 V;	-	5	-	nC
Q _{G(tot)}	total gate charge	T _j = 25 °C	-	30	-	nC
Source-drain	n diode			•		'
Q _r	recovered charge	$I_S = 32 \text{ A}; dI_S/dt = -1000 \text{ A/}\mu\text{s};$ $V_{GS} = 0 \text{ V}; V_{DS} = 400 \text{ V}; Fig. 3$	-	150	-	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	1 2 3 4 5 6	D
2	S	source		
3	S	source		
4	S	source		
5	S	source		
6	S	source	12 11 10 9 8 7	
7	D	drain	CCPAK (SOT8000)	s
8	D	drain		aaa-028116
9	D	drain		
10	D	drain		
11	D	drain		
12	D	drain		
mb	S	mounting base; connected to source		

6. Ordering information

Table 3. Ordering information

Type number	Package	ackage					
	Name	Description	Version				
GAN039-650NBBA	CCPAK	Plastic, surface mounted copper clip package (CCPAK1212); 13 terminals; 2.0 mm pitch, 12 mm x 12 mm x 2.5 mm body	SOT8000				

7. Marking

Table 4. Marking codes

Type number	Marking code
GAN039-650NBBA	039INBBA

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	-55 °C ≤ T _j ≤ 175 °C	-	650	V
V _{TDS}	transient drain to source voltage	pulsed; $t_p = 1 \mu s$; $\delta_{factor} = 0.01$	-	[tbd]	V
V_{GS}	gate-source voltage		-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>	-	300	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C	-	60	А
		V _{GS} = 10 V; T _{mb} = 100 °C	-	42	А
I _{DM}	peak drain current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 °C$	-	240	А
T _{stg}	storage temperature		-55	175	°C
Tj	junction temperature		-55	175	°C
T _{sld(M)}	peak soldering temperature		-	260	°C
Source-drain	diode			•	
Is	source current	T _{mb} = 25 °C; V _{GS} = 0 V	-	55	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 °C$	-	240	А

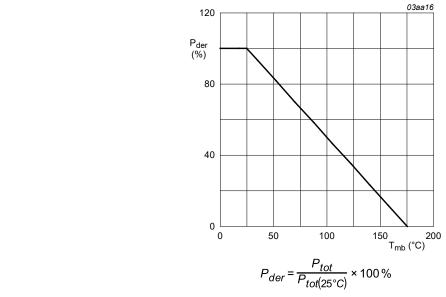


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base		-	-	0.5	K/W

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
V _{GS(th)}	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C}$	3.3	4	4.8	V
I _{DSS}	drain leakage current	$V_{DS} = 650 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	[tbd]	[tbd]	μΑ
		V _{DS} = 650 V; V _{GS} = 0 V; T _j = 175 °C	-	[tbd]	-	μΑ
I _{GSS}	gate leakage current	$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	10	400	nA
		V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	10	400	nA
R _{DSon}	drain-source on-state	$V_{GS} = 10 \text{ V}; I_D = 32 \text{ A}; T_j = 25 ^{\circ}\text{C}$	-	33	39	mΩ
	resistance	V_{GS} = 10 V; I_D = 32 A; T_j = 175 °C; Fig. 2	-	80	-	mΩ
R _G	gate resistance	f = 1 MHz	-	1.88	-	Ω
Dynamic ch	naracteristics		'			
Q _{G(tot)}	total gate charge	I _D = 32 A; V _{DS} = 400 V; V _{GS} = 10 V; T _j = 25 °C	-	30	-	nC
Q _{GS}	gate-source charge		-	9	-	nC
Q_{GD}	gate-drain charge		-	5	-	nC
C _{iss}	input capacitance	$V_{DS} = 400 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ °C}$	-	1500	-	pF
C _{oss}	output capacitance		-	147	-	pF
C _{rss}	reverse transfer capacitance		-	5	-	pF
C _{o(er)}	effective output capacitance, energy related	0 V ≤ V _{DS} ≤ 400 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C	-	220	-	pF
C _{o(tr)}	effective output capacitance, time related		-	380	-	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 400 \text{ V}; R_L = 12.5 \Omega; V_{GS} = 12 \text{ V};$	-	[tbd]	-	ns
t _r	rise time	$R_{G(ext)} = 30 \Omega$	-	[tbd]	-	ns
t _{d(off)}	turn-off delay time	1	-	[tbd]	-	ns
t _f	fall time	1	-	[tbd]	-	ns
Q _{oss}	output charge	V _{GS} = 0 V; V _{DS} = 400 V	-	150	-	nC
Source-dra	in diode		'			
V_{SD}	source-drain voltage	$I_S = 32 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}$	-	1.8	-	V
		I _S = 16 A; V _{GS} = 0 V; T _j = 25 °C	-	1.3	-	V
t _{rr}	reverse recovery time	I _S = 32 A; dI _S /dt = -1000 A/µs;	-	[tbd]	-	ns
Qr	recovered charge	V _{GS} = 0 V; V _{DS} = 400 V; <u>Fig. 3</u>	-	150	-	nC

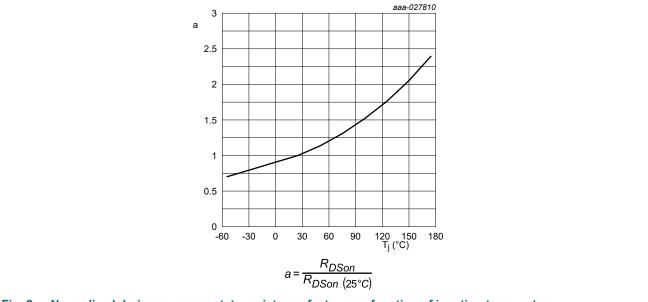
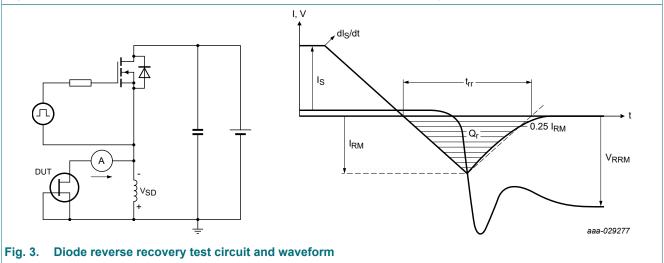
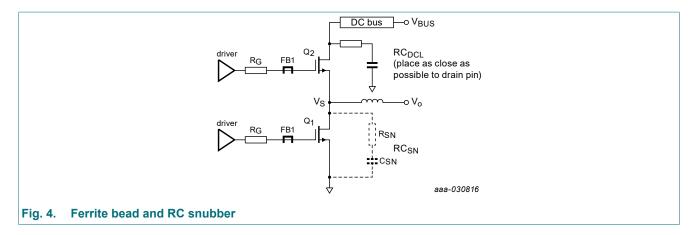


Fig. 2. Normalized drain-source on-state resistance factor as a function of junction temperature



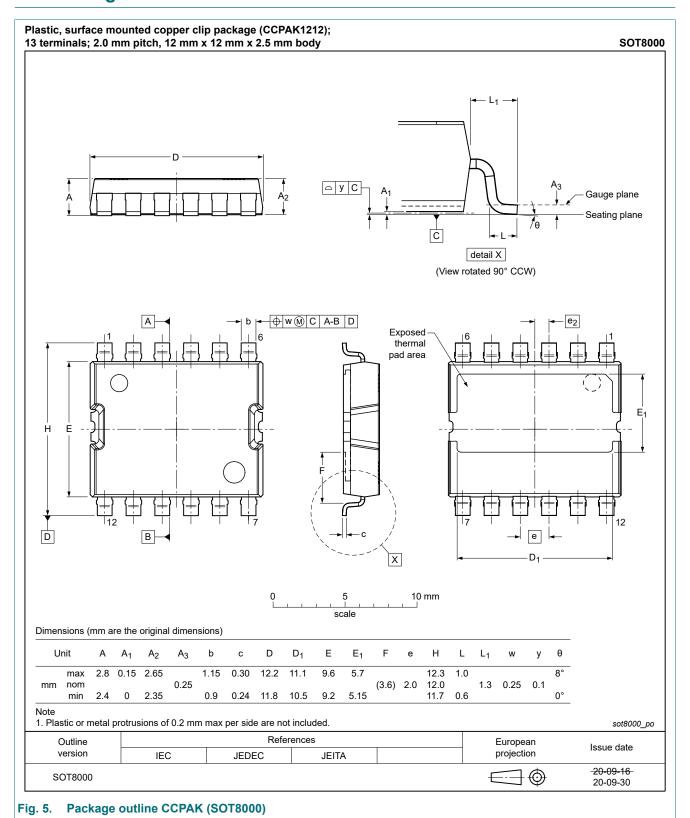
11. Application information

A Ferrite bead must be fitted in series with the gate of the GaN FET and should be located as close as possible to the gate pin, (see figure below). Keeping the gate-source loop as compact as possible minimizes the gate loop inductance. The Ferrite bead damps the resonant circuit made up of the gate source loop inductance and the GaN FET input capacitance, thus providing fast switching stability. It is recommended that the impedance of the ferrite bead should be 30 Ω @ 100 MHz, (recommended p/n BLM18PG300SN1D). A series resistance (R_G) of 10 - 15 Ω is also recommended.



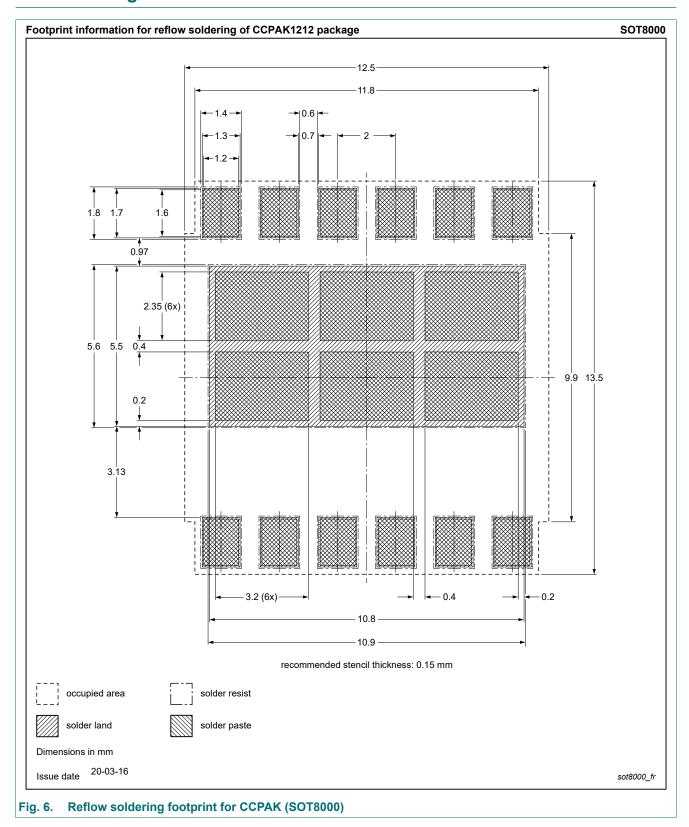
A DC-link snubber is recommended in all cases. Optimal is 20 nF in series with 4 Ω , most easily achieved with parallel combination 10 nF and 8 Ω . This snubber lowers the Q factor of any resonance in the bus. That resonance will act as a load on the high gain amplifier that is the GaN FET and can lead to instability.

12. Package outline



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13. Soldering



14. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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