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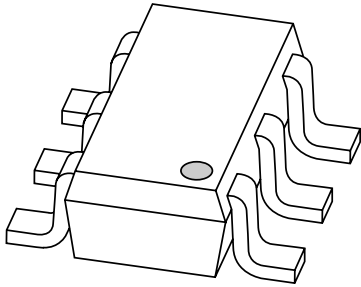
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Kind regards,

Team Nexperia

DATA SHEET



BZA462A

Quadruple ESD transient voltage
suppressor

Product data sheet
Supersedes data of 1998 Oct 30

1999 May 25

Quadruple ESD transient voltage suppressor

BZA462A

FEATURES

- ESD rating >15 kV, according to IEC1000-4-2
- SOT457 surface mount package
- Common anode configuration
- Non-clamping range -0.5 to 6.2 V
- Maximum reverse peak power dissipation: 24 W at $t_p = 1$ ms
- Maximum clamping voltage at peak pulse current: 9 V at $I_{ZSM} = 2.66$ A.

APPLICATIONS

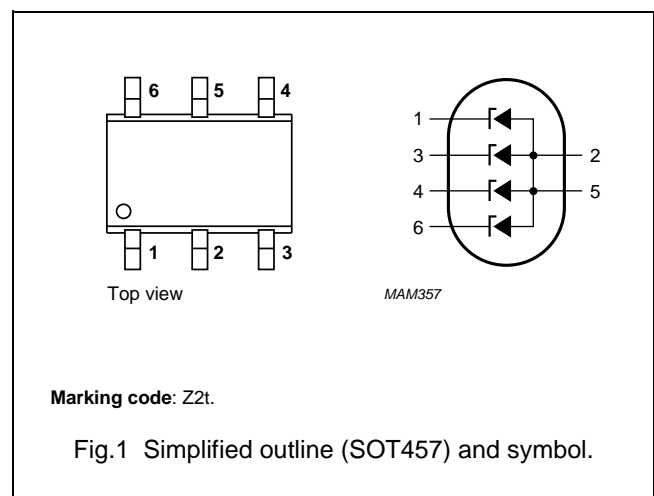
- Computers and peripherals
- Audio and video equipment
- Communication systems
- Medical equipment.

DESCRIPTION

Monolithic transient voltage suppressor diode in a six lead SOT457 (SC-74) package for 4-bit wide ESD transient suppression at 6.2 V level.

PINNING

PIN	DESCRIPTION
1	cathode 1
2	common
3	cathode 2
4	cathode 3
5	common
6	cathode 4



LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per diode					
I_Z	working current	$T_s = 60$ °C; note 1	-	note 2	mA
I_F	continuous forward current	$T_s = 60$ °C	-	100	mA
I_{FSM}	non-repetitive peak forward current	$t_p = 1$ ms; square pulse	-	3.75	A
I_{ZSM}	non-repetitive peak reverse current	$t_p = 1$ ms; square pulse; see Fig.2	-	2.66	A
P_{tot}	total power dissipation	$T_s = 60$ °C; see Fig.3	-	720	mW
P_{ZSM}	non repetitive peak reverse power dissipation	square pulse; $t_p = 1$ ms; see Fig.4	-	24	W
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-65	+150	°C

Notes

1. T_s is the temperature at the soldering point of the anode pin.
2. DC working current limited by $P_{tot\ max}$.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-s}$	thermal resistance from junction to soldering point	one or more diodes loaded	125	K/W

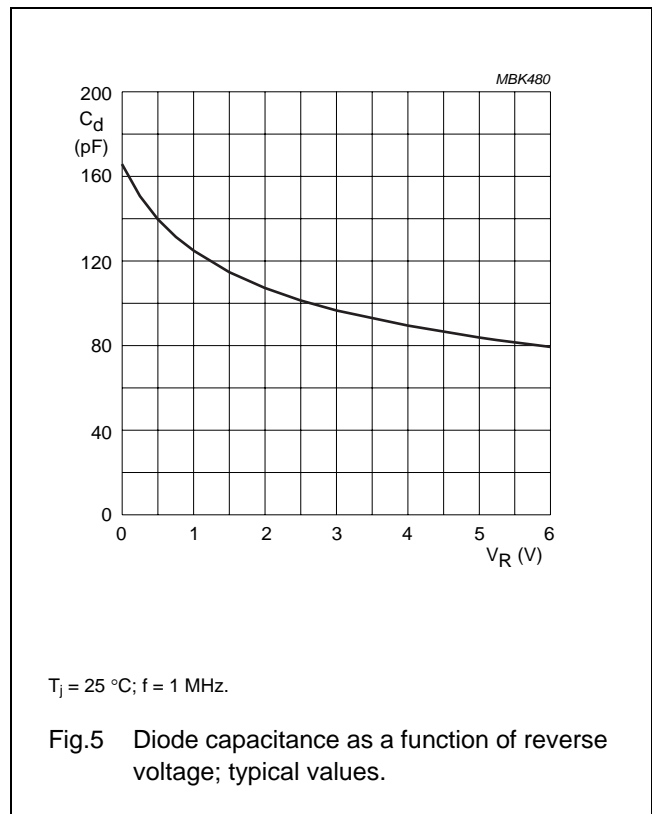
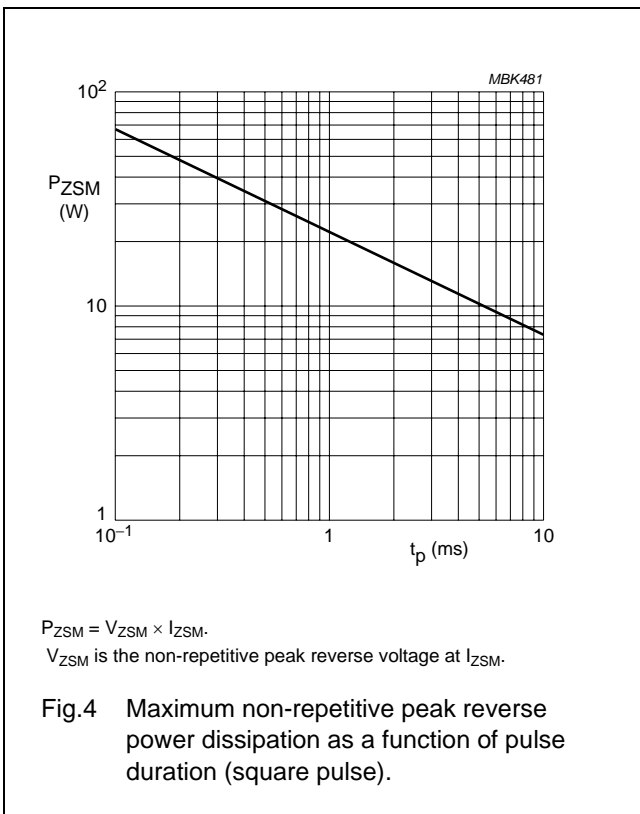
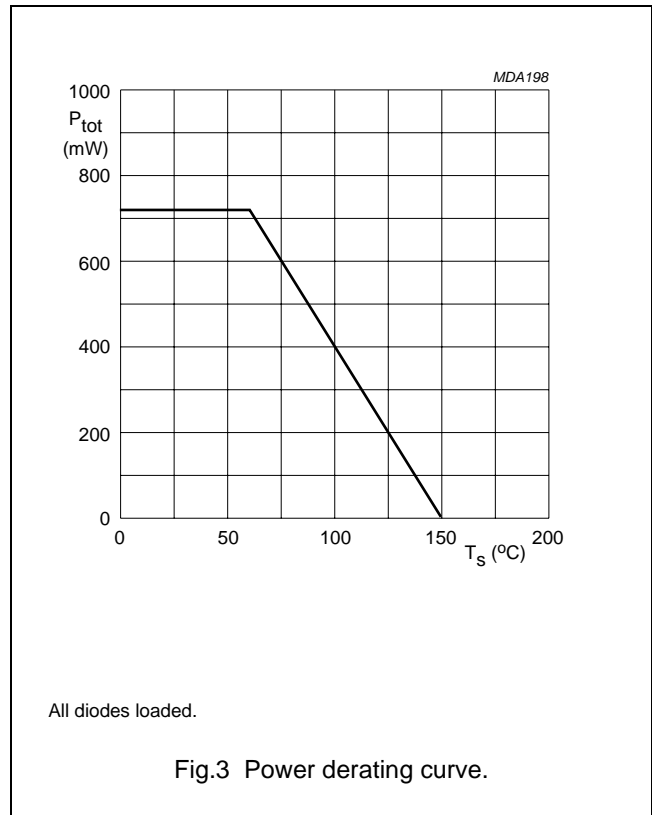
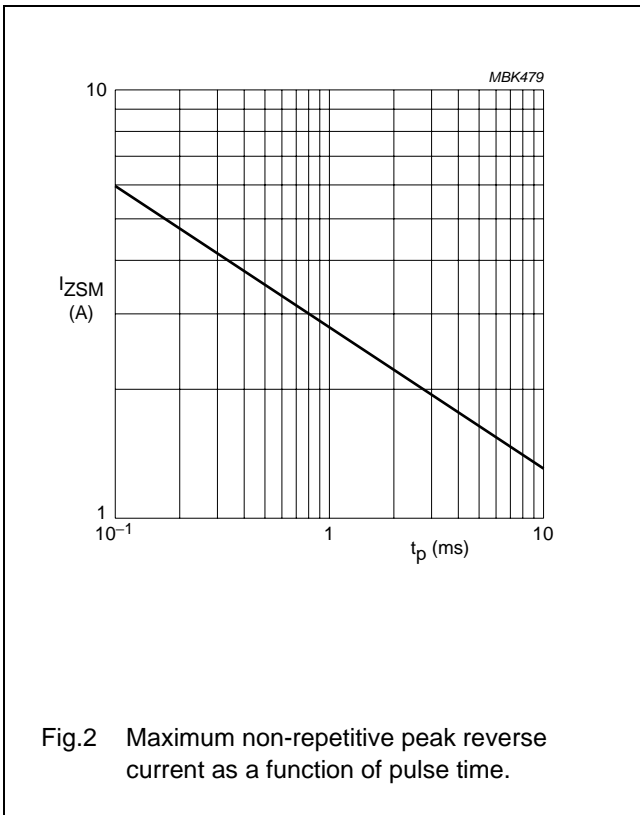
ELECTRICAL CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per diode						
V_Z	working voltage	$I_Z = 1\text{ mA}$	5.89	6.2	6.51	V
V_F	forward voltage	$I_F = 200\text{ mA}$	–	–	1.3	V
V_{ZSM}	non-repetitive peak reverse voltage	$I_{ZSM} = 3.5\text{ A}; t_p = 1\text{ ms}$	–	–	9	V
I_R	reverse current	$V_R = 4\text{ V}$	–	–	700	nA
r_{dif}	differential resistance	$I_Z = 1\text{ mA}$	–	–	300	Ω
S_Z	temperature coefficient of working voltage	$I_Z = 5\text{ mA}$	–	1.2	–	mV/K
C_d	diode capacitance	see Fig.5 $V_R = 0; f = 1\text{ MHz}$ $V_R = 4\text{ V}; f = 1\text{ MHz}$	–	–	200	pF
			–	–	110	pF

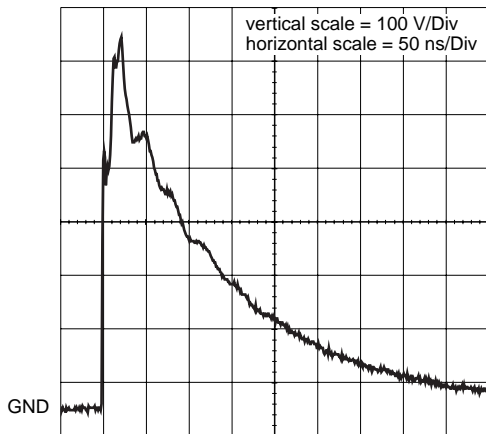
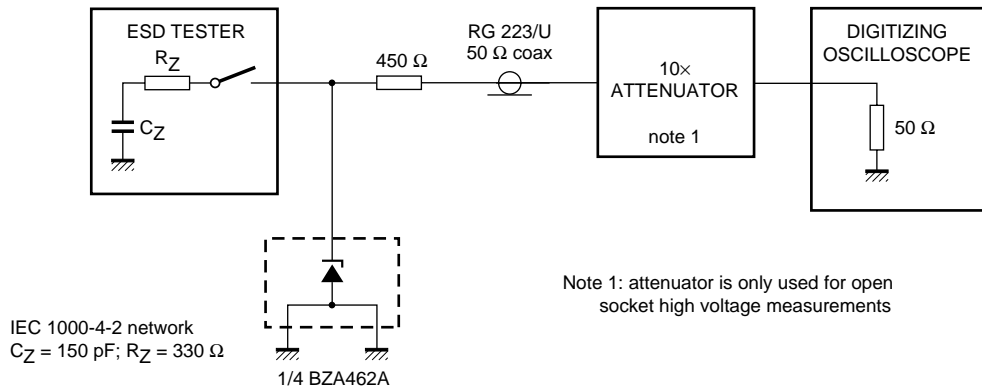
Quadruple ESD transient voltage suppressor

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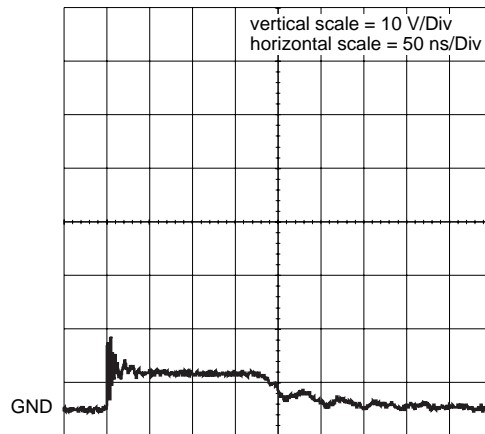


Quadruple ESD transient voltage suppressor

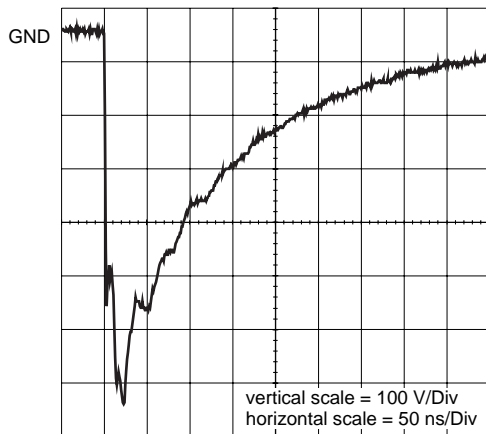
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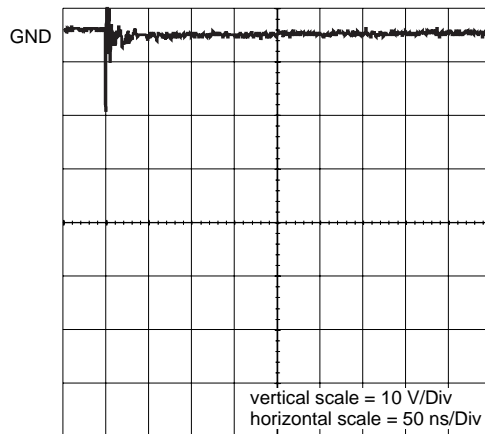
unclamped +1 kV ESD voltage waveform (IEC 1000-4-2 network)



clamped +1 kV ESD voltage waveform (IEC 1000-4-2 network)



unclamped -1 kV ESD voltage waveform (IEC 1000-4-2 network)



clamped -1 kV ESD voltage waveform (IEC 1000-4-2 network)

MBK478

Fig.6 ESD clamping test set-up and waveforms.

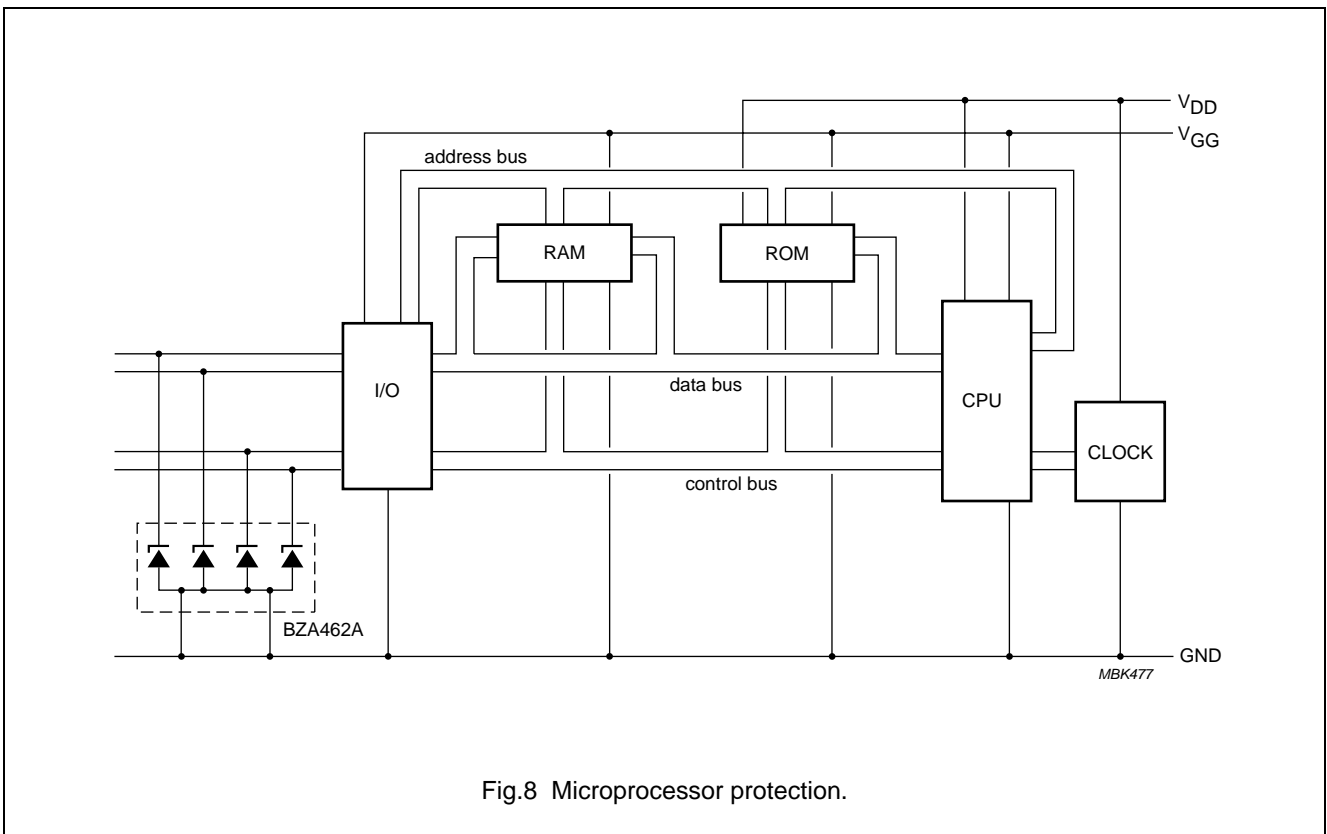
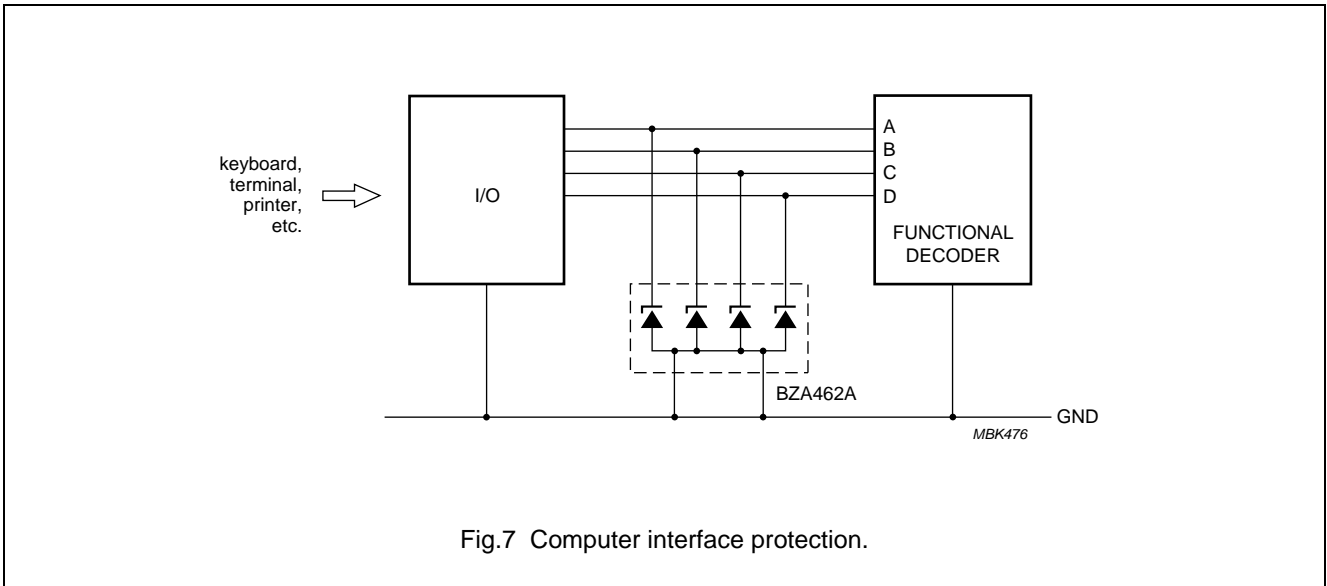
Quadruple ESD transient voltage suppressor

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APPLICATION INFORMATION

Typical common anode application

A quadruple transient suppressor in a SOT457 package makes it possible to protect four separate lines using only one package. Two simplified examples are shown in Figs 7 and 8.



Quadruple ESD transient voltage suppressor

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Device placement and printed-circuit board layout

Circuit board layout is of extreme importance in the suppression of transients. The clamping voltage of the BZA462A is determined by the peak transient current and the rate of rise of that current (di/dt). Since parasitic inductances can further add to the clamping voltage ($V = L di/dt$) the series conductor lengths on the printed-circuit board should be kept to a minimum. This includes the lead length of the suppression element.

In addition to minimizing conductor length the following printed-circuit board layout guidelines are recommended:

1. Place the suppression element close to the input terminals or connectors.
2. Keep parallel signal paths to a minimum.
3. Avoid running protection conductors in parallel with unprotected conductors.
4. Minimize all printed-circuit board loop areas including power and ground loops.
5. Minimize the length of the transient return path to ground.
6. Avoid using shared transient return paths to a common ground point.

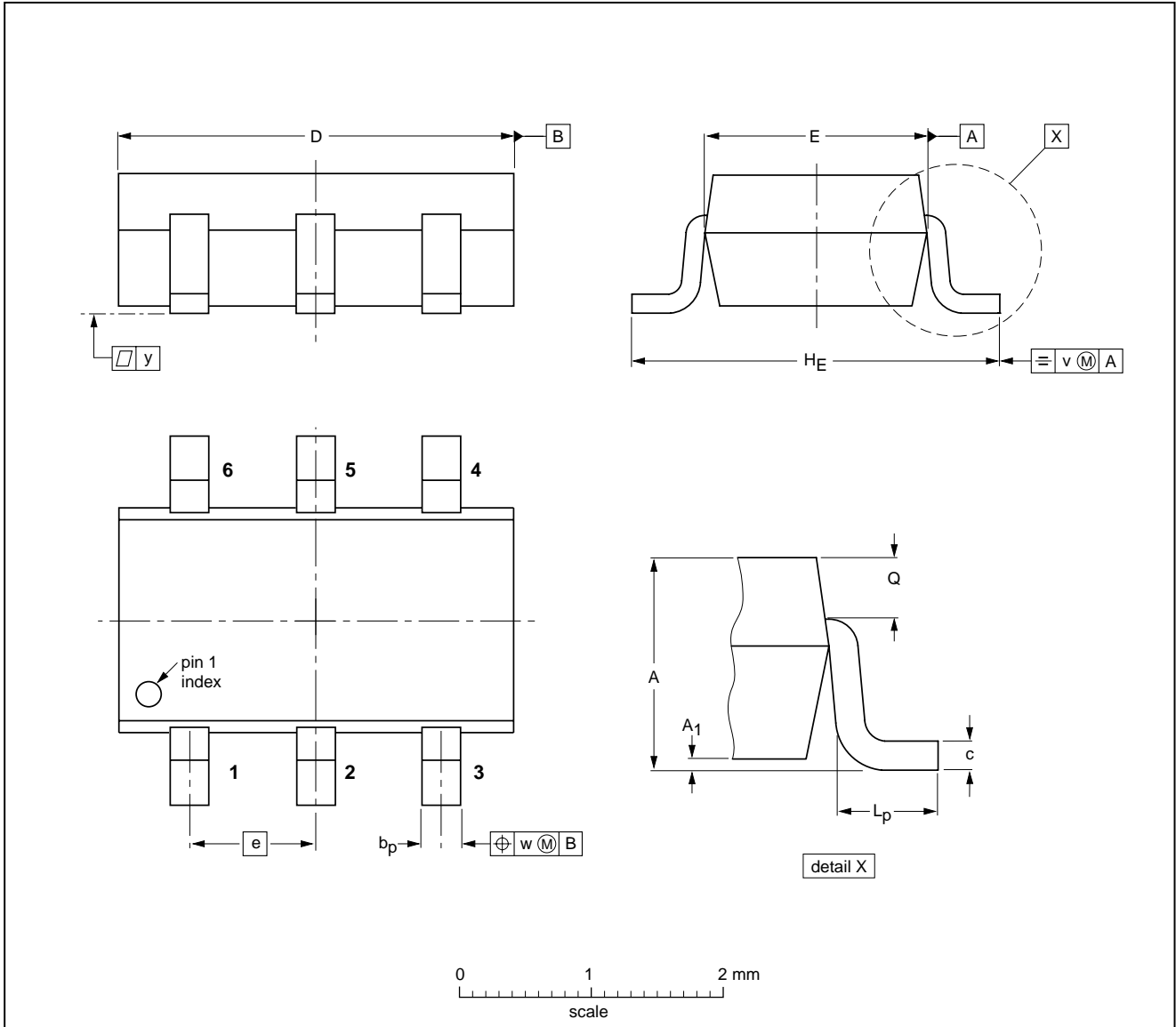
Quadruple ESD transient voltage suppressor

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PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT457



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b _p	c	D	E	e	H _E	L _p	Q	v	w	y
mm	1.1 0.9	0.1 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT457			SC-74			-97-02-28- 01-05-04

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DATA SHEET STATUS

DOCUMENT STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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NXP Semiconductors

Customer notification

This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

Contact information

For additional information please visit: <http://www.nxp.com>

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