TwinDie™ RLDRAM 3

MT44K64M18 – 2 Meg x 18 x 16 Banks x 2 Ranks

MT44K32M36 – 2 Meg x 36 x 16 Banks

Features

- Uses 576Mb Micron RLDRAM 3 die
- Organization
  - 32 Meg x 18 x 2 ranks
  - 32 Meg x 36 x 1 rank
  - 16 banks per die
  - Common I/O (CIO)
- 1.2V center-terminated push/pull I/O
- 2.5V V_{EXT}, 1.35V V_{DD}, 1.2V V_{DDQ} I/O

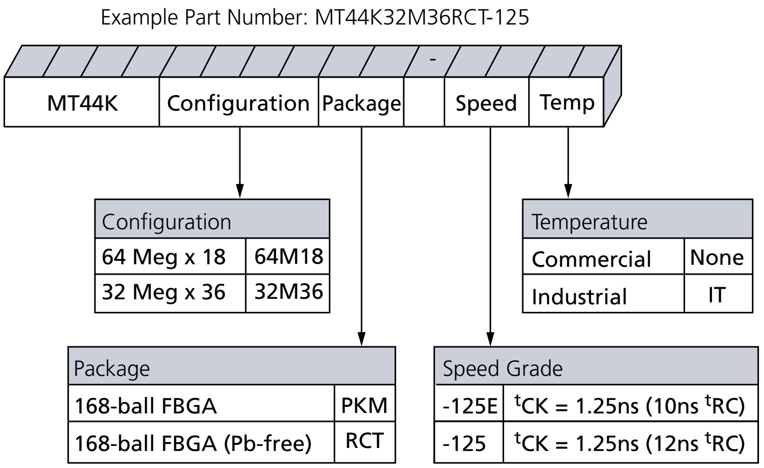
Description

The 1Gb (TwinDie™) RLDRAM 3 uses Micron's 576Mb RLDRAM 3 die. Refer to Micron's 576Mb RLDRAM 3 data sheet for the specifications not included in this document. Specifications for base part number MT44K32M18 correlate to both TwinDie manufacturing part numbers MT44K64M18 and MT44K32M36.

Options

Options	Marking
• 168-ball FBGA package	
– 1.25ns and $^{t}RC_{min}$ = 10ns (RL3-1600)	-125E
– 1.25ns and $^{t}RC_{min}$ = 12ns (RL3-1600)	-125
• Configuration	
– 64 Meg x 18	64M18
– 32 Meg x 36	32M36
• Operating temperature	
– Commercial (T_C = 0° to +95°C)	None
– Industrial (T_C = -40°C to +95°C)	IT
• Package	
– 168-ball FBGA	PKM
– 168-ball FBGA (Pb-free)	RCT

Figure 1: 576Mb RLDRAM 3 Part Numbers



Configuration	
64 Meg x 18	64M18
32 Meg x 36	32M36

Temperature	
Commercial	None
Industrial	IT

Package	
168-ball FBGA	PKM
168-ball FBGA (Pb-free)	RCT

Speed Grade	
-125E	^{t}CK = 1.25ns (10ns ^{t}RC)
-125	^{t}CK = 1.25ns (12ns ^{t}RC)

BGA Part Marking Decoder

Due to space limitations, BGA-packaged components have an abbreviated part marking that is different from the part number. Micron's BGA Part Marking Decoder is available on Micron's Web site at www.micron.com.

General Description

The 1Gb Micron® TwinDie RLDRAM® 3 is a high-speed memory device designed for high-bandwidth data storage—telecommunications, networking, cache applications, and so forth. Both the x18 and x36 configurations are composed of two 16-bank 576Mb RLDRAM 3 x18 devices. The TwinDie x18 RLDRAM 3 is a 2-rank device that shares address, control, and data signals between both die in the package. Separate CS# pins enable each of the ranks within the package. The TwinDie x36 RLDRAM 3 is a single-rank device that shares command, address, and control signals, but not the data bus.

The DDR I/O interface transfers two data bits per clock cycle at the I/O balls. Output data is referenced to the READ strobes.

Commands, addresses, and control signals are also registered at every positive edge of the differential input clock, while input data is registered at both positive and negative edges of the input data strobes.

Read and write accesses to the RL3 device are burst-oriented. The burst length (BL) is programmable to 2, 4, or 8 by a setting in the mode register.

The device is supplied with 1.35V for the core and 1.2V for the output drivers. The 2.5V supply is used for an internal supply.

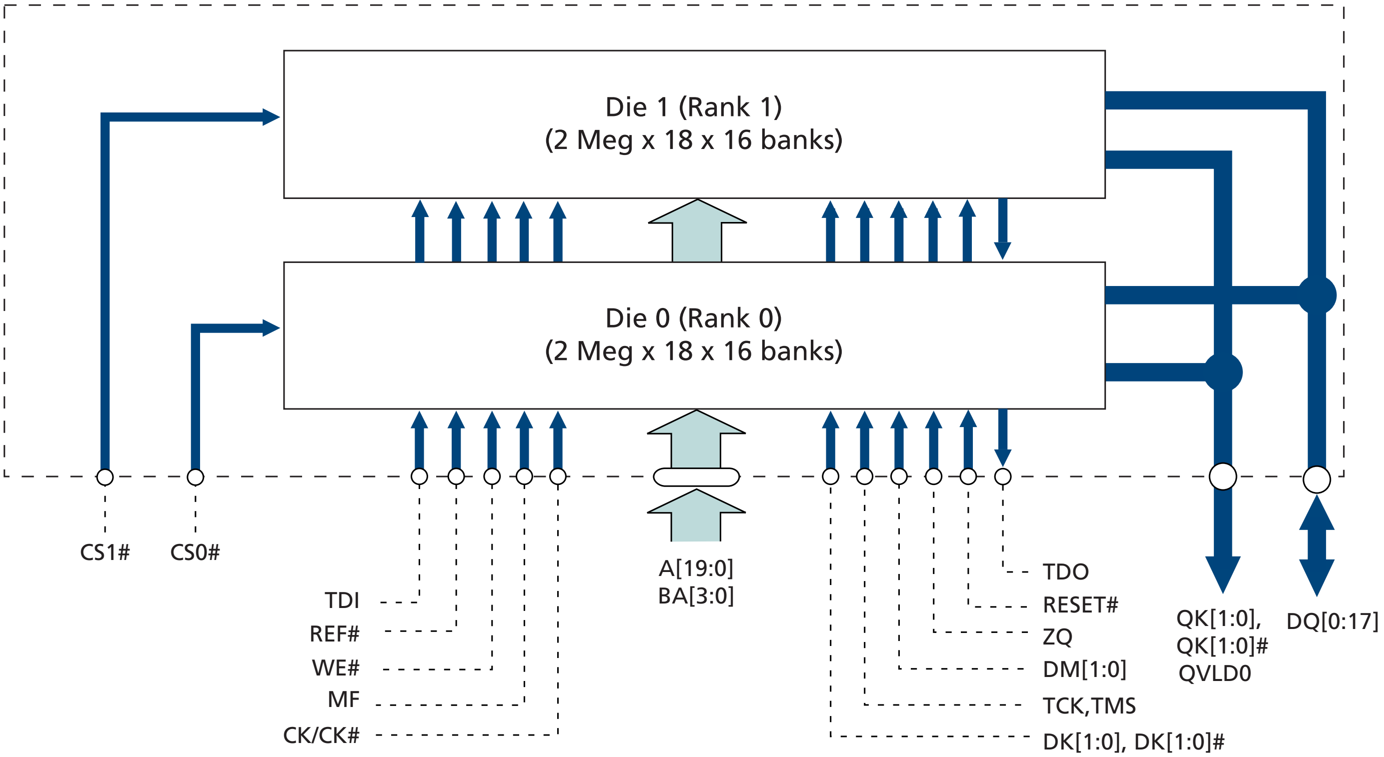
Bank-scheduled refresh is supported, with the row address generated internally.

The 168-ball FBGA package is used to enable ultra-high-speed data transfer rates.

This data sheet provides a general description, package dimensions, and ballout as well as specifications that differ from the monolithic RLDRAM3 device. Refer to the Micron 576Mb RLDRAM 3 data sheet for complete information on power-up and initialization, command descriptions, and die operation.

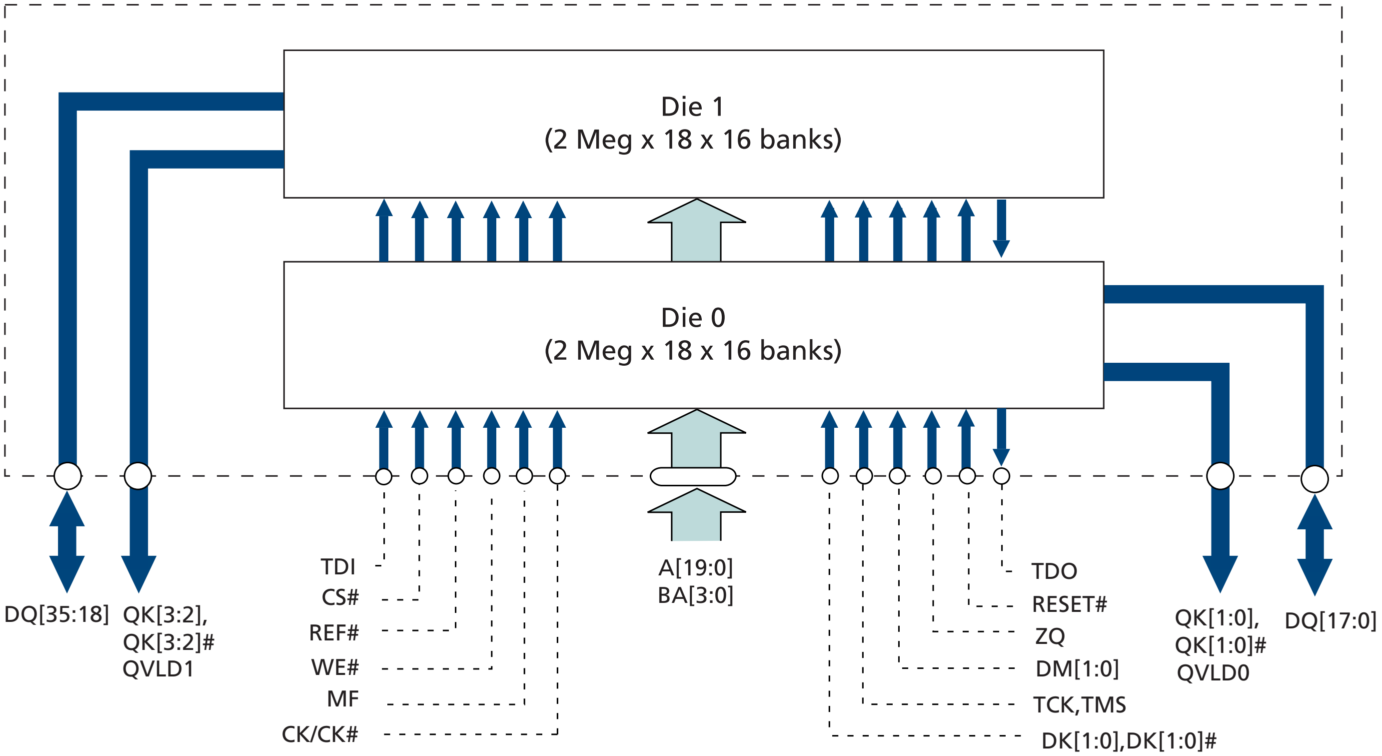
Functional Block Diagrams

Figure 2: 64 Meg x 18 Functional Block Diagram



Note: 1. Example for BL = 2; address bus width will be reduced with an increase in burst length.

Figure 3: 32 Meg x 36 Functional Block Diagram



Note: 1. Example for BL = 2; address bus width will be reduced with an increase in burst length.

Ball Assignments and Descriptions

Table 1: 64 Meg x 18 Ball Assignments – 168-Ball FBGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A		V_{SS}	V_{DD}	NC	V_{DDQ}	NC[1]	V_{REF}	DQ7	V_{DDQ}	DQ8	V_{DD}	V_{SS}	RESET#
B	V_{EXT}	V_{SS}	NC	V_{SSQ}	NC	V_{DDQ}	DM0	V_{DDQ}	DQ5	V_{SSQ}	DQ6	V_{SS}	V_{EXT}
C	V_{DD}	NC	V_{DDQ}	NC	V_{SSQ}	NC	DK0#	DQ2	V_{SSQ}	DQ3	V_{DDQ}	DQ4	V_{DD}
D	A11	V_{SSQ}	NC	V_{DDQ}	NC	V_{SSQ}	DK0	V_{SSQ}	QK0	V_{DDQ}	DQ0	V_{SSQ}	A13
E	V_{SS}	A0	V_{SSQ}	NC	V_{DDQ}	NC	MF[2]	QK0#	V_{DDQ}	DQ1	V_{SSQ}	CS0#	V_{SS}
F	A7	CS1#	V_{DD}	A2	A1	WE#	ZQ	REF#	A3	A4	V_{DD}	A5	A9
G	V_{SS}	A15	A6	V_{SS}	BA1	V_{SS}	CK#	V_{SS}	BA0	V_{SS}	A8	A18	V_{SS}
H	A19	V_{DD}	A14	A16	V_{DD}	BA3	CK	BA2	V_{DD}	A17	A12	V_{DD}	A10
J	V_{DDQ}	NC	V_{SSQ}	NC	V_{DDQ}	NC	V_{SS}	QK1#	V_{DDQ}	DQ9	V_{SSQ}	QVLD	V_{DDQ}
K	NC	V_{SSQ}	NC	V_{DDQ}	NC	V_{SSQ}	DK1	V_{SSQ}	QK1	V_{DDQ}	DQ10	V_{SSQ}	DQ11
L	V_{DD}	NC	V_{DDQ}	NC	V_{SSQ}	NC	DK1#	DQ12	V_{SSQ}	DQ13	V_{DDQ}	DQ14	V_{DD}
M	V_{EXT}	V_{SS}	NC	V_{SSQ}	NC	V_{DDQ}	DM1	V_{DDQ}	DQ15	V_{SSQ}	DQ16	V_{SS}	V_{EXT}
N	V_{SS}	TCK	V_{DD}	TDO	V_{DDQ}	NC	V_{REF}	DQ17	V_{DDQ}	TDI	V_{DD}	TMS	V_{SS}

Notes: 1. NC balls for the x18 configuration are not connected to the DRAM die but do have parasitic capacitance associated with the package substrate. Balls may be connected to V_{SSQ}.
2. MF is assumed to be tied LOW for this ball assignment.

Table 2: 32 Meg x 36 Ball Assignments – 168-Ball FBGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A		V_{SS}	V_{DD}	DQ26	V_{DDQ}	DQ25	V_{REF}	DQ7	V_{DDQ}	DQ8	V_{DD}	V_{SS}	RESET#
B	V_{EXT}	V_{SS}	DQ24	V_{SSQ}	DQ23	V_{DDQ}	DM0	V_{DDQ}	DQ5	V_{SSQ}	DQ6	V_{SS}	V_{EXT}
C	V_{DD}	DQ22	V_{DDQ}	DQ21	V_{SSQ}	DQ20	DK0#	DQ2	V_{SSQ}	DQ3	V_{DDQ}	DQ4	V_{DD}
D	A11	V_{SSQ}	DQ18	V_{DDQ}	QK2	V_{SSQ}	DK0	V_{SSQ}	QK0	V_{DDQ}	DQ0	V_{SSQ}	A13
E	V_{SS}	A0	V_{SSQ}	DQ19	V_{DDQ}	QK2#	MF[2]	QK0#	V_{DDQ}	DQ1	V_{SSQ}	CS#	V_{SS}
F	A7	NF$_{(CS1)}$[1]	V_{DD}	A2	A1	WE#	ZQ	REF#	A3	A4	V_{DD}	A5	A9
G	V_{SS}	A15	A6	V_{SS}	BA1	V_{SS}	CK#	V_{SS}	BA0	V_{SS}	A8	A18	V_{SS}
H	A19	V_{DD}	A14	A16	V_{DD}	BA3	CK	BA2	V_{DD}	A17	A12	V_{DD}	A10
J	V_{DDQ}	QVLD1	V_{SSQ}	DQ27	V_{DDQ}	QK3#	V_{SS}	QK1#	V_{DDQ}	DQ9	V_{SSQ}	QVLD0	V_{DDQ}
K	DQ29	V_{SSQ}	DQ28	V_{DDQ}	QK3	V_{SSQ}	DK1	V_{SSQ}	QK1	V_{DDQ}	DQ10	V_{SSQ}	DQ11
L	V_{DD}	DQ32	V_{DDQ}	DQ31	V_{SSQ}	DQ30	DK1#	DQ12	V_{SSQ}	DQ13	V_{DDQ}	DQ14	V_{DD}
M	V_{EXT}	V_{SS}	DQ34	V_{SSQ}	DQ33	V_{DDQ}	DM1	V_{DDQ}	DQ15	V_{SSQ}	DQ16	V_{SS}	V_{EXT}
N	V_{SS}	TCK	V_{DD}	TDO	V_{DDQ}	DQ35	V_{REF}	DQ17	V_{DDQ}	TDI	V_{DD}	TMS	V_{SS}

Notes: 1. The location of the additional chip select (CS1) is required on the 1Gb RLDRAM 3 x18 DDP configuration. It is internally connected so it can mirror with the address signal, A5, when MF is asserted HIGH. It also has the parasitic characteristics of an address pin.
2. MF is assumed to be tied LOW for this ball assignment.

Table 3: Ball Descriptions

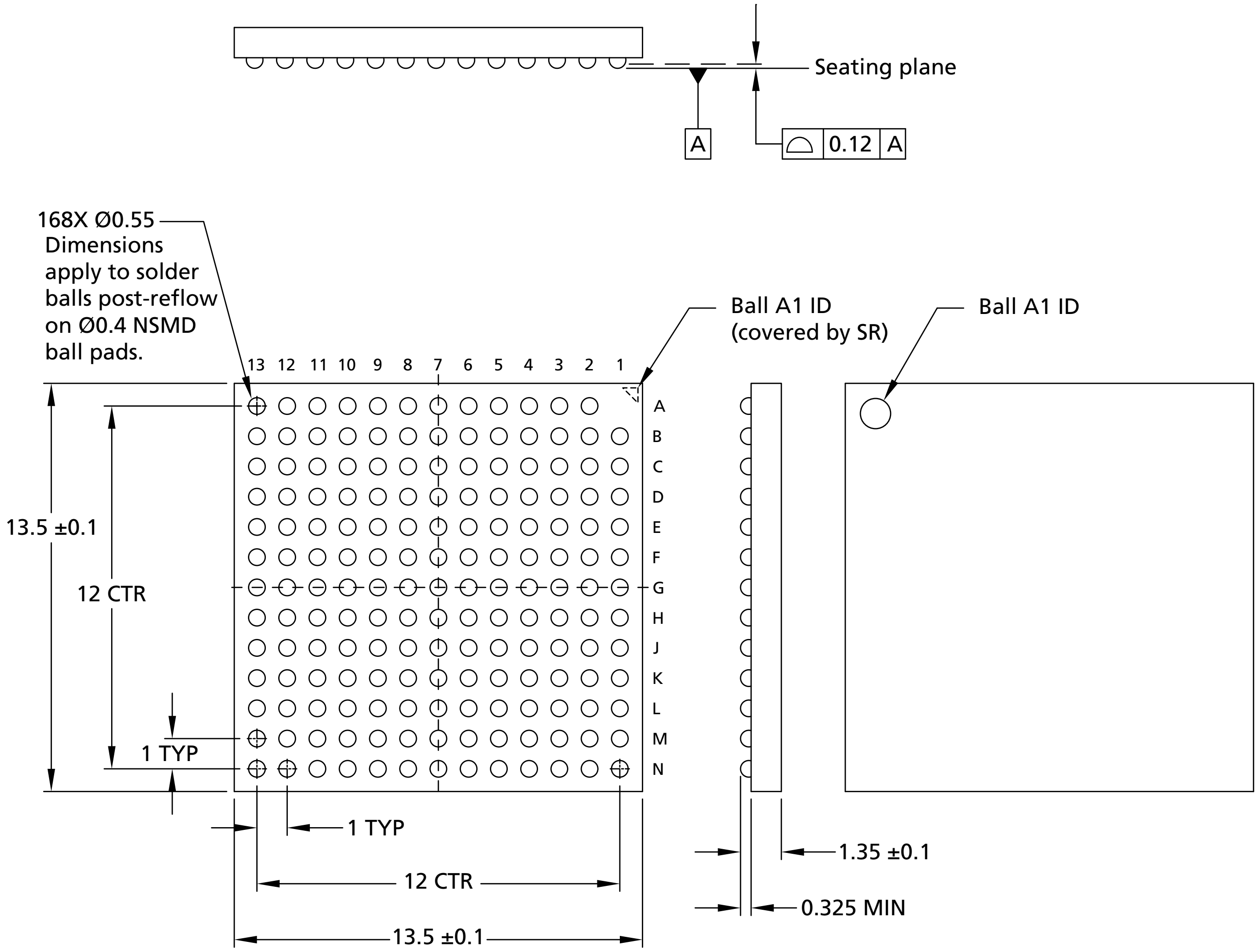
Symbol	Type	Description
A[19:0]	Input	**Address inputs:** A[19:0] define the row and column addresses for READ and WRITE operations. During a MODE REGISTER SET, the address inputs define the register settings, along with BA[3:0]. They are sampled at the rising edge of CK.
BA[3:0]	Input	**Bank address inputs:** Select the internal bank to which a command is being applied.
CK/CK#	Input	**Input clock:** CK and CK# are differential input clocks. Addresses and commands are latched on the rising edge of CK.
CS[0:1]#	Input	**Chip select:** CS[0:1]# enables the command decoder when LOW and disables it when HIGH. The TwinDie x18 device uses CS0# and CS1# to enable and disable the command decoder of each rank. The TwinDie x36 device has only a single CS# pin whereby the command decoder of both die are enabled and disabled simultaneously. When the command decoder is disabled, new commands are ignored, but internal operations continue.
DQ[35:0]	I/O	**Data input:** The DQ signals form the 36-bit data bus. During READ commands, the data is referenced to both edges of QK. During WRITE commands, the data is sampled at both edges of DK.
DK*x*, DK*x*#	Input	**Input data clock:** DK*x* and DK*x*# are differential input data clocks. All input data is referenced to both edges of DK*x*. For the x36 device, DQ[8:0] and DQ[26:18] are referenced to DK0 and DK0#, and DQ[17:9] and DQ[35:27] are referenced to DK1 and DK1#. For the x18 device, DQ[8:0] are referenced to DK0 and DK0#, and DQ[17:9] are referenced to DK1 and DK1#. DK*x* and DK*x*# are free-running signals and must always be supplied to the device.
DM[1:0]	Input	**Input data mask:** DM is the input mask signal for WRITE data. Input data is masked when DM is sampled HIGH. DM0 is used to mask the lower byte for the x18 device and DQ[8:0] and DQ[26:18] for the x36 device. DM1 is used to mask the upper byte for the x18 device and DQ[17:9] and DQ[35:27] for the x36 device. Tie DM[1:0] to V_{SS} if not used.
TCK	Input	**IEEE 1149.1 clock input:** This ball must be tied to V_{SS} if the JTAG function is not used.
TMS, TDI	Input	**IEEE 1149.1 test inputs:** These balls may be left as no connects if the JTAG function is not used.
WE#, REF#	Input	**Command inputs:** Sampled at the positive edge of CK, WE# and REF# (together with CS#) define the command to be executed.
RESET#	Input	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. RESET# assertion and deassertion are asynchronous. RESET# is a CMOS input defined with DC HIGH ≥ 0.8 x V_{DD} and DC LOW ≤ 0.2 x V_{DDQ}.
ZQ	Input	**External impedance:** This signal is used to tune the device's output impedance and ODT. RZQ needs to be 240Ω, where RZQ is a resistor from this signal to ground.
QK*x*, QK*x*#	Output	**Output data clocks:** QK and QK# are opposite-polarity output data clocks. They are free-running signals and during READ commands are edge-aligned with the DQs. For the x36 device, QK0, QK0# align with DQ[8:0]; QK1, QK1# align with DQ[17:9]; QK2, QK2# align with DQ[26:18]; and QK3, QK3# align with DQ[35:27]. For the x18 device, QK0, QK0# align with DQ[8:0]; QK1, QK1# align with DQ[17:9].
QVLD*x*	Output	**Data valid:** The QVLD ball indicates that valid output data will be available on the subsequent rising clock edge. There is a single QVLD ball for the x18 device and two, QVLD0 and QVLD1, for the x36 device. QVLD0 aligns with DQ[17:0]; QVLD1 aligns with DQ[35:18].
MF	Input	**Mirror function:** The mirror function ball is a DC input used to create mirrored ballouts for simple dual-loaded clamshell mounting. If the ball is tied to V_{SS}, the address and command balls are in their true layout. If the ball is tied to V_{DDQ}, they are in the complement location. MF must be tied HIGH or LOW and cannot be left floating. MF is a CMOS input defined with DC HIGH ≥ 0.8 x V_{DD} and DC LOW ≤ 0.2 x V_{DDQ}.

Table 3: Ball Descriptions (Continued)

Symbol	Type	Description
TDO	Output	**IEEE 1149.1 test output:** JTAG output. This ball may be left as no connect if the JTAG function is not used.
V_{DD}	Supply	**Power supply:** 1.35V nominal.
V_{DDQ}	Supply	**DQ power supply:** 1.2V nominal. Isolated on the device for improved noise immunity.
V_{EXT}	Supply	**Power supply:** 2.5V nominal.
V_{REF}	Supply	**Input reference voltage:** $V_{DDQ}/2$ nominal. Provides a reference voltage for the input buffers.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
NC	-	**No connect:** These balls are not connected to the DRAM.

Package Dimensions

Figure 4: 168-Ball FBGA



Note: 1. All dimensions are in millimeters.

Electrical Characteristics - I_{DD} Specifications

Table 4: I_{DD} Operating Conditions and Maximum Limits

Combined Symbol	Individual Die Status	-125E	-125	Units
I_{CSB1} (V_{DD}) x18	$I_{CSB1} = I_{SB1} + I_{SB1}$	250	250	mA
I_{CSB1} (V_{EXT}) x18		60	60	
I_{CSB1} (V_{DD}) x36	$I_{CSB1} = I_{SB1} + I_{SB1}$	250	250	
I_{CSB1} (V_{EXT}) x36		60	60	
I_{CSB2} (V_{DD}) x18	$I_{CSB2} = I_{SB2} + I_{SB2}$	1450	1450	mA
I_{CSB2} (V_{EXT}) x18		60	60	
I_{CSB2} (V_{DD}) x36	$I_{CSB2} = I_{SB2} + I_{SB2}$	1480	1480	
I_{CSB2} (V_{EXT}) x36		60	60	
I_{CDD1} (V_{DD}) x18	$I_{CDD1} = I_{DD1} + I_{SB2}$	1665	1640	mA
I_{CDD1} (V_{EXT}) x18		65	65	
I_{CDD1} (V_{DD}) x36	$I_{CDD1} = I_{DD1} + I_{DD1}$	1880	1830	
I_{CDD1} (V_{EXT}) x36		70	70	
I_{CDD2} (V_{DD}) x18	$I_{CDD2} = I_{DD2} + I_{SB2}$	1695	1670	mA
I_{CDD2} (V_{EXT}) x18		65	65	
I_{CDD2} (V_{DD}) x36	$I_{CDD2} = I_{DD2} + I_{DD2}$	1940	1890	
I_{CDD2} (V_{EXT}) x36		70	70	
I_{CDD3} (V_{DD}) x18	$I_{CDD3} = I_{DD3} + I_{SB2}$	1755	1725	mA
I_{CDD3} (V_{EXT}) x18		65	65	
I_{CDD3} (V_{DD}) x36	$I_{CDD3} = I_{DD3} + I_{DD3}$	NA	NA	
I_{CDD3} (V_{EXT}) x36		NA	NA	
I_{CREF1} (V_{DD}) x18	$I_{CREF1} = I_{REF1} + I_{SB2}$	1955	1955	mA
I_{CREF1} (V_{EXT}) x18		100	100	
I_{CREF1} (V_{DD}) x36	$I_{CREF1} = I_{REF1} + I_{REF1}$	2460	2460	
I_{CREF1} (V_{EXT}) x36		140	140	
I_{CREF2} (V_{DD}) x18	$I_{CREF2} = I_{REF2} + I_{SB2}$	1435	1435	mA
I_{CREF2} (V_{EXT}) x18		60	60	
I_{CREF2} (V_{DD}) x36	$I_{CREF2} = I_{REF2} + I_{REF2}$	1485	1485	
I_{CREF2} (V_{EXT}) x36		60	60	
$I_{CMBREF4}$ (V_{DD}) x18	$I_{CMBREF4} = I_{MBREF4} + I_{SB2}$	2610	2370	mA
$I_{CMBREF4}$ (V_{EXT}) x18		135	135	
$I_{CMBREF4}$ (V_{DD}) x36	$I_{CMBREF4} = I_{MBREF4} + I_{MBREF4}$	3770	3290	
$I_{CMBREF4}$ (V_{EXT}) x36		210	210	
I_{CDD2W} (V_{DD}) x18	$I_{CDD2W} = I_{DD2W} + I_{SB2}$	2390	2390	mA
I_{CDD2W} (V_{EXT}) x18		100	100	
I_{CDD2W} (V_{DD}) x36	$I_{CDD2W} = I_{DD2W} + I_{DD2W}$	3330	3330	
I_{CDD2W} (V_{EXT}) x36		140	140	

Table 4: I_{DD} Operating Conditions and Maximum Limits (Continued)

Combined Symbol	Individual Die Status	-125E	-125	Units
I_{CDD4W} (V_{DD}) x18	$I_{CDD4W} = I_{DD4W} + I_{SB2}$	2120	2120	mA
I_{CDD4W} (V_{EXT}) x18		80	80	
I_{CDD4W} (V_{DD}) x36	$I_{CDD4W} = I_{DD4W} + I_{DD4W}$	2790	2790	
I_{CDD4W} (V_{EXT}) x36		100	100	
I_{CDD8W} (V_{DD}) x18	$I_{CDD8W} = I_{DD8W} + I_{SB2}$	1915	1915	mA
I_{CDD8W} (V_{EXT}) x18		70	70	
I_{CDD8W} (V_{DD}) x36	$I_{CDD8W} = I_{DD8W} + I_{DD8W}$	NA	NA	
I_{CDD8W} (V_{EXT}) x36		NA	NA	
I_{CDBWR} (V_{DD}) x18	$I_{CDBWR} = I_{DBWR} + I_{SB2}$	2610	2610	mA
I_{CDBWR} (V_{EXT}) x18		100	100	
I_{CDBWR} (V_{DD}) x36	$I_{CDBWR} = I_{DBWR} + I_{DBWR}$	3770	3770	
I_{CDBWR} (V_{EXT}) x36		140	140	
I_{CQBWR} (V_{DD}) x18	$I_{CQBWR} = I_{QBWR} + I_{SB2}$	3250	3250	mA
I_{CQBWR} (V_{EXT}) x18		130	130	
I_{CQBWR} (V_{DD}) x36	$I_{CQBWR} = I_{QBWR} + I_{QBWR}$	5050	5050	
I_{CQBWR} (V_{EXT}) x36		200	200	
I_{CDD2R} (V_{DD}) x18	$I_{CDD2R} = I_{DDR2} + I_{SB2}$	2510	2510	mA
I_{CDD2R} (V_{EXT}) x18		100	100	
I_{CDD2R} (V_{DD}) x36	$I_{CDD2R} = I_{DD2R} + I_{DD2R}$	3570	3570	
I_{CDD2R} (V_{EXT}) x36		140	140	
I_{CDD4R} (V_{DD}) x18	$I_{CDD4R} = I_{DDR4} + I_{SB2}$	2125	2125	mA
I_{CDD4R} (V_{EXT}) x18		80	80	
I_{CDD4R} (V_{DD}) x36	$I_{CDD4R} = I_{DD4R} + I_{DD4R}$	2800	2800	
I_{CDD4R} (V_{EXT}) x36		100	100	
I_{CDD8R} (V_{DD}) x18	$I_{CDD8R} = I_{DDR8} + I_{SB2}$	1900	1900	mA
I_{CDD8R} (V_{EXT}) x18		70	70	
I_{CDD8R} (V_{DD}) x36	$I_{CDD8R} = I_{DD8R} + I_{DD8R}$	NA	NA	
I_{CDD8R} (V_{EXT}) x36		NA	NA	

Note: 1. I_{CDD} values reflect the combined current of both individual die. I_{DDx} and I_{SBx} represent individual die values.

Electrical Specifications – Absolute Ratings and I/O Capacitance

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 5: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	V_{DD} supply voltage relative to V_{SS}	–0.4	1.975	V
V_{DDQ}	Voltage on V_{DDQ} supply relative to V_{SS}	–0.4	1.66	V
V_{IN},V_{OUT}	Voltage on any ball relative to V_{SS}	–0.4	1.66	V
V_{EXT}	Voltage on V_{EXT} supply relative to V_{SS}	–0.4	2.8	V

Input/Output Capacitance

Table 6: Input/Output Capacitance

Notes 1 and 2 apply to entire table

Capacitance Parameters	Symbol	x18 DDP - 1600		x36 DDP - 1600		Units	Notes
		Min	Max	Min	Max		
CK/CK#	C_{CK}	4.25	5.5	4.25	5.5	pF	
ΔC: CK to CK#	C_{DCK}	0	0.15	0	0.15	pF	
Single-ended I/O: DQ	C_{IO}	5.25	7.0	3.0	4.5	pF	
Single-ended I/O: DM	C_{IO}	5.25	7.0	5.25	7.0	pF	
Input strobe: DK/DK#	C_{IO}	5.25	7.0	5.25	7.0	pF	
Output strobe: QK/QK#, QVLD	C_{IO}	5.25	7.0	3.0	4.5	pF	
ΔC: DK to DK#	C_{DDK}	0	0.15	0	0.15	pF	
ΔC: QK to QK#	C_{DQK}	0	0.15	0	0.15	pF	
ΔC: DQ to QK	C_{DIO}	–0.5	0.3	–0.5	0.3	pF	3
ΔC: DQ to DK	C_{DIO}	–0.5	0.3	–3.6	–3.05	pF	3
Inputs (CMD, ADDR)	C_I	4.25	6.0	4.25	6.0	pF	4
ΔC: CMD_ADDR to CK	$C_{DI\_CMD\_ADDR}$	–0.5	0.8	–0.5	0.8	pF	5
JTAG balls	C_{JTAG}	2.9	4.9	2.9	4.9	pF	6
RESET#, MF balls	C_I	–	5.5	–	5.5	pF	

Notes:
1. $+1.28V \le V_{DD} \le +1.42V$, $+1.14V \le V_{DDQ} \le 1.26V$, $+2.38V \le V_{EXT} \le +2.63V$, $V_{REF} = V_{SS}$, $f = 100$ MHz, $T_C = 25°C$, $V_{OUT(DC)} = 0.5 \times V_{DDQ}$, V_{OUT} (peak-to-peak) = 0.1V.
2. Capacitance is not tested on the ZQ ball.
3. $C_{DIO} = C_{IO(DQ)} - 0.5 \times (C_{IO}$ [QK/DK] + C_{IO} [QK#/DK#]).
4. Includes CS#, REF#, WE#, A[19:0], and BA[3:0].
5. $C_{DI\_CMD\_ADDR} = C_I$ (CMD_ADDR) - 0.5 × (C_{CK} [CK] + C_{CK} [CK#]).
6. JTAG balls are tested at 50 MHz.

ODT Characteristics

ODT Resistors

The following tables provide an overview of the ODT DC electrical characteristics. Note that 10Ω is added to account for the RDL needed to stack the die. The 10Ω is constant across V_{OUT}. The 10Ω RDL addition is an advance estimate and will need characterization data for more accurate values. The values provided are not specification requirements; however, they can be used as design guidelines to indicate what R_{TT} is targeted to provide:

- R_{TT} of 130Ω is made up of $R_{TT120(PD240)}$ and $R_{TT120(PU240)}$ plus 10Ω from RDL needed to stack die.
- R_{TT} of 125Ω is made up of $R_{TT120(PD240)}$ plus 10Ω from RDL needed to stack die and $R_{TT120(PU240)}$ plus 10Ω from RDL needed to stack die.
- R_{TT} of 70Ω is made up of $R_{TT60(PD120)}$ and $R_{TT60(PU120)}$ plus 10Ω from RDL needed to stack die.
- R_{TT} of 65Ω is made up of $R_{TT60(PD120)}$ plus 10Ω from RDL needed to stack die and $R_{TT60(PU120)}$ plus 10Ω from RDL needed to stack die.
- R_{TT} of 50Ω is made up of $R_{TT40(PD80)}$ and $R_{TT40(PU80)}$ and 10Ω from RDL needed to stack die.

Table 7: R_{TT} Effective Impedances

Selected Termination	Configuration	Effective DQ Termination	Effective DM Termination	Effective DK Termination	Units
40	x18	Reserved	Reserved	Reserved	Ω
	x36	50	65	65	Ω
60	x18	70	70	65	Ω
	x36	70	65	65	Ω
120	x18	130	130	125	Ω
	x36	130	125	125	Ω

Table 8: R_{TT} Effective Impedance Ranges

R_{TT}	Resistor	V_{OUT}	Min	Nom	Max	Units
130Ω	$R_{TT120(PD240)}$	0.2 x V_{DDQ}	164	260	284	Ω
		0.5 x V_{DDQ}	236	260	284	Ω
		0.8 x V_{DDQ}	236	260	356	Ω
	$R_{TT120(PU240)}$	0.2 x V_{DDQ}	236	260	356	Ω
		0.5 x V_{DDQ}	236	260	284	Ω
		0.8 x V_{DDQ}	164	260	284	Ω
130Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	118	130	202	Ω

Table 8: R_{TT} Effective Impedance Ranges (Continued)

R_{TT}	Resistor	V_{OUT}	Min	Nom	Max	Units
125Ω	$R_{TT120(PD240)}$	0.2 x V_{DDQ}	154	250	274	Ω
		0.5 x V_{DDQ}	226	250	274	Ω
		0.8 x V_{DDQ}	226	250	346	Ω
	$R_{TT120(PU240)}$	0.2 x V_{DDQ}	226	250	346	Ω
		0.5 x V_{DDQ}	226	250	274	Ω
		0.8 x V_{DDQ}	154	250	274	Ω
125Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	113	125	197	Ω
70Ω	$R_{TT60(PD120)}$	0.2 x V_{DDQ}	92	140	152	Ω
		0.5 x V_{DDQ}	128	140	152	Ω
		0.8 x V_{DDQ}	128	140	188	Ω
	$R_{TT60(PU120)}$	0.2 x V_{DDQ}	128	140	188	Ω
		0.5 x V_{DDQ}	128	140	152	Ω
		0.8 x V_{DDQ}	92	140	152	Ω
70Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	64	70	106	Ω
65Ω	$R_{TT60(PD120)}$	0.2 x V_{DDQ}	82	130	142	Ω
		0.5 x V_{DDQ}	118	130	142	Ω
		0.8 x V_{DDQ}	118	130	178	Ω
	$R_{TT60(PU120)}$	0.2 x V_{DDQ}	118	130	178	Ω
		0.5 x V_{DDQ}	118	130	142	Ω
		0.8 x V_{DDQ}	82	130	142	Ω
65Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	59	65	101	Ω
50Ω	$R_{TT40(PD80)}$	0.2 x V_{DDQ}	68	100	108	Ω
		0.5 x V_{DDQ}	92	100	108	Ω
		0.8 x V_{DDQ}	92	100	132	Ω
	$R_{TT40(PU80)}$	0.2 x V_{DDQ}	92	100	132	Ω
		0.5 x V_{DDQ}	92	100	108	Ω
		0.8 x V_{DDQ}	68	100	108	Ω
50Ω		$V_{IL(AC)}$ to $V_{IH(AC)}$	46	50	74	Ω

ODT Sensitivity

If either temperature or voltage changes after I/O calibration, then the tolerance limits listed in Table 8 (page 12) can be expected to widen according to Table 9 (page 14) and Table 10 (page 14).

Table 9: ODT Sensitivity Definition

Symbol	Min	Max	Units
R_{TT}	0.9 - $dR_{TT}dT$ × |DT| - $dR_{TT}dV$ × |DV|	1.6 + $dR_{TT}dT$ × |DT| + $dR_{TT}dV$ × |DV|	RZQ/(2,4,6)

Note: 1. DT = T - T(@ calibration), DV = V_{DDQ} - V_{DDQ}(@ calibration) or V_{DD} - V_{DD}(@ calibration).

Table 10: ODT Temperature and Voltage Sensitivity

Change	Min	Max	Units
$dR_{TT}dT$	0	1.5	%/°C
$dR_{TT}dV$	0	0.15	%/mV

Output Driver Impedance

The output driver impedance is selected by MR1[1:0] during initialization. The selected value is able to maintain the tight tolerances specified if proper ZQ calibration is performed.

Output specifications refer to the default output driver unless specifically stated otherwise. A functional representation of the output buffer is shown below. The output driver impedance R_{ON} is defined by the value of the external reference resistor RZQ plus 10Ω RDL resistance from stacking the die. The 10Ω RDL addition is an advance estimate and will need characterization data for more accurate values.

- $R_{ON,x} = RZQ/y + 10\Omega$ (with $RZQ = 240\Omega \pm 1\%$; $x = 34.3\Omega$ or 48Ω with $y = 7$ or 5, respectively)

The individual pull-up and pull-down resistors ($R_{ON(PU)}$ and $R_{ON(PD)}$) are defined as follows:

- $R_{ON(PU)} = (V_{DDQ} - V_{OUT})/|I_{OUT}|$, when $R_{ON(PD)}$ is turned off
- $R_{ON(PD)} = (V_{OUT})/|I_{OUT}|$, when $R_{ON(PU)}$ is turned off

Figure 5: Output Driver

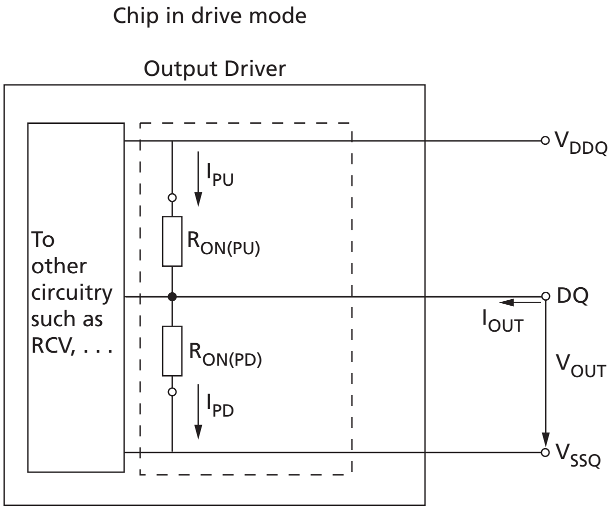


Table 11: Driver Pull-Up and Pull-Down Impedance Calculations

R_{ON}		Min	Nom	Max	Units
RZQ/7 = (240Ω ±1%)/7 + 10Ω		43.9	44.3	44.6	Ω
RZQ/5 = (240Ω ±1%)/5 + 10Ω		57.5	58	58.5	Ω
Driver	**V_{OUT}**	**Min**	**Nom**	**Max**	**Units**
44.3Ω pull-down	0.2 × V_{DDQ}	30.6	44.3	47.7	Ω
	0.5 × V_{DDQ}	40.9	44.3	47.7	Ω
	0.8 × V_{DDQ}	40.9	44.3	58.0	Ω
44.3Ω pull-up	0.2 × V_{DDQ}	40.9	44.3	58.0	Ω
	0.5 × V_{DDQ}	40.9	44.3	47.7	Ω
	0.8 × V_{DDQ}	30.6	44.3	47.7	Ω
58Ω pull-down	0.2 × V_{DDQ}	38.8	58	62.8	Ω
	0.5 × V_{DDQ}	53.2	58	62.8	Ω
	0.8 × V_{DDQ}	53.2	58	77.2	Ω
58Ω pull-up	0.2 × V_{DDQ}	53.2	58	77.2	Ω
	0.5 × V_{DDQ}	53.2	58	62.8	Ω
	0.8 × V_{DDQ}	38.8	58	62.8	Ω

Output Driver Sensitivity

If either the temperature or the voltage changes after ZQ calibration, then the tolerance limits listed in Table 11 (page 16) can be expected to widen according to Table 12 (page 17) and Table 13 (page 17).

Table 12: Output Driver Sensitivity Definition

Symbol	Min	Max	Units
$R_{ON(PD)}$ @ 0.2 x V_{DDQ}	0.6 - $dR_{ON}dTH$ x DT - $dR_{ON}dVH$ x DV	1.1 + $dR_{ON}dTH$ x DT + $dR_{ON}dVH$ x DV	RZQ/(7,5)+10Ω
$R_{ON(PD)}$ @ 0.5 x V_{DDQ}	0.9 - $dR_{ON}dTM$ x DT - $dR_{ON}dVM$ x DV	1.1 + $dR_{ON}dTM$ x DT + $dR_{ON}dVM$ x DV	RZQ/(7,5)+10Ω
$R_{ON(PD)}$ @ 0.8 x V_{DDQ}	0.9 - $dR_{ON}dTL$ x DT - $dR_{ON}dVL$ x DV	1.4 + $dR_{ON}dTL$ x DT + $dR_{ON}dVL$ x D	RZQ/(7,5)+10Ω
$R_{ON(PU)}$ @ 0.2 x V_{DDQ}	0.9 - $dR_{ON}dTH$ x DT - $dR_{ON}dVH$ x DV	1.4 + $dR_{ON}dTH$ x DT + $dR_{ON}dVH$ x DV	RZQ/(7,5)+10Ω
$R_{ON(PU)}$ @ 0.5 x V_{DDQ}	0.9 - $dR_{ON}dTM$ x DT - $dR_{ON}dVM$ x DV	1.1 + $dR_{ON}dTM$ x DT + $dR_{ON}dVM$ x DV	RZQ/(7,5)+10Ω
$R_{ON(PU)}$ @ 0.8 x V_{DDQ}	0.6 - $dR_{ON}dTL$ x DT - $dR_{ON}dVL$ x DV	1.1 + $dR_{ON}dTL$ x DT + $dR_{ON}dVL$ x DV	RZQ/(7,5)+10Ω

Note: 1. DT = T - T(@ calibration), DV = V_{DDQ} - V_{DDQ}(@ calibration) or V_{DD} - V_{DD}(@ calibration).

Table 13: Output Driver Voltage and Temperature Sensitivity

Change	Min	Max	Unit
$dR_{ON}dTM$	0	1.5	%/°C
$dR_{ON}dVM$	0	0.15	%/mV
$dR_{ON}dTL$	0	1.5	%/°C
$dR_{ON}dVL$	0	0.15	%/mV
$dR_{ON}dTH$	0	1.5	%/°C
$dR_{ON}dVH$	0	0.15	%/mV

Output Characteristics and Operating Conditions

Table 14: Single-Ended Output Driver Characteristics

Note 1–4 apply to entire table

Parameter/Condition	Symbol		Min	Max	Units
Output slew rate: Single-ended; For rising and falling edges, measures between $V_{OL(AC)} = V_{REF} - 0.1 \times V_{DDQ}$ and $V_{OH(AC)} = V_{REF} + 0.1 \times V_{DDQ}$	SRQ_{SE}	x18	TBD	TBD	V/ns
		x36	2.5	6	V/ns

Notes:
1. All voltages are referenced to V_{SS}.
2. RZQ is 240Ω (±1%) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage.
3. The 6 V/ns maximum is applicable for a single DQ signal when it is switching either from HIGH to LOW or LOW to HIGH, while the remaining DQ signals in the same byte lane are all either static or switching to the opposite direction. For all other DQ signal-switching combinations, the maximum limit of 6 V/ns is reduced to 5 V/ns.
4. These slew rate specifications are defined for a 1.875ns ^tCK.

Table 15: Differential Output Driver Characteristics

Notes 1–3 apply to entire table

Parameter/Condition	Symbol		Min	Max	Units
Output slew rate: Differential; For rising and falling edges, measures between $V_{OL,diff(AC)} = -0.2 \times V_{DDQ}$ and $V_{OH,diff(AC)} = +0.2 \times V_{DDQ}$	SRQ_{diff}	x18	TBD	TBD	V/ns
		x36	5	12	V/ns

Notes:
1. All voltages are referenced to V_{SS}.
2. RZQ is 240Ω (±1%) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage.
3. These slew rate specifications are defined for a 1.875ns ^tCK.

Timing Adjustments

Table 16: DDP Timing adjustments

Parameter		Symbol		RL3-1600		Units	Notes
				Min	Max		
DQ Input Timing							
Data setup time to DK, DK#	Base (specification)	^{t}DS(AC150)		60	–	ps	1, 2
	V_{REF} @ 1 V/ns			210	–	ps	2, 3
Data hold time from DK, DK#	Base (specification)	^{t}DH(DC100)		95	–	ps	1, 2
	V_{REF} @ 1 V/ns			195	–	ps	
DQ Output Timing							
QK, QK# edge to output data edge within byte group		^{t}QKQ$_x$	x18	–	TBD	ps	
			x36	–	100		
QK, QK# edge to any output data edge within specific data-word grouping (for x36 only)		^{t}QKQ02, ^{t}QKQ13		–	Not Applicable	ps	
DQ output hold time from QK, QK#		^{t}QH	x18	TBD	–	^{t}CK(avg)	4
			x36	0.38	–		
Input and Output Strobe Timing							
QK (rising), QK# (falling) edge to CK (rising), CK# (falling) edge		^{t}CKQK	x18	TBD	TBD	ps	6
			x36	–160 - 5%^{t}CK	160 + 5% ^{t}CK		
QK (falling), QK# (rising) edge to QVLD edge		^{t}QKVLD	x18	–	TBD	ps	5
			x36	–	150		
Calibration Timing							
ZQCL: Long calibration time		^{t}ZQinit	x18	512	–	CK	
			x36	1024	–	CK	
		^{t}ZQoper	x18	256	–	CK	
			x36	512	–	CK	
ZQCS: Short calibration time		^{t}ZQcs	x18	64	–	CK	
			x36	128	–	CK	

Notes:
1. ^{t}DS(base) and ^{t}DH(base) values are for a single-ended 1 V/ns DQ slew rate and 2 V/ns differential DK, DK# slew rate.
2. These parameters are measured from a data signal (DM, DQ0, DQ1, and so forth) transition edge to its respective data strobe signal (DK, DK#) crossing.
3. The setup and hold times are listed converting the base specification values (to which derating tables apply) to V_{REF} when the slew rate is 1 V/ns. These values, with a slew rate of 1 V/ns, are for reference only.
4. When the device is operated with input clock jitter, this parameter needs to be derated by the actual ^{t}JIT(per) (the larger of ^{t}JIT(per), MIN or ^{t}JIT(per), MAX of the input clock; output deratings are relative to the SDRAM input clock).

5. For the x36 device, this specification references the skew between the falling edge of QK0 and QK1 to QVLD0 and the falling edge of QK2 and QK3 to QVLD1.
6. The DRAM output timing is aligned to the nominal or average clock. The following output parameters must be derated by the actual jitter error when input clock jitter is present, even when within specification. This results in each parameter's becoming larger. The following parameters are required to be derated by subtracting ^{t}ERR(10per), MAX: ^{t}CKQK(MIN), and ^{t}LZ(MIN). The following parameters are required to be derated by subtracting ^{t}ERR(10per), MIN: ^{t}CKQK(MAX), ^{t}HZ(MAX), and ^{t}LZ(MAX).

Thermal Impedance Characteristics

Table 17: Thermal Impedance

Package	Substrate	θ JA (°C/W) Airflow = 0 m/s	θ JA (°C/W) Airflow = 1 m/s	θ JA (°C/W) Airflow = 2 m/s	θ JB (°C/W)	θ JC (°C/W)
FBGA	2-layer	41.3	29.8	26.2	NA	2.0
	4-layer	24.0	18.8	17.3	7.6	

Note: 1. Thermal impedance data is based on a number of samples from multiple lots and should be viewed as a typical number.

Commands

The following table provides descriptions of the valid commands of the RLDRAM 3 device. All command and address inputs must meet setup and hold times with respect to the rising edge of CK.

Table 18: Command Descriptions

Command	Description
NOP	The NOP command prevents new commands from being executed by the DRAM. Operations already in progress are not affected by NOP commands. Output values depend on command history.
MRS	Mode registers MR0, MR1, and MR2 are used to define various modes of programmable operations of the DRAM. A mode register is programmed via the MODE REGISTER SET (MRS) command during initialization and retains the stored information until it is reprogrammed, RESET# goes LOW, or until the device loses power. The MRS command can be issued only when all banks are idle, and no bursts are in progress.
READ	The READ command is used to initiate a burst read access to a bank. The BA[3:0] inputs select a bank, and the address provided on inputs A[19:0] select a specific location within a bank.
WRITE	The WRITE command is used to initiate a burst write access to a bank (or banks). MRS bits MR2[4:3] select a single-, dual-, or quad-bank WRITE protocol. The BA[*x*:0] inputs select the bank(s) (x = 3, 2, or 1 for a single-, dual-, or quad-bank WRITE, respectively). The address provided on inputs A[19:0] selects a specific location within the bank. Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If the DM signal is registered LOW, the corresponding data will be written to memory. If the DM signal is registered HIGH, the corresponding data inputs will be ignored (that is, this part of the data word will not be written).
AREF	The AREF command is used during normal operation of the RLDRAM 3 to refresh the memory content of a bank. There are two methods by which the RLDRAM 3 can be refreshed, both of which are selected within the mode register. The first method, bank address-controlled AREF, is identical to the method used in RLDRAM 2. The second method, multibank AREF, enables refreshing of up to four banks simultaneously. More information is available in the Auto Refresh section. For both methods, the command is nonpersistent, so it must be issued each time a refresh is required.

Table 19: x36 Command Table

Note 1 applies to entire table; notes appear after x18 Command Table

Operation	Code	CS#	WE#	REF#	A[19:0]	BA[3:0]	Notes
NOP	NOP	H	H	H	X	X	
MRS	MRS	L	L	L	OPCODE	OPCODE	
READ	READ	L	H	H	A	BA	3
WRITE	WRITE	L	L	H	A	BA	3
AUTO REFRESH	AREF	L	H	L	A	BA	4

Table 20: x18 Command Table

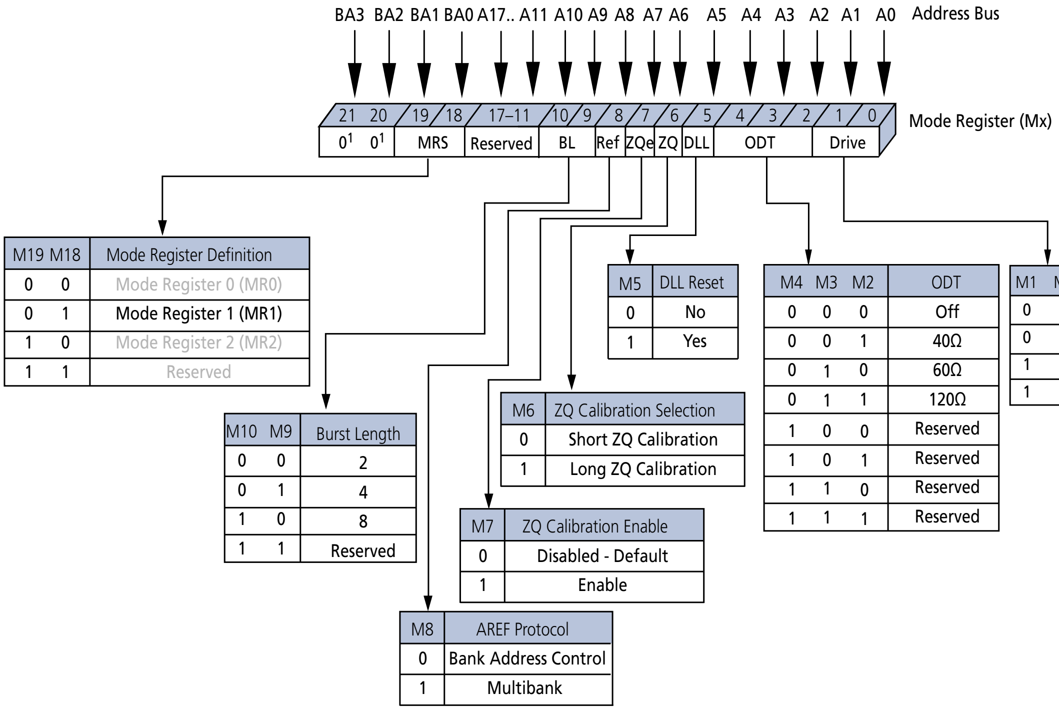
Note 1 and 2 apply to entire table

Operation	Code	CS0#	CS1#	WE#	REF#	A[19:0]	BA[3:0]	Notes
NOP	NOP	H	H	H	L	X	X	
MRS	MRS_{both}	L	L	L	L	OPCODE	OPCODE	
	MRS_0	L	H	L	L	OPCODE	OPCODE	
	MRS_1	H	L	L	L	OPCODE	OPCODE	
READ	READ_0	L	H	H	H	A	BA	3
	READ_1	H	L	H	H	A	BA	
WRITE	WRITE_0	L	H	L	H	A	BA	3
	WRITE_1	H	L	L	H	A	BA	
AUTO REFRESH	$\text{AREF}_{\text{both}}$	L	L	H	L	A	BA	4
	AREF_0	L	H	H	L	A	BA	
	AREF_1	H	L	H	L	A	BA	

Notes:
1. X = “Don’t Care;” H = logic HIGH; L = logic LOW; A = valid address; BA = valid bank address; OPCODE = mode register bits
2. Subcripts on command codes (both, 0, and 1) refer to the die being accessed. 0 = die 0, 1 = die 1, and both = both die simultaneously.
3. Address width varies with burst length and configuration; see the Address Widths of Different Burst Lengths table for more information.
4. Bank address signals (BA) are used only during bank address-controlled AREF; address signals (A) are used only during multibank AREF.

Mode Register 1 (MR1)

Figure 6: MR1 Definition for Non-Multiplexed Address Mode



M19	M18	Mode Register Definition
0	0	Mode Register 0 (MR0)
0	1	Mode Register 1 (MR1)
1	0	Mode Register 2 (MR2)
1	1	Reserved

M10	M9	Burst Length
0	0	2
0	1	4
1	0	8
1	1	Reserved

M8	AREF Protocol
0	Bank Address Control
1	Multibank

M7	ZQ Calibration Enable
0	Disabled - Default
1	Enable

M6	ZQ Calibration Selection
0	Short ZQ Calibration
1	Long ZQ Calibration

M5	DLL Reset
0	No
1	Yes

M4	M3	M2	ODT
0	0	0	Off
0	0	1	40Ω
0	1	0	60Ω
0	1	1	120Ω
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M1	M0	Output Drive
0	0	44.3Ω
0	1	58Ω
1	0	Reserved
1	1	Reserved

Note: 1. BA2, BA3, and all address balls corresponding to reserved bits must be held LOW during the MRS command.

Output Drive Impedance

The RLDRAM 3 uses programmable impedance output buffers. This enables a user to match the driver impedance to the system. MR1[0] and MR1[1] are used to select 44.3Ω or 58Ω output impedance. The drivers have symmetrical output impedance. The device will power-up with an output impedance of 44.3Ω. To calibrate the impedance, a 240Ω ±1% external precision resistor (RZQ) is connected between the ZQ ball and V_{SSQ}.

The output impedance is calibrated during initialization through the ZQCL command. Subsequent periodic calibrations (ZQCS) may be performed to compensate for shifts in output impedance due to changes in temperature and voltage. More detailed information on calibration can be found in the ZQ Calibration section.

On-Die Termination (ODT)

MR1[4:2] are used to select the value of the on-die termination (ODT) for the DQ, DK*x*, and DM balls. When enabled, ODT terminates these balls to $V_{DDQ}/2$. The TwinDie RLDRAM 3 ODT values differ depending on the configuration and the pin. See the ODT Characteristics section for the effective impedances. The ODT function is dynamically switched off when a DQ begins to drive after a READ command has been issued. Similarly, ODT is designed to switch on at the DQs after the RLDRAM has issued the last piece of data. The DM and DK*x* balls are always terminated after ODT is enabled.

The ODT is calibrated during initialization through the ZQCL command. Subsequent periodic calibrations (ZQCS) may be performed to compensate for shifts in termination due to changes in temperature and voltage. More detailed information on calibration can be found in the ZQ Calibration section.

ZQ Calibration

The ZQ CALIBRATION mode register command is used to calibrate the DRAM output drivers (R_{ON}) and ODT values (R_{TT}) over process, voltage, and temperature, provided a dedicated 240Ω (±1%) external resistor is connected from the DRAM's RZQ ball to V_{SSQ}. Bit MR1[6] selects between ZQ calibration long (ZQCL) and ZQ calibration short (ZQCS), each of which are described in detail below. When bit MR1[7] is set HIGH, it enables the calibration sequence. Upon completion of the ZQ calibration sequence, MR1[7] automatically resets LOW.

The RLDRAM 3 needs a longer time to calibrate R_{ON} and ODT at power-up initialization and a relatively shorter time to perform periodic calibrations. An example of ZQ calibration timing is shown below.

All banks must have ^tRC met before ZQCL or ZQCS commands can be issued to the DRAM. No other activities (other than another ZQCL or ZQCS command issued to another DRAM) can be performed on the DRAM channel by the controller for the duration of ^tZQinit or ^tZQoper. The quiet time on the DRAM channel helps accurately calibrate R_{ON} and ODT. After DRAM calibration is achieved, the DRAM disables the ZQ ball's current consumption path to reduce power.

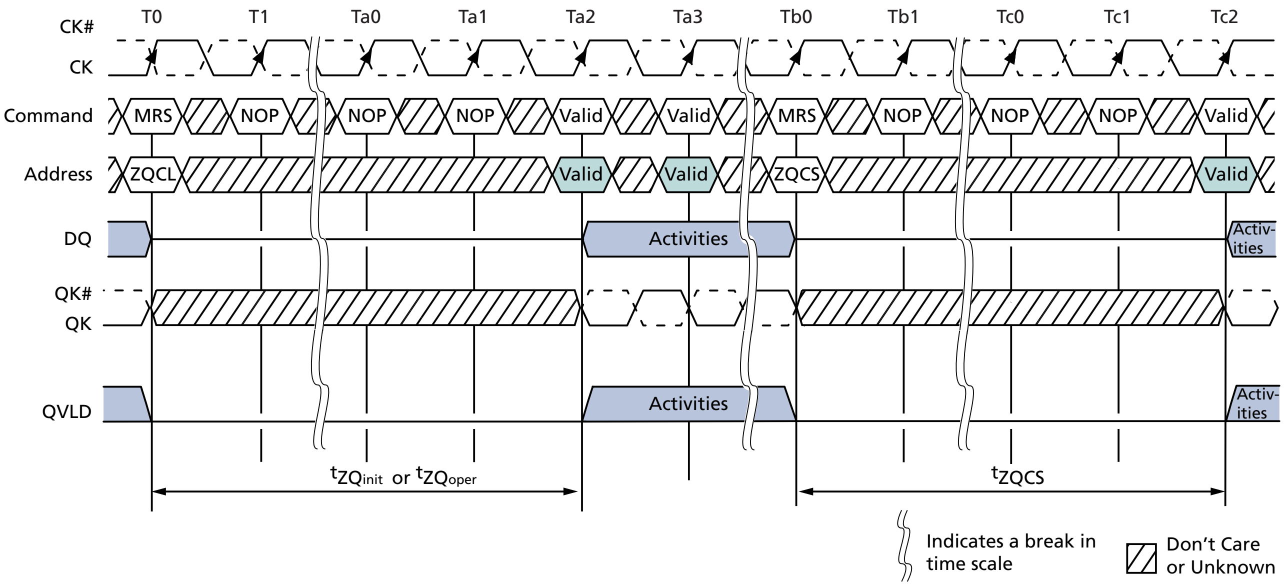
Because the two ranks within the x18 configuration TwinDie device share a ZQ resistor, only NOP commands are permitted for the duration of ^tZQinit, ^tZQoper, or ^tZQcs. Both ranks must be calibrated independently.

For the x36 configuration TwinDie device, the calibration timing is twice that of the x18 configuration because a single ZQ CALIBRATION mode register command calibrates one die in the stacked package and then the other.

ZQ CALIBRATION commands can be issued in parallel to DLL reset and locking time.

In systems that share the ZQ resistor between devices, the controller must not allow overlap of ^tZQinit, ^tZQoper, or ^tZQcs between devices. This is true of the two ranks in the x18 configuration TwinDie device, as well.

Figure 7: ZQ Calibration Timing (ZQCL and ZQCS)



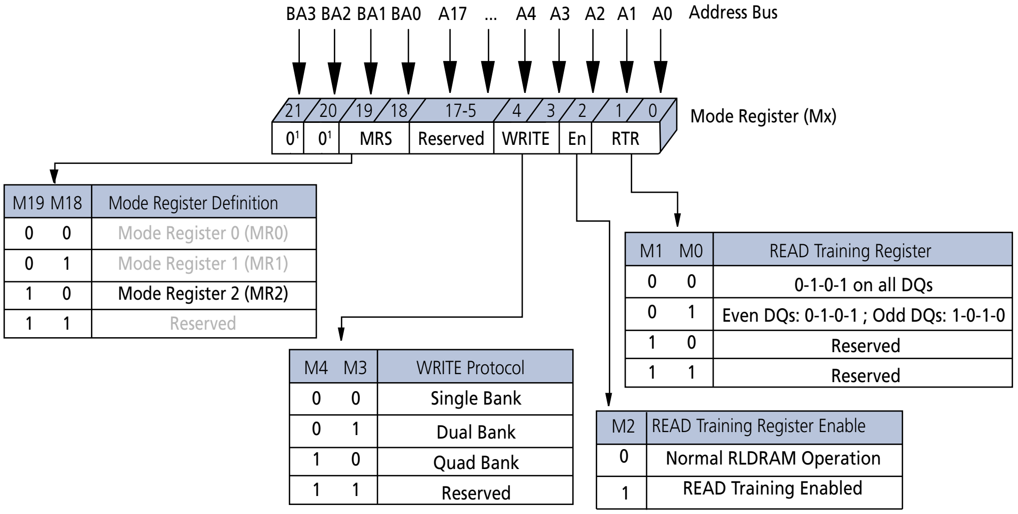
Notes:
1. All devices connected to the DQ bus should be held High-Z during calibration.
2. The state of QK and QK# are unknown during ZQ calibration.
3. ^{t}MRSC after loading the MR1 settings, QVLD output drive strength will be at the value selected or higher (lower resistance) until ZQ calibration is complete.

AUTO REFRESH Protocol

The AUTO REFRESH (AREF) protocol is selected with bit MR1[8]. There are two ways in which AREF commands can be issued to the RLDRAM. Depending upon how bit MR1[8] is programmed, the memory controller can either issue bank address-controlled or multibank AREF commands. A bank address-controlled AREF uses the BA[3:0] inputs to refresh a single bank per command. A multibank AUTO REFRESH is enabled by setting bit MR1[8] HIGH during an MRS command. This refresh protocol allows for the simultaneous refreshing of a row in up to four banks. In this method, the address pins A[15:0] represent banks 0–15, respectively. More information on both AREF protocols may be found in the MT44K32M18 data sheet.

Mode Register 2 (MR2)

Figure 8: MR2 Definition for Non-Multiplexed Address Mode



M19	M18	Mode Register Definition
0	0	Mode Register 0 (MR0)
0	1	Mode Register 1 (MR1)
1	0	Mode Register 2 (MR2)
1	1	Reserved

M4	M3	WRITE Protocol
0	0	Single Bank
0	1	Dual Bank
1	0	Quad Bank
1	1	Reserved

M1	M0	READ Training Register
0	0	0-1-0-1 on all DQs
0	1	Even DQs: 0-1-0-1 ; Odd DQs: 1-0-1-0
1	0	Reserved
1	1	Reserved

M2	READ Training Register Enable
0	Normal RLDRAM Operation
1	READ Training Enabled

Note: 1. BA2, BA3, and all address balls corresponding to reserved bits must be held LOW during the MRS command.

READ Training Register (RTR)

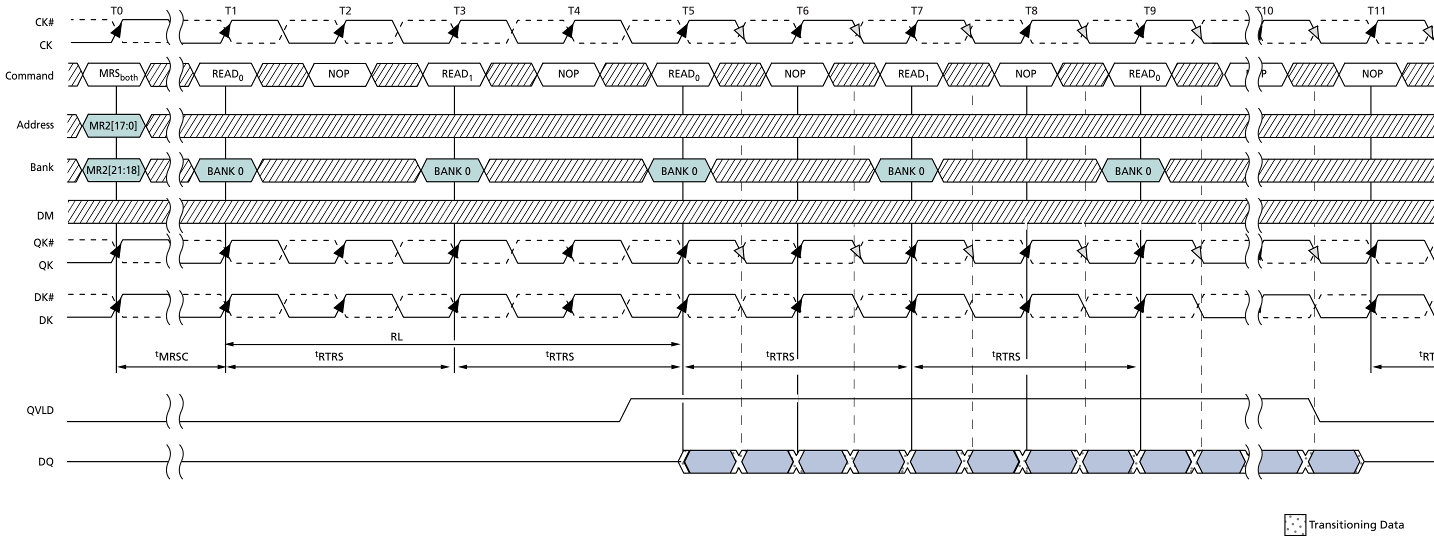
The READ training register (RTR) is controlled through MR2[2:0]. It is used to output a predefined bit sequence on the output balls to aid in system timing calibration. MR2[2] is the master bit that enables or disables access to the READ training register, and MR2[1:0] determine which predefined pattern for system calibration is selected. If MR2[2] is set to 0, the RTR is disabled, and the DRAM operates in normal mode. When MR2[2] is set to 1, the DRAM no longer outputs normal read data, but a predefined pattern that is defined by MR2[1:0].

Prior to enabling the RTR, all banks must be in the idle state (^{t}RC met). When the RTR is enabled, all subsequent READ commands will output four bits of a predefined sequence from the RTR on all DQs. The READ latency during RTR is defined with the data latency bits in MR0. To loop on the predefined pattern when the RTR is enabled, successive READ commands must be issued and satisfy ^{t}RTRS. x18 devices should issue interleaved READ commands (a READ to die 0, followed by a READ to die 1 as shown in Figure 9 (page 28)) to ensure proper READ training for both die. Address balls A[19:0] are considered "Don't Care" during RTR READ commands. Bank address bits BA[3:0] must access Bank 0 with each RTR READ command. ^{t}RC does not need to be met in between RTR READ commands to Bank 0. When the RTR is enabled, only READ commands are allowed. When the last RTR READ burst has completed and ^{t}RTRE has been satisfied, an MRS command can be issued to exit the RTR. Standard RLDRAM3 operation may then start after ^{t}MRSC has been met. The RESET function is supported when the RTR is enabled.

If MR2[1:0] is set to 00, a 0-1-0-1 pattern will be output on all DQs with each RTR READ command. If MR2[1:0] is set to 01, a 0-1-0-1 pattern will output on all even DQs, and the opposite pattern, a 1-0-1-0, will output on all odd DQs with each RTR READ command.

Note: Enabling RTR may corrupt previously written data.

Figure 9: READ Training Function - x18 Die Interleave Training



Note: 1. RL = READ latency defined with data latency MR0 setting.

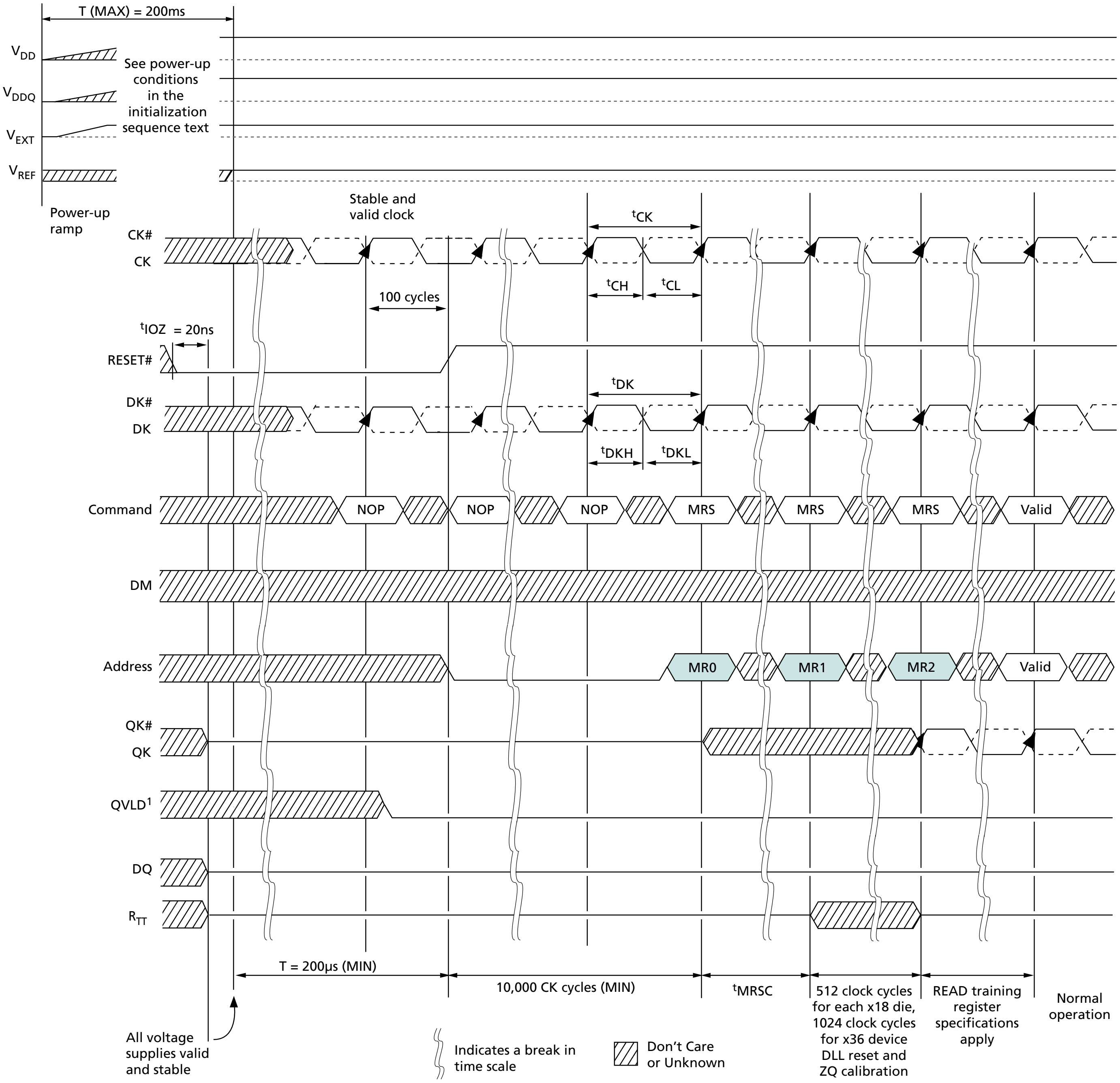
INITIALIZATION Operation

The RLDRAM 3 device must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operations or permanent damage to the device.

The following sequence is used for power-up:

1. Apply power (V_{EXT}, V_{DD}, V_{DDQ}). Apply V_{DD} and V_{EXT} before, or at the same time as, V_{DDQ}. V_{DD} must not exceed V_{EXT} during power supply ramp. V_{EXT}, V_{DD}, V_{DDQ} must all ramp to their respective minimum DC levels within 200ms.
2. Ensure that RESET# is below $0.2 \times V_{DDQ}$ during power ramp to ensure the outputs remain disabled (High-Z) and ODT is off (R_{TT} is also High-Z). DQs and QK signals will remain High-Z until the MR0 command is issued. All other inputs may be undefined during the power ramp.
3. After the power is stable, RESET# must be LOW for at least 200µs to begin the initialization process.
4. After 100 or more stable input clock cycles with NOP commands, bring RESET# HIGH.
5. After RESET# goes HIGH, a stable clock must be applied in conjunction with NOP commands, and all address pins (A[19:0] and BA[3:0]) must be held LOW for 10,000 cycles.
6. Load the desired settings into MR0. The x18 DDP device should have both CSx# asserted for this step.
7. ^{t}MRSC after loading the MR0 settings, load the operating parameters into MR1, including DLL reset and long ZQ calibration. This step must be done on each die of the x18 DDP independently.
8. After the DLL is reset and long ZQ calibration is enabled, the input clock must be stable for 512 clock cycles for x18 devices and 1024 clock cycles for x36 devices, while NOPs are issued.
9. Load the desired settings into MR2. The x18 DDP device should have both CSx# asserted for this step. If READ training is being used for the x18 device, follow the procedure outlined in the READ Training Function – x18 Die Interleave Training figure contained in this data sheet prior to entering normal operation; for the x36 device, refer to the READ Training Function - Back-to-Back Training figure located in the Micron 576Mb RLDRAM3 data sheet.
10. The RLDRAM 3 is now ready for normal operation.

Figure 10: Power-Up/Initialization Sequence



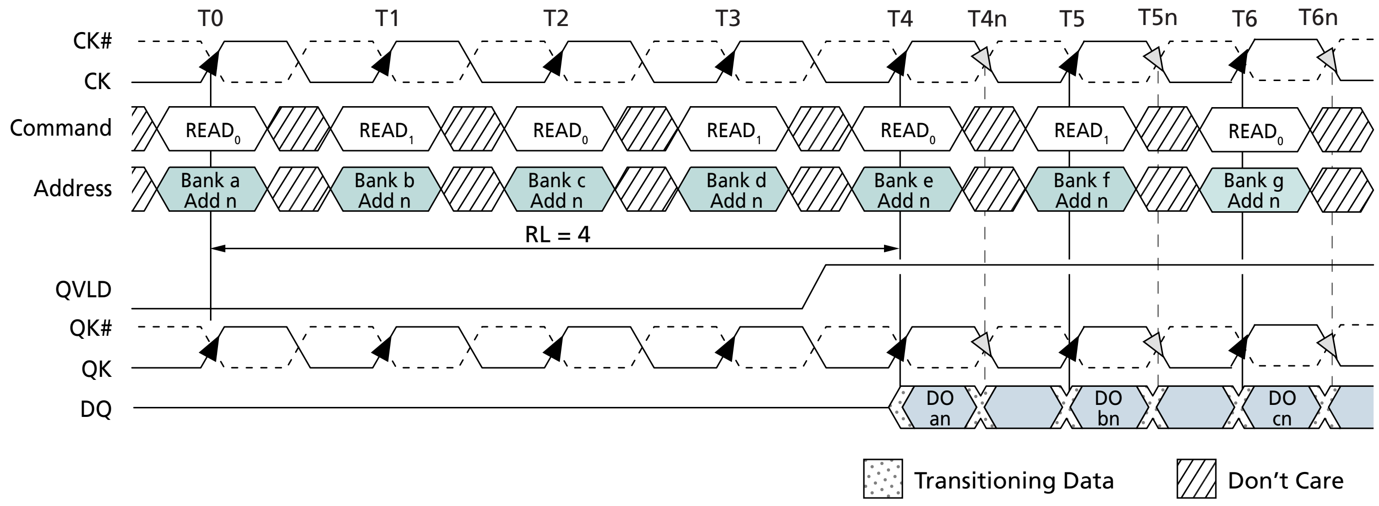
Notes: 1. QVLD output drive status during power-up and initialization:
   a. QVLD remains High-Z until 20ns after power supplies are stable and TCK or CK has cycled four times.
   b. QVLD will then drive LOW with 40Ω or lower until the output drive value selected in MR1 is enabled.

  c. ^{t}MRSC after loading the MR1 settings, QVLD output drive strength will be at the value selected or lower until ZQ calibration is complete.
  d. QVLD will meet the output drive strength specifications upon completion of the ZQ calibration timing.

2. After MR2 has been issued, R_{TT} is either High-Z or enabled to the ODT value selected in MR1.

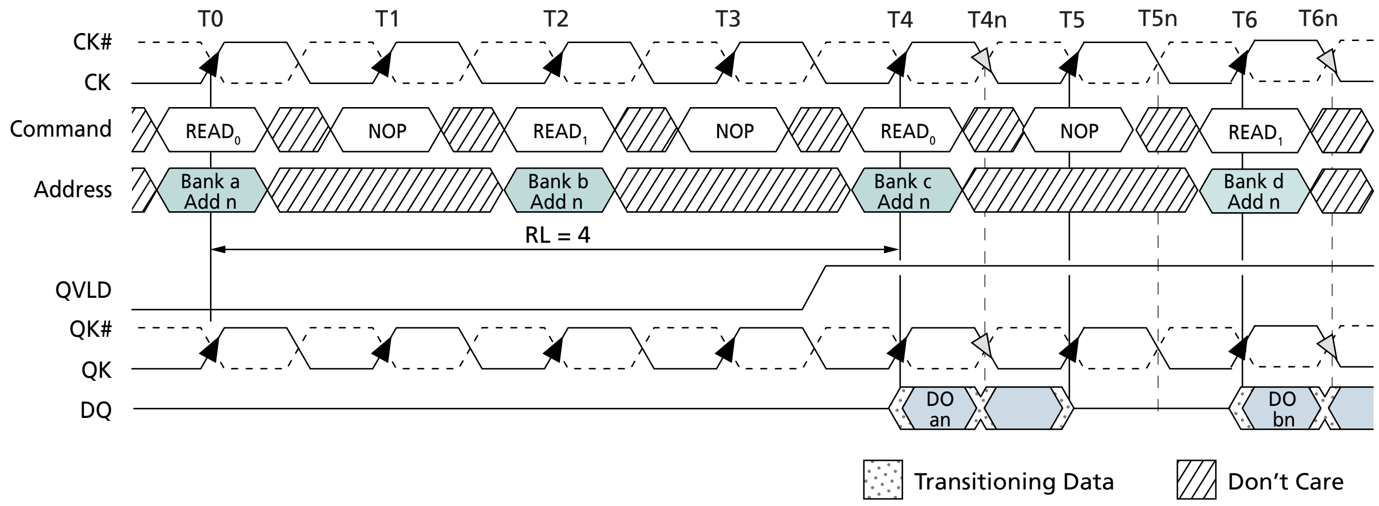
READ Operation

Figure 11: x18 Consecutive Die Interleave READ Bursts (BL = 2)



Note: 1. DO *an* (or *bn, cn*) = data-out from bank *a* (or bank *b, c*) and address *n*.

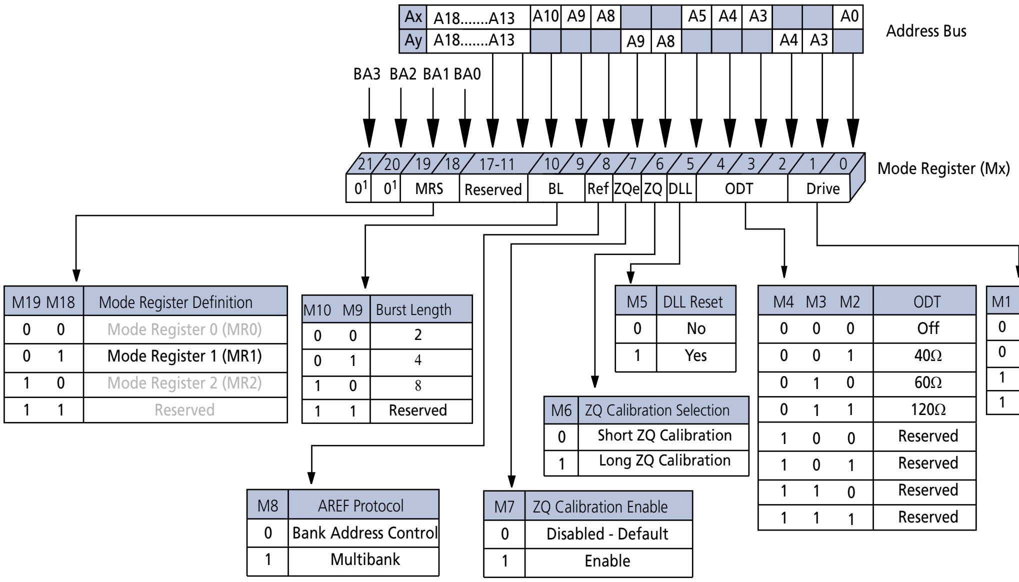
Figure 12: x18 Non-Consecutive Die Interleave READ Bursts (BL = 2)



Note: 1. DO *an* (or *bn*) = data-out from bank *a* (or bank *b*) and address *n*.

Multiplexed Address Mode

Figure 13: MR1 Definition for Multiplexed Address Mode



M19	M18	Mode Register Definition
0	0	Mode Register 0 (MR0)
0	1	Mode Register 1 (MR1)
1	0	Mode Register 2 (MR2)
1	1	Reserved

M10	M9	Burst Length
0	0	2
0	1	4
1	0	8
1	1	Reserved

M5	DLL Reset
0	No
1	Yes

M4	M3	M2	ODT
0	0	0	Off
0	0	1	40Ω
0	1	0	60Ω
0	1	1	120Ω
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M1	M0	Output Drive
0	0	44.3 Ω
0	1	58 Ω
1	0	Reserved
1	1	Reserved

M6	ZQ Calibration Selection
0	Short ZQ Calibration
1	Long ZQ Calibration

M8	AREF Protocol
0	Bank Address Control
1	Multibank

M7	ZQ Calibration Enable
0	Disabled - Default
1	Enable

Notes:
1. BA2, BA3, and all address balls corresponding to reserved bits must be held LOW during the MRS command.
2. BL8 not available in x36.

Table 21: Address Mapping in Multiplexed Address Mode

Data Width	Burst Length	Ball	Address										
			A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
x36	2	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	A19	A11	A12	A16	A15
	4	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15
x18	2	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	A19	A11	A12	A16	A15
	4	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15
	8	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	X
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15

Note: 1. X = "Don't Care"

Mirror Function

The mirror function ball (MF) is a DC input used to create mirrored ballouts for simple dual-loaded clamshell mounting. If the MF ball is tied LOW, the address and command balls are in their true layout. If the MF ball is tied HIGH, the address and command balls are mirrored around the central y-axis (column 7). The following table shows the ball assignments when the MF ball is tied HIGH for a x18 device. Compare this table to Table 1 (page 5) to see how the address and command balls are mirrored. The same balls are mirrored on the x36 device.

Table 22: 64 Meg x 18 Ball Assignments with MF Ball Tied HIGH

	1	2	3	4	5	6	7	8	9	10	11	12	13
A		V_{SS}	V_{DD}	NC	V_{DDQ}	NC	V_{REF}	DQ7	V_{DDQ}	DQ8	V_{DD}	V_{SS}	RESET#
B	V_{EXT}	V_{SS}	NC	V_{SSQ}	NC	V_{DDQ}	DM0	V_{DDQ}	DQ5	V_{SSQ}	DQ6	V_{SS}	V_{EXT}
C	V_{DD}	NC	V_{DDQ}	NC	V_{SSQ}	NC	DK0#	DQ2	V_{SSQ}	DQ3	V_{DDQ}	DQ4	V_{DD}
D	A13	V_{SSQ}	NC	V_{DDQ}	NC	V_{SSQ}	DK0	V_{SSQ}	QK0	V_{DDQ}	DQ0	V_{SSQ}	A11
E	V_{SS}	CS0#[1]	V_{SSQ}	NC	V_{DDQ}	NC	MF	QK0#	V_{DDQ}	DQ1	V_{SSQ}	A0	V_{SS}
F	A9	A5	V_{DD}	A4	A3	REF#	ZQ	WE#	A1	A2	V_{DD}	CS1#[1]	A7
G	V_{SS}	A18	A8	V_{SS}	BA0	V_{SS}	CK#	V_{SS}	BA1	V_{SS}	A6	A15	V_{SS}
H	A10	V_{DD}	A12	A17	V_{DD}	BA2	CK	BA3	V_{DD}	A16	A14	V_{DD}	A19[1]
J	V_{DDQ}	NC	V_{SSQ}	NC	V_{DDQ}	NC	V_{SS}	QK1#	V_{DDQ}	DQ9	V_{SSQ}	QVLD	V_{DDQ}
K	NC	V_{SSQ}	NC	V_{DDQ}	NC	V_{SSQ}	DK1	V_{SSQ}	QK1	V_{DDQ}	DQ10	V_{SSQ}	DQ11
L	V_{DD}	NC	V_{DDQ}	NC	V_{SSQ}	NC	DK1#	DQ12	V_{SSQ}	DQ13	V_{DDQ}	DQ14	V_{DD}
M	V_{EXT}	V_{SS}	NC	V_{SSQ}	NC	V_{DDQ}	DM1	V_{DDQ}	DQ15	V_{SSQ}	DQ16	V_{SS}	V_{EXT}
N	V_{SS}	TCK	V_{DD}	TDO	V_{DDQ}	NC	V_{REF}	DQ17	V_{DDQ}	TDI	V_{DD}	TMS	V_{SS}

Note: 1. This table shows the mirrored pinout for the x18 device. The x36 device mirrors in the same manner, but has the following changes: CS0# is CS#, CS1# is NF, A19 is NF, and DQs are as shown in Table 2 (page 5).

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.