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MT29C2G24MAABAKAKD-5 IT

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DATA SHEETS (1)

SPECS

SIM MODELS & SOFTWARE

Data Sheets (1)

Data Sheet



137-Ball, 10.5 x 13.0mm, NAND Flash + LPDDR MCP Data Sheet

J41L; MT29C2G24MAAAAKAKD-5 IT, MT29C2G24MAABAKAKD-5 IT, MT29C2G24MAAAAKAHH-5 AIT

File Type: PDF

Updated: 11/2015

Automotive Embedded Multichip Packages NAND LPDDR NAND-Based MCP

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Specs

Orderable Parts for: MT29C2G24MAABAKAKD-5 IT

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	Status	Media	FBGA Code	SPD Data	Chipset Validation	PLP	Start Date	Alternative Part
MT29C2G24MAABAKAKD-5 IT	Production	N/A	JW617	N/A	N/A	No		N/A

Detailed Specifications

Part Status Code	Production	NAND Density	2Gb	DRAM Type	LPDDR	DRAM Density	1Gb
Bus Width	x16	Secondary Bus Width	x32	RoHS	Yes	Voltage	1.7V-1.9V
Package	TFBGA	Pin Count	137-ball	Clock Rate	200 MHz	Operating Temp	-40C to +85C

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Sim Models & Software

Sim Models

IBIS



IBIS (ZIP)

NAND Flash + LPDDR MCP (Rev 1.7)

File Type: ZIP

Updated: 07/31/2014

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NAND LPDDR

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HSpice



HSpice: J41L (ZIP)

Rev 1.4

File Type: ZIP

Updated: 08/17/2010

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RoHS Certificates

RoHS Certificates

RoHS Certificate of Compliance (PDF)

MT29C2G24MAABAKAKD-5 IT

Part-specific certification of how this product meets the requirements of the current DIRECTIVE 2002/95/EC, a.k.a. Restriction of Hazardous Substances (RoHS) Directive.

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Updated: 05/2017

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RoHS Certificates

China RoHS Certificate (PDF)

MT29C2G24MAABAKAKD-5 IT

Part-specific certification as required by China's Management Methods for Controlling Pollution by Electronic Information Products.

File Type: (PDF)

Updated: 05/2017

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Documentation & Support

Technical Notes

[SEARCH \(2\) NAND-BASED MCP TECHNICAL NOTES](#)

Technical Notes

[TN-00-01: Moisture Sensitivity of Plastic Packages \(PDF\)](#)

(TN-00-01) This technical note describes shipping procedures for preventing memory devices from absorbing moisture and recommendations for baking devices exposed to excessive moisture.

File Type: PDF

Updated: 02/14/2013

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Technical Notes

[TN-10-08: Thermal Implications for LPDDR Die Stacks \(PDF\)](#)

(TN-10-08) This technical note presents a case study of a handset simulation in which an LPDRAM is stacked on an application processor (PoP) and the resulting thermal-profile modeling. This note also explains how thermal detection features included in LPDDR and LPDDR2 can be used to...

File Type: PDF

Updated: 07/26/2010

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Customer Service Note

Customer Service Note

Customer Service Note

[Micron Component and Module Packaging \(PDF\)](#)

(CSN-16) Explanation of Micron packaging labels and procedures.

File Type: PDF

Updated: 05/03/2017

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[PoP User Guide \(PDF\)](#)

(CSN-34) Provides several well-established guidelines for package-on-package (PoP) semiconductor package design and assembly, which requires unique considerations in both the up-front design and the manufacturing process.

File Type: PDF

Updated: 05/16/2016

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Parts with the same Data Sheet (2)

MT29C2G24MAABAKAKD-5 I T (Current)		MT29C2G24MAAAAKAKD-5 I T	MT29C2G24MAAAAKAHH-5 AIT
Part Status Code	Production	Production	Production
NAND Density	2Gb	2Gb	2Gb
DRAM Type	LPDDR	LPDDR	LPDDR
DRAM Density	1Gb	1Gb	1Gb
Bus Width	x16	x8	x8
Secondary Bus Width	x32	x32	x32
RoHS	Yes	Yes	Yes
Voltage	1.7V-1.9V	1.7V-1.9V	1.7V-1.9V
Package	TFBGA	TFBGA	TFBGA
Pin Count	137-ball	137-ball	137-ball
Clock Rate	200 MHz	200 MHz	200 MHz
Operating Temp	-40C to +85C	-40C to +85C	-40C to +85C

MT29C2G24MAABAKAKD-5 I T (Current)	
Part Status Code	Production
NAND Density	2Gb
DRAM Type	LPDDR
DRAM Density	1Gb
Bus Width	x16
Secondary Bus Width	x32
RoHS	Yes

Where to Buy

Status	Media	FBGA Code	SPD Data	Chipset Validation	PLP	Start Date	Alternative Part
Production	N/A	JW617	N/A	N/A	No		N/A

Voltage	1.7V-1.9V
Package	TFBGA
Pin Count	137-ball
Clock Rate	200 MHz
Operating Temp	-40C to +85C

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