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Summary

The ZABG6003 is an advanced GaAs and HEMT FETs bias controller designed to operate from minimal supply rails and intended primarily for satellite Low Noise Blocks (LNBs). With the addition of one capacitor and a resistor, the ZABG6003 provides drain voltage and current control for up to 6 external grounded source FETs. Generating the regulated negative rail required for FET gate biasing whilst operating from a single supply of 2.1V to 5V. The -2V negative bias can also be used to supply other external circuits.

Setting drain currents on the ZABG6003 only requires one resistor which controls the drain current of the first stage FETS (D1 and D4). The drain current is set internally to 10mA for the remaining 4 FETs for the second and third stages. This allows the operating current of input FETs to be adjusted to minimize noise, whilst the following FET stages are fixed to minimize the number of external components used.

Features

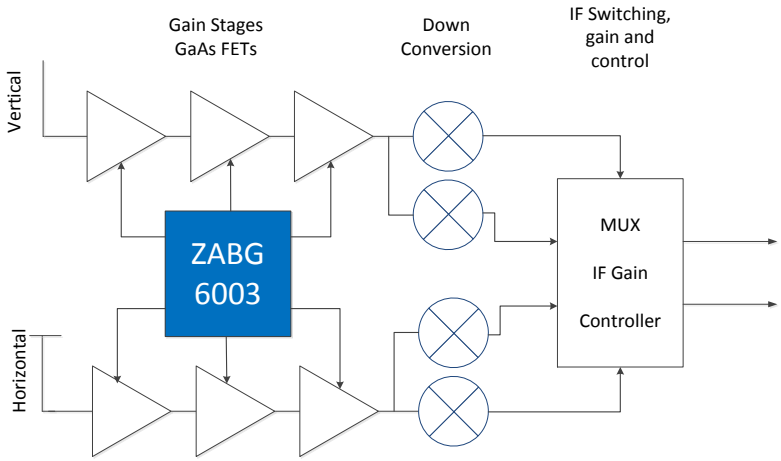
- Provides Bias for up to 6 GaAs and HEMT FETs
  - 2 × Amplifier FET Drain Current Programmable (4mA to 15mA)
  - 4 × Amplifier FET Drain Current Internally Fixed to 10mA
- Operating Range of 2.1V to 5V
- Ultra-Low Operating Current of 1.1mA
- Dynamic FET Protection
- Regulated Negative Rail Generator Requires only 1 External Capacitor
- Expended Temperature Range of -40°C to +105°C
- U-QFN3030-16 (Type B) Surface Mount Package
- Low External Component Count
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3**)

Applications

- Low Power LNB's
- Digital LNB's
- IP LNB's
- Twin and Quad LNB's
- General Purpose LNA Bias

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Twin LNB System Diagrams



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Device Description

The ZABG series of devices are designed to meet the bias requirements of GaAs and HEMT FETs commonly used in satellite receiver LNBs with a minimum of external components whilst operating from a minimal voltage supply and using minimal current.

The ZABG6003 has six FET bias stages. To optimize the system for noise and gain the drain current for two of the six stages can be programmed over the range of 4mA to 15mA. Programming the drain current of FETS D1 and D4 is achieved by a resistor connected to the R_{CAL1} pin. The Drain current of the remaining four FETS D2, D3, D5 and D6 are internally set to 10mA.

Drain voltages of amplifier stages are set at 2.0V and are current limited to approximately current set by their associated R_{CAL} resistors.

Depletion mode FETs require a negative voltage bias supply when operated in grounded source circuits. The ZABG6003 includes an integrated switched capacitor DC-DC converter generating a regulated output of -2V to allow single supply operation. The ZABG6003 has been designed to be used with supply rails of 2.1V to 5.0V and the V_{DD} range has been extended to 5.5V to allow for 10% supply variation.

It is possible to use less than the full complement of FET bias controls, unused drain and gate connections can be left open circuit without affecting operation of the remaining bias circuits.

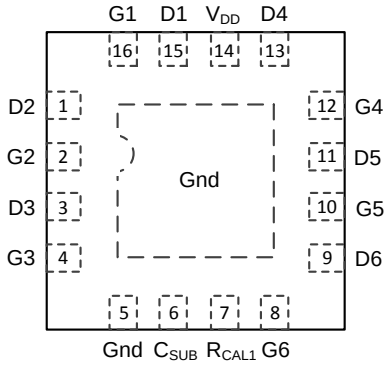
To protect the external FETs the circuits have been designed to ensure that, under any conditions including power up/down transients, the gate drive from the bias circuits cannot exceed -2.5V. Additionally each stage has its own individual current limiter. Furthermore if the negative rail experiences a fault condition, such as overload or short circuit, the drain supply to the FETs will be limited, avoiding excessive current flow.

The ZABG6003 is available in the U-QFN3030-16 (Type B) package.

Device operating temperature is -40°C to +105°C to suit a wide range of environmental conditions.

Pin Assignments and Descriptions

(Top View)



U-QFN3030-16 (Type B)

Pin Number	Pin Name	Description
1	D2	Drain GaAs FET 2
2	G2	Gate GaAs FET 2
3	D3	Drain GaAs FET 3
4	G3	Gate GaAs FET 3
5	Gnd	Ground
6	C_{SUB}	Negative rail reservoir capacitor
7	R_{CAL1}	Drain current setting for D1 and D4
8	G6	Gate GaAs FET 6
9	D6	Drain GaAs FET 6
10	G5	Gate GaAs FET 5
11	D5	Drain GaAs FET 5
12	G4	Gate GaAs FET 4
13	D4	Drain GaAs FET 4
14	V_{DD}	Supply voltage
15	D1	Drain GaAs FET 1
16	G1	Gate GaAs FET 1
Pad	Gnd	Must be connected to Ground or No Connection

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Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage	-0.6 to +6	V
I_{DD}	Supply Current	100	mA
—	Power Dissipation U-QFN3030-16 (Type B)	650	mW
T_J	Junction Temperature	+135	°C
T_{STG}	Storage Temperature Range	-40 to +150	°C

Recommended Operating Conditions (Note 8)

Symbol	Parameter	Min	Max	Unit
V_{DD}	Operating Voltage Range	2.1	5.5	V
T_A	Operating Temperature Range	-40	+105	°C

Electrical Characteristics (@T_A = +25°C, V_{DD} = 2.3V, I_{D1} to I_{D6} set to 10mA.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply Current	I_{D1-6} = 0	—	1.1	2.5	mA
$I_{DD(L)}$		I_{D1-6} = 10mA	—	—	65	mA
V_{CSUB}	Substrate Voltage (Note 5)	I_{CSUB} = 0	-2.5	-2.0	-1.5	V
$V_{CSUB(L)}$		I_{CSUB} = -20µA	—	—	-1.5	V
f_{OSC}	Oscillator Frequency	—	—	7.5	—	MHz
$V_{D(NOISE)}$	Drain Voltage (Note 6)	$C_{GATE-GND}$ = 10nF $C_{DRAIN-GND}$ = 10nF	—	—	0.02	V_{PK-PK}
$V_{G(NOISE)}$	Gate Voltage (Note 6)	$C_{GATE-GND}$ = 10nF $C_{DRAIN-GND}$ = 10nF	—	—	0.005	V_{PK-PK}
Gate Characteristics						
Gate (G1 to G6)						
I_G	Current Range	—	-50	—	60	µA
$V_{G(L)}$	Voltage Low	I_D = 12mA, I_G = -10µA	-2.5	-2.0	-1.5	V
$V_{G(H)}$	Voltage High	I_D = 8mA, I_G = 0	0	0.7	1.0	V
Drain Characteristics						
Drain (D1 to D6)						
I_D	Current Range	D1 and D4	4	—	15	mA
I_{DD}		D2, D3, D5, D6 Internally Fixed	—	10	—	mA
$I_{D(OP)}$	Current Operating (Note 4)	Standard Application Circuit	8	10	12	mA
$V_{D(OP)}$	Voltage Operating (Note 7)	I_D = 10mA	1.8	2.0	2.2	V
dV_D/dV_{DD}	delta V_D vs V_{DD}	V_{DD} = 2.3V to 5.5V	—	0.075	—	%/V
dI_D/dV_{DD}	delta I_D vs V_{DD}	V_{DD} = 2.3V to 5.5V	—	0.7	—	%/V
dV_D/dT_A	delta V_D vs T_A	T_A = -40°C to +105°C	—	150	—	ppm

Notes:
4. Characteristics are measured using one external reference resistor, R_{CAL1}.
5. The negative bias voltages are generated on-chip using an internal oscillator. An external 47nF capacitor is required for this purpose.
6. Noise voltage measurements are made with FETs and gate and drain capacitors of value 10nF in place. Noise voltages are not measured in production.
7. The maximum operating drain voltage is equal to V_{DD} or $V_{D(OP)}$ max whichever is lower.
8. ESD sensitive, handling precautions are recommended.

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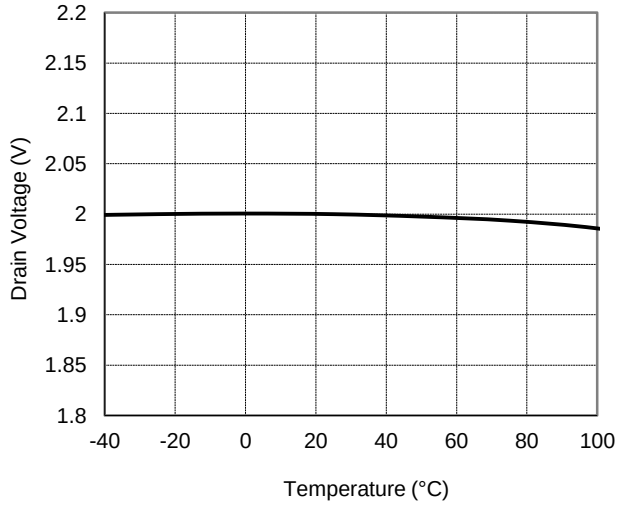
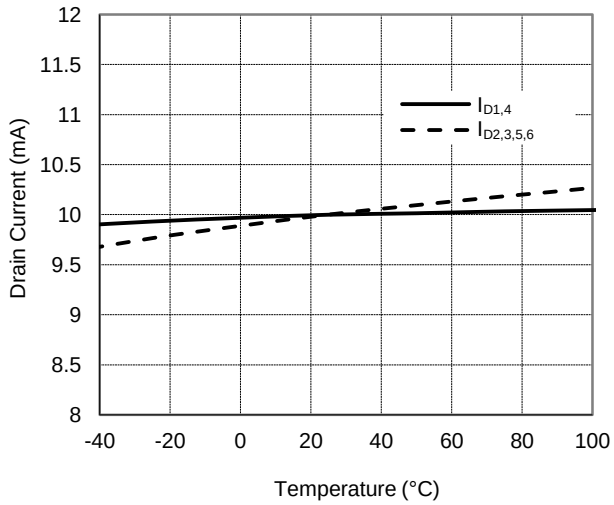
Typical Characteristics (@T_A = +25°C, V_{DD} = 2.3V, I_{D1} to I_{D6} set to 10mA (setting I_D to 10mA), unless otherwise stated.)

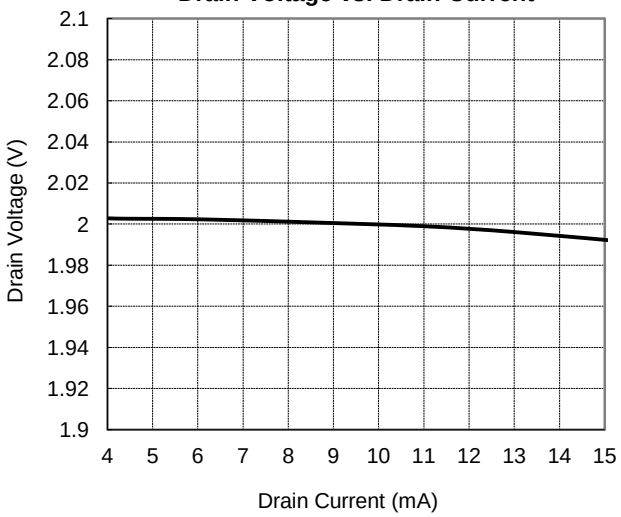
Drain Voltage vs. Temperature



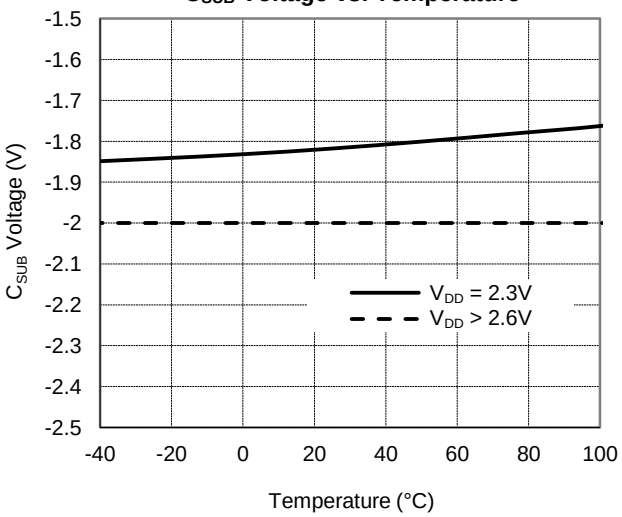
Drain Current vs. Temperature



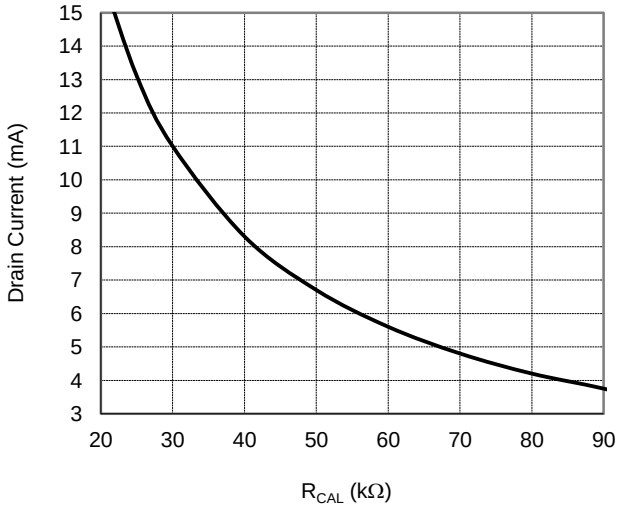
Drain Voltage vs. Drain Current



C_{SUB} Voltage vs. Temperature



Drain Current vs. R_{CAL}



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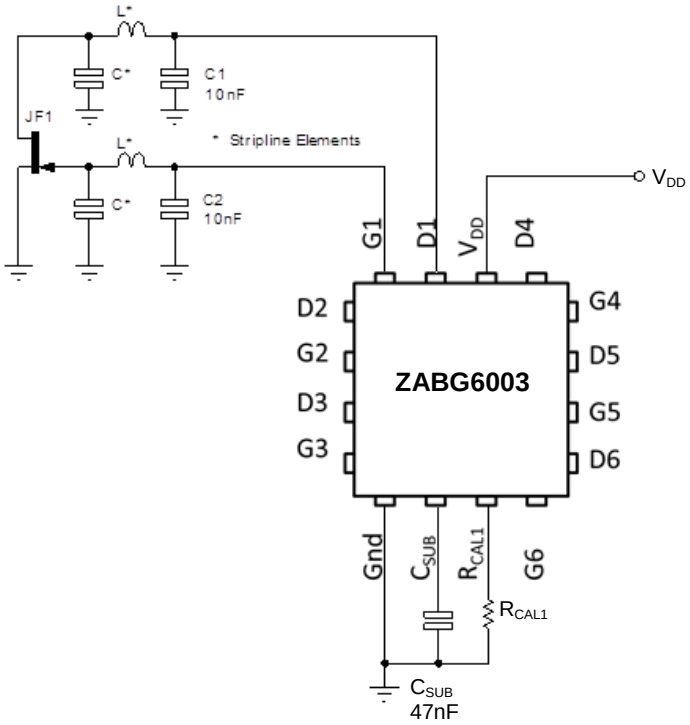
Application Information

Below is a partial applications circuit for the ZABG6003 showing all external components needed for biasing one of the six FET stages available as a typical LNA (Low Noise Amplifier). Each bias stage is provided with a gate and drain pin. The drain pin provides a regulated 2.0V supply that includes a drain current monitor. The drain current taken by the external FET is compared with a user selected level, generating a signal that adjusts the gate voltage of the FET to obtain the required drain current. If for any reason, an attempt is made to draw more than the user set drain current from the drain pin, the drain voltage will be reduced to ensure excess current is not taken. The gate pin drivers are also current limited.



The bias stages are split up into two groups, with the drain current for D1 and D4 set by an external R_{CAL1} resistor within the range of 4mA to 15mA. Drain currents for D2, D3, D5 and D6 are internally fixed to 10mA. This allows the optimization of drain currents for differing tasks such as input stages where noise can be critical and later amplifier stages where gain may be more important. A graph showing the relationship between the value of R_{CAL} and I_D is provided in the *Typical Characteristics* section of this datasheet.

The ZABG6003 includes a switched capacitor DC-DC converter that is used to generate the negative supply required to bias depletion mode FETs used in common source circuit configuration as shown above. This converter uses an external capacitor C_{SUB} as the output reservoir capacitor. The circuit provides a regulated -2V supply both for gate driver use and for external use if required (for extra discrete bias stages, mixer bias, local oscillator bias etc.). The -2V supply is available from the C_{SUB} pin.

If any bias stages are not required, their gate and drain pins may be left open circuit. If all bias stages associated with a R_{CAL} resistor are not required, then this resistor may be omitted. The Gnd flag on the underside of the DFN package can be connected to Gnd or left open circuit.

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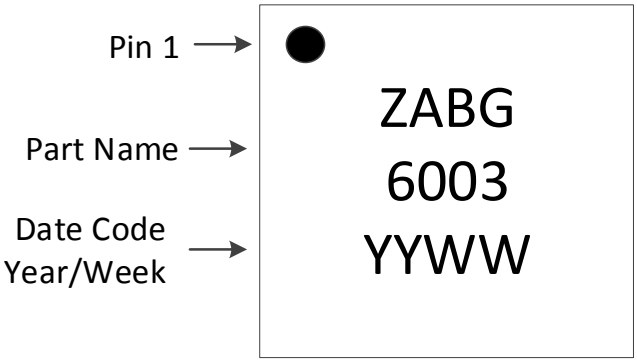
Ordering Information

Part Number	Package	Reel Size (inches)	Tape Width (mm)	Quantity Per Reel
ZABG6003JA16TC	U-QFN3030-16 (Type B)	13	8	3,000

Marking Information

U-QFN3030-16 (Type B)

(Top View)



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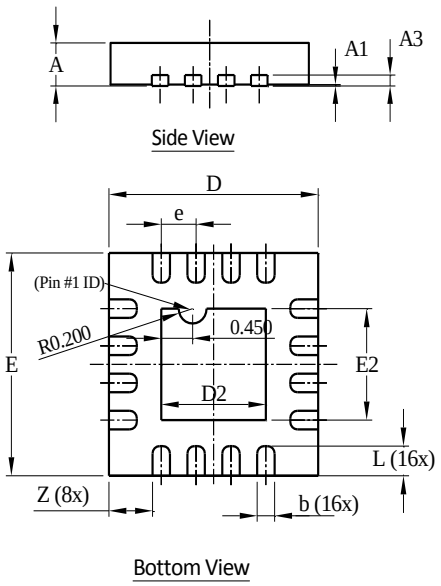
Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-QFN3030-16 (Type B)

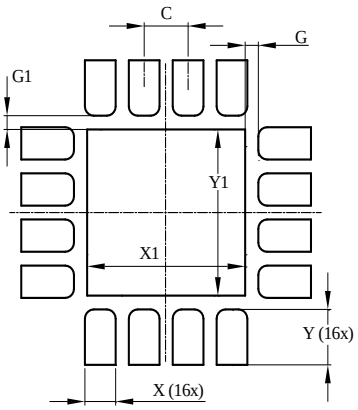


U-QFN3030-16 Type B			
Dim	**Min**	**Max**	**Typ**
A	0.55	0.65	0.60
A1	0	0.05	0.02
A3	-	-	0.15
b	0.18	0.28	0.23
D	2.95	3.05	3.00
D2	1.40	1.60	1.50
E	2.95	3.05	3.00
E2	1.40	1.60	1.50
e	-	-	0.50
L	0.35	0.45	0.40
Z	-	-	0.625
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-QFN3030-16 (Type B)



Dimensions	Value (in mm)
C	0.500
G	0.150
G1	0.150
X	0.350
X1	1.800
Y	0.600
Y1	1.800

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