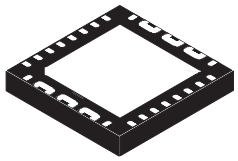
Document Number: MC34717
Rev 5.0, 12/2014

5.0 A 1.0 MHz Fully Integrated Dual Switch-Mode Power Supply

34717

DUAL SWITCH-MODE POWER SUPPLY



EP SUFFIX (PB_FREE)
98ASA00702D
26-PIN QFN

The 34717 is a highly integrated, space-efficient, low cost, dual synchronous buck switching regulator with integrated N-channel power MOSFETs. It is a high performance dual point-of-load (PoL) power supply with many desired features for the 3.3 and 5.0 V environments.

Both channels can provide up to 5.0 A of continuous output current capability with high efficiency and tight output regulation. The second channel has the ability to track an external reference voltage in different configurations.

The 34717 SMARTMOS device offers the designer the flexibility of many control, supervisory, and protection functions to allow for easy implementation of complex designs. It is housed in a Pb-free, thermally enhanced, and space efficient 26 pin exposed pad QFN.

Features

- 50 mΩ integrated N-channel power MOSFETs
- Input voltage operating range from 3.0 to 6.0 V
- ±1% accurate output voltages, ranging from 0.7 to 3.6 V
- The second output has voltage tracking capability in different configurations
- Programmable switching frequency range from 200 kHz to 1.0 MHz
- Programmable soft start timing
- Over-current limit and short-circuit protection
- Thermal shutdown
- Output overvoltage and undervoltage detection
- Active low power good output signal
- Active low shutdown input.

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MC34717EP/R2	-40 °C to 85 °C	26 QFN

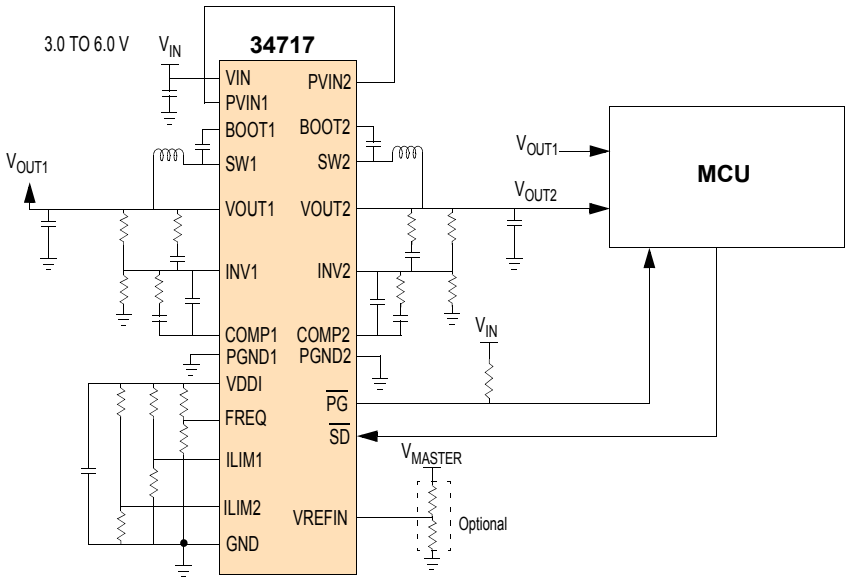


Figure 1. 34717 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

INTERNAL BLOCK DIAGRAM

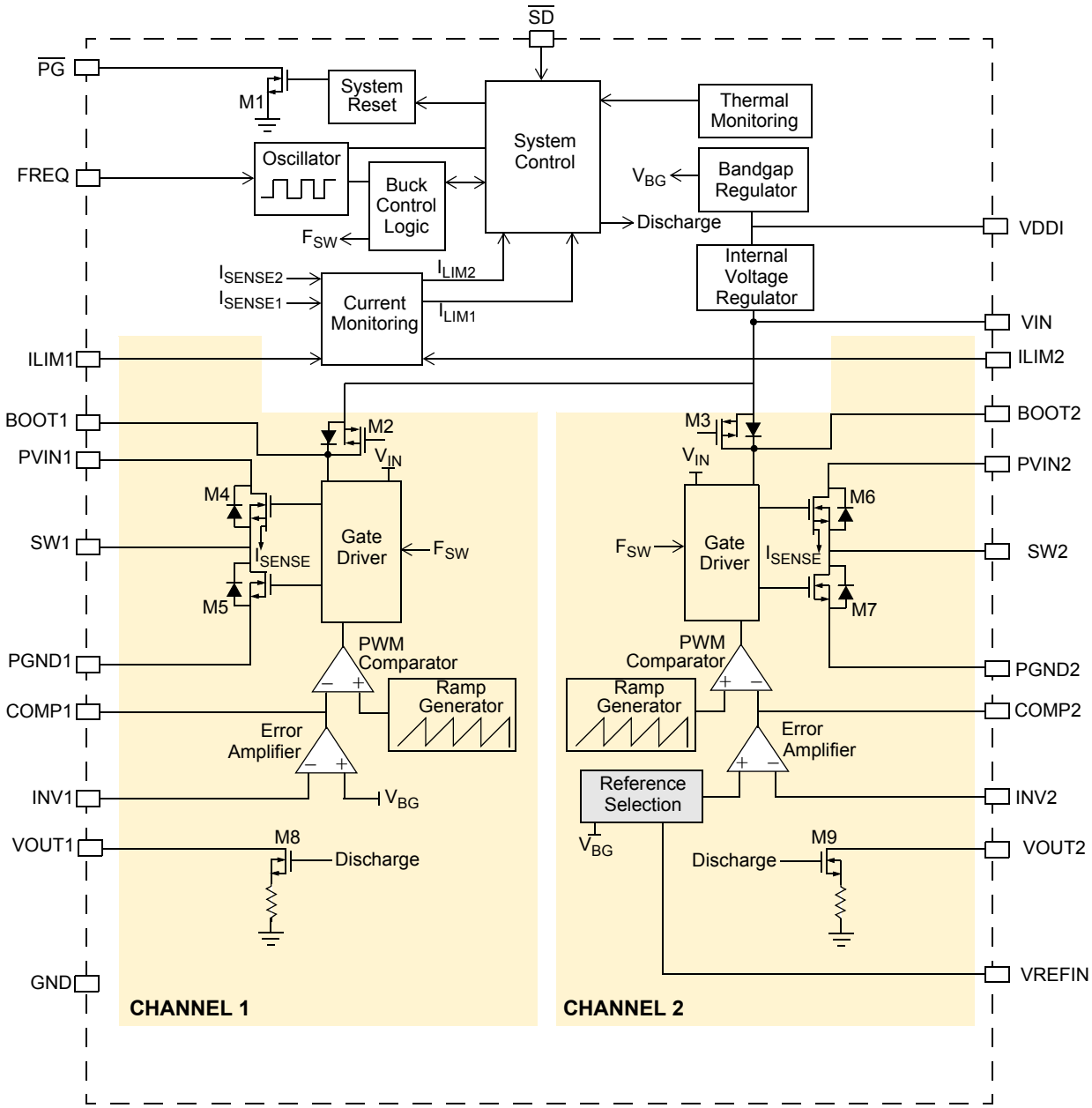


Figure 2. 34717 Simplified Internal Block Diagram

PIN CONNECTIONS

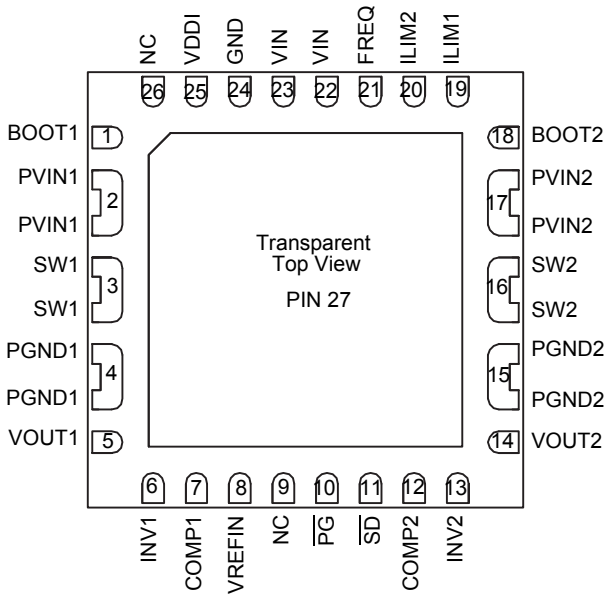


Figure 3. 34717 Pin Connections

Table 1. 34717 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 12.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1	BOOT1	Passive	Bootstrap	Channel 1 Bootstrap capacitor input pin
2	PVIN1	Supply	Power Input Voltage	Channel 1 Buck converter power input
3	SW1	Output	Switching Node	Channel 1 Buck converter switching node
4	PGND1	Ground	Power Ground	Channel 1 Buck converter and discharge MOSFETs power ground
5	VOUT1	Output	Output Voltage Discharge Path	Channel 1 Buck converter output voltage discharge pin
6	INV1	Input	Error Amplifier Inverting Input	Channel 1 Buck converter error amplifier inverting input
7	COMP1	Input	Buck Convertor Compensation Input	Channel 1 Buck converter external compensation network input
8	VREFIN	Input	Reference Voltage Input	Voltage tracking reference voltage input
9, 26	NC	None	No Connect	No internal connections to this pin. Recommend attaching a 0.1 µF capacitor from pin 9 to GND.
10	$\overline{PG}$	Output	Power Good Output Signal	It is an active low open drain power good status reporting output
11	$\overline{SD}$	Input	Shutdown Input	Shutdown mode input control pin
12	COMP2	Input	Buck Convertor Compensation Input	Channel 2 Buck converter external compensation network input
13	INV2	Input	Error Amplifier Inverting Input	Channel 2 Buck converter error amplifier inverting input

Table 1. 34717 Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 12.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
14	VOUT2	Output	Output Voltage Discharge Path	Channel 2 Buck converter output voltage discharge pin
15	PGND2	Ground	Power Ground	Channel 2 Buck converter and discharge MOSFETs power ground
16	SW2	Output	Switching Node	Channel 2 Buck converter switching node
17	PVIN2	Power	Power Input Voltage	Channel 2 Buck converter power input
18	BOOT2	Input	Bootstrap Input	Channel 2 Bootstrap capacitor input pin
19	ILIM1	Input	Soft Start Adjustment Input CH 1	Channel 1 soft start adjustment
20	ILIM2	Input	Soft Start Adjustment Input CH 2	Channel 2 soft start adjustment
21	FREQ	Input	Frequency Adjustment Input	The buck converters switching frequency adjustment input
22,23	VIN	Power	Input Supply Voltage	Power supply voltage of the IC
24	GND	Ground	Signal Ground	Analog ground of the IC
25	VDDI	Output	Internal Supply Voltage	Internal Supply Voltage Output
27	GND	Ground	Thermal Pad	Thermal pad for heat transfer. Connect the thermal pad to the analog ground and the ground plane for heat sinking.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Input Supply Voltage (VIN) Pin	V_{IN}	-0.3 to 7.0	V
High-side MOSFET Drain Voltage (PVIN1, PVIN2) Pins	PV_{IN}	-0.3 to 7.0	V
Switching Node (SW1, SW2) Pins	V_{SW}	-0.3 to 7.0	V
BOOT1, BOOT2 Pins (Referenced to SW1, SW2 Pins Respectively)	V_{BOOT} - V_{SW}	-0.3 to 7.0	V
$\overline{PG}$, VOUT1, VOUT2, and $\overline{SD}$ Pins	-	-0.3 to 7.0	V
VDDI, FREQ, ILIM1, ILIM2, INV1, INV2, COMP1, COMP2, and VREFIN Pins	-	-0.3 to 3.0	V
Channel 1 Continuous Output Current[1]	I_{OUT1}	+5.0	A
Channel 2 Continuous Output Current[1]	I_{OUT2}	+5.0	A
ESD Voltage[2]			V
Human Body Model	V_{ESD1}	±2000	
Machine Model (MM)	V_{ESD2}	±200	
Charge Device Model	V_{ESD3}	±750	
THERMAL RATINGS			
Operating Ambient Temperature[3]	T_A	-40 to 85	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Peak Package Reflow Temperature During Reflow[4],[5]	T_{PPRT}	Note 5	°C
Maximum Junction Temperature	$T_{J(MAX)}$	+150	°C
Power Dissipation (T_A = 85°C)[6]	P_D	2.03	W

Notes

1. Continuous output current capability so long as T_J is $\leq T_{J(MAX)}$.
2. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), the Machine Model (MM) (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω), and the Charge Device Model (CDM), Robotic (C_{ZAP} = 4.0 pF).
3. The limiting factor is junction temperature, taking into account power dissipation, thermal resistance, and heatsinking.
4. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
5. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.
6. Maximum power dissipation at indicated ambient temperature.

Table 2. Maximum Ratings *(continued)*

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
THERMAL RESISTANCE[7]			
Thermal Resistance, Junction to Ambient, Single-Layer Board (1s)[8]	$R_{\theta JA}$	93	°C/W
Thermal Resistance, Junction to Ambient, Four-Layer Board (2s2p)[9]	R_{qJMA}	32	°C/W
Thermal Resistance, Junction to Board[10]	R_{qJB}	13.6	°C/W

Notes

7. The PVIN, SW, and PGND pins comprise the main heat conduction paths.
8. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.
9. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal. There are thermal vias connecting the package to the two planes in the board. (per JESD51-5)
10. Thermal resistance between the device and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 3.0 V ≤ V_{IN} ≤ 6.0 V, -40 °C ≤ T_A ≤ 85 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
IC INPUT SUPPLY VOLTAGE (VIN)					
Input Supply Voltage Operating Range	V_{IN}	3.0	-	6.0	V
Input DC Supply Current[11] (Normal Mode: $\overline{SD}$ = 1, Unloaded Outputs)	I_{IN}	-	-	35	mA
Input DC Supply Current[11] (Shutdown Mode, $\overline{SD}$ = 0)	I_{INOFF}	-	-	100	µA
INTERNAL SUPPLY VOLTAGE OUTPUT (VDDI)					
Internal Supply Voltage Range	V_{DDI}	2.35	2.5	2.65	V
CHANNEL 1 BUCK CONVERTER (PVIN1, SW1, PGND1, BOOT1, INV1, COMP1, ILIM1)					
Channel 1 High-side MOSFET Drain Voltage Range	P_{VIN}	2.5	-	6.0	V
Output Voltage Adjustment Range[12]	V_{OUTHI1}	0.7	-	3.6	V
Output Voltage Accuracy[12],[13]	-	-1.0	-	1.0	%
Line Regulation[12] (Normal Operation, V_{IN} = 3.0 to 6.0 V, I_{OUT1} = 2.5 A)	REG_{LN1}	-1.0	-	1.0	%
Load Regulation[12] (Normal Operation, I_{OUT1} = 0.0 to 5.0 A)	REG_{LD1}	-1.0	-	1.0	%
Error Amplifier Reference Voltage[12]	V_{REF1}	-	0.7	-	V
Output Under-voltage Threshold	V_{UVR1}	-8.0	-	-1.5	%
Output Over-voltage Threshold	V_{OVR1}	1.5	-	8.0	%
Continuous Output Current	I_{OUT1}	-	-	5.0	A
Over-current Limit	I_{LIM1}	-	6.5	-	A
Soft Start Adjusting Reference Voltage Range	V_{ILIM1}	1.25	-	V_{DDI}	V
Short-circuit Current Limit	I_{SHORT1}	-	8.5	-	A
High-side N-CH Power MOSFET (M4) $R_{DS(on)}$[12] (I_{OUT1} = 1.0 A, V_{BOOT1} - V_{SW1}= 3.3 V)	$R_{DS(on)HS1}$	10	-	50	mΩ
Low-side N-CH Power MOSFET (M5) $R_{DS(on)}$[12] (I_{OUT1} = 1.0 A, V_{IN} = 3.3 V)	$R_{DS(on)LS1}$	10	-	50	mΩ
M2 $R_{DS(ON)}$ (V_{IN} = 3.3 V, M2 is on)	$R_{DS(on)M2}$	2.0	-	4.0	Ω

Notes

11. Section “MODES OF OPERATION”, page 16 has a detailed description of the different operating modes of the 34717
12. Design information only, this parameter is not production tested.
13. This is directly affected by the accuracy of the external feedback network, 1% feedback resistors are recommended.

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 3.0 V ≤ V_{IN} ≤ 6.0 V, -40 °C ≤ T_A ≤ 85 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SW1 Leakage Current (Standby and Shutdown modes)	I_{SW}	-10	-	10	µA
PVIN1 Pin Leakage Current (Shutdown Mode)	I_{PVIN1}	-10	-	10	µA
Error Amplifier DC Gain(14)	A_{EA}	-	150	-	dB
Error Amplifier Unit Gain Bandwidth(14)	$UGBW_{EA}$	-	3.0	-	MHz
Error Amplifier Slew Rate(14)	SR_{EA}	-	7.0	-	V/µs
Error Amplifier Input Offset(14)	$OFFSET_{EA}$	-3.0	0	3.0	mV
INV1 Pin Leakage Current	I_{INV1}	-1.0	-	1.0	µA
Thermal Shutdown Threshold(14)	T_{SDFET1}	-	170	-	°C
Thermal Shutdown Hysteresis(14)	$T_{SDHYFET1}$	-	25	-	°C
CHANNEL 2 BUCK CONVERTER (PVIN2, SW2, PGND2, BOOT2, INV2, COMP2, ILIM2)					
Channel 2 High-side MOSFET Drain Voltage Range	P_{VIN}	2.5	-	6.0	V
Output Voltage Adjustment Range(14)	V_{OUTHI2}	0.7	-	3.6	V
Output Voltage Accuracy(14),(15),(16)	-	-1.0	-	1.0	%
Line Regulation(14) (Normal Operation, V_{IN} = 3.0 to 6.0 V, I_{OUT2} = 2.5 A)	REG_{LN2}	-1.0	-	1.0	%
Load Regulation(14) (Normal Operation, I_{OUT2} = 0.0 to 5.0 A)	REG_{LD2}	-1.0	-	1.0	%
Error Amplifier Reference Voltage(14)	V_{REF2}	-	0.7	-	V
Output Under-voltage Threshold	V_{UVR2}	-8.0	-	-1.5	%
Output Over-voltage Threshold	V_{OVR2}	1.5	-	8.0	%
Continuous Output Current	I_{OUT2}	-	-	5.0	A
Over-current Limit	I_{LIM2}	-	6.5	-	A
Soft Start Adjusting Reference Voltage Range	V_{ILIM2}	1.25	-	V_{DDI}	V
Short-circuit Current Limit	I_{SHORT2}	-	8.5	-	A
High-side N-CH Power MOSFET (M6) $R_{DS(on)}$(14) (I_{OUT2} = 1.0 A, V_{BOOT2} - V_{SW2}= 3.3 V)	$R_{DS(on)HS2}$	10	-	50	mΩ
Low-side N-CH Power MOSFET (M7) $R_{DS(on)}$(14) (I_{OUT2} = 1.0 A, V_{IN} = 3.3 V)	$R_{DS(on)LS2}$	10	-	50	mΩ
M3 $R_{DS(ON)}$ (V_{IN} = 3.3 V, M3 is on)	$R_{DS(on)M3}$	2.0	-	4.0	Ω
SW2 Leakage Current (Standby and Shutdown modes)	I_{SW}	-10	-	10	A
PVIN2 Pin Leakage Current (Shutdown Mode)	I_{PVIN2}	-10	-	10	µA

Notes
14. Design information only, this parameter is not production tested.
15. This is directly affected by the accuracy of the external feedback network, 1% feedback resistors are recommended.
16. ±1% is assured at room temperature

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 3.0 V ≤ V_{IN} ≤ 6.0 V, -40 °C ≤ T_A ≤ 85 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Error Amplifier DC Gain[17]	A_{EA}	-	150	-	dB
Error Amplifier Unit Gain Bandwidth[17]	$UGBW_{EA}$	-	3.0	-	MHz
Error Amplifier Slew Rate[17]	SR_{EA}	-	7.0	-	V/µs
Error Amplifier Input Offset[17]	$OFFSET_{EA}$	-3.0	0	3.0	mV
INV2 Pin Leakage Current	I_{INV2}	-1.0	-	1.0	µA
Thermal Shutdown Threshold[17]	T_{SDFET2}	-	170	-	°C
Thermal Shutdown Hysteresis[17]	$T_{SDHYFET2}$	-	25	-	°C
OSCILLATOR (FREQ)					
Oscillator Frequency Adjusting Reference Voltage Range	V_{FREQ}	0.0	-	V_{DDI}	V
TRACKING (VREFIN, VOUT1, VOUT2)					
VREFIN External Reference Voltage Range[17]	V_{REFIN}	0.0	-	1.35	V
VOUT1 Total Discharge Resistance[17]	$R_{TDS(M8)}$	-	50	-	Ω
VOUT2 Total Discharge Resistance[17]	$R_{TDS(M9)}$	-	50	-	Ω
CONTROL AND SUPERVISORY ($\overline{SD}$, $\overline{PG}$)					
$\overline{SD}$ High Level Input Voltage	V_{SDHI}	2.0	-	-	V
$\overline{SD}$ Low Level Input Voltage	V_{SDLO}	-	-	0.4	V
$\overline{SD}$ Pin Internal Pull-up Resistor	R_{SDUP}	1.0	-	2.0	MΩ
$\overline{PG}$ Low Level Output Voltage (I_{PG} = 3.0 mA)	V_{PGLO}	-	-	0.4	V
$\overline{PG}$ Pin Leakage Current (M1 is off, Pulled up to VIN)	I_{PGLKG}	-1.0	-	1.0	µA

Notes

17. Design information only, this parameter is not production tested.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 3.0 V ≤ V_{IN} ≤ 6.0 V, -40 °C ≤ T_A ≤ 85 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CHANNEL 1 BUCK CONVERTER (PVIN1, SW1, PGND1, BOOT1, INV1, COMP1, ILIM1)					
Switching Node (SW1) Rise Time[18] (P_{VIN} = 3.3 V, I_{OUT1} = 5.0 A)	t_{RISE1}	-	8.0	-	ns
Switching Node (SW1) Fall Time[18] (P_{VIN} = 3.3 V, I_{OUT1} = 5.0 A)	t_{FALL1}	-	5.0	-	ns
Minimum OFF Time	t_{OFFMIN}	-	150	-	ns
Minimum ON Time	t_{ONMIN}	-	0[19]	-	ns
Soft Start Duration (Normal Mode)	t_{SS1}				ms
ILIM1: 1.25 to 1.49 V		-	3.2	-	
1.5 to 1.81 V		-	1.6	-	
1.82 to 2.13 V		-	0.8	-	
2.14 to 2.5 V		-	0.4	-	
Over-current Limit Timer	t_{LIM1}	-	10	-	ms
Over-current Limit Retry Timeout Period	$t_{TIMEOUT1}$	80	-	120	ms
Output Under-voltage/Over-voltage Filter Delay Timer	$t_{FILTER1}$	5.0	-	25	µs
CHANNEL 2 BUCK CONVERTER (PVIN2, SW2, PGND2, BOOT2, INV2, COMP2, ILIM2)					
Switching Node (SW2) Rise Time[18] (P_{VIN} = 3.3 V, I_{OUT2} = 5.0 A)	t_{RISE2}	-	28	-	ns
Switching Node (SW2) Fall Time[18] (P_{VIN} = 3.3 V, I_{OUT2} = 5.0 A)	t_{FALL2}	-	12.0	-	ns
Minimum OFF Time	t_{OFFMIN}	-	150	-	ns
Minimum ON Time	t_{ONMIN}	-	0[19]	-	ns
Soft Start Duration (Normal Mode)	t_{SS2}				ms
ILIM2: 1.25 to 1.49 V		-	3.2	-	
1.5 to 1.81 V		-	1.6	-	
1.82 to 2.13 V		-	0.8	-	
2.14 to 2.5 V		-	0.4	-	
Over-current Limit Timer	t_{LIM2}	-	10	-	ms
Over-current Limit Retry Timeout Period	$t_{TIMEOUT2}$	80	-	120	ms
Output Under-voltage/Over-voltage Filter Delay Timer	$t_{FILTER2}$	5.0	-	25	µs

Notes

18. Design information only, this parameter is not production tested.
19. The regulator has the ability to enter into pulse skip mode when the inductor current ripple reaches the threshold for the LS zero detect, which has a typical value of 500 mA.

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 3.0 V ≤ V_{IN} ≤ 6.0 V, -40 °C ≤ T_A ≤ 85 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR (FREQ)[20]					
Oscillator Default Switching Frequency (FREQ = GND)	F_{SW}	-	1.0	-	MHz
Oscillator Switching Frequency Range	F_{SW}	200	-	1000	kHz
CONTROL AND SUPERVISORY ($\overline{SD}$, $\overline{PG}$)					
$\overline{PG}$ Reset Delay	$t_{PGRESET}$	8.0	-	12	ms
Thermal Shutdown Retry Timeout Period[21]	$t_{TIMEOUT}$	80	-	120	ms

Notes
20. Oscillator frequency is ±10%
21. Design information only, this parameter is not production tested.

FUNCTIONAL DESCRIPTION

INTRODUCTION

Today's advanced systems are increasingly requiring more efficient and accurate power supplies. They present a set of challenges that include highly accurate voltage regulation, high current and fast transient response capability, voltage monitoring (power sequencing), and increased operating frequency. Point of Load power supplies offer adequate solutions to these challenges. They are non-isolated DC to DC converters that are located near their load and take their input voltage from an intermediate not, necessarily, regulated bus. their close proximity to the load is of a high importance with newer device requirements. While meeting the challenges, they allow for higher efficiency, localized protection, and minimum distribution losses. Their compact design and value makes them cost effective.

The 34717 is a PoL dual output power supply. Its integrated solution offers a cost effective system and reliable operation. It utilizes a voltage mode synchronous buck switching converter topology with integrated low $R_{DS(on)}$ (50 mΩ) N-channel power MOSFETs for higher efficiency operation. It provides an output voltage with an accuracy of less than ±2.0%, and capable of supplying up to 5.0 A of continuous current from both channels. The second output tracking abilities makes it ideal for systems with multiple related supply rails. It has a programmable switching frequency that allows for flexibility and optimization over the operating conditions and can operate at up to 1.0 MHz to significantly reduce the external components size and cost. It also provides the ability to program the over-current limit for both channels. It protects against output over-current, over-voltage, under-voltage, and over-temperature conditions. It also protects the system from short-circuit events. It incorporates a power good output signal to alert the host when a fault occurs.

It can be enabled and disabled by controlling the $\overline{SD}$ pin, which offers power sequencing capabilities.

By integrating the control/supervisory circuitry along with the Power MOSFET switches for the buck converter into a space-efficient package, the 34717 offers a complete, small-size, cost-effective, and simple solution to satisfy the needs of today's systems.

FUNCTIONAL PIN DESCRIPTION

BOOTSTRAP INPUT (BOOT1, BOOT2)

Bootstrap capacitor input pin. Connect a capacitor (as discussed in Bootstrap capacitor on page 23) between this pin and the SW pin of the respective channel to enhance the gate of the high-side Power MOSFET during switching.

POWER INPUT VOLTAGE (PVIN1, PVIN2)

Buck converter power input voltage. This is the drain of the buck converter high-side power MOSFET.

SWITCHING NODE (SW1, SW2)

Buck converter switching node. This pin is connected to the output inductor.

POWER GROUND (PGND1, PGND2)

Buck converter and discharge MOSFETs power ground. It is the source of the buck converter low-side power MOSFET.

COMPENSATION INPUT (COMP1, COMP2)

Buck converter external compensation network connects to this pin. Use a type III compensation network.

ERROR AMPLIFIER INVERTING INPUT (INV1, INV2)

Buck converter error amplifier inverting input. Connect the V_{DDQ} voltage (channel 1) to INV1 pin through a resistor divider and connect the V_{TT} voltage (channel 2) directly to INV2 pin.

INTERNAL SUPPLY VOLTAGE OUTPUT (VDDI)

This is the output of the internal bias voltage regulator. Connect a 1.0 µF, 6.0 V low ESR ceramic filter capacitor between this pin and the GND pin. Filtering any spikes on this output is essential to the internal circuitry stable operation.

SIGNAL GROUND (GND)

Analog ground of the IC. Internal analog signals are referenced to this pin voltage.

INPUT SUPPLY VOLTAGE (VIN)

IC power supply input voltage. Input filtering is required for the device to operate properly.

POWER GOOD OUTPUT SIGNAL ($\overline{PG}$)

This is an active low open drain output that is used to report the status of the device to a host. This output activates after a successful power up sequence and stays active as long as the device is in normal operation and is not experiencing any faults. This output activates after a 10 ms delay and must be pulled up by an external resistor to a supply voltage like V_{IN}.

SHUTDOWN INPUT ($\overline{SD}$)

If this pin is tied to the GND pin, the device will be in Shutdown mode. If left unconnected or tied to the VIN pin, the device will be in Normal mode. The pin has an internal pull-up of 1.5 MΩ.

REFERENCE VOLTAGE INPUT (VREFIN)

The output of channel two will track the voltage applied at this pin.

FREQUENCY ADJUSTMENT INPUT (FREQ)

The buck converters switching frequency can be adjusted by connecting this pin to an external resistor divider between VDDI and GND pins. The default switching frequency (FREQ pin connected to ground, GND) is set at 1.0 MHz.

SOFT START ADJUSTMENT INPUT (ILIM1, ILIM2)

Soft Start can be adjusted by applying a voltage between 1.25 V and VDDI on each ILIM pin.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION

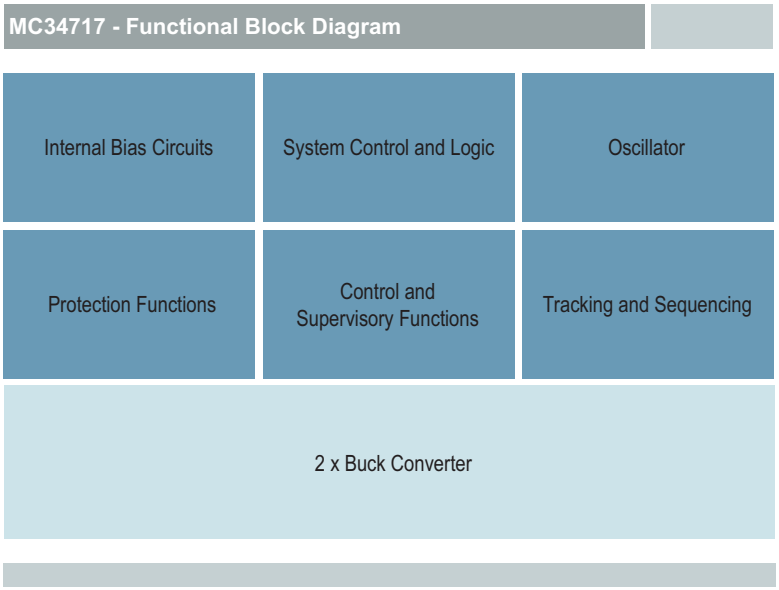


Figure 4. Block Illustration

INTERNAL BIAS CIRCUITS

This block contains all circuits that provide the necessary supply voltages and bias currents for the internal circuitry. It consists of:

- Internal voltage supply regulator: This regulator supplies the V_{DDI} voltage that is used to drive the digital/analog internal circuits. It is equipped with a Power-On-Reset (POR) circuit that watches for the right regulation levels. External filtering is needed on the VDDI pin. This block will turn off during the shutdown mode.
- Internal bandgap reference voltage: This supplies the reference voltage to some of the internal circuitry.
- Bias circuit: This block generates the bias currents necessary to run all of the blocks in the IC.

SYSTEM CONTROL AND LOGIC

This block is the brain of the IC where the device processes data and reacts to it. Based on the status of the $\overline{SD}$ pin, the system control reacts accordingly and orders the device into the right status. It also takes inputs from all of the monitoring/protection circuits and initiates power up or power down commands. It communicates with the buck converter to manage the switching operation and protects it against any faults.

OSCILLATOR

This block generates the clock cycles necessary to run the IC digital blocks. It also generates the buck converters switching frequency. The switching frequency can be programmed by connecting a resistor divider to the FREQ pin, between VDDI and GND pins (See Figure 1).

PROTECTION FUNCTIONS

This block contains the following circuits:

- Over-current limit and short-circuit detection: This block monitors the output of the buck converters for over-current conditions and short-circuit events and alerts the system control for further command.
- Thermal limit detection: This block monitors the temperature of the device for overheating events. If the temperature rises above the thermal shutdown threshold, this block will alert the system control for further commands.
- Output over-voltage and under-voltage monitoring: This block monitors the buck converters output voltages to ensure they are within regulation boundaries. If not, this block alerts the system control for further commands.

CONTROL AND SUPERVISORY FUNCTIONS

This block is used to interface with an outside host. It contains the following circuits.

- Shutdown control input: An outside host can put the 34717 device into shutdown mode by sending a logic “0” to the $\overline{SD}$ pin.
- Power good output signal: The 34717 can communicate to an outside host that a fault has occurred by pulling the voltage on the $\overline{PG}$ pin high.

TRACKING AND SEQUENCING

This block allows the second output of the 34717 to track the voltage applied at the VREFIN pin in different tracking configurations. This will be discussed in further details later in this document. For power down during a shutdown mode, the 34717 uses internal discharge MOSFETs (M8 and M9 on Figure 2, page 2) to discharge the first and second output respectively. The discharge MOSFETs are only active during shutdown mode. Using this block along with controlling the $\overline{SD}$ pin can offer the user power sequencing capabilities by controlling when to turn the 34717 outputs on or off.

BUCK CONVERTER

This block provides the main function of the 34717: DC to DC conversion from an un-regulated input voltage to a regulated output voltage used by the loads for reliable operation. The buck converter is a high performance, fixed frequency (externally adjustable), synchronous buck PWM voltage-mode control. It drives integrated 50mΩ N-channel power MOSFETs saving board space and enhancing efficiency. The switching regulator output voltage is adjustable with an accuracy of less than ±2% to meet today’s requirements. The second channel’s output has the ability to track the voltage applied at the VREFIN pin. The regulator's voltage control loop is compensated using a type III compensation network, with external components to allow for optimizing the loop compensation, for a wide range of operating conditions. A typical Bootstrap circuit with an internal PMOS switch is used to provide the voltage necessary to properly enhance the high-side MOSFET gate.

The 34717 has the ability to supply up to 5.0 A of continuous current from each channel, making it suitable for many high current applications.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

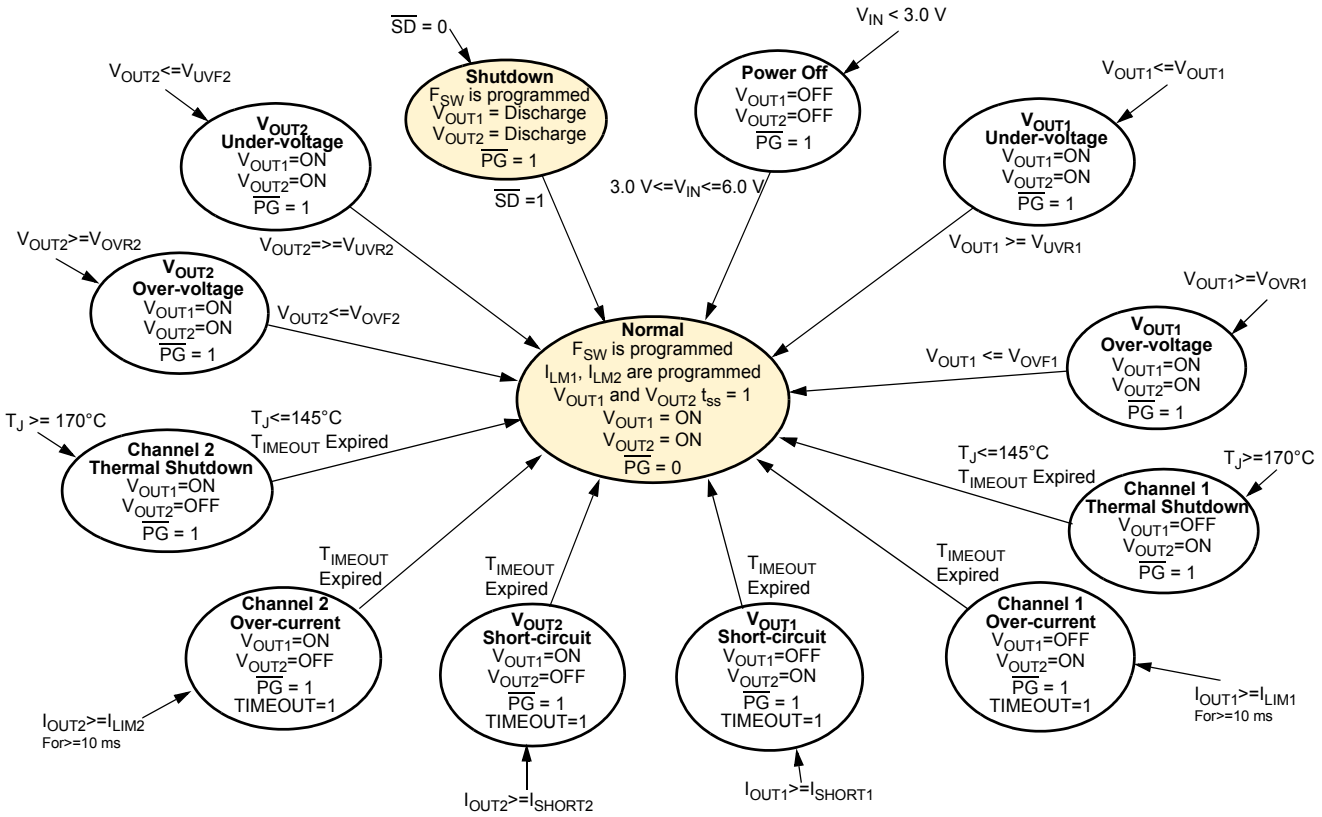


Figure 5. Operation Modes Diagram

MODES OF OPERATION

The 34717 has two primary modes of operation:

Normal Mode

In Normal mode, all functions and outputs are fully operational. To be in this mode, the V_{IN} needs to be within its operating range, Shutdown input is high, and no faults are present. This mode consumes the most amount of power.

Shutdown Mode

In this mode, activated by pulling the $\overline{SD}$ pin low, the chip is in a shutdown state and the output is disabled and discharged. In this mode, the 34717 consumes the least amount of power since almost all of the internal blocks are disabled.

START-UP SEQUENCE

When power is first applied, the 34717 checks the status of the $\overline{SD}$ pin. If the device is in a shutdown mode, no block will power up and the output will not attempt to ramp. Once the $\overline{SD}$ pin is set to high, the V_{DDI} internal supply voltage and the bias currents will be established, so the internal V_{DDI} POR signal can be released. The rest of the internal blocks will be enabled and the buck converter switching frequency and soft start timing values are determined by reading the FREQ, ILIM1, and ILIM2 pins. A soft start cycle is then initiated to ramp up the output of the buck converter. The first channel uses an internal 0.7 V reference for its error amplifier while the second channel's error amplifier uses the voltage on the VREFIN pin as its reference voltage until V_{REFIN} is equal to 0.7 V, then the error amplifier defaults to the internal 0.7 V reference voltage. This method allows the second output to achieve multiple tracking configurations as will be explained later in this document.

Soft start is used to prevent the output voltage from overshooting during startup. At initial startup, the output capacitor is at zero volts; V_{OUT} = 0 V. Therefore, the voltage across the inductor will be PV_{IN} during the capacitor charge phase which will create a very sharp di/dt ramp. Allowing the inductor current to rise too high can result in a large difference between the charging current and the actual load current that can result in an undesired voltage spike once the capacitor is fully charged. The soft start is active each time the IC goes out of standby or shutdown mode, power is recycled, or after a fault retry.

After a successful start-up cycle where the device is enabled, no faults have occurred, and the output voltage has reached its regulation point, the 34717 pulls the power good output signal low after a 10 ms reset delay, to indicate to the host that the device is in normal operation.

PROTECTION FUNCTIONS

The 34717 monitors the application for several fault conditions to protect the load from overstress. The reaction of the IC to these faults ranges from turning off the outputs to just alerting the host that something is wrong. In the following paragraphs, each fault condition is explained:

Output Over-voltage

An over-voltage condition occurs once the output voltage goes higher than the rising over-voltage threshold (V_{OVR}). In this case, the power good output signal is pulled high, alerting the host that a fault is present, but the output will stay active. To avoid erroneous over-voltage conditions, a 20 µs filter is implemented. The buck converter will use its feedback loop to attempt to correct the fault. Once the output voltage falls below the falling over-voltage threshold (V_{OVF}), the fault is cleared and the power good output signal is pulled low, the device is back in normal operation.

Output Under-voltage

An under-voltage condition occurs once the output voltage falls below the falling under-voltage threshold (V_{UVF}). In this case, the power good output signal is pulled high, alerting the host that a fault is present, but the output will stay active. To avoid erroneous under-voltage conditions, a 20 µs filter is implemented. The buck converter will use its feedback loop to attempt to correct the fault. Once the output voltage rises above the rising under-voltage threshold (V_{UVR}), the fault is cleared and the power good output signal is pulled low, the device is back in normal operation.

Output Over-current

This block detects over-current in the Power MOSFETs of the buck converter. It is comprised of a sense MOSFET and a comparator. The sense MOSFET acts as a current detecting device by sampling a ratio of the load current. That sample is compared via the comparator with an internal reference to determine if the output is in over-current or not. If the peak current in the output inductor reaches the over current limit (I_{LIM}), the converter will start a cycle-by-cycle operation to limit the current, and a 10 ms over-current limit timer (t_{LIM}) starts. The converter will stay in this mode of operation until one of the following occurs:

- The current is reduced back to the normal level before t_{LIM} expires, and in this case normal operation is regained.
- t_{LIM} expires without regaining normal operation, at which point the device turns off the output and the power good output signal is pulled high. At the end of a time-out period of 100 ms ($t_{TIMEOUT}$), the device will attempt another soft start cycle.
- The device reaches the thermal shutdown limit (T_{SDFET}) and turns off the output. The power good output signal is pulled high.
- The output current keeps increasing until it reaches the short-circuit current limit (I_{SHORT}). See below for more details.

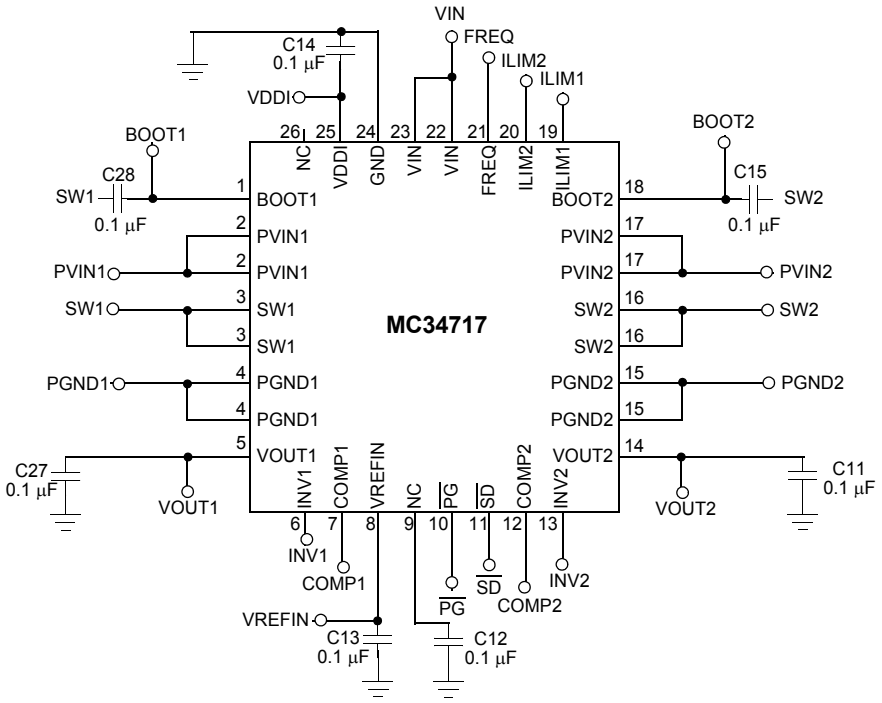
Short-circuit Current Limit

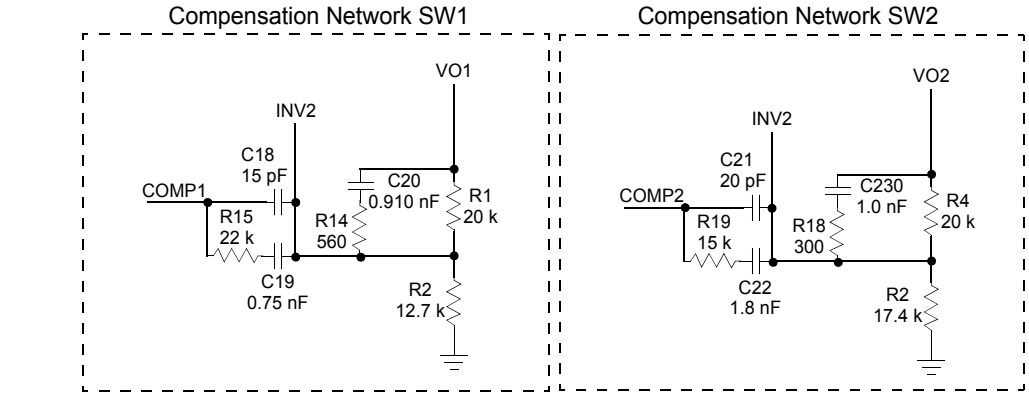
This block uses the same current detection mechanism as the over-current limit detection block. If the load current reaches the I_{SHORT} value, the device reacts by shutting down the output immediately. This is necessary to prevent damage in case of a permanent short-circuit. Then, at the end of a timeout period of 100 ms ($t_{TIMEOUT}$), the device will attempt another soft start cycle.

Thermal Shutdown

Thermal limit detection block monitors the temperature of the device and protects against excessive heating. If the temperature reaches the thermal shutdown threshold (T_{SDFET}), the converter output switches off and the power good output signal indicates a fault by pulling high. The device will stay in this state until the temperature has decreased by the hysteresis value and then After a timeout period ($t_{TIMEOUT}$) of 100 ms, the device will retry automatically and the output will go through a soft start cycle. If successful normal operation is regained, the power good output signal is asserted low to indicate it.

TYPICAL APPLICATIONS





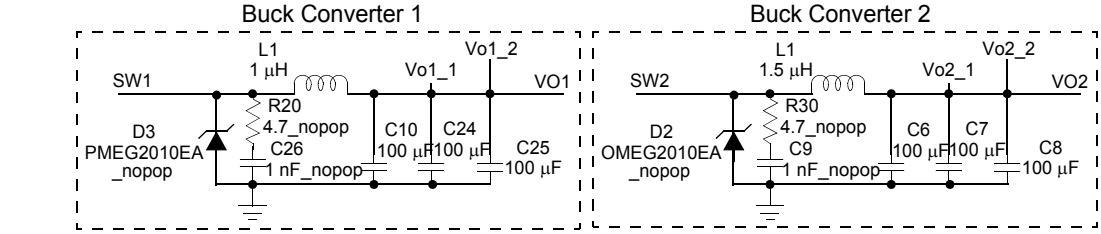


Figure 6. 34717 Typical Application

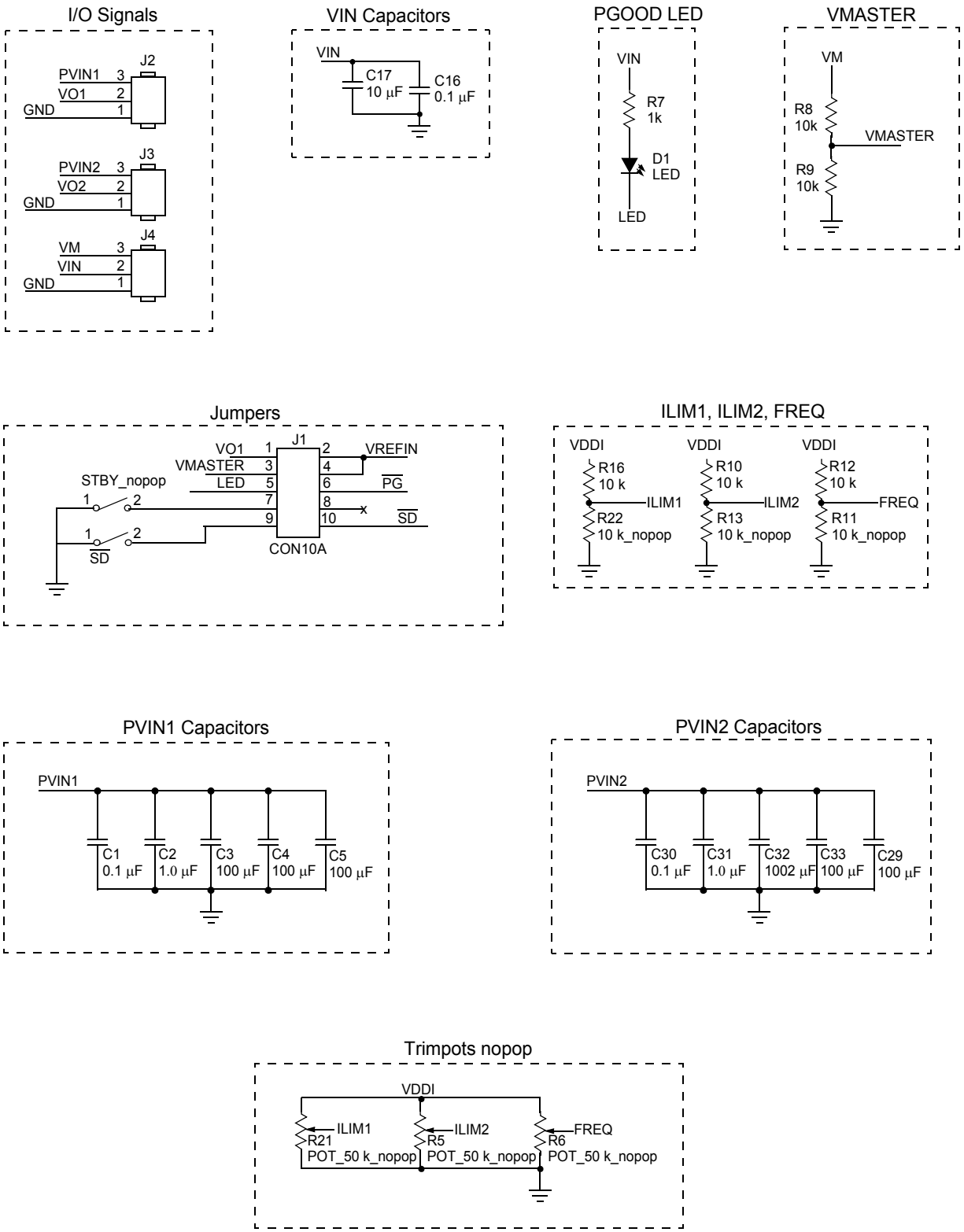


Figure 7. 34717 Typical Application

CONFIGURING THE OUTPUT VOLTAGE:

Both channels for the 34717 are general purpose DC-DC converters. The resistor divider to the INV node is responsible for setting the output voltage. The equation is:

$$V_{OUT} = V_{REF}\left(\frac{R1}{R2}+1\right)$$

For channel 1: $V_{REF}=V_{BG}=0.7V$.

For channel 2: The second channel of the 34717 has an internal reference selector, thus V_{REF} can be either the voltage at VREFIN pin or the internal reference voltage V_{BG}. The reference value is given by the following condition: V_{REF}=VREFIN if VREFIN is less than V_{BG}=0.7 V. Otherwise, $V_{REF}=V_{BG}$. Usually the output regulation voltage is calculated using the internal reference V_{BG}, and the condition V_{REF}=VREFIN is used for tracking purposes.

SWITCHING FREQUENCY CONFIGURATION

The switching frequency will have a value of 1.0MHz by connecting the FREQ pin to the GND. If the smallest frequency value of 200 kHz is desired, then connect the FREQ pin to VDDI. To program the switching frequency to another value, an external resistor divider must be connected to the FREQ pin to achieve the voltages given by Table 5.

Table 5. Frequency Selection

FREQUENCY	VOLTAGE APPLIED TO PIN FREQ
200	2.341 – 2.500
253	2.185 - 2.340
307	2.029 - 2.184
360	1.873 - 2.028
413	1.717 – 1.872
466	1.561 – 1.716
520	1.405 - 1.560
573	1.249 - 1.404
627	1.093 - 1.248
680	0.936 - 1.092
733	0.781 - 0.936
787	0.625 - 0.780
840	0.469 - 0.624
893	0.313 - 0.468
947	0.157 - 0.312
1000	0.000 - 0.156

SOFT START ADJUSTMENT

Table 6 shows the voltage that should be applied to the ILIM1and ILIM2 pins to get the desired soft start timing.

Table 6. Soft Start Configurations

SOFT START [MS]	VOLTAGE APPLIED TO ILIM
3.2	1.19 - 1.49 V
1.6	1.50 - 1.81 V
0.8	1.82 - 2.13 V
0.4	2.14 - 2.50 V

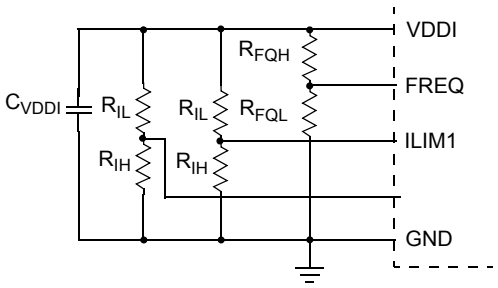


Figure 8. Resistor Divider for Frequency and Soft Start Adjustment

SELECTING INDUCTOR

The Inductor calculation process is the same for both Channels. The equation is the following:

$$L = D'_{MAX} * T * \frac{(V_{OUT} + I_{OUT} * (Rds(on)\_ls + r\_w))}{\Delta I_{OUT}}$$

$D'_{MAX} = 1 - \frac{V_{OUT}}{Vin\_\max}$	Maximum Off Time Percentage
T	Switching Period
$Rds(on)\_ls$	Drain – to – Source Resistance of FET
r_w	Winding Resistance of Inductor
ΔI_{OUT}	Output Current Ripple

SELECTING THE OUTPUT FILTER CAPACITOR

The following considerations are most important for the output capacitor, and not the actual Farad value: the physical size, the ESR of the capacitor, and the voltage rating.

Calculate the minimum output capacitor using the following formula:

$$Co = \frac{I_{OUT} * dt\_I\_rise}{TR\_V\_dip}$$

Transient Response percentage:

TR_%

(Use a recommended value of 2 to 4% to assure a good transient response.)

Maximum Transient Voltage:

TR_V_dip = V_{OUT}*TR_%

Maximum Current Step:

$$\Delta Iout\_step = \frac{(Vin\_\min - Vout) * D\_\max}{Fsw * L}$$

Inductor Current Rise Time:

$$dt\_I\_rise = \frac{T * I_{OUT}}{\Delta I_{OUT}\_step}$$

The following formula is helpful to find the maximum allowed ESR.

$$ESR_{\max} = \frac{\Delta V_{OUT} * Fsw * L}{V_{OUT}(1 - D\min)}$$

The effects of the ESR is often neglected by the designers and may present a hidden danger to the ultimate supply stability. Poor quality capacitors have a widely disparate ESR value, which can make the closed loop response inconsistent.

BOOTSTRAP CAPACITOR

The bootstrap capacitor is needed to supply the gate voltage for the high-side MOSFET. This N-Channel MOSFET needs a voltage difference between its gate and source to be able to turn on. The high-side MOSFET source is the SW node, so it is not at ground and it is floating and shifting in voltage. We cannot just apply a voltage directly to the gate of the high-side that is referenced to ground. We need a voltage referenced to the SW node. This is why the bootstrap capacitor is needed. This capacitor charges during the high- side off time. The low-side will be on during that time. The SW node and the bottom of the bootstrap capacitor will be connected to ground, and the top of the capacitor will be connected to a voltage source. The capacitor will charge up to that voltage source (for example 5.0 V). Now when the low- side MOSFET switches off and the high-side MOSFET switches on, the SW nodes will rise to V_{IN}, and the voltage on the boot pin will be V_{CAP} + V_{IN}. The gate of the high-side will have V_{CAP} across it and it will be able to stay enhanced. A 0.1 μF capacitor is a good value for this bootstrap element.

TYPE III COMPENSATION NETWORK

Power supplies are desired to offer accurate and tight regulation output voltages. A high DC gain is required to accomplish this, but with high gain comes the possibility of instability. The purpose of adding compensation to the internal error amplifier is to counteract some of the gains and phases contained in the control-to-output transfer function that could jeopardized the stability of the power supply. The Type III compensation network used for the 34717 comprises two poles (one integrator and one high frequency to cancel the zero generated from the ESR of the output capacitor) and two zeros to cancel the two poles generated from the LC filter as shown in Figure 9.

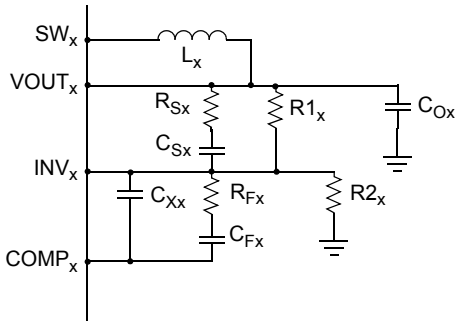


Figure 9. Type III compensation network

1. Choose a value for R1
2. Consider a Crossover frequency of one tenth of the switching frequency, set the Zero pole frequency to Fcross/10

$$F_{P0} = \frac{1}{10} F_{CROSS} = \frac{1}{2\pi * R_1 C_F}$$

$$C_F = \frac{1}{2\pi * R_1 F_{PO}}$$

3. Knowing the LC frequency, the Frequency of Zero 1 and Zero 2 in the compensation network are equal to F_{LC}

$$F_{LC} = \frac{1}{2\pi\sqrt{L_X Co_X}} = F_{Z1} = F_{Z2}$$

$$F_{Z1} = \frac{1}{2\pi * R_F C_F} \qquad F_{Z2} = \frac{1}{2\pi * R_1 C_S}$$

This gives the result

$$R_F = \frac{1}{2\pi * C_F F_{Z1}} \qquad C_S = \frac{1}{2\pi * R_1 F_{Z2}}$$

4. Calculate R_S by placing the first pole at the ESR zero frequency

$$F_{ESR} = \frac{1}{2\pi * Co_X * ESR} = F_{P1}$$

$$F_{P1} = \frac{1}{2\pi * R_S C_S} \rightarrow R_S = \frac{1}{2\pi * F_{P1} C_S}$$

5. Equating pole 2 to 5 times the Crossover Frequency achieves a faster response and a proper phase margin

$$5 \bullet F_{CROSS} = F_{P2} = \frac{1}{2\pi \bullet R_F \frac{C_F C_X}{C_F + C_x}} \rightarrow$$

$$C_X = \frac{C_F}{2\pi * R_F C_F F_{P2} - 1}$$

TRACKING CONFIGURATIONS.

This device allows two tracking configurations: Ratiometric and Co-incidental Tracking.

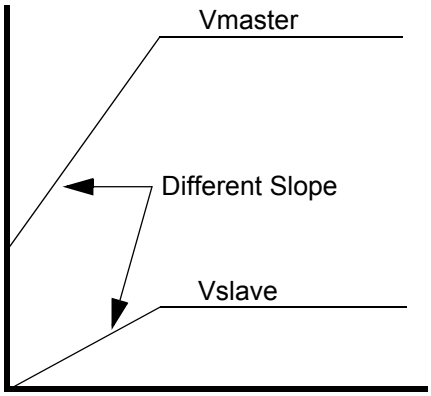


Figure 10. Ratiometric Tracking

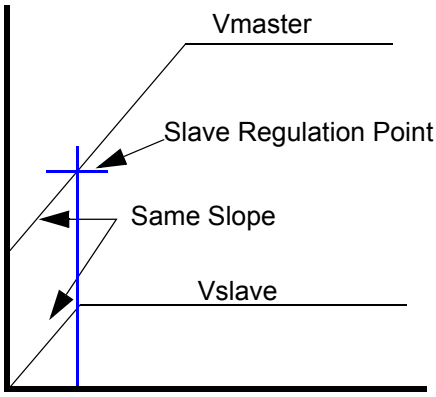


Figure 11. Co-incidental Tracking

RATIOMETRIC TRACKING CIRCUIT CONFIGURATION

The master voltage feedback resistor divider network is used in place of R_3 and R_4 as shown in Figure 12. The slave output is connected through its own feedback resistor divider network to the INV- pin, resistors R_1 and R_2. All four resistors will affect the accuracy of the system and must be 1% accurate resistors.

To achieve this tracking configuration, the master voltage must be connected in the way shown and cannot be directly connected to the VREFIN pin.

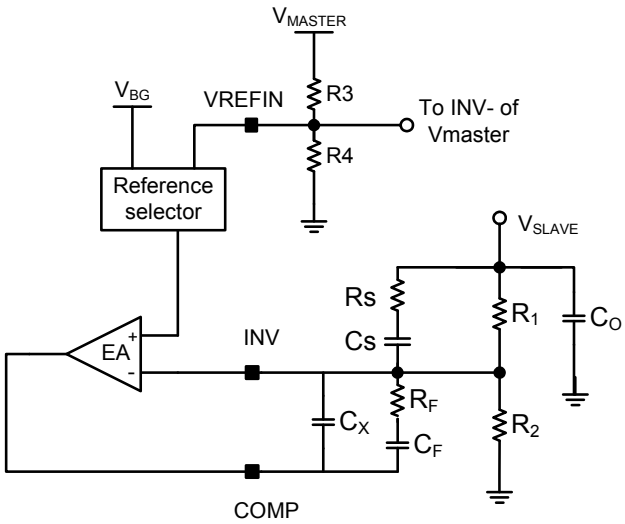


Figure 12. Ratiometric Tracking Circuit Connections

EQUATIONS

- $V_M = V_{BG\_M}(1+R_3/R_4)$
- $V_{REFIN} = V_M * R_4/(R_3+R_4)$
- $V_{REFOUT} = V_{REFIN}$
- $V_S = V_{REFOUT}(1+R_1/R_2) = V_M * R_4/(R_3+R_4)*(R_2+R_1)/R_2$, if $V_{REFOUT} < V_{BG\_S}$
- $V_S = V_{BG\_S}(1+R_1/R_2)$, if $V_{REFOUT} \geq V_{BG\_S}$

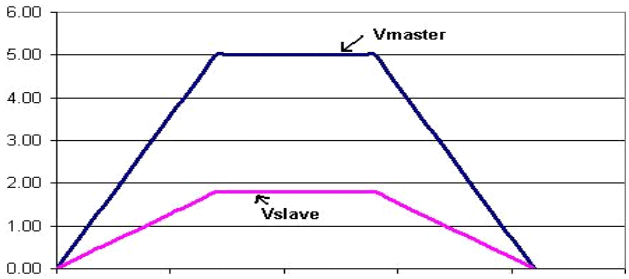


Figure 13. Ratiometric Tracking Plot

CO-INCIDENTAL TRACKING CIRCUIT CONFIGURATION:

Connect a three resistor divider to the master voltage (V_M) and Route the upper tap point of the divider to the VREFIN pin, resistors R_3, R_4, and R_5 as shown in Figure 14. This resistor divider must be the same ratio as the slave output's (V_S) feedback resistor divider, which in turn connects to the INV- pin, resistors R_1 and R_2 below (**Condition: $R_1 = R_3$ and $R_2 = R_4 + R_5$**). The master's feedback resistor divider would be (R_3+R_4) and R_5. All five resistors will affect the accuracy of the system and must be 1% accurate resistors.

To achieve this tracking configuration, the master voltage must be connected in the way shown and cannot be directly connected to the VREFIN pin.

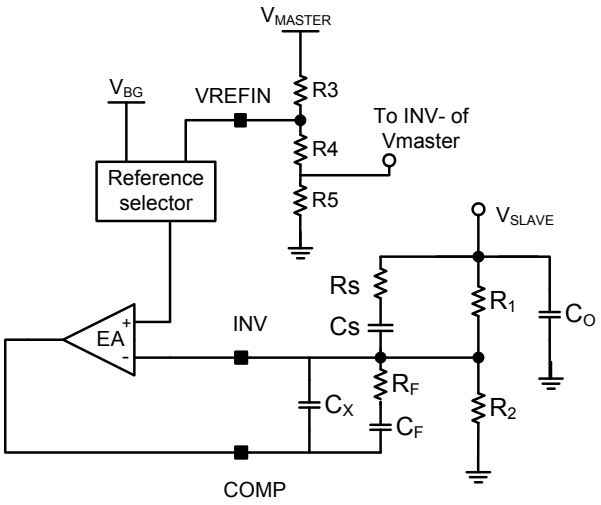


Figure 14. Co-incidental Tracking Circuit Connections

EQUATIONS

- $V_M = V_{BG\_M}[1+(R_3+R_4)/R_5]$
- $V_{REFIN} = V_M*(R_4+R_5)/(R_3+R_4+R_5)$
- $V_{REFOUT} = V_{REFIN}$
- $V_S = V_{REFOUT}(1+R_1/R_2) = V_M*(R_4+R_5)/(R_3+R_4+R_5)*(R_2+R_1)/R_2 = V_M$ if $V_{REFOUT} < V_{BG\_S}$
- $V_S = V_{BG\_S}(1+R_1/R_2)$, if $V_{REFOUT} \geq V_{BG\_S}$

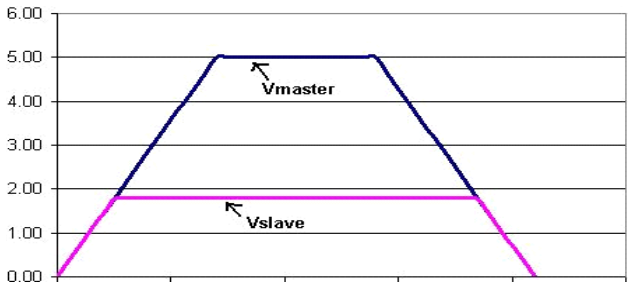


Figure 15. Co-incidental Tracking Plot

Not-DDR Mode (Source Only Mode) is the case when no tracking is needed. VREFIN should be connected to VDDI and the reference selection block will use the internal band gap voltage as the error amplifier's reference voltage.

A user can potentially apply a voltage to the VREFIN pin directly or through a resistor divider to get a buffered output for use in the application. The condition here is, the voltage applied to the VREFIN pin is greater than V_{BG} to guarantee that the reference selection block will not switch back to the V_{REFOUT} voltage.

LAYOUT GUIDELINES

The layout of any switching regulator requires careful consideration. First, there are high di/dt signals present, and the traces carrying these signals need to be kept as short and as wide as possible to minimize the trace inductance, and therefore reduce the voltage spikes they can create. To do this, an understanding of the major current carrying loops is important. See Figure 16. These loops, and their associated components, should be placed in such a way as to minimize the loop size to prevent coupling to other parts of the circuit. Also, the current carrying power traces and their associated return traces should run adjacent to one another, to minimize the amount of noise coupling. If sensitive traces must cross the current carrying traces, they should be made perpendicular to one another to reduce field interaction.

Second, small signal components which connect to sensitive nodes need consideration. The critical small signal components are the ones associated with the feedback circuit. The high impedance input of the error amp is especially sensitive to noise, and the feedback and compensation components should be placed as far from the switch node, and as close to the input of the error amplifier as possible. Other critical small signal components include the bypass capacitors for VIN, VREFIN, and VDDI. Locate the bypass capacitors as close to the pin as possible.

The use of a multi-layer printed circuit board is recommended. Dedicate one layer, usually the layer under the top layer, as a ground plane. Make all critical component ground connections with vias to this layer. Make sure that the power grounds, PGND1 and PGND2 are connected directly to the ground plane and not routed through the thermal pad or analog ground. Dedicate another layer as a power plane and split this plane into local areas for common voltage nets.

The IC input supply (VIN) should be connected with a dedicated trace to the input supply. This will help prevent noise on the buck regulator's power inputs (PVIN1 and PVIN2) from injecting switching noise into the IC's analog circuitry.

In order to effectively transfer heat from the top layer to the ground plane and other layers of the printed circuit board, thermal vias need to be used in the thermal pad design. It is recommended that 5 to 9 vias be spaced evenly and have a finished diameter of 0.3 mm.

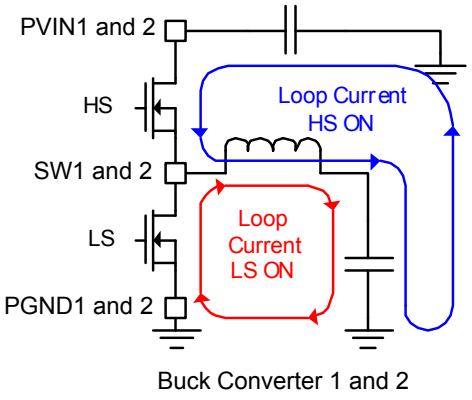
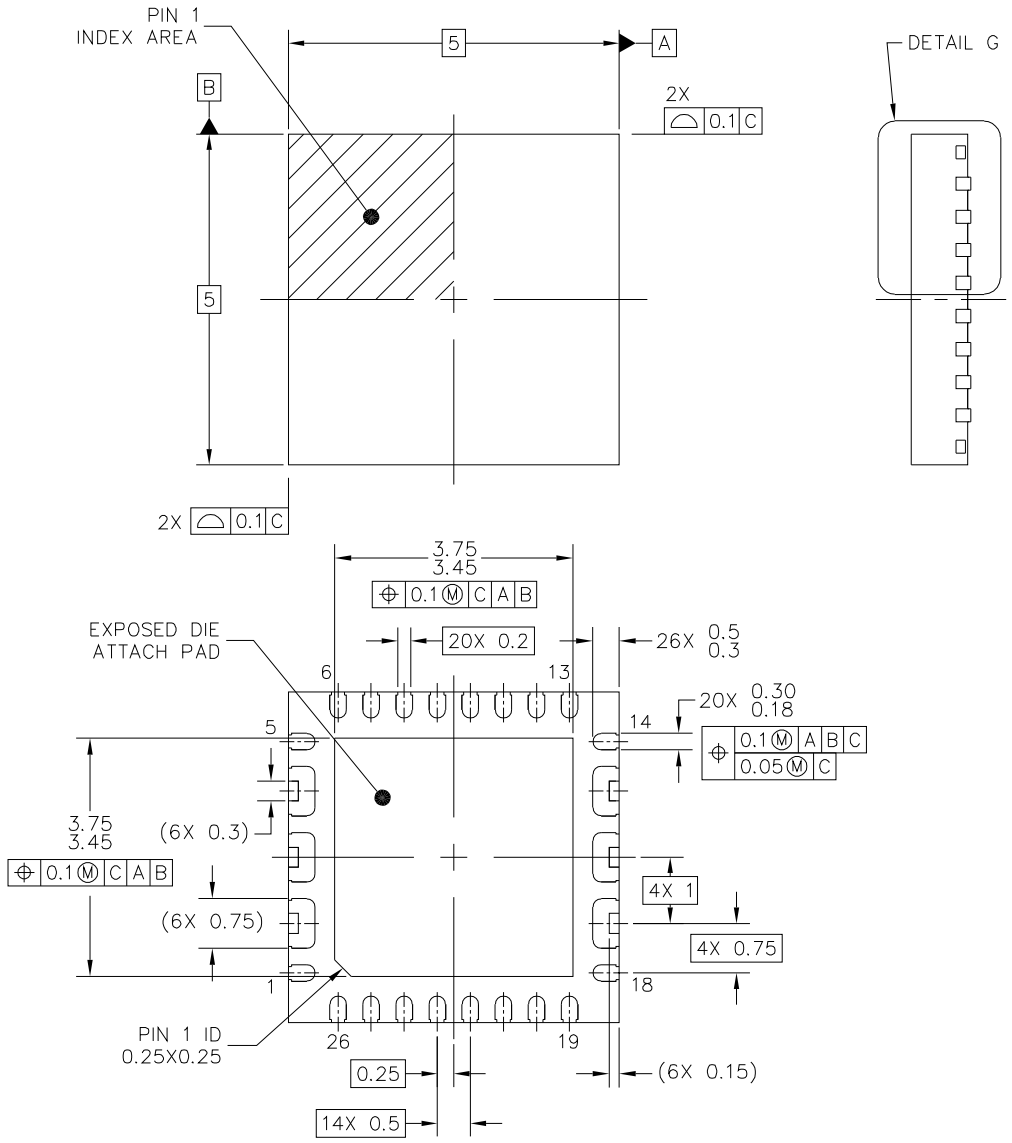


Figure 16. Current Loop

PACKAGING

PACKAGING DIMENSIONS



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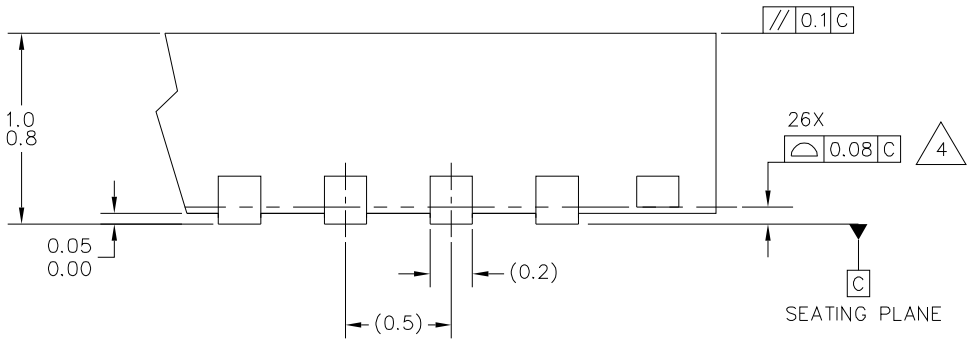

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3. THIS IS A NON–JEDEC REGISTERED PACKAGE.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
5. MIN. METAL GAP SHOULD BE 0.2 MM.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: QFN, THERMALLY ENHANCED, 5 X 5 X 0.9, 0.5 PITCH, 26 TERMINAL	DOCUMENT NO: 98ASA00702D	REV: O
	STANDARD: NON–JEDEC	
	01 APR 2014	

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
1.0	2/2006	• Pre-release version • Implemented Revision History page
2.0	1/2007	• Initial release • Converted format from Market Assessment to Product Preview • Major updates to the data, form, and style
3.0	5/2007	• Changed Feature from 2% to 1%, relabeled to include soft start • Change references for 45 mΩ Integrated N-Channel Power MOSFETs to 50 mΩ • Removed Machine Model in Maximum Ratings • Added Channel 1 High-side MOSFET Drain Voltage Range • Changed Output Voltage Accuracy(12),(13) • Changed Soft Start Adjusting Reference Voltage Range and Short-circuit Current Limit • Changed High-side N-CH Power MOSFET (M4) RDS(on)(12) and Low-side N-CH Power MOSFET (M5) RDS(on)(12) • Changed M2 RDS(ON) and PVIN1 Pin Leakage Current • Added Channel 2 High-side MOSFET Drain Voltage Range • Changed Soft Start Adjusting Reference Voltage Range • Changed Short-circuit Current Limit • Changed High-side N-CH Power MOSFET (M6) RDS(on)(14) and Low-side N-CH Power MOSFET (M7) RDS(on)(14) • Changed M3 RDS(ON) and PVIN2 Pin Leakage Current • Changed SD Pin Internal Pull-up Resistor • Changed Channel 1 Soft Start Duration (Normal Mode), Over-current Limit Retry Timeout Period, and Output Under-voltage/Over-voltage Filter Delay Timer • Changed Channel 2 Soft Start Duration (Normal Mode), Over-current Limit Retry Timeout Period, and Output Under-voltage/Over-voltage Filter Delay Timer • Changed Oscillator Default Switching Frequency • Changed PG Reset Delay and Thermal Shutdown Retry Timeout Period(21) • Changed definition for Soft Start ADJUStment input (ILIM1, ILIM2) • Changed drawings in 34717 Typical Application • Changed table for Soft Start Adjustment • Removed PC34717EP/R2 from the ordering information and added MC34717EP/R2 • Changed data sheet status to Advance Information
4.0	12/2008	• Made changes to Switching Node (SW1, SW2) Pins, BOOT1, BOOT2 Pins (Referenced to SW1, SW2 Pins Respectively), Output Under-voltage Threshold, Output Over-voltage Threshold, Both channels of High-side N-CH Power MOSFET (M4) RDS(on)(12), Both channels of Low-side N-CH Power MOSFET (M5) RDS(on)(12), Charge Device Model • Added Machine Model (MM), Both channels of SW2 Leakage Current (Standby and Shutdown modes), Both channels of (Error Amplifier DC Gain(14), Error Amplifier Unit Gain Bandwidth(14), Error Amplifier Slew Rate(14), Error Amplifier Input Offset(14)) • Fixed drawing for Type III compensation network • Added pin 27 to Figure 3 and the 34717 Pin Definitions • Added the section Layout Guidelines
5.0	12/2014	• Updated case outline (changed 98ASA10728D to 98ASA00702D) as per PCN 16331

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