CBTL04GP043

Dual 2 x 2 differential channel crossbar switch

Rev. 1.1 — 27 July 2015 Product data sheet

1. General description

The CBTL04GP043 is a high-performance 4-channel bidirectional crossbar switch supporting both high speed and large swing signals. The high-speed differential signals include PCIe-Gen3, USB3 and DisplayPort. The large swing signals include UART, USB 2.0 and HDMI 1.4 signals.

This chip can be configured as pair straight through or cross to the output ports through the CROSS signal. It can be placed under Low-power mode using the XSDN pin.

This crossbar switch supports wide common-mode voltage range from 0 V to V_{DD} on all input and output ports.

CBTL04GP043 is available in 2.00 mm × 4.00 mm × 0.5 mm XFBGA28 package with 0.5 mm pitch.

2. Features and benefits

- 4-channel, bidirectional crossbar switch
- The input of the CROSS pin
  - CROSS is LOW for connecting input and output ports straight through
  - CROSS is HIGH for crossbar connection between input and output ports
- When XSDN is LOW, the switch is in low-power sleep mode
- Low ON-state resistance: 11 Ω (typical)
- Bandwidth: 8.5 GHz (typical) for V_{IC} = 2.2 V
- Low insertion loss: −1.5 dB at 2.5 GHz; −1 dB at 100 MHz
- Low return loss: −20 dB at 2.5 GHz
- Low off-state isolation: −16 dB at 2.5 GHz; −40 dB at 100 MHz
- Low DDNEXT crosstalk: −20 dB at 2.5 GHz
- V_{IC} common-mode input voltage V_{IC}: 0 V to V_{DD}
- Differential input voltage V_{ID}: 1.4 V (maximum)
- Intra-pair skew: 5 ps (typical)
- Supports power supply voltage range from 2.7 V to 3.5 V
- Back current protection on all I/O pins of these switches
- All channels support rail-to-rail input voltage
- XFBGA28 2 mm × 4 mm × 0.5 mm package with 0.5 mm pitch
- ESD: 2000 V HBM; 750 V CDM
- Operating temperature range: −20 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
CBTL04GP043EX	GP43* [1]	XFBGA28	plastic, extremely thin fine-pitch ball grid array package; 28 balls; body 2.00 × 4.00 × 0.5 mm; 0.5 mm pitch	SOT1356-1

[1] '*' changes based on date code.

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
CBTL04GP043EX	CBTL04GP043EXJ	XFBGA28	Reel 13" Q1/T1 *standard mark SMD	7000	T_{amb} = −20 °C to +85 °C

4. Block diagram

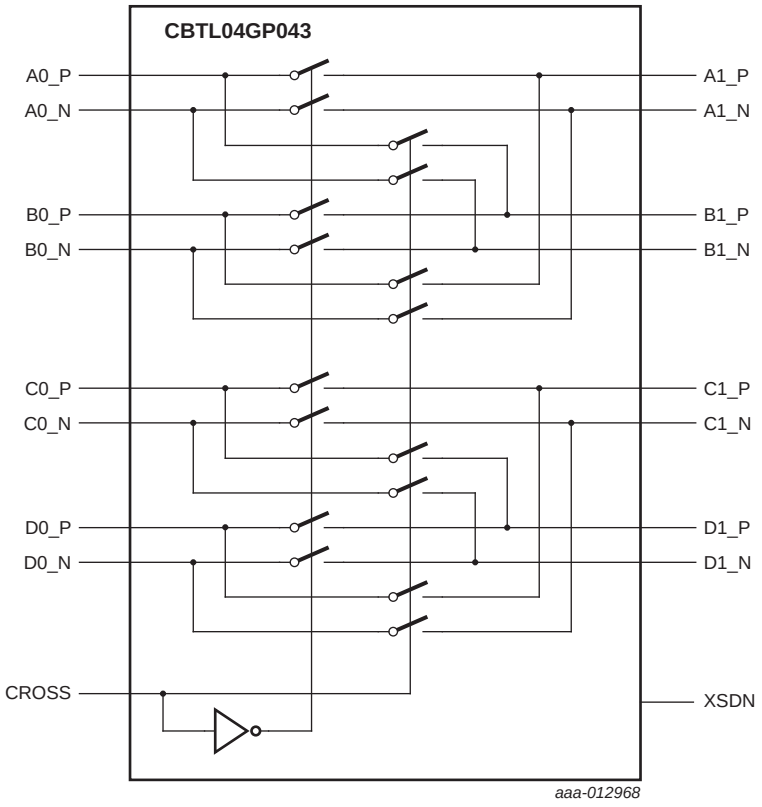
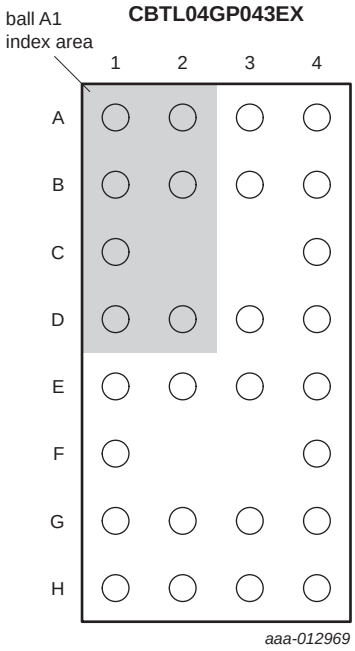


Fig 1. Block diagram of CBTL04GP043

5. Pinning information

5.1 Pinning



Transparent top view

a. Pin configuration

	1	2	3	4
A	A1_P	B1_P	D1_P	C1_P
B	A1_N	B1_N	D1_N	C1_N
C	CROSS			V_{DD}
D	n.c.	n.c.	n.c.	n.c.
E	n.c.	n.c.	n.c.	n.c.
F	V_{SS}			XSDN
G	A0_P	B0_P	C0_P	D0_P
H	A0_N	B0_N	C0_N	D0_N

Transparent top view

An empty cell indicates no ball is populated at that grid point.

n.c. = ball present, but not internally connected.

aaa-013489

b. Ball mapping

Fig 2. Pin configuration for XFBGA28

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
Data path signals			
A1_P	A1	I/O	Port A1
A1_N	B1	I/O	
B1_P	A2	I/O	Port B1
B1_N	B2	I/O	
C1_P	A4	I/O	Port C1
C1_N	B4	I/O	
D1_P	A3	I/O	Port D1
D1_N	B3	I/O	
A0_P	G1	I/O	Port A0
A0_N	H1	I/O	
B0_P	G2	I/O	Port B0
B0_N	H2	I/O	
C0_P	G3	I/O	Port C0
C0_N	H3	I/O	
D0_P	G4	I/O	Port D0
D0_N	H4	I/O	
Control signals			
CROSS	C1	CMOS input	When CROSS = HIGH, selects cross function. When CROSS = LOW, selects pass-through function. CROSS input must be LOW for more than 500 μs during start up time.
XSDN	F4	CMOS input	When XSDN = HIGH, enables XBAR switches. When XSDN = LOW, all switches are 3-stated.
Power supply			
V_{DD}	C4	power	Power supply range from 3.0 V to 3.5 V.
Ground connection			
V_{SS}	F1	ground	Supply ground (0 V).
n.c.	D1, D2, D3, D4, E1, E2, E3, E4	-	Not connected. These balls should be connected to solid ground plane on PCB to improve signal integrity.

6. Functional description

Refer to Figure 1 “Block diagram of CBTL04GP043”.

When CROSS input is LOW, Port 0 pins are connected to their respective Port 1 pins. When CROSS input is HIGH, Port 0 A and B are crossed to Port 1 B and A, Port 0 C and D are crossed to Port 1 D and C.

When XSDN input is HIGH, the crossbar switch is in normal operation mode. When XSDN input is LOW, the crossbar switch is placed under high-impedance state.

Table 4. Function table

Port 1 connected to Port 0	XSDN = 0	XSDN = 1, CROSS = 0	XSDN = 1, CROSS = 1
A1_P	high-Z	A0_P	B0_P
A1_N	high-Z	A0_N	B0_N
B1_P	high-Z	B0_P	A0_P
B1_N	high-Z	B0_N	A0_N
C1_P	high-Z	C0_P	D0_P
C1_N	high-Z	C0_N	D0_N
D1_P	high-Z	D0_P	C0_P
D1_N	high-Z	D0_N	C0_N

7. Power-up sequence

The CROSS pin must be LOW before start-up time has elapsed. After both V_{DD} and XSDN go HIGH for 500 µs ($t_{startup}$ time), CROSS input can be toggled to HIGH.

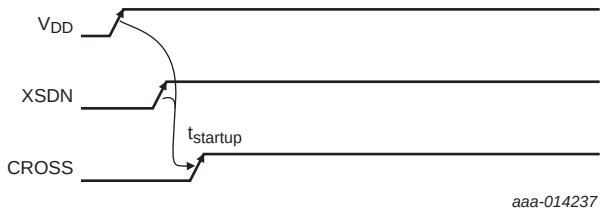


Fig 3. CROSS pin power-up sequence

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage		[1]	–0.3	+4.6	V
V_I	input voltage	control pins	[1]	–0.3	+5.5	V
		I/O pins of switches	[1]	–0.3	+4.6	V
T_{stg}	storage temperature			–65	+150	°C
V_{ESD}	electrostatic discharge voltage	HBM	[2]	-	2000	V
		CDM	[3]	-	750	V

[1] All voltage values, except differential voltages, are with respect to network ground terminal.

[2] Human Body Model: ANSI/ESDA/JEDEC JDS-001-2012 (Revision of ANSI/ESDA/JEDEC JS-001-2011), ESDA/JEDEC Joint standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA; JEDEC Solid State Technology Association, Arlington, VA, USA.

[3] Charged Device Model; JESD22-C101E December 2009 (Revision of JESD22-C101D, October 2008), standard for ESD sensitivity testing, Charged Device Model - Component level; JEDEC Solid State Technology Association, Arlington, VA, USA.

9. Recommended operating conditions

Table 6. Operating conditions

Over operating free-air temperature range (unless otherwise noted).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage	3.3 V supply option	2.7	-	3.5	V
V_I	input voltage	CMOS inputs	–0.3	-	+5.5	V
		MUX I/O pins	–0.3	-	+3.5	V
T_{amb}	ambient temperature	operating in free air	–20	-	+85	°C
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC still air test environment	-	149	-	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case	to case top; top cold plate at ambient temperature of 85 °C	-	69	-	°C/W

10. Characteristics

10.1 Device general characteristics

Table 7. General characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_{cons}	power consumption	V_{DD} = 3.5 V	-	-	1.75	mW
$P_{cons(sleep)}$	sleep mode power consumption	XSDN = 0	-	-	42	µW
I_{DD}	supply current	V_{DD} = 3.5 V	-	-	0.5	mA
$t_{startup}$	start-up time	supply voltage valid and XSDN goes HIGH to channel-specified operating characteristics	-	-	500	µs
t_{rcfg}	reconfiguration time	CROSS pin	-	300	1000	µs

10.2 Switch channel characteristics

Table 8. Dynamic and static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DDRL	differential return loss	f = 2.5 GHz	-	–20	-	dB
DDIL	differential insertion loss	channel is OFF				
		f = 2.5 GHz	-	–16	-	dB
		f = 100 MHz	-	–40	-	dB
		channel is ON				
		f = 2.5 GHz	-	–1.5	-	dB
		f = 100 MHz	-	–1	-	dB
DDNEXT	differential near-end crosstalk	channels among Port 0 or channels among Port 1				
		f = 2.5 GHz	-	–20	-	dB
		f = 240 MHz	-	–44	-	dB
DDFEXT	differential far-end crosstalk	between channels of Port 0 and Port 1				
		f = 2.5 GHz	-	–23	-	dB
		f = 240 MHz	-	–53	-	dB
R_{on}	ON-state resistance	V_{DD} = 2.7 V; V_I = 2.2 V; I_I = 10 mA	-	11	15	Ω
C_{in}	input capacitance	single-ended; V_{DD} = 2.8 V; V_I = 2.2 V	-	3	-	pF
B_{-3dB}	–3 dB bandwidth	V_{IC} = 0 V	-	7	-	GHz
		V_{IC} = 2.2 V	-	8.5	-	GHz
t_{PD}	propagation delay	from input to output pairs	-	70	-	ps
$t_{sk(dif)}$	differential skew time	intra-pair	-	5	-	ps
V_I	input voltage	for all switch ports	0	-	3.5	V
V_{IC}	common-mode input voltage	for all switch ports	0	-	V_{DD}	V
$V_{I(dif)(p-p)}$	peak-to-peak differential input voltage	for all switch ports	0	-	1.4	V
I_{LIH}	HIGH-level input leakage current	V_{DD} = max.; V_I = V_{DD}	-	-	±1	µA
I_{LIL}	LOW-level input leakage current	V_{DD} = max.; V_I = V_{SS}	-	-	±1	µA

10.3 Control signals characteristics

Table 9. CROSS input buffer characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	CMOS input	2.15	-	-	V
V_{IL}	LOW-level input voltage	CMOS input	-	-	0.5	V
I_{LI}	input leakage current	measured with input at $V_{IH} = V_{DD}$ and $V_{IL} = 0$ V [1]	-	-	0.2	μA

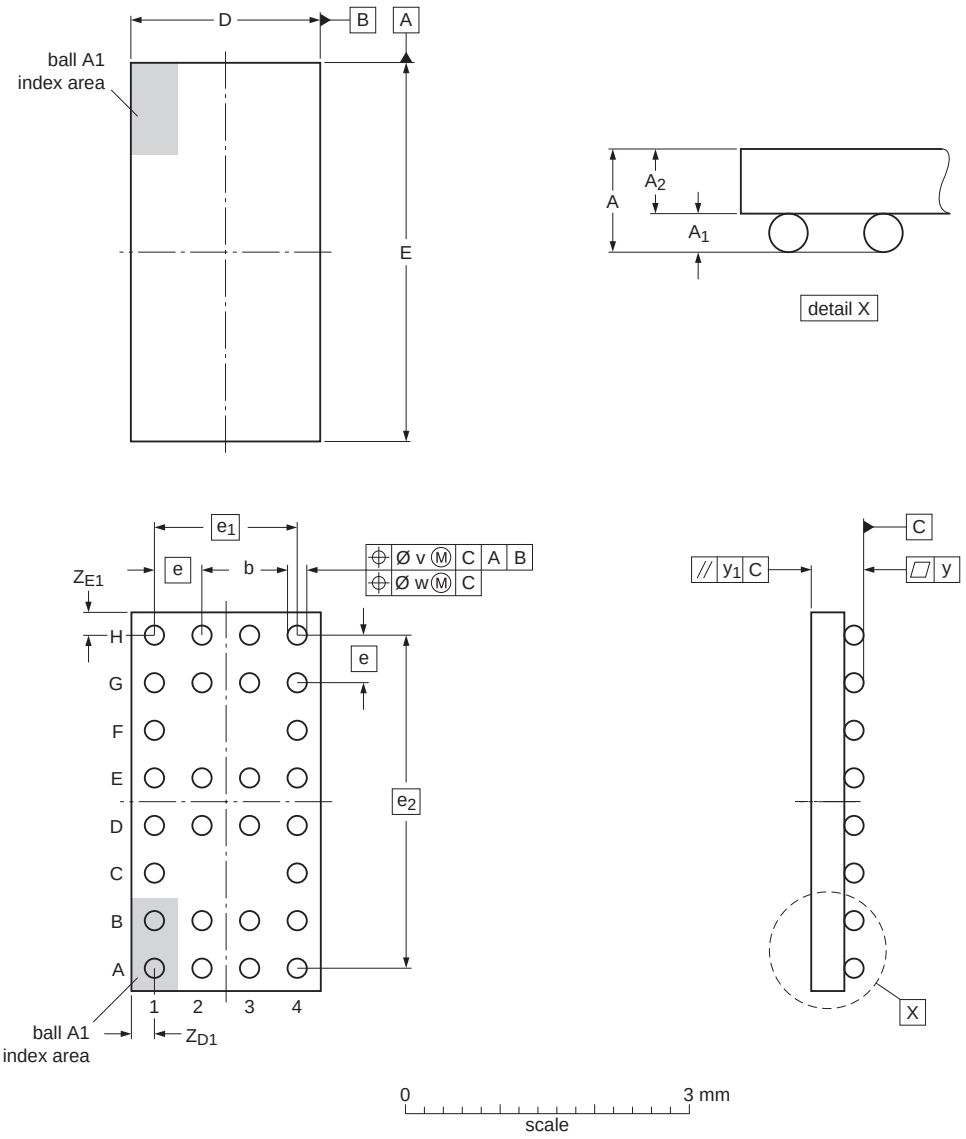
[1] This I_{LI} value is guaranteed by design and bench test.

Table 10. XSDN input buffer characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	CMOS inputs	2.15	-	-	V
V_{IL}	LOW-level input voltage	CMOS inputs	-	-	0.5	V
I_{LI}	input leakage current	measured with input at $V_{IH} = V_{DD}$ and $V_{IL} = 0$ V	-	-	1	μA

11. Package outline

XFBGA28: plastic, extremely thin fine-pitch ball grid array package; 28 balls **SOT1356-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1	Z_{D1}	Z_{E1}
mm	max	0.5	0.15	0.35	0.25	2.10	4.10								0.35	0.35
	nom		0.10	0.34	0.20	2.00	4.00	0.5	1.5	3.5	0.15	0.05	0.1	0.1	0.25	0.25
	min		0.05	0.33	0.15	1.90	3.90								0.15	0.15

sot1356-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1356-1	- - -	- - -	- - -			~~13-08-02~~ 13-09-09

Fig 4. Package outline SOT1356-1 (XFBGA28)

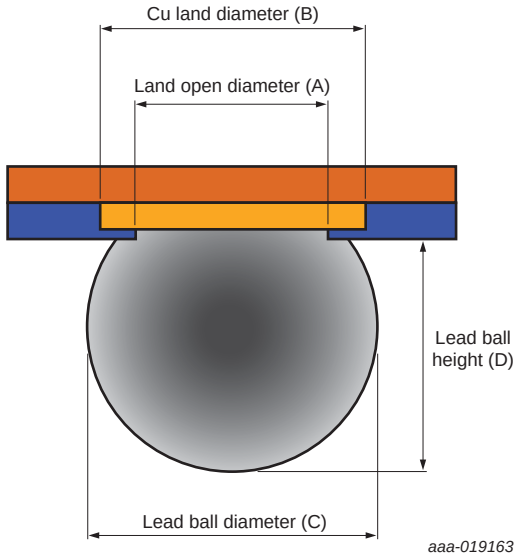


Fig 5. XFBGA28 Under Ball Metal (UBM) structure

Table 11. For 2 x 4 mm HLA AEX device

Ball pitch (mm)	Land open diameter (A) (mm)	Cu land diameter (B) (mm)	Lead ball diameter (C) (mm)	Lead ball height (D) (mm)
0.5	0.18 ± 0.013	0.25 ± 0.05	0.2 ± 0.05	0.1 ± 0.05

12. Packing information

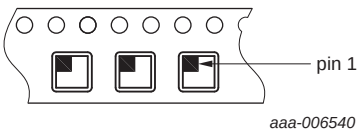
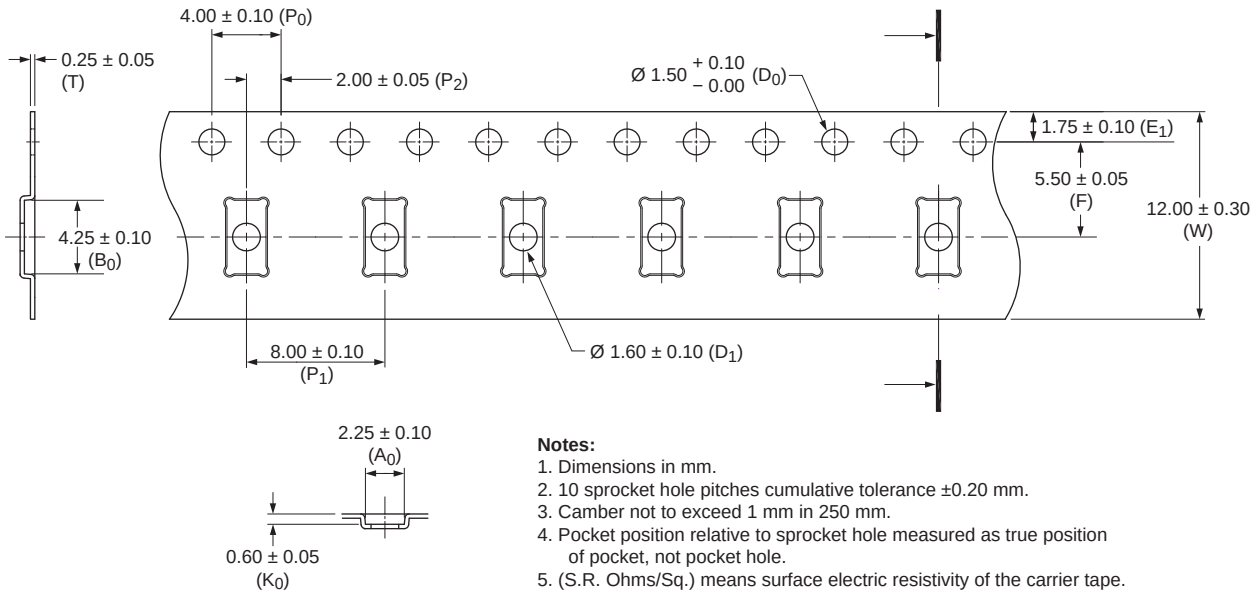


Fig 6. Product orientation in carrier tape



Notes:

1. Dimensions in mm.
2. 10 sprocket hole pitches cumulative tolerance ±0.20 mm.
3. Camber not to exceed 1 mm in 250 mm.
4. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
5. (S.R. Ohms/Sq.) means surface electric resistivity of the carrier tape.

aaa-009530

Fig 7. Carrier tape

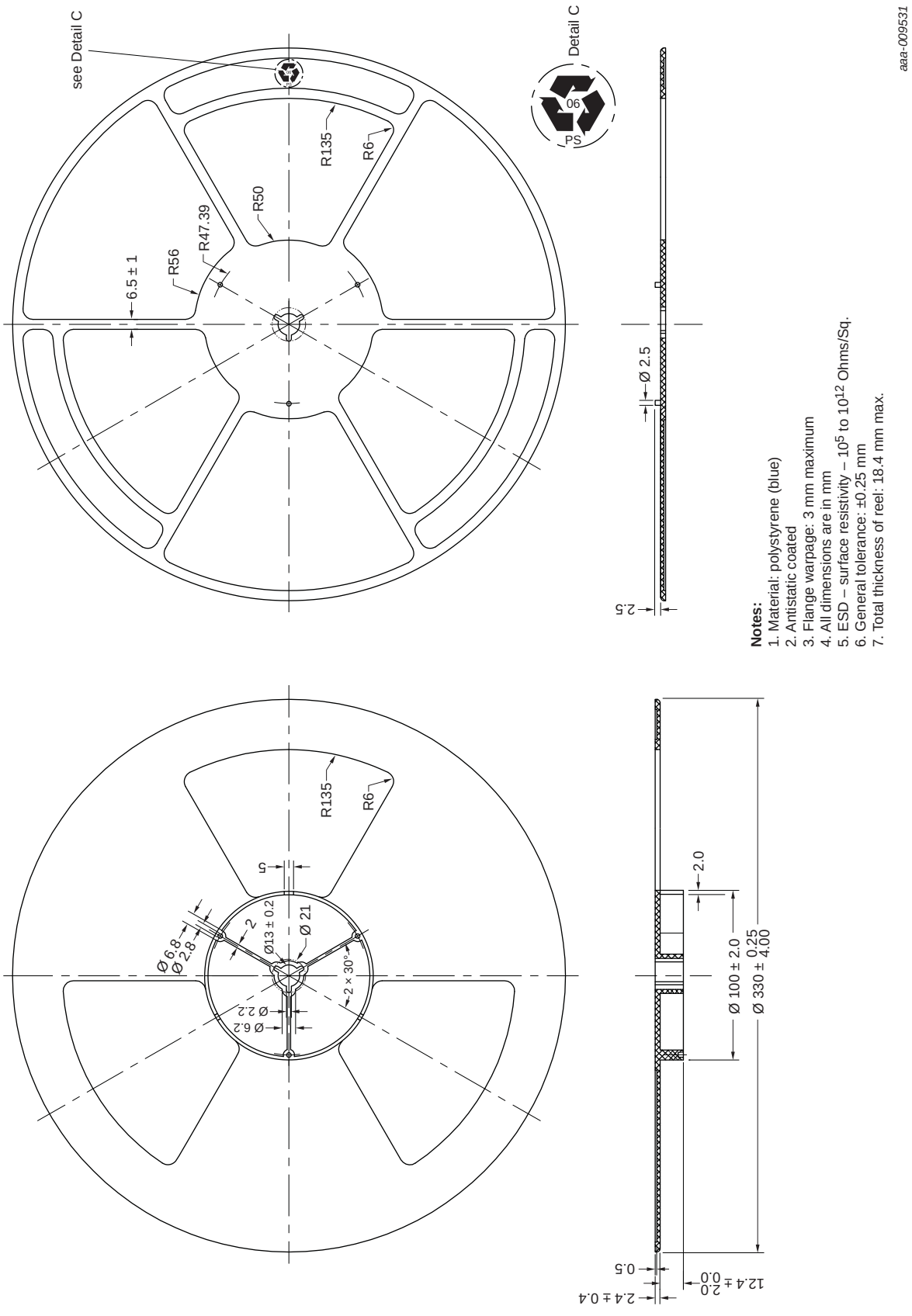
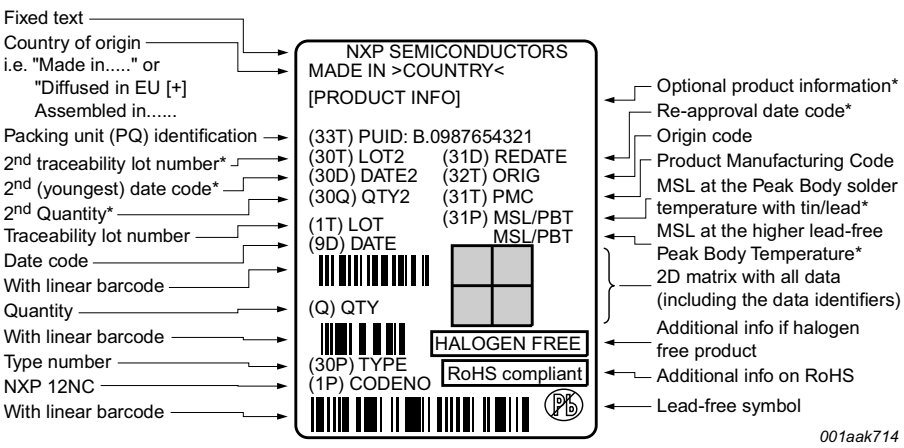


Fig 8. 13-inch reel



Box barcode label: 76 mm × 102 mm

Fig 9. Box information barcode

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 10) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 12 and 13

Table 12. SnPb eutectic process (from J-STD-020D)

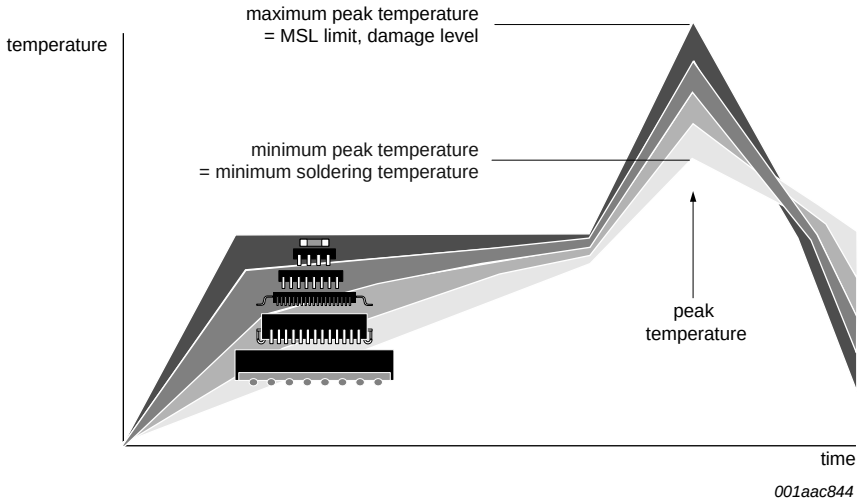
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 13. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 10.



MSL: Moisture Sensitivity Level

Fig 10. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Abbreviations

Table 14. Abbreviations

Acronym	Description
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MUX	Multiplexer
POR	Power-On Reset
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

15. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBTL04043A1 v.1.1	20150727	Product data sheet	-	CBTL04043A1 v.1
Modifications:	• Added Figure 5 “XFBGA28 Under Ball Metal (UBM) structure” and Table 11 “For 2 x 4 mm HLA AEX device”.			
CBTL04GP043 v.1	20141024	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 27 July 2015
Document identifier: CBTL04GP043