PCA9500

8-bit I²C-bus and SMBus I/O port with 2-kbit EEPROM

Rev. 04 — 15 April 2009 Product data sheet

1. General description

The PCA9500 is an 8-bit I/O expander with an on-board 2-kbit EEPROM.

The I/O expander's eight quasi-bidirectional data pins can be independently assigned as inputs or outputs to monitor board level status or activate indicator devices such as LEDs. The system master writes to the I/O configuration bits in the same way as for the PCF8574. The data for each input or output is kept in the corresponding Input or Output register. The system master can read all registers.

The EEPROM can be used to store error codes or board manufacturing data for read-back by application software for diagnostic purposes and is included in the I/O expander package.

The PCA9500 has 3 address pins with internal pull-up resistors allowing up to 8 devices to share the common two-wire I²C software protocol serial data bus. The fixed GPIO I²C-bus address is the same as the PCF8574 and the fixed EEPROM I²C-bus address is the same as the PCF8582C-2, so the PCA9500 appears as two separate devices to the bus master.

The PCA9500 supports hot insertion to facilitate usage in removable cards on backplane systems.

The PCA9501 is an alternative to the functionally similar PCA9500 for systems where a higher number of devices are required to share the same I²C-bus or an interrupt output is required.

2. Features

- 8 general purpose input/output expander/collector
- Drop-in replacement for PCF8574 with integrated 2-kbit EEPROM
- Internal 256 × 8 EEPROM
- Self timed write cycle
- 4 byte page write operation
- I²C-bus and SMBus interface logic
- Internal power-on reset
- Noise filter on SCL/SDA inputs
- 3 address pins allowing up to 8 devices on the I²C-bus/SMBus
- No glitch on power-up
- Supports hot insertion
- Power-up with all channels configured as inputs
- Low standby current
- Operating power supply voltage range of 2.5 V to 3.6 V

founded by Philips

- 5 V tolerant inputs/outputs
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO16, TSSOP16, HVQFN16

3. Applications

- Board version tracking and configuration
- Board health monitoring and status reporting
- Multi-card systems in telecommunications, networking, and base station infrastructure equipment
- Field recall and troubleshooting functions for installed boards
- General-purpose integrated I/O with memory
- Drop-in replacement for PCF8574 with integrated 2-kbit EEPROM
- Bus master sees GPIO and EEPROM as two separate devices
- Three hardware address pins allow up to 8 PCA9500s to be located in the same I²C-bus/SMBus

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCA9500D	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
PCA9500PW	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
PCA9500BS	HVQFN16	plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 4 × 4 × 0.85 mm	SOT629-1

4.1 Ordering options

Table 2. Ordering options

Type number	Topside mark	Temperature range
PCA9500D	PCA9500D	–40 °C to +85 °C
PCA9500PW	PCA9500	–40 °C to +85 °C
PCA9500BS	9500	–40 °C to +85 °C

5. Block diagram

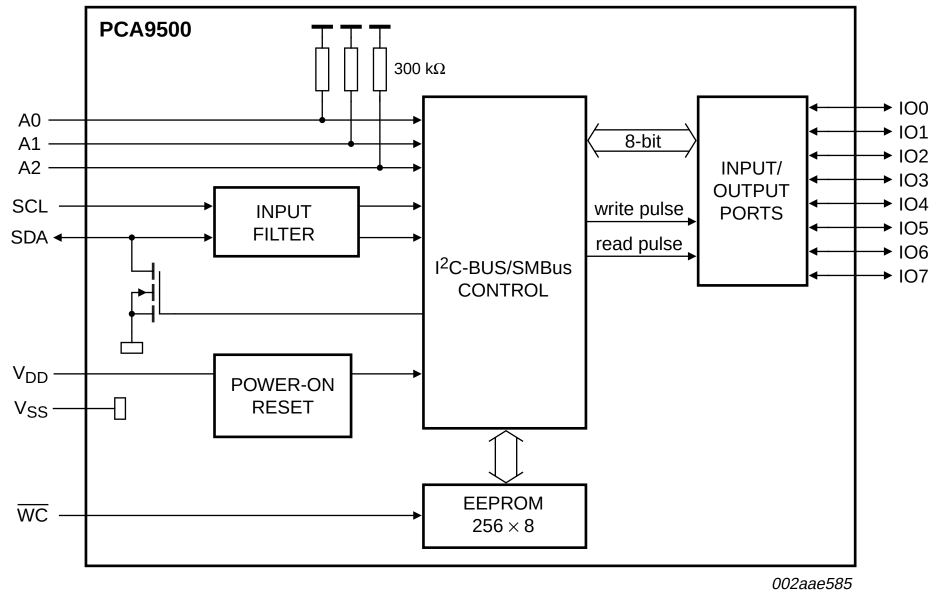


Fig 1. Block diagram of PCA9500

6. Pinning information

6.1 Pinning

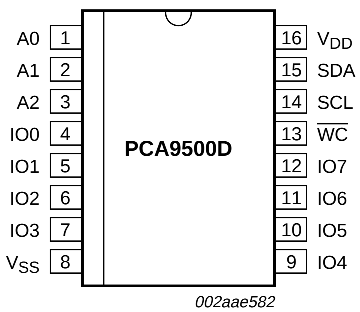


Fig 2. Pin configuration for SO16

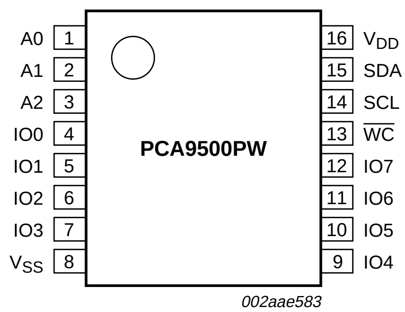


Fig 3. Pin configuration for TSSOP16

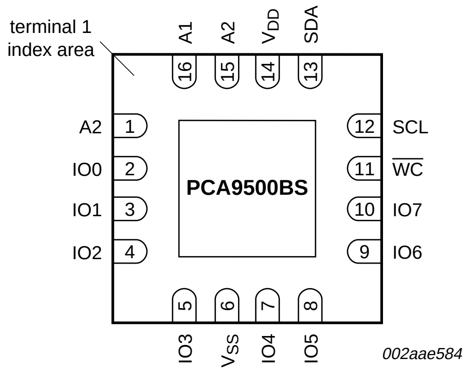


Fig 4. Pin configuration for HVQFN16

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SO16, TSSOP16	HVQFN16	
A0	1	15	address lines (internal pull-up)
A1	2	16	
A2	3	1	
IO0	4	2	quasi-bidirectional I/O pins
IO1	5	3	
IO2	6	4	
IO3	7	5	
IO4	9	7	
IO5	10	8	
IO6	11	9	
IO7	12	10	
V_{SS}	8	6[1]	supply ground
$\overline{WC}$	13	11	active LOW write control pin
SCL	14	12	I²C-bus serial clock
SDA	15	13	I²C-bus serial data
V_{DD}	16	14	supply voltage

[1] HVQFN16 package supply ground is connected to both V_{SS} pin and exposed center pad. V_{SS} pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

7. Functional description

Refer also to Figure 1 “Block diagram of PCA9500”.

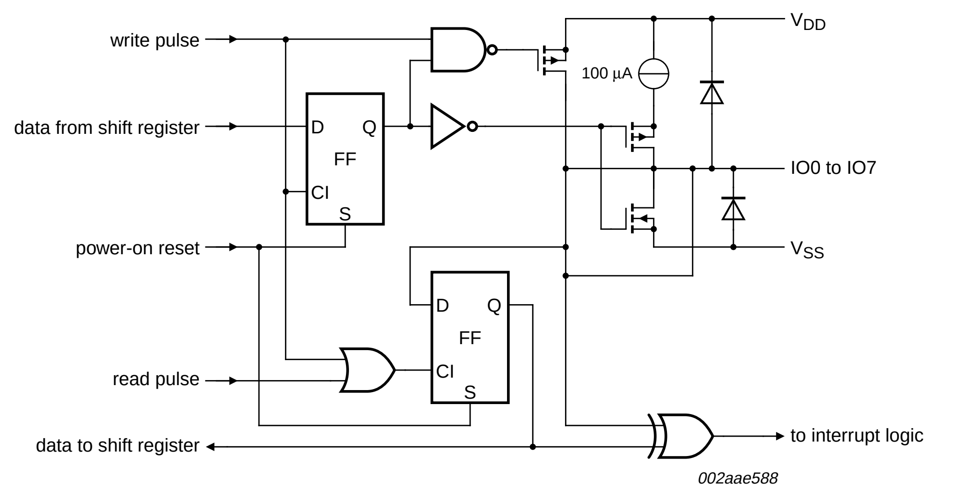


Fig 5. Simplified schematic diagram of each I/O

7.1 Device addressing

Following a START condition, the bus master must output the address of the slave it is accessing. The address of the PCA9500 is shown in Figure 6. Internal pull-up resistors are incorporated on the hardware selectable address pins.

The last bit of the address byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

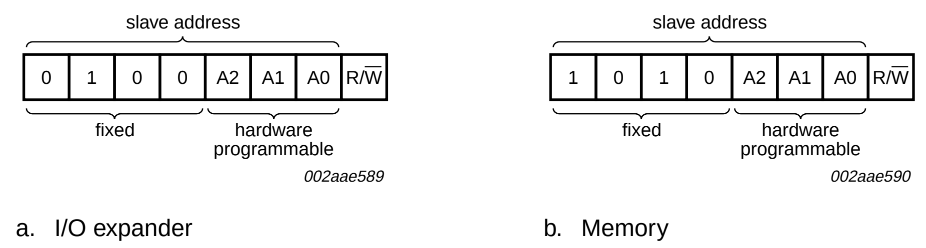


Fig 6. PCA9500 slave addresses

7.2 Control register

The PCA9500 contains a single 8-bit register called the Control register, which can be written and read via the I^{2}C-bus. This register is sent after a successful acknowledgment of the slave address. It contains the I/O operation information.

7.3 I/O operations

(Refer also to Figure 5.)

Each of the PCA9500's eight I/Os can be independently used as an input or output. Output data is transmitted to the port by the I/O Write mode (see Figure 7). Input I/O data is transferred from the port to the microcontroller by the Read mode (see Figure 8).

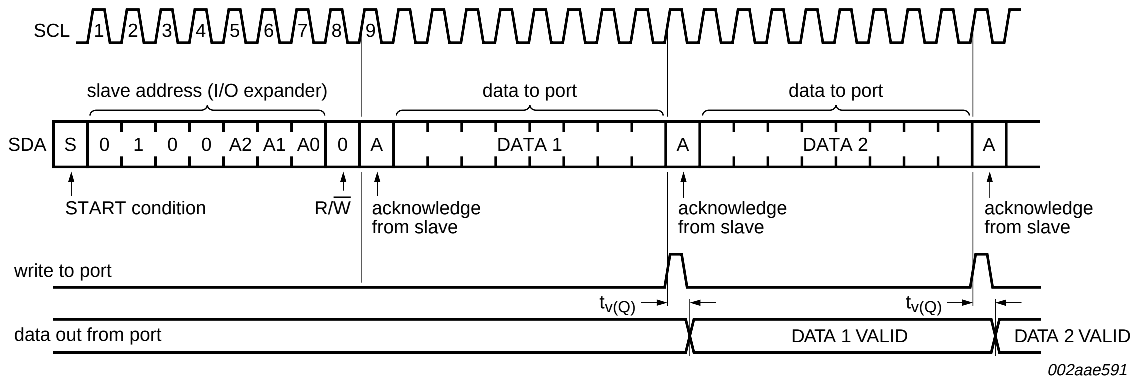


Fig 7. I/O Write mode (output)

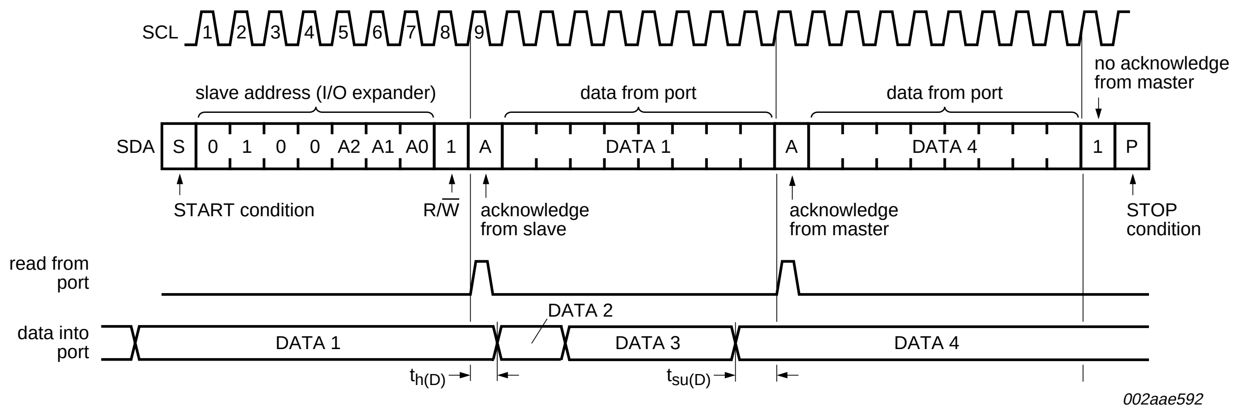


Fig 8. I/O Read mode (input)

7.3.1 Quasi-bidirectional I/Os

A quasi-bidirectional I/O can be used as an input or output without the use of a control signal for data direction. At power-on the I/Os are HIGH. In this mode, only a current source to V_{DD} is active. An additional strong pull-up to V_{DD} allows fast rising edges into heavily loaded outputs. These devices turn on when an output is written HIGH, and are switched off by the negative edge of SCL. The I/Os should be HIGH before being used as inputs. See Figure 9.

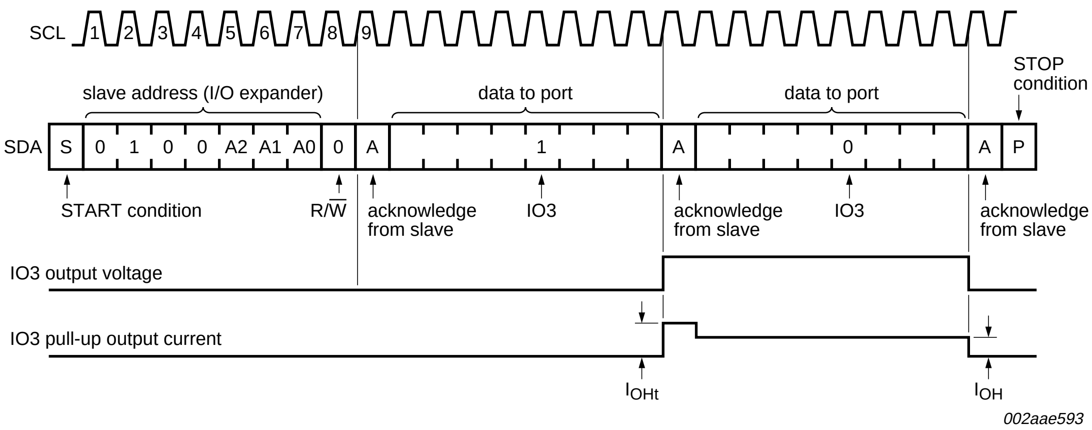


Fig 9. Transient pull-up current (I_{OHt}) while IO3 changes from LOW to HIGH and back to LOW

7.4 Memory operations

7.4.1 Write operations

Write operations require an additional address field to indicate the memory address location to be written. The address field is eight bits long, providing access to any one of the 256 words of memory. There are two types of write operations, 'byte write' and 'page write'.

Write operation is possible when the Write Control pin ($\overline{WC}$) is put at a LOW logic level (0). When this control signal is set at 1, write operation is not possible and data in the memory is protected.

'Byte write' and 'page write' explained below assume that $\overline{WC}$ is set to 0.

7.4.1.1 Byte write

To perform a byte write the START condition is followed by the memory slave address and the R/$\overline{W}$ bit set to 0. The PCA9500 will respond with an acknowledge and then consider the next eight bits sent as the word address and the eight bits after the word address as the data. The PCA9500 will issue an acknowledge after the receipt of both the word address and the data. To terminate the data transfer the master issues the STOP condition, initiating the internal write cycle to the non-volatile memory. Only write and read operations to the quasi-bidirectional I/Os are allowed during the internal write cycle.

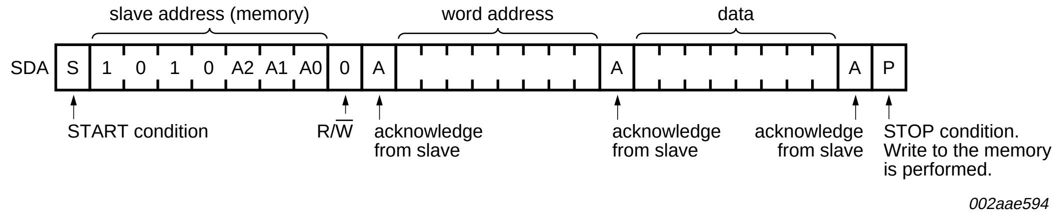


Fig 10. Byte write

7.4.1.2 Page write

A page write is initiated in the same way as the byte write. If after sending the first word of data, the STOP condition is not received, the PCA9500 considers subsequent words as data. After each data word the PCA9500 responds with an acknowledge and the two least significant bits of the memory address field are incremented. Should the master not send a STOP condition after four data words, the address counter will return to its initial value and overwrite the data previously written. After the receipt of the STOP condition the inputs will behave as with the byte write during the internal write cycle.

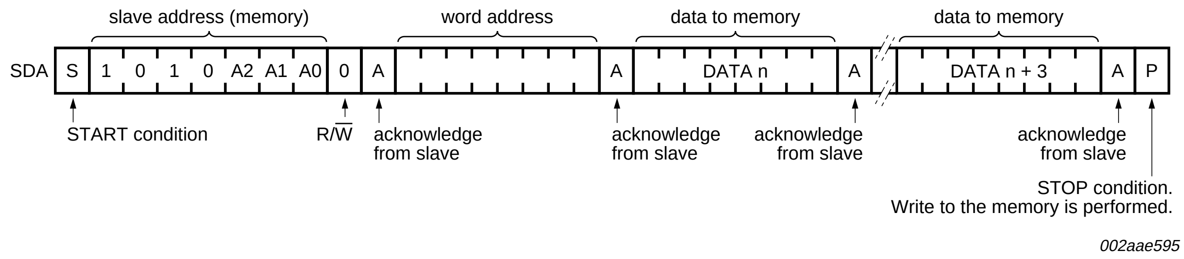


Fig 11. Page write

7.4.2 Read operations

PCA9500 read operations are initiated in an identical manner to write operations with the exception that the memory slave address R/$\overline{W}$ bit is set to '1'. There are three types of read operations: current address read, random read and sequential read.

7.4.2.1 Current address read

The PCA9500 contains an internal address counter that increments after each read or write access and as a result, if the last word accessed was at address 'n', then the address counter contains the address 'n + 1'.

When the PCA9500 receives its memory slave address with the R/$\overline{W}$ bit set to one it issues an acknowledge and uses the next eight clocks to transmit the data contained at the address stored in the address counter. The master ceases the transmission by issuing the STOP condition after the eighth bit. There is no ninth clock cycle for the acknowledge. See Figure 12.

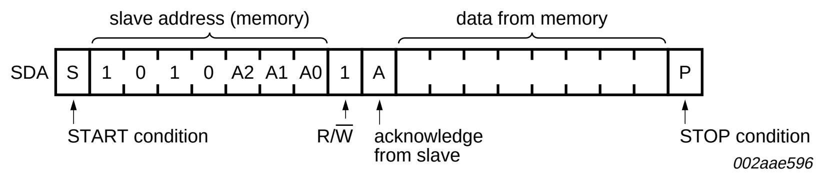


Fig 12. Current address read

7.4.2.2 Random read

The PCA9500's random read mode allows the address to be read from to be specified by the master. This is done by performing a dummy write to set the address counter to the location to be read. The master must perform a byte write to the address location to be read, but instead of transmitting the data after receiving the acknowledge from the PCA9500, the master re-issues the START condition and memory slave address with the $R/\overline{W}$ bit set to one. The PCA9500 will then transmit an acknowledge and use the next eight clock cycles to transmit the data contained in the addressed location. The master ceases the transmission by issuing the STOP condition after the eighth bit, omitting the ninth clock cycle acknowledge.

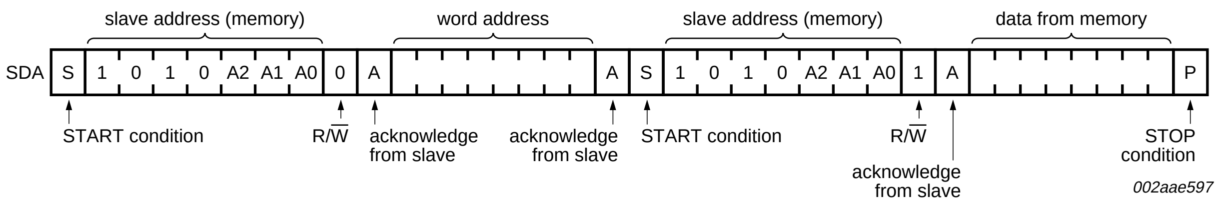


Fig 13. Random read

7.4.2.3 Sequential read

The PCA9500 sequential read is an extension of either the current address read or random read. If the master does not issue a STOP condition after it has received the eighth data bit, but instead issues an acknowledge, the PCA9500 will increment the address counter and use the next eight cycles to transmit the data from that location. The master can continue this process to read the contents of the entire memory. Upon reaching address 255 the counter will return to address 0 and continue transmitting data until a STOP condition is received. The master ceases the transmission by issuing the STOP condition after the eighth bit, omitting the ninth clock cycle acknowledge.

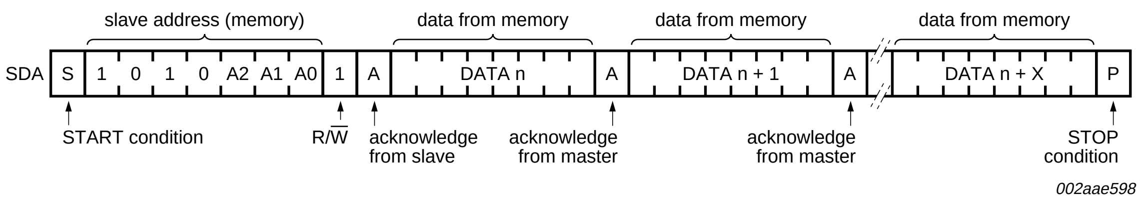


Fig 14. Sequential read

8. Characteristics of the I^2C-bus

The I^2C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 15).

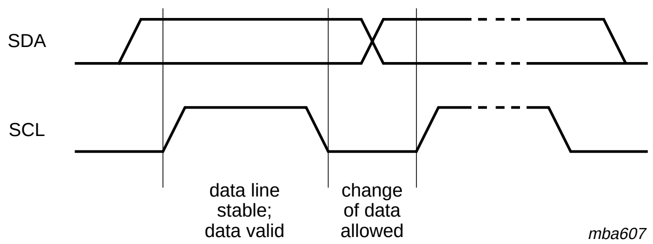


Fig 15. Bit transfer

8.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 16).

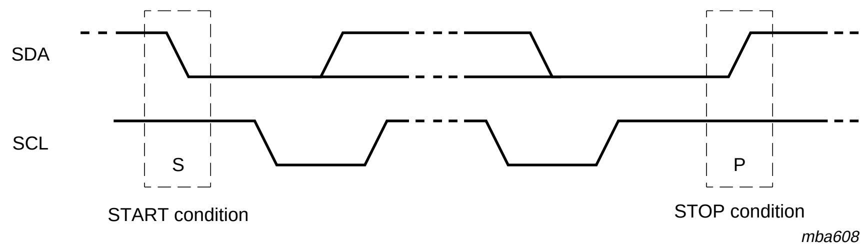


Fig 16. Definition of START and STOP conditions

8.2 System configuration

A device generating a message is a ‘transmitter’; a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Figure 17).

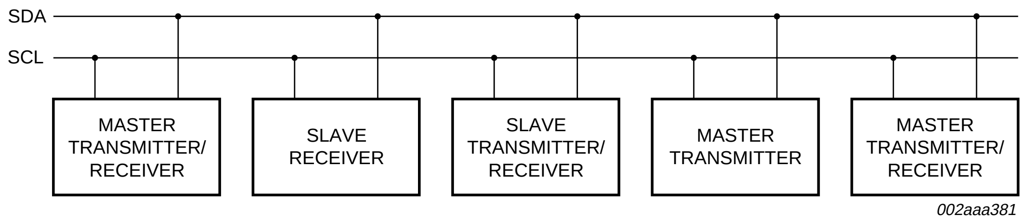


Fig 17. System configuration

8.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up time and hold time must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

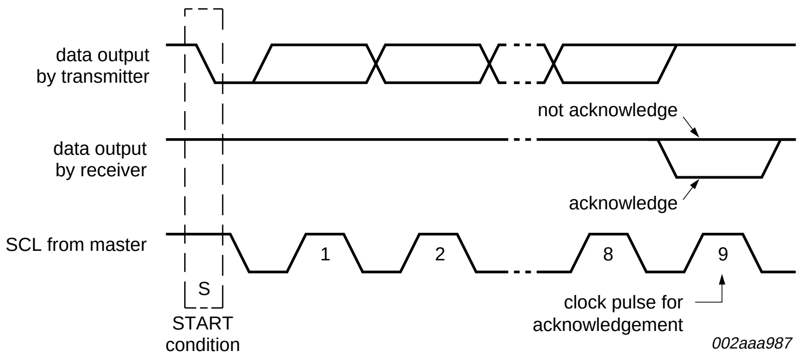


Fig 18. Acknowledgement on the I²C-bus

9. Application design-in information

A central processor/controller typically located on the system main board can use the 400 kHz I²C-bus/SMBus to poll the PCA9500 devices located on the system cards for status or version control type of information. The PCA9500 may be programmed at manufacturing to store information regarding board build, firmware version, manufacturer identification, configuration option data, and so on. Alternately, these devices can be used as convenient interface for board configuration, thereby utilizing the I²C-bus/SMBus as an intra-system communication bus.

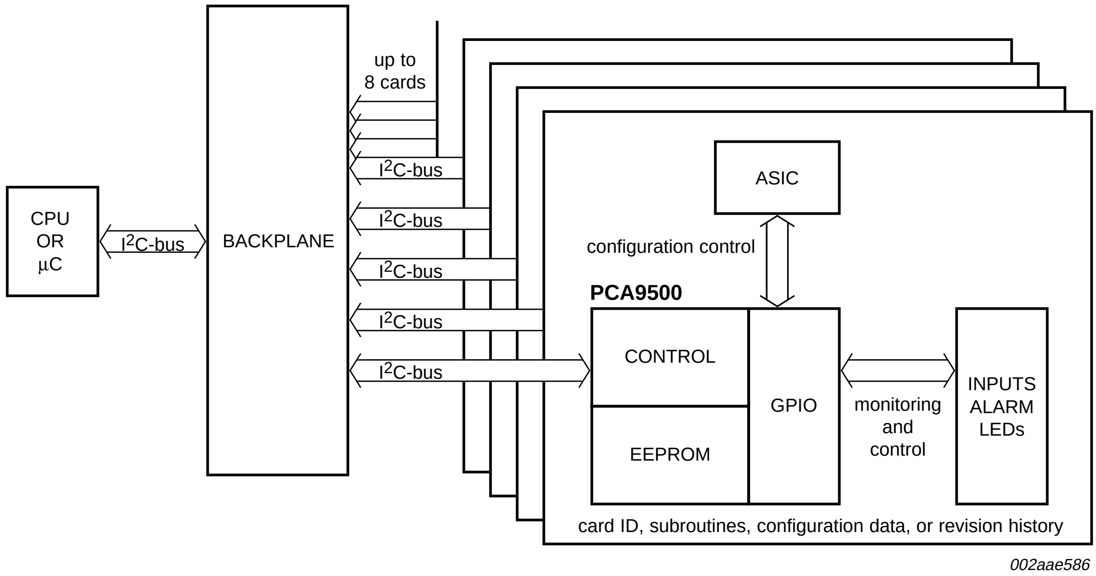
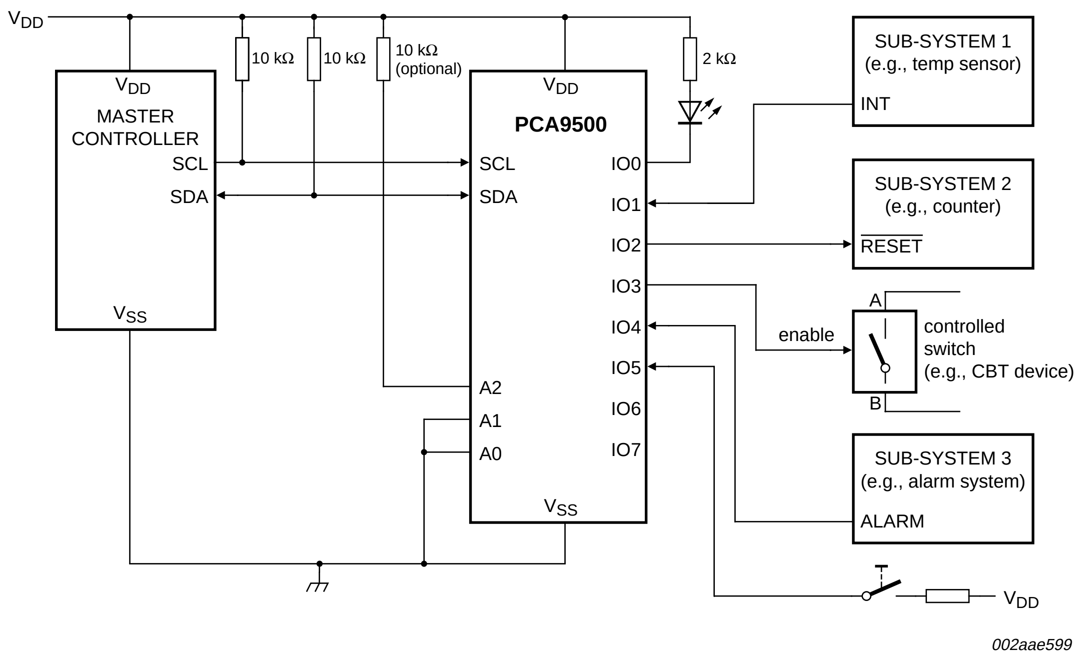


Fig 19. PCA9500 used as interface for board configuration



GPIO device address configured as 0100 100x for this example.

EEPROM device address configured as 1010 100x for this example.

IO0, IO2, IO3 configured as outputs.

IO1, IO4, IO5 configured as inputs.

IO6, IO7 are not used and must be configured as outputs.

Fig 20. Typical application

10. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

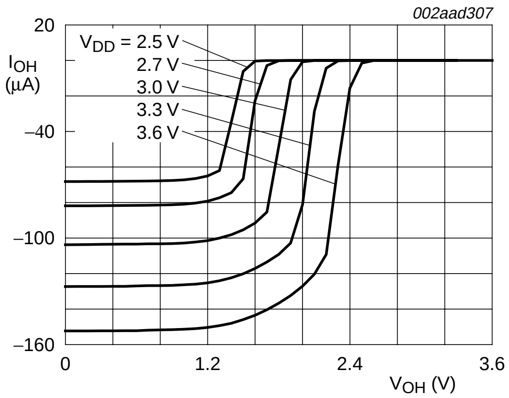
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+4.0	V
V_I	input voltage		V_{SS} – 0.5	5.5	V
I_I	input current		–20	+20	mA
I_O	output current		–25	+25	mA
I_{DD}	supply current		–100	+100	mA
I_{SS}	ground supply current		–100	+100	mA
P_{tot}	total power dissipation		-	400	mW
P/out	power dissipation per output		-	100	mW
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient temperature	operating	–40	+85	°C

11. Static characteristics

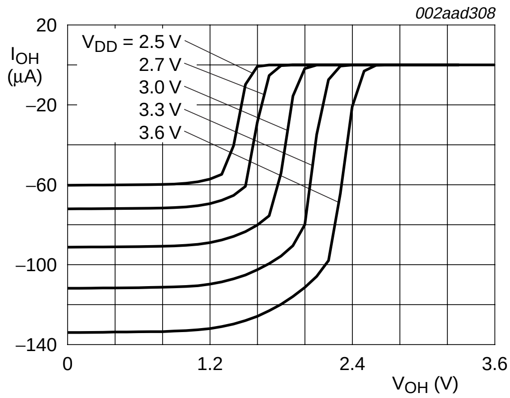
Table 5. Static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{DD}	supply voltage		2.5	3.3	3.6	V
I_{DDQ}	standby current	A0, A1, A2, $\overline{WC}$ = HIGH	-	-	60	µA
I_{DD1}	supply current read		-	-	1	mA
I_{DD2}	supply current write		-	-	2	mA
V_{POR}	power-on reset voltage		-	-	2.4	V
Input SCL; input/output SDA						
V_{IL}	LOW-level input voltage		–0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	-	-	mA
I_{LI}	input leakage current	V_I = V_{DD} or V_{SS}	–1	-	+1	µA
C_i	input capacitance	V_I = V_{SS}	-	-	7	pF
I/O expander port						
V_{IL}	LOW-level input voltage		–0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	5.5	V
$I_{IHL(max)}$	input current through protection diodes		–400	-	+400	µA
I_{OL}	LOW-level output current	V_{OL} = 1 V [1]	10	25	-	mA
I_{OH}	HIGH-level output current	V_{OH} = V_{SS}	30	100	300	µA
I_{OHt}	transient pull-up current		-	2	-	mA
C_i	input capacitance		-	-	10	pF
C_o	output capacitance		-	-	10	pF
Address inputs A0, A1, A2; $\overline{WC}$ input						
V_{IL}	LOW-level input voltage		–0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	5.5	V
I_{LI}	input leakage current	V_I = V_{DD}	–1	-	+1	µA
		pull-up; V_I = V_{SS}	10	25	100	µA

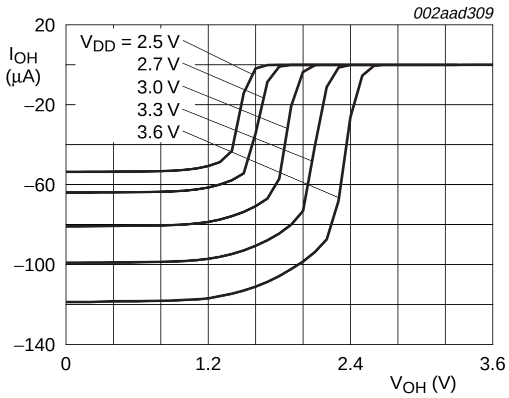
[1] Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 100 mA.



a. T_{amb} = −40 °C



b. T_{amb} = 25 °C



c. T_{amb} = 85 °C

Fig 21. V_{OH} versus I_{OH}

Remark: Rapid fall-off in V_{OH} at current inception is due to a diode that provides 5 V overvoltage protection for the GPIO I/O pins. When the GPIO I/O are being used as inputs, the internal current source V_{OH} should be evaluated to determine if external pull-up resistors are required to provide sufficient V_{IH} threshold noise margin.

12. Dynamic characteristics

Table 6. Dynamic characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I^2C-bus timing[1] (see Figure 22)							
f_{SCL}	SCL clock frequency			-	-	400	kHz
t_{SP}	pulse width of spikes that must be suppressed by the input filter			-	-	50	ns
t_{BUF}	bus free time between a STOP and START condition			1.3	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			0.6	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition			0.6	-	-	µs
t_r	rise time of both SDA and SCL signals			-	-	0.3	µs
t_f	fall time of both SDA and SCL signals			-	-	0.3	µs
$t_{SU;DAT}$	data set-up time			250	-	-	ns
$t_{HD;DAT}$	data hold time			0	-	-	ns
$t_{VD;DAT}$	data valid time	SCL LOW to data output		-	-	1.0	µs
$t_{SU;STO}$	set-up time for STOP condition			0.6	-	-	µs
Port timing							
$t_{v(Q)}$	data output valid time	$C_L \leq 100$ pF		-	-	4	µs
$t_{su(D)}$	data input set-up time	$C_L \leq 100$ pF		0	-	-	µs
$t_{h(D)}$	data input hold time	$C_L \leq 100$ pF		4	-	-	µs
Power-up timing							
$t_{pu(R)}$	read power-up time		[2]	-	-	1	ms
$t_{pu(W)}$	write power-up time		[2]	-	-	5	ms
Write cycle limits (see Figure 23)							
$T_{cy(W)}$	write cycle time		[3]	-	5	10	ms

[1] All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

[2] $t_{pu(R)}$ and $t_{pu(W)}$ are the delays required from the time V_{DD} is stable until the specified operation can be initiated. These parameters are guaranteed by design.

[3] $T_{cy(W)}$ is the maximum time that the device requires to perform the internal write operation.

Table 7. Non-volatile storage specifications

Parameter	Specification
memory cell data retention	10 years minimum
number of memory cell write cycles	100,000 cycles minimum

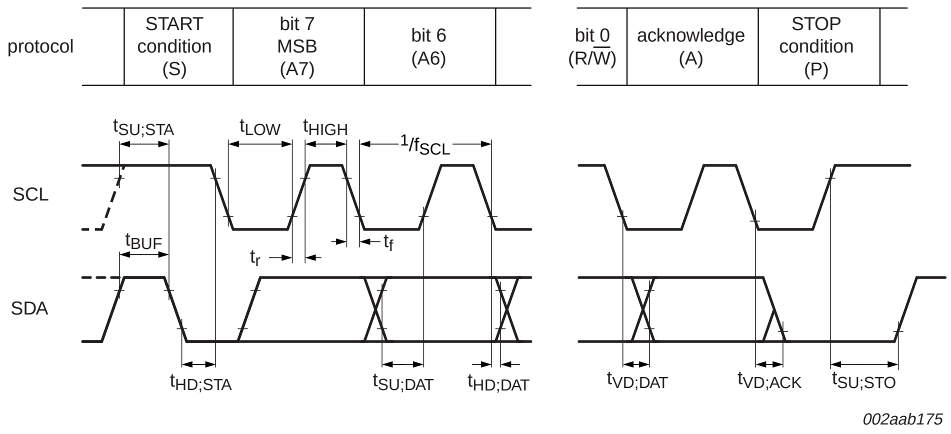


Fig 22. I2C-bus timing

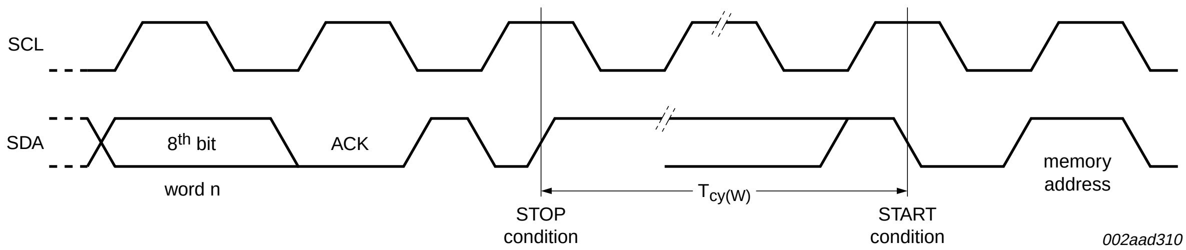
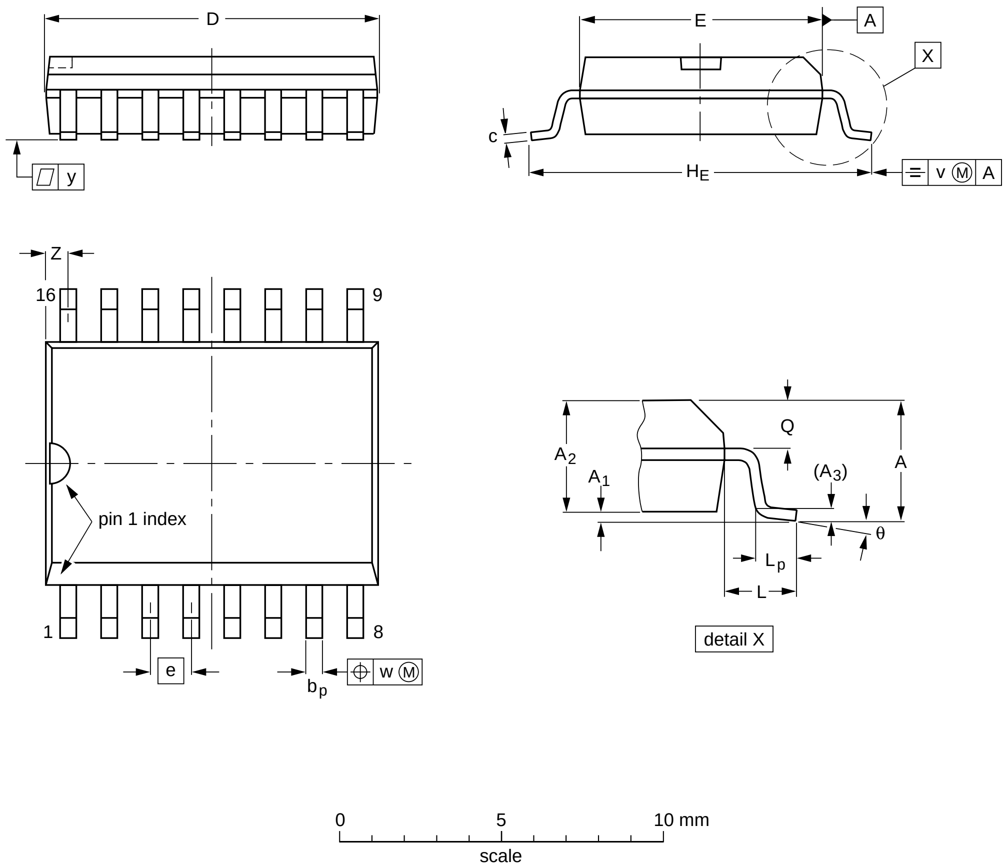


Fig 23. Write cycle timing

13. Package outline

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

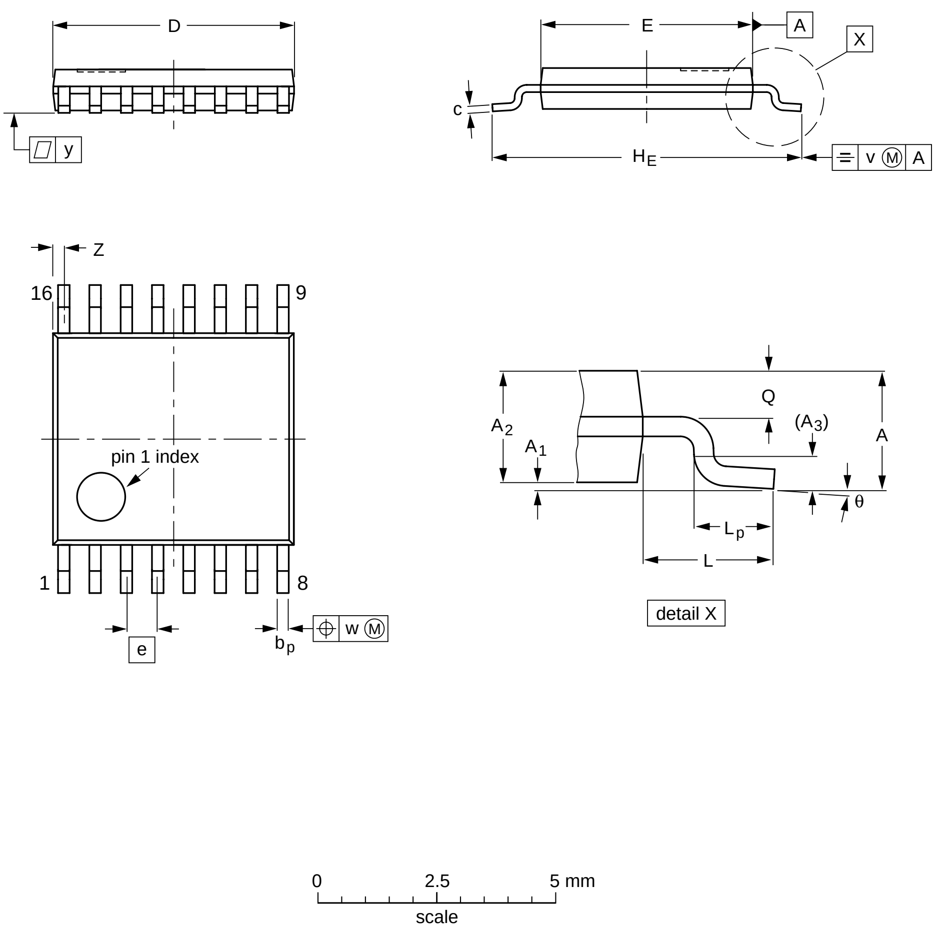
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT162-1	075E03	MS-013				~~99-12-27~~ 03-02-19

Fig 24. Package outline SOT162-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

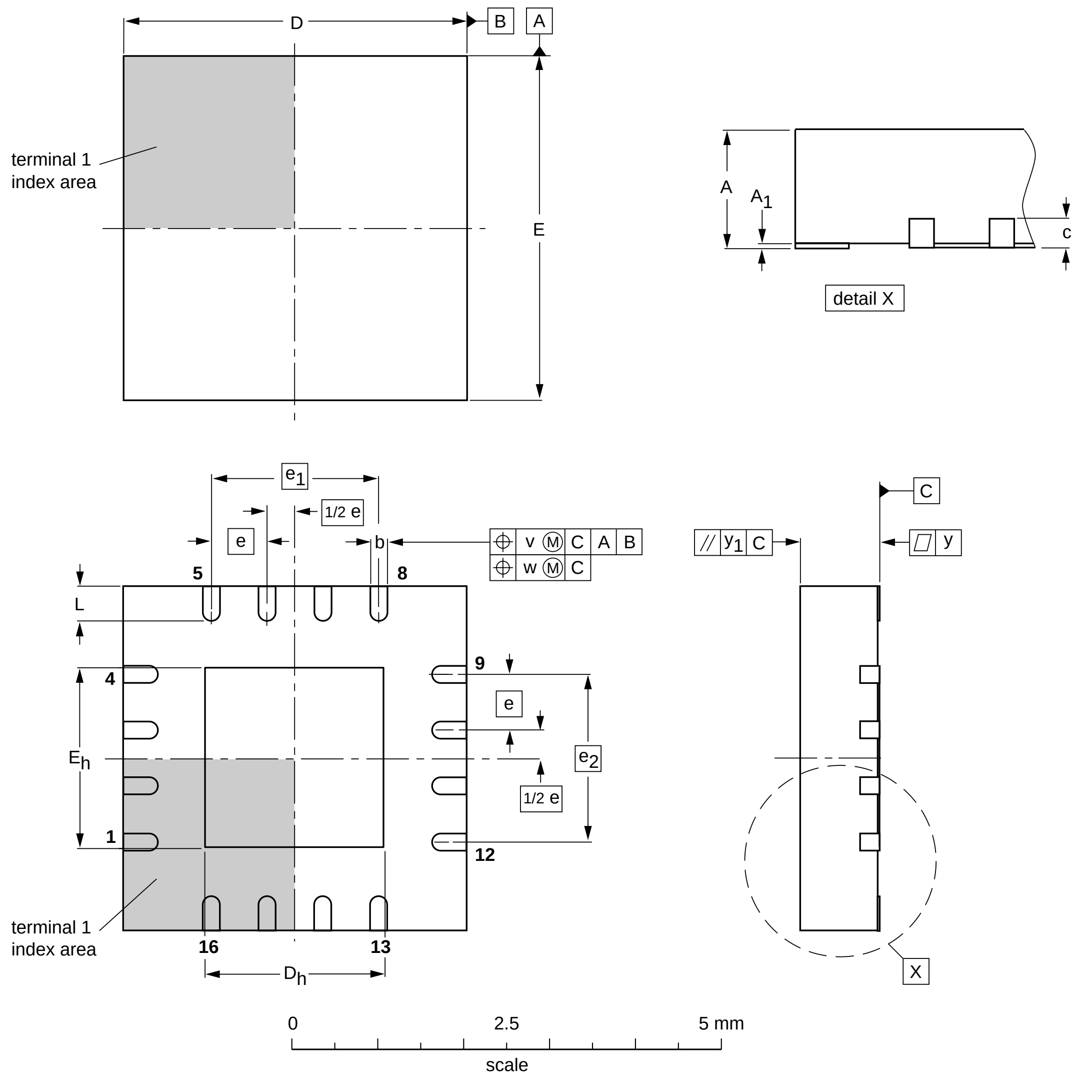
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 25. Package outline SOT403-1 (TSSOP16)

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 4 x 4 x 0.85 mm **SOT629-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.38 0.23	0.2	4.1 3.9	2.25 1.95	4.1 3.9	2.25 1.95	0.65	1.95	1.95	0.75 0.50	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT629-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

Fig 26. Package outline SOT629-1 (HVQFN16)

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 27) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 8 and 9

Table 8. SnPb eutectic process (from J-STD-020C)

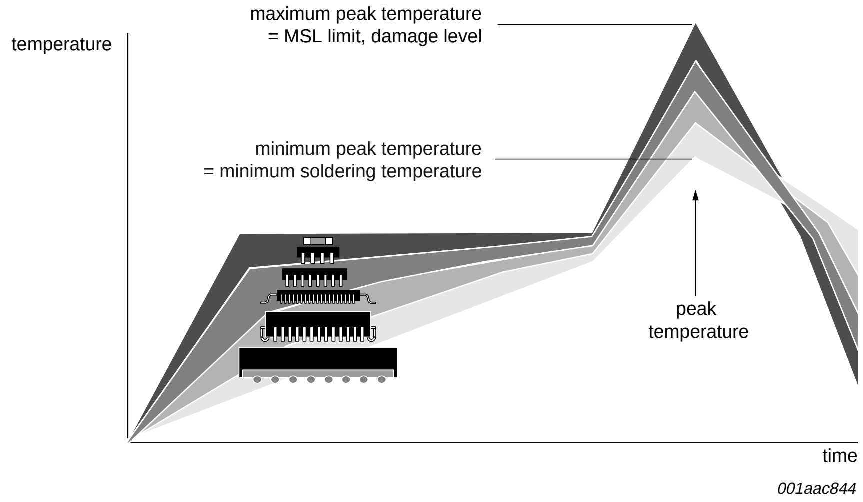
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 9. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 27.



MSL: Moisture Sensitivity Level

Fig 27. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

15. Abbreviations

Table 10. Abbreviations

Acronym	Description
ASIC	Application Specific Integrated Circuit
CBT	Cross-Bar Technology
CDM	Charged-Device Model
CPU	Central Processing Unit
EEPROM	Electrically Erasable Programmable Read-Only Memory
ESD	ElectroStatic Discharge
FF	Flip-Flop
GPIO	General Purpose Input/Output
I²C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
HBM	Human Body Model
LED	Light-Emitting Diode
MM	Machine Model
SMBus	System Management Bus

16. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9500_4	20090415	Product data sheet	-	PCA9500_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 3 "Pin description": – added Table note [1] and its reference at HVQFN16 pin 6 – changed naming convention for pins I/On to "IOn" • Figure 7 "I/O Write mode (output)": changed symbol "t_{pv}" to "$t_{v(Q)}$" • Figure 8 "I/O Read mode (input)": – changed symbol "t_{ph}" to "$t_{h(D)}$" – changed symbol "t_{ps}" to "$t_{su(D)}$" • Table 4 "Limiting values": – changed symbol "V_{CC}" to "V_{DD}" – changed parameter for I_{SS} from "supply current" to "ground supply current" – changed symbol "P_O" to "P/out" – changed parameter for T_{amb} from "operating temperature" to "ambient temperature"; placed "operating" in Conditions column • Table 5 "Static characteristics": – added reference to Table note [1] at I_{OL} in sub-section "I/O expander port" • Table 6 "Dynamic characteristics": – sub-section "I^2C-bus timing": changed symbol/parameter from "t_{SW}, tolerable spike width on bus" to "t_{SP}, pulse width of spikes that must be suppressed by the input filter" – sub-section "Port timing": changed symbol "t_{pv}" to "$t_{v(Q)}$" – sub-section "Port timing": changed symbol "t_{ps}" to "$t_{su(D)}$" – sub-section "Port timing": changed symbol "t_{ph}" to "$t_{h(D)}$" – sub-section "Power-up timing": changed symbol "t_{PUR}" to "$t_{pu(R)}$" – sub-section "Power-up timing": changed symbol "t_{PUW}" to "$t_{pu(W)}$" – sub-section "Write cycle limits": changed symbol "t_{WR}" to "$T_{cy(W)}$" • Figure 23 "Write cycle timing": changed symbol "t_{WR}" to "$T_{cy(W)}$" • added Section 15 "Abbreviations" • updated soldering information			
PCA9500_3 (9397 750 14134)	20040930	Product data sheet	-	PCA9500_2
PCA9500_2	20030627	Product data	853-2369 30018 of 2003 Jun 11	PCA9500_1
PCA9500_1	20020927	Product data	853-2369 28875 of 2002 Sep 27	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Date of release: 15 April 2009
Document identifier: PCA9500_4