



# PTVS18VU1UPA

## 300 W Transient Voltage Suppressor

19 May 2020

Product data sheet

### 1. General description

300 W unidirectional Transient Voltage Suppressor (TVS) in a DFN2020-3 (SOT1061) leadless medium power Surface-Mounted Device (SMD) plastic package, designed for transient overvoltage protection.

### 2. Features and benefits

- Unidirectional protection of one line
- Reverse standoff voltage:  $V_{RWM} = 18\text{ V}$
- Surge robustness:  $I_{PPM} = 97\text{ A (8/20 }\mu\text{s) / } I_{PPM} = 10.3\text{ A (10/1000 }\mu\text{s)}$
- Reverse current:  $I_{RM} = 1\text{ nA}$
- Very low package height: 0.65 mm
- AEC-Q101 qualified

### 3. Applications

- Power supply protection
- Industrial application
- Power management

### 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{RWM}$	reverse standoff voltage	$T_j = 25\text{ }^\circ\text{C}$		-	-	18	V
$I_{PPM}$	rated peak pulse current	$t_p = 8/20\text{ }\mu\text{s}$	[1] [2]	-	-	97	A
		$t_p = 10/1000\text{ }\mu\text{s}$	[3] [2]	-	-	10.3	A

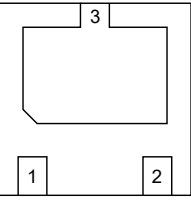

[1] In accordance with IEC 61000-4-5 and IEC 61643-321 (8/20  $\mu\text{s}$  current waveform).

[2] Measured from pin 1 and 2 to pin 3.

[3] In accordance with IEC 61643-321 (10/1000  $\mu\text{s}$  current waveform).

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	A	anode	 <p>Transparent top view DFN2020-3 (SOT1061)</p>	 <p>006aab838</p>
2	A	anode		
3	K	cathode		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PTVS18VU1UPA	DFN2020-3	plastic, leadless thermal enhanced ultra thin small outline package; 3 terminals; 1.3 mm pitch; 2 mm x 2 mm x 0.65 mm body	SOT1061

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PTVS18VU1UPA	D2

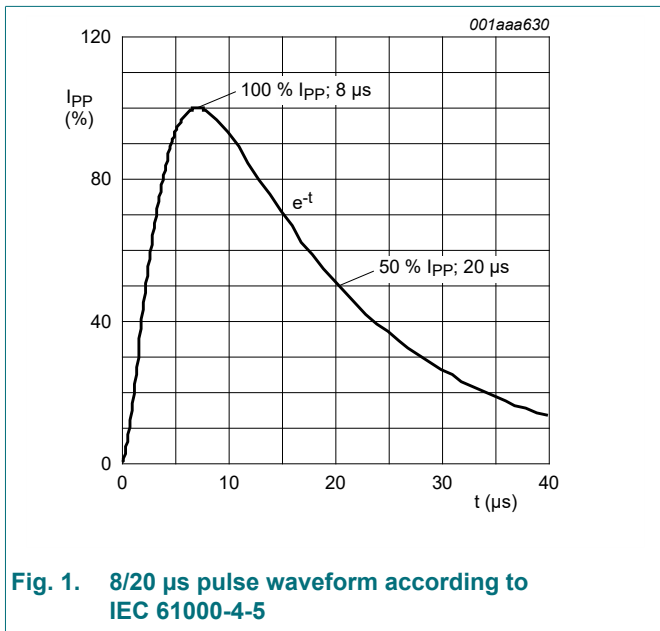
## 8. Limiting values

**Table 5. Limiting values**

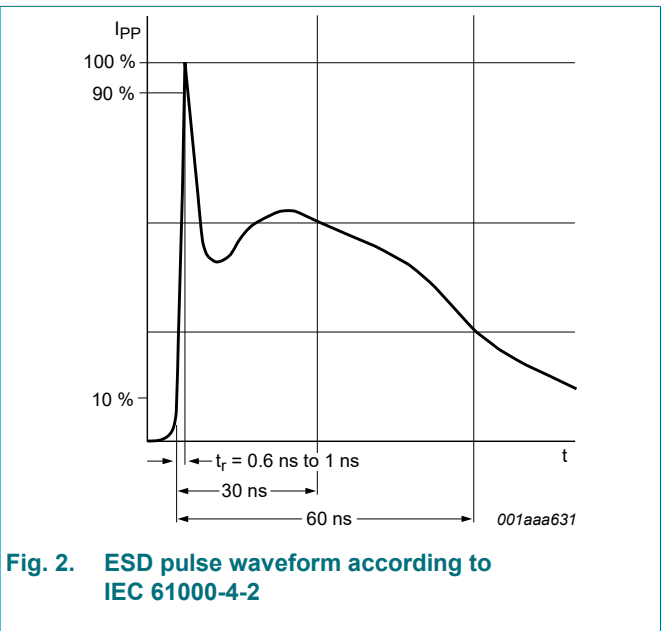
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
P <sub>PPM</sub>	rated peak pulse power	t <sub>p</sub> = 8/20 μs	[1] [2]	-	3000	W
		t <sub>p</sub> = 10/1000 μs	[3] [2]	-	300	W
I <sub>PPM</sub>	rated peak pulse current	t <sub>p</sub> = 8/20 μs	[1] [2]	-	97	A
		t <sub>p</sub> = 10/1000 μs	[3] [2]	-	10.3	A
T <sub>j</sub>	junction temperature			-	150	°C
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C
<b>ESD maximum ratings</b>						
V <sub>ESD</sub>	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[4] [2]	-	30	kV
		IEC 61000-4-2; air discharge	[4] [2]	-	30	kV

- [1] In accordance with IEC 61000-4-5 and IEC 61643-321 (8/20 μs current waveform).
- [2] Measured from pin 1 and 2 to pin 3.
- [3] In accordance with IEC 61643-321 (10/1000 μs current waveform).
- [4] Device stressed with ten non-repetitive ESD pulses.



**Fig. 1. 8/20 μs pulse waveform according to IEC 61000-4-5**



**Fig. 2. ESD pulse waveform according to IEC 61000-4-2**

### 9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{RWM}$	reverse standoff voltage	$T_j = 25\text{ }^\circ\text{C}$	-	-	18	V
$V_{BR}$	breakdown voltage	$I_R = 1\text{ mA}$	20	21	22.1	V
$I_{RM}$	reverse leakage current	$V_{RWM} = 18\text{ V}$	-	1	50	nA
$C_d$	diode capacitance	$f = 1\text{ MHz}; V_R = 0\text{ V}$	-	830	-	pF
$V_{CL}$	clamping voltage	$I_{PPM} = 97\text{ A}; t_p = 8/20\text{ }\mu\text{s}$	[1] [2]	-	32	V
		$I_{PPM} = 10.3\text{ A}; t_p = 10/1000\text{ }\mu\text{s}$	[3] [2]	-	29.2	V

- [1] In accordance with IEC 61000-4-5 and IEC 61643-321 (8/20  $\mu\text{s}$  current waveform).
- [2] Measured from pin 1 and 2 to pin 3.
- [3] In accordance with IEC 61643-321 (10/1000  $\mu\text{s}$  current waveform).

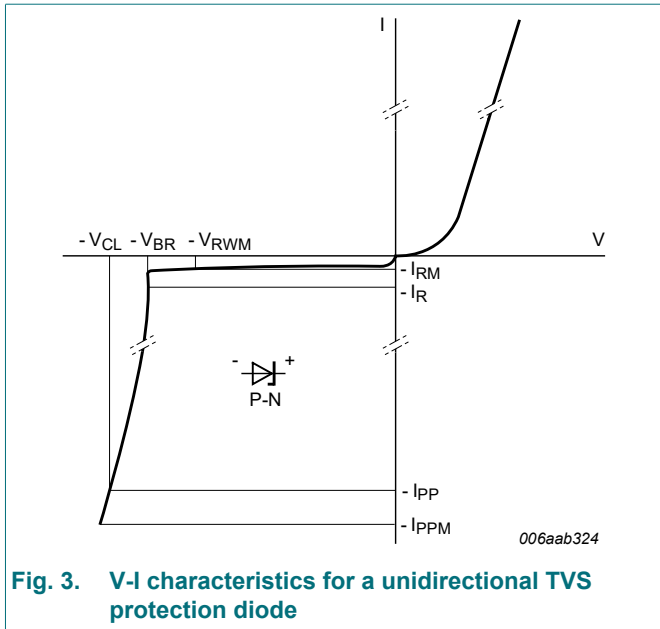


Fig. 3. V-I characteristics for a unidirectional TVS protection diode

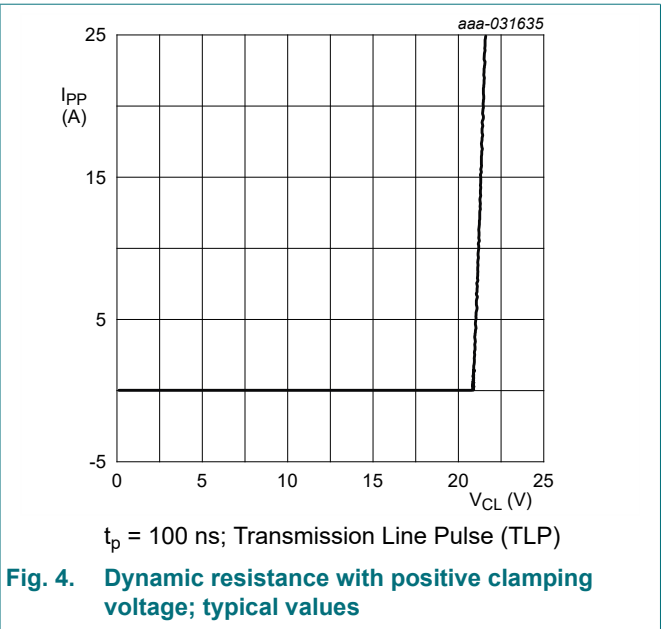


Fig. 4. Dynamic resistance with positive clamping voltage; typical values

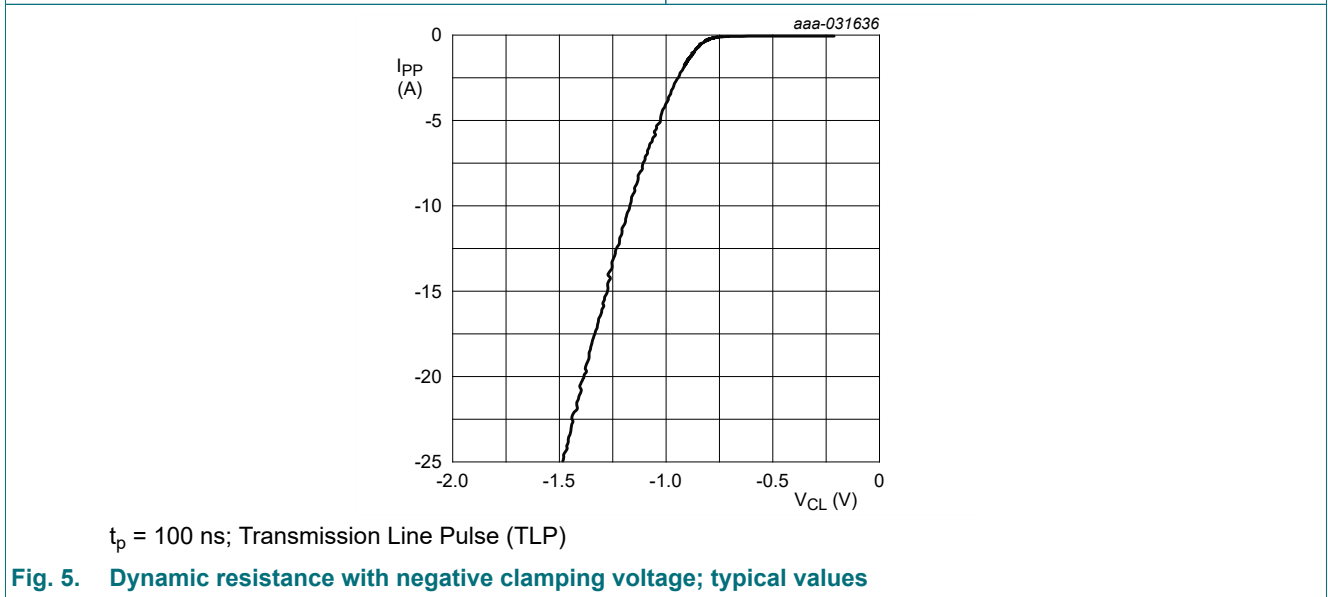


Fig. 5. Dynamic resistance with negative clamping voltage; typical values

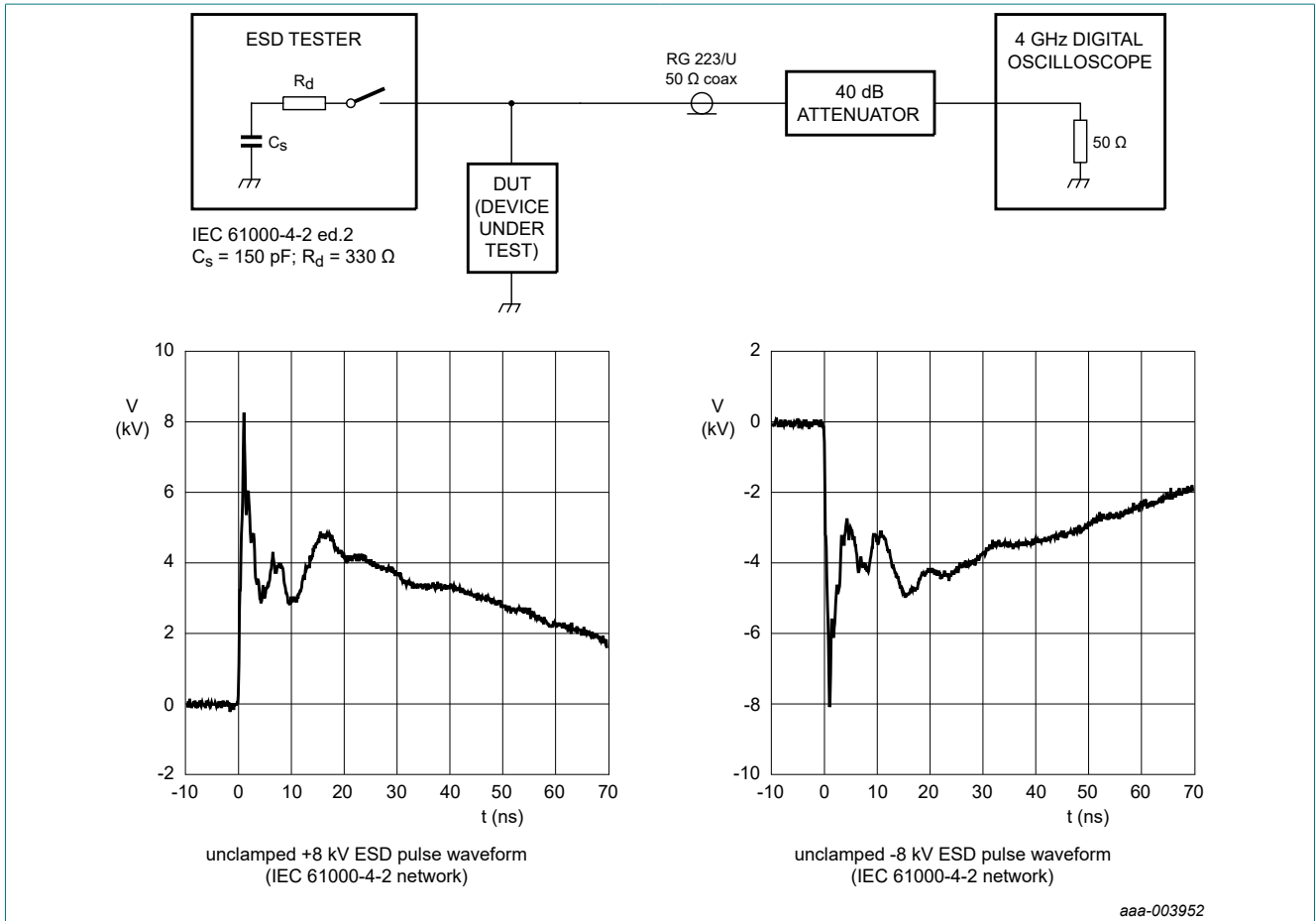


Fig. 6. ESD clamping test setup and waveforms

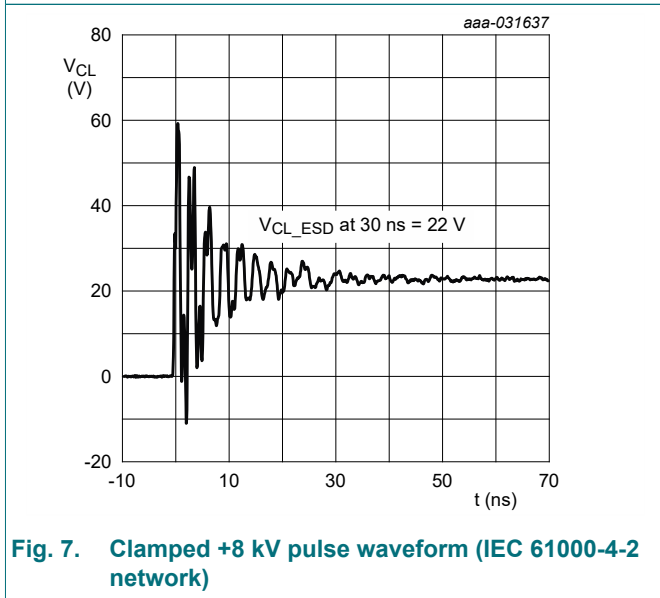


Fig. 7. Clamped +8 kV pulse waveform (IEC 61000-4-2 network)

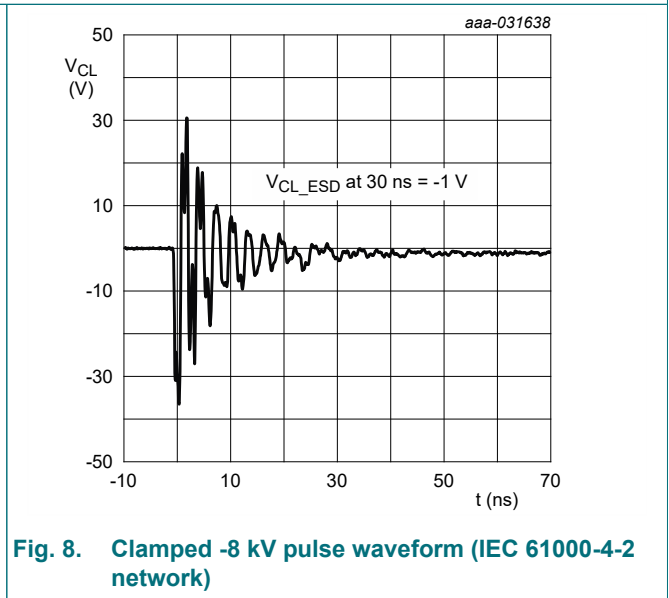
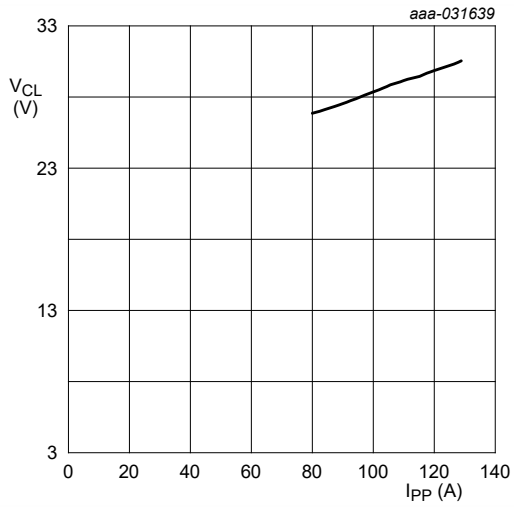
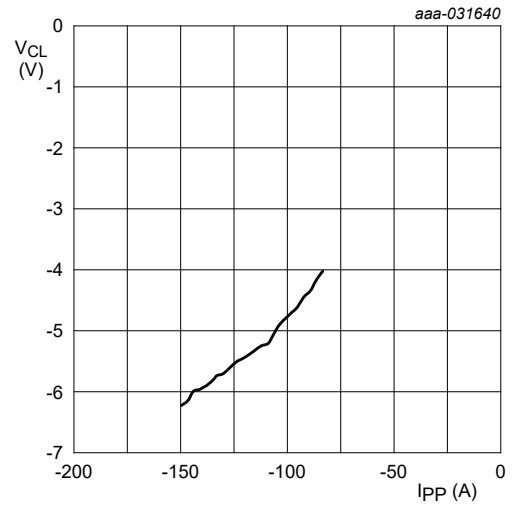


Fig. 8. Clamped -8 kV pulse waveform (IEC 61000-4-2 network)



$t_p = 8/20 \mu s$ ; according to IEC 61000-4-5

**Fig. 9. Positive clamping voltage (8/20 μs pulse); typical values**

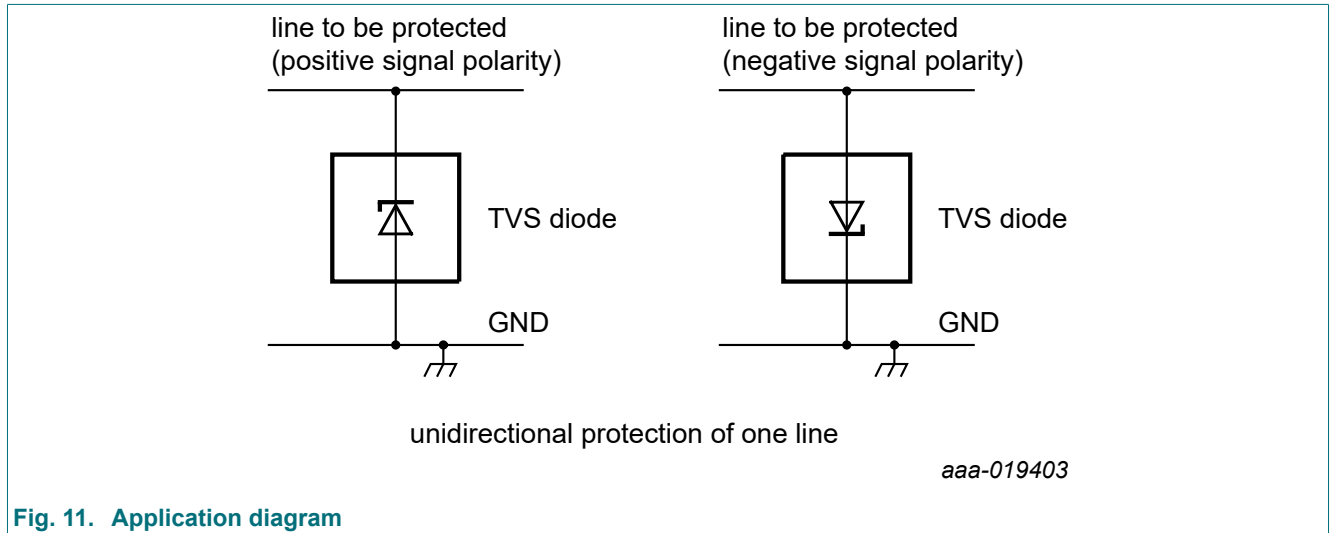


$t_p = 8/20 \mu s$ ; according to IEC 61000-4-5

**Fig. 10. Negative clamping voltage (8/20 μs pulse); typical values**

## 10. Application information

The device is designed for the protection of one unidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are either positive or negative with respect to ground.



**Fig. 11. Application diagram**

### Circuit board layout and protection device placement

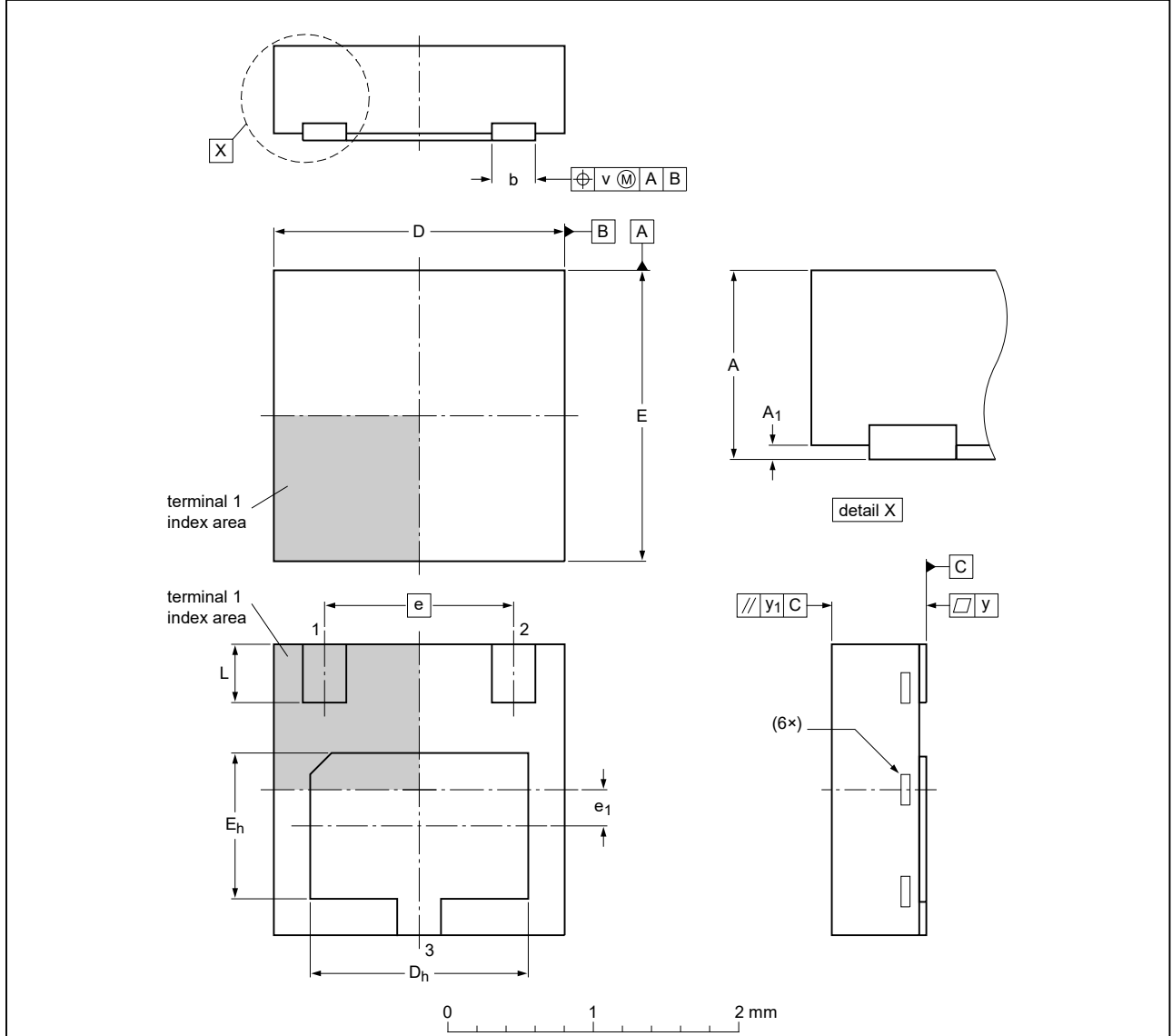
Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Package outline

HUSON3: plastic thermal enhanced ultra thin small outline package; no leads;  
3 terminals; body 2 x 2 x 0.65 mm

SOT1061



Dimensions

Unit	A <sup>(1)</sup>	A <sub>1</sub>	b	D	D <sub>h</sub>	E	E <sub>h</sub>	e	e <sub>1</sub>	L	v	y	y <sub>1</sub>
mm	max	0.65	0.04	0.35	2.1	1.6	2.1	1.1	0.3	0.45			
	nom			2.0		2.0		1.3			0.1	0.05	0.05
	min		0.25	1.9	1.4	1.9	0.9	0.2	0.35				

Note

1. Including plating thickness

sot1061\_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1061		---			08-02-04 08-10-07

Fig. 12. Package outline DFN2020-3 (SOT1061)



## 12. Soldering

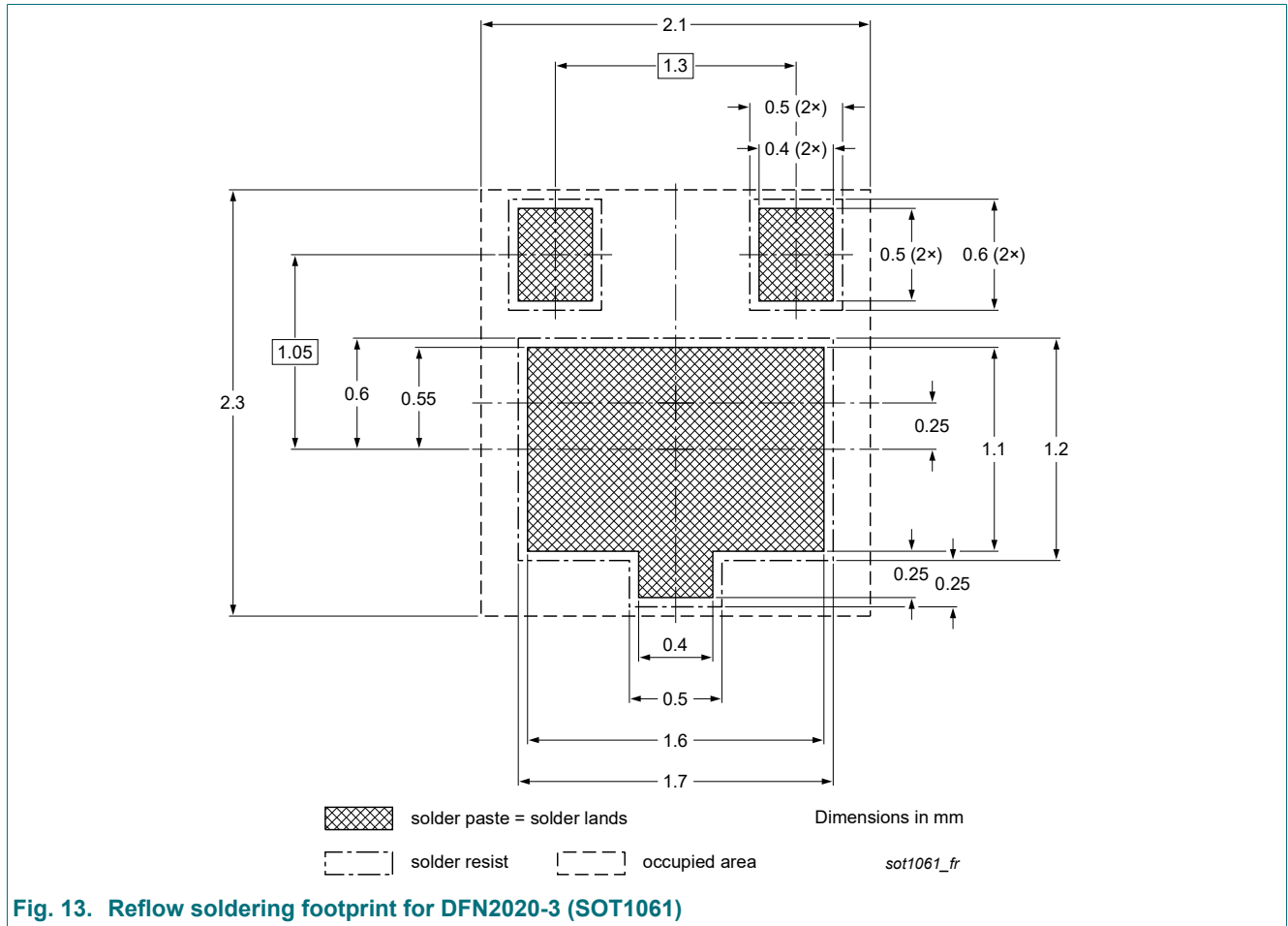


Fig. 13. Reflow soldering footprint for DFN2020-3 (SOT1061)

### 13. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PTVS18VU1UPA v.1	20200519	Product data sheet	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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