

# 74HC4020; 74HCT4020

## 14-stage binary ripple counter

Rev. 8 — 7 September 2021

Product data sheet

## 1. General description

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The 74HC4020; 74HCT4020 is a 14-stage binary ripple counter with a clock input ( $\overline{CP}$ ), an overriding asynchronous master reset input (MR) and 12 buffered parallel outputs (Q0, and Q3 to Q13). The counter advances on the HIGH-to-LOW transition of  $\overline{CP}$ . A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of  $\overline{CP}$ . Each counter stage is a static toggle flip-flop. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

## 2. Features and benefits

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- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- Input levels:
  - For 74HC4020: CMOS level
  - For 74HCT4020: TTL level
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

## 3. Applications

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- Frequency dividing circuits
- Time delay circuits
- Control counters

### 4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC4020D 74HCT4020D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC4020PW 74HCT4020PW				TSSOP16
74HC4020BQ 74HCT4020BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

### 5. Functional diagram

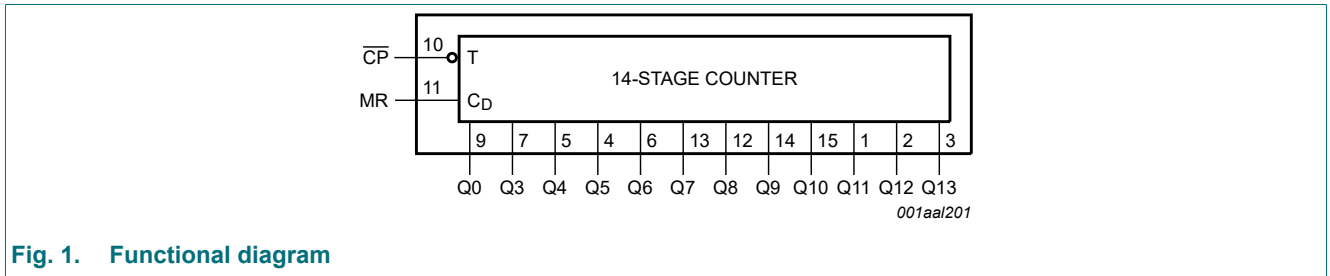


Fig. 1. Functional diagram

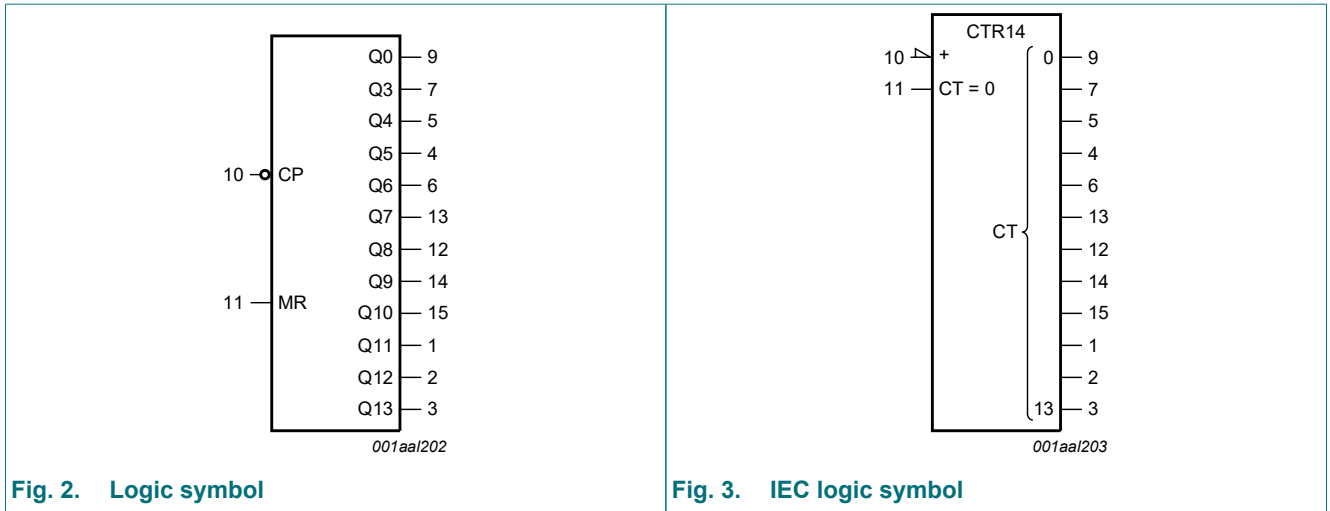


Fig. 2. Logic symbol

Fig. 3. IEC logic symbol

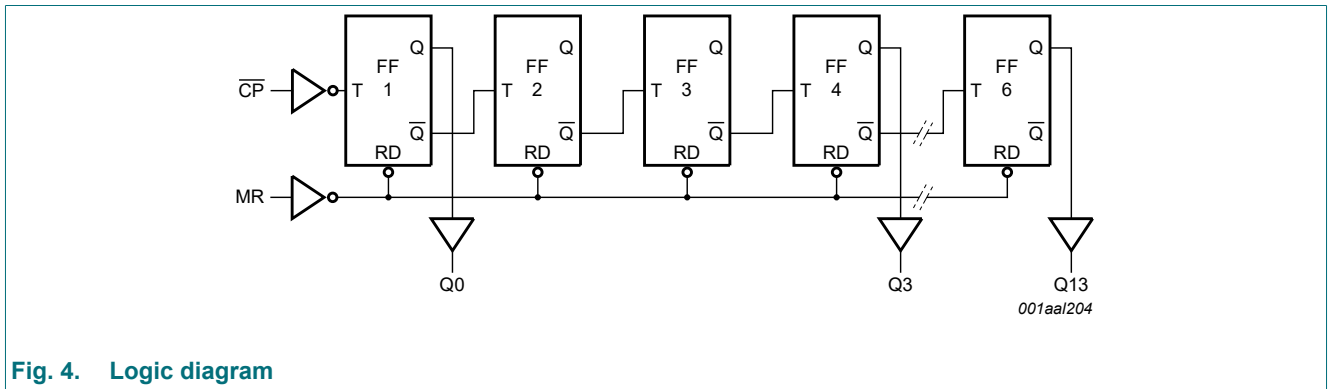


Fig. 4. Logic diagram

## 6. Pinning information

### 6.1. Pinning

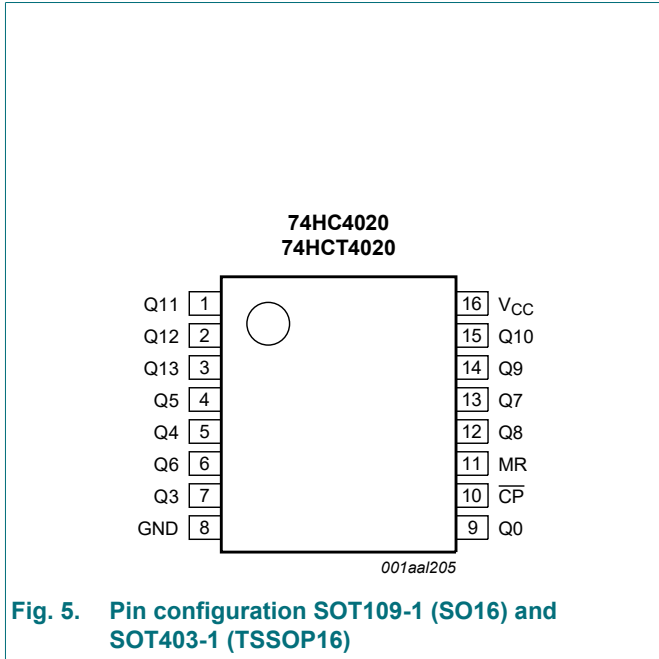


Fig. 5. Pin configuration SOT109-1 (SO16) and SOT403-1 (TSSOP16)

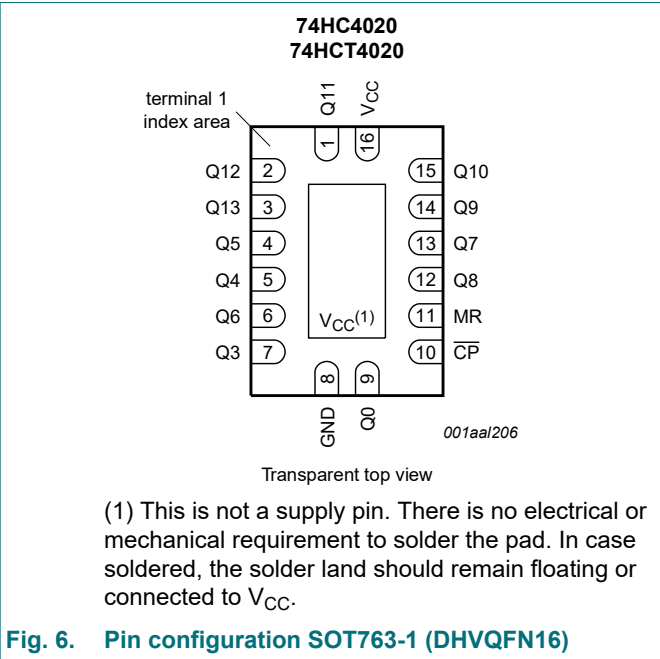


Fig. 6. Pin configuration SOT763-1 (DHVQFN16)

### 6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
Q0, Q3 to Q13	9, 7, 5, 4, 6, 13, 12, 14, 15, 1, 2, 3	output
GND	8	ground (0 V)
CP	10	clock input (HIGH-to-LOW, edge-triggered)
MR	11	master reset input (active HIGH)
V <sub>CC</sub>	16	positive supply voltage

## 7. Functional description

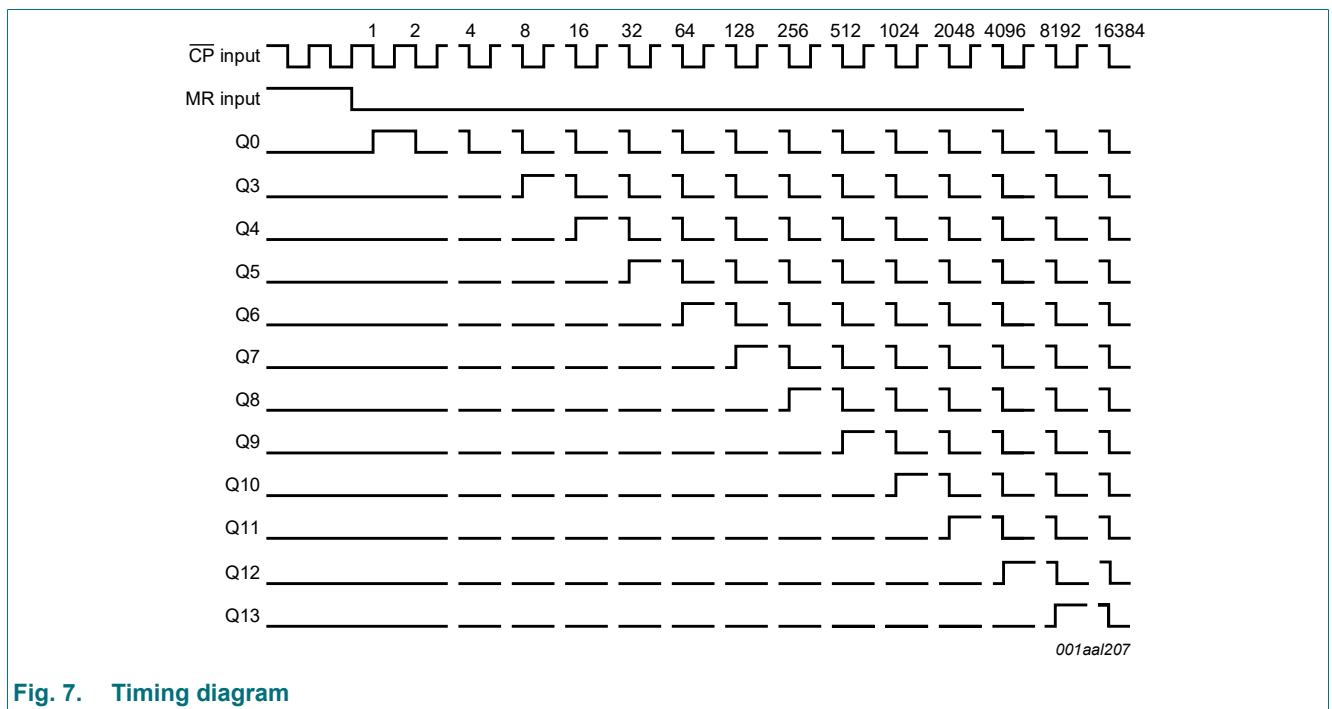
**Table 3. Function table**

H = HIGH voltage level; L = LOW voltage level; X = don't care;

↑ = LOW-to-HIGH clock transition; ↓ = HIGH-to-LOW clock transition.

Input		Output
CP	MR	Q0, Q3 to Q13
↑	L	no change
↓	L	count
X	H	L

### 7.1. Timing diagram



**Fig. 7. Timing diagram**

## 8. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_{OK}$	output clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_O$	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	-	$\pm 25$	mA
$I_{CC}$	supply current		-	$\pm 50$	mA
$I_{GND}$	ground current		-	$\pm 50$	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [1]	-	500	mW

- [1] For SOT109-1 (SO16) package:  $P_{tot}$  derates linearly with 12.4 mW/K above 110 °C.  
 For SOT403-1 (TSSOP16) package:  $P_{tot}$  derates linearly with 8.5 mW/K above 91 °C.  
 For SOT763-1 (DHVQFN16) package:  $P_{tot}$  derates linearly with 11.2 mW/K above 106 °C.

## 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	74HC4020			74HCT4020			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$\Delta t/\Delta V$	input transition rise and fall rate	except for Schmitt trigger inputs							
		$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V
$T_{amb}$	ambient temperature		-40	+25	+125	-40	+25	+125	°C

## 10. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC4020</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	-	±1	-	±1	μA
		V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	8.0	-	80	-	160	μA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HCT4020</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 20 µA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±0.1	-	±1	-	±1	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	8.0	-	80	-	160	µA
ΔI <sub>CC</sub>	additional supply current	V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; I <sub>O</sub> = 0 A; other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 4.5 V to 5.5 V								
		pin MR	-	110	396	-	495	-	539	µA
		pin $\overline{CP}$	-	85	306	-	383	-	417	µA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF

## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**

GND (ground = 0 V); C<sub>L</sub> = 50 pF unless otherwise specified; for test circuit, see Fig. 10

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC4020</b>										
t <sub>pd</sub>	propagation delay	$\overline{CP}$ to Q <sub>0</sub> ; see Fig. 8 [1]								
		V <sub>CC</sub> = 2.0 V	-	39	140	-	175	-	210	ns
		V <sub>CC</sub> = 4.5 V	-	14	28	-	35	-	42	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	11	-	-	-	-	-	ns
		V <sub>CC</sub> = 6.0 V	-	11	24	-	30	-	36	ns
		Q <sub>n</sub> to Q <sub>n+1</sub> ; see Fig. 9								
		V <sub>CC</sub> = 2.0 V	-	22	75	-	95	-	110	ns
		V <sub>CC</sub> = 4.5 V	-	8	15	-	19	-	22	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	6	-	-	-	-	-	ns
V <sub>CC</sub> = 6.0 V	-	6	13	-	16	-	19	ns		
t <sub>PHL</sub>	HIGH to LOW propagation delay	MR to Q <sub>n</sub> ; see Fig. 8								
		V <sub>CC</sub> = 2.0 V	-	55	170	-	215	-	225	ns
		V <sub>CC</sub> = 4.5 V	-	20	34	-	43	-	51	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	17	-	-	-	-	-	ns
		V <sub>CC</sub> = 6.0 V	-	16	29	-	37	-	43	ns

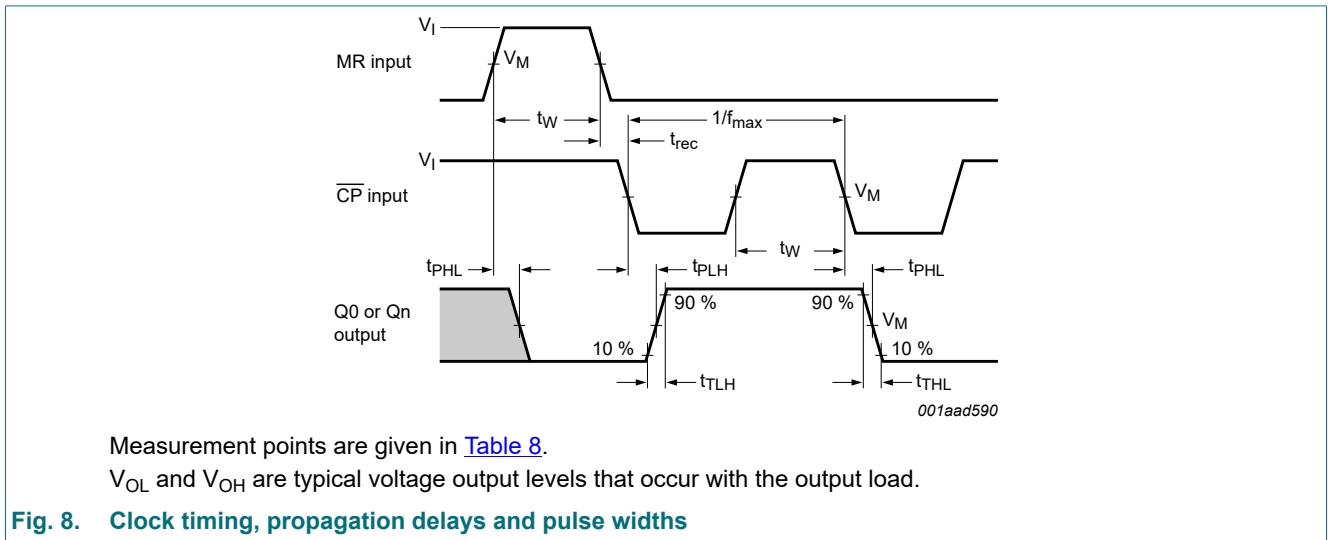
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t <sub>t</sub>	transition time	Q <sub>n</sub> ; see Fig. 8 [2]								
		V <sub>CC</sub> = 2.0 V	-	19	75	-	95	-	110	ns
		V <sub>CC</sub> = 4.5 V	-	7	15	-	19	-	22	ns
		V <sub>CC</sub> = 6.0 V	-	6	13	-	16	-	19	ns
t <sub>W</sub>	pulse width	CP HIGH or LOW; see Fig. 8								
		V <sub>CC</sub> = 2.0 V	80	14	-	100	-	120	-	ns
		V <sub>CC</sub> = 4.5 V	16	4	-	20	-	24	-	ns
		V <sub>CC</sub> = 6.0 V	14	3	-	17	-	20	-	ns
		MR HIGH; see Fig. 8								
		V <sub>CC</sub> = 2.0 V	80	17	-	100	-	120	-	ns
		V <sub>CC</sub> = 4.5 V	16	6	-	20	-	24	-	ns
V <sub>CC</sub> = 6.0 V	14	5	-	17	-	20	-	ns		
t <sub>rec</sub>	recovery time	MR to CP; see Fig. 8								
		V <sub>CC</sub> = 2.0 V	50	6	-	65	-	75	-	ns
		V <sub>CC</sub> = 4.5 V	10	2	-	13	-	15	-	ns
		V <sub>CC</sub> = 6.0 V	9	2	-	11	-	13	-	ns
f <sub>max</sub>	maximum frequency	see Fig. 8								
		V <sub>CC</sub> = 2.0 V	6.0	30	-	4.8	-	4.0	-	MHz
		V <sub>CC</sub> = 4.5 V	30	92	-	24	-	20	-	MHz
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	101	-	-	-	-	-	MHz
V <sub>CC</sub> = 6.0 V	35	109	-	28	-	24	-	MHz		
C <sub>PD</sub>	power dissipation capacitance	[3]	-	19	-	-	-	-	-	pF
<b>74HCT4020</b>										
t <sub>pd</sub>	propagation delay	CP to Q <sub>0</sub> ; see Fig. 8 [1]								
		V <sub>CC</sub> = 4.5 V	-	18	36	-	45	-	54	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	15	-	-	-	-	-	ns
		Q <sub>n</sub> to Q <sub>n+1</sub> ; see Fig. 9								
		V <sub>CC</sub> = 4.5 V	-	8	15	-	19	-	22	ns
V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	6	-	-	-	-	-	ns		
t <sub>PHL</sub>	HIGH to LOW propagation delay	MR to Q <sub>n</sub> ; see Fig. 8								
		V <sub>CC</sub> = 4.5 V	-	22	45	-	56	-	68	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	19	-	-	-	-	-	ns
t <sub>t</sub>	transition time	Q <sub>n</sub> ; see Fig. 8 [2]								
		V <sub>CC</sub> = 4.5 V	-	7	15	-	19	-	22	ns
t <sub>W</sub>	pulse width	CP HIGH or LOW; see Fig. 8								
		V <sub>CC</sub> = 4.5 V	20	7	-	25	-	30	-	ns
		MR HIGH; see Fig. 8								
V <sub>CC</sub> = 4.5 V	20	8	-	25	-	30	-	ns		
t <sub>rec</sub>	recovery time	MR to CP; see Fig. 8								
		V <sub>CC</sub> = 4.5 V	10	2	-	13	-	15	-	ns



Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
f <sub>max</sub>	maximum frequency	see Fig. 8								
		V <sub>CC</sub> = 4.5 V	25	47	-	20	-	17	-	MHz
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	52	-	-	-	-	-	MHz
C <sub>PD</sub>	power dissipation capacitance	[3]	-	20	-	-	-	-	-	pF

- [1] t<sub>pd</sub> is the same as t<sub>PHL</sub> and t<sub>PLH</sub>.
- [2] t<sub>i</sub> is the same as t<sub>THL</sub> and t<sub>TLH</sub>.
- [3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz;  
 f<sub>o</sub> = output frequency in MHz;  
 Σ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs;  
 C<sub>L</sub> = output load capacitance in pF;  
 V<sub>CC</sub> = supply voltage in V.

### 11.1. Waveforms and test circuit



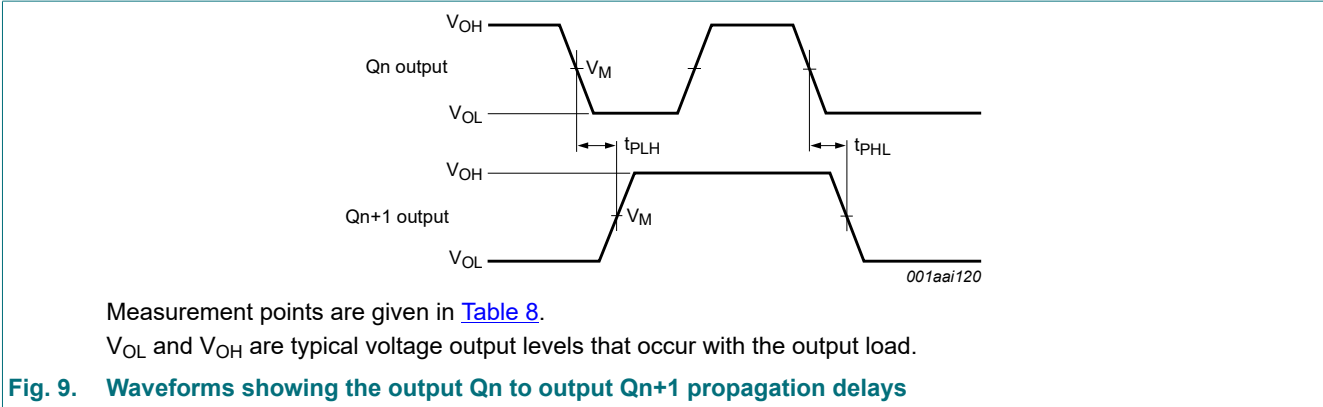


Table 8. Measurement points

Type	Input	Output
	$V_M$	$V_M$
74HC4020	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74HCT4020	1.3 V	1.3 V

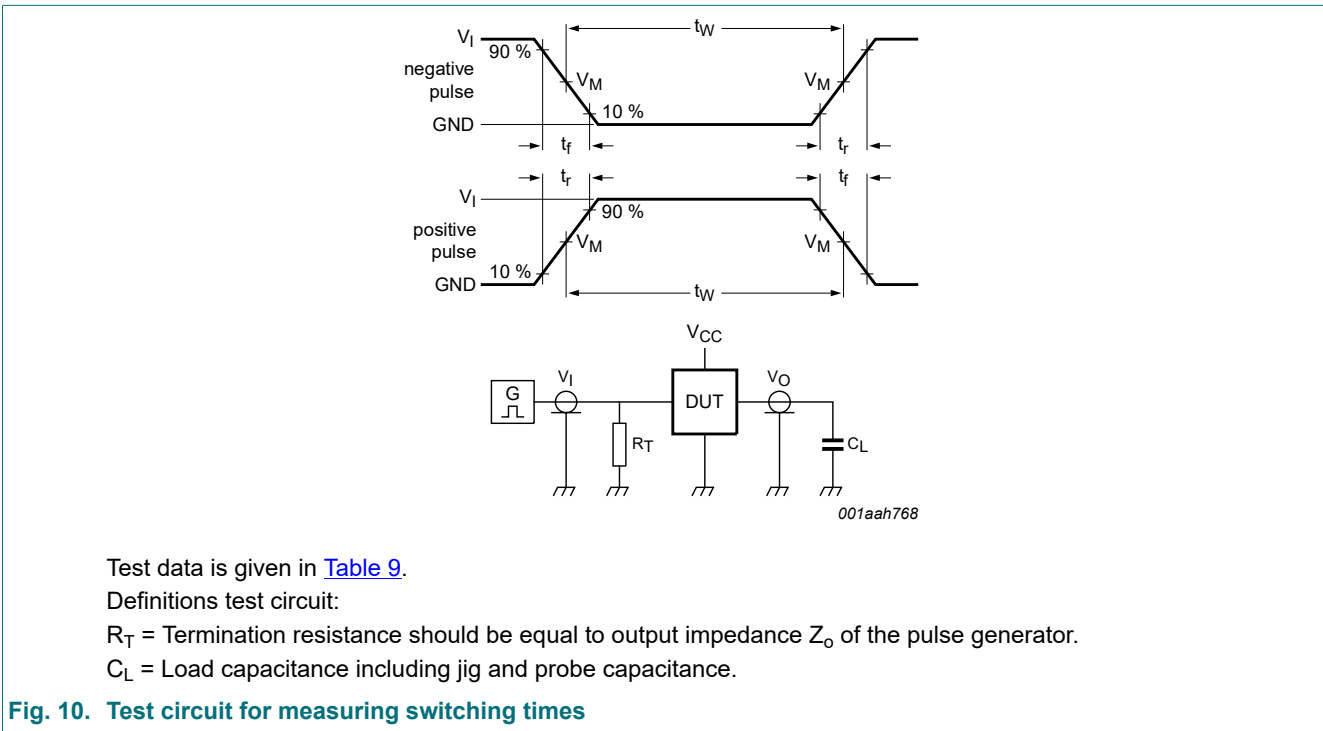


Table 9. Test data

Type	Input		Load
	$V_I$	$t_r, t_f$	$C_L$
74HC4020	$V_{CC}$	6 ns	15 pF, 50 pF
74HCT4020	3 V	6 ns	15 pF, 50 pF

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

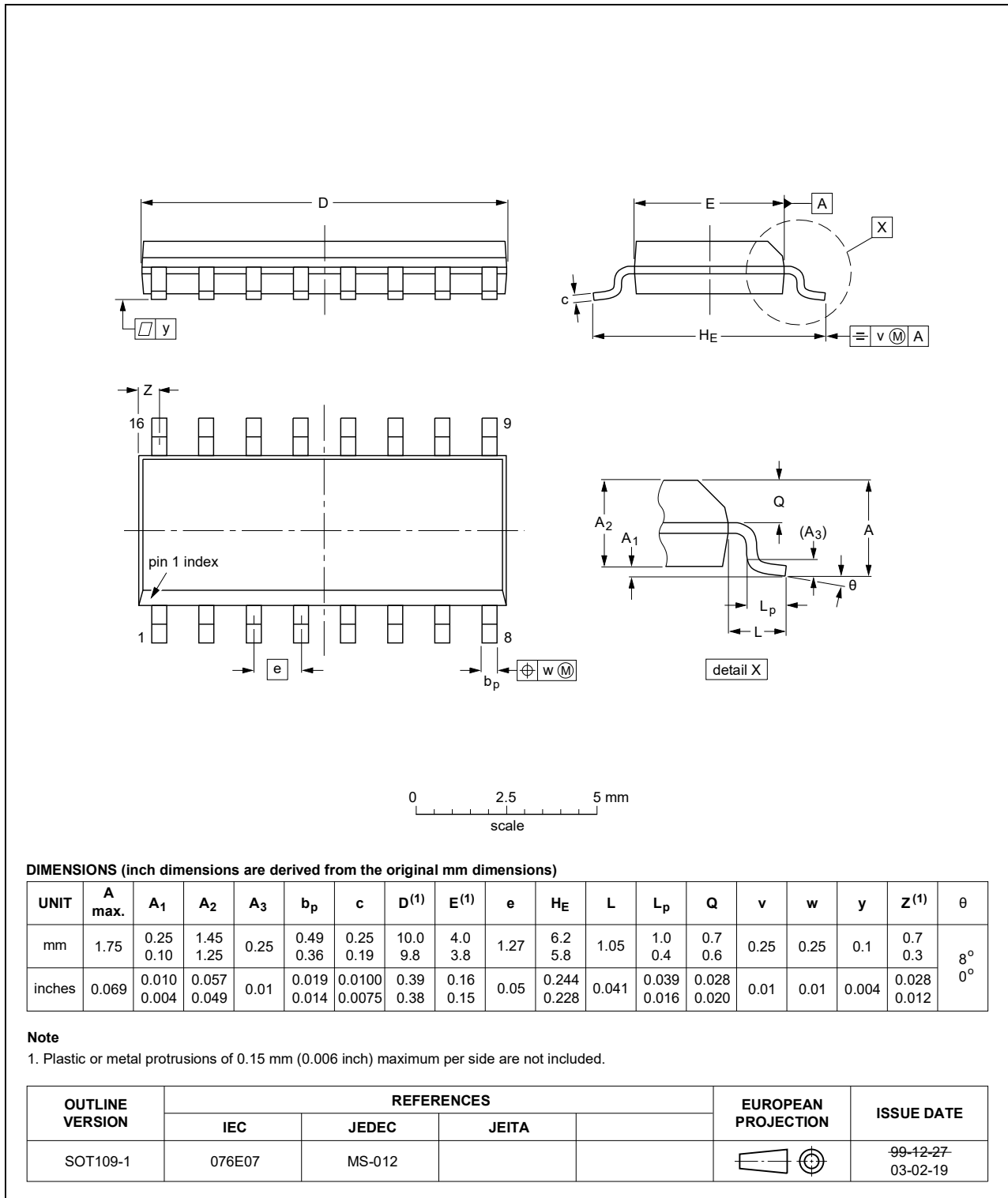


Fig. 11. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

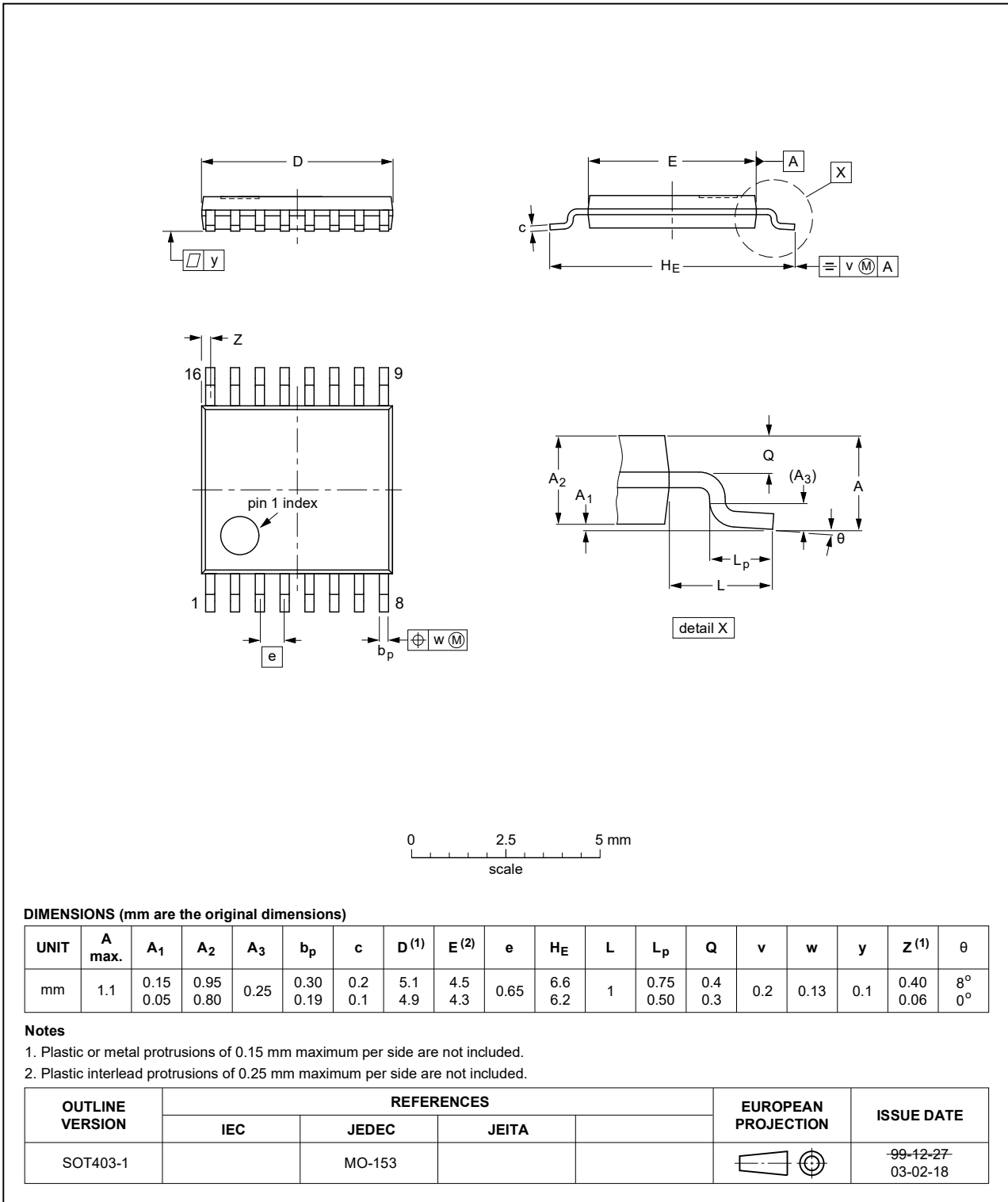


Fig. 12. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

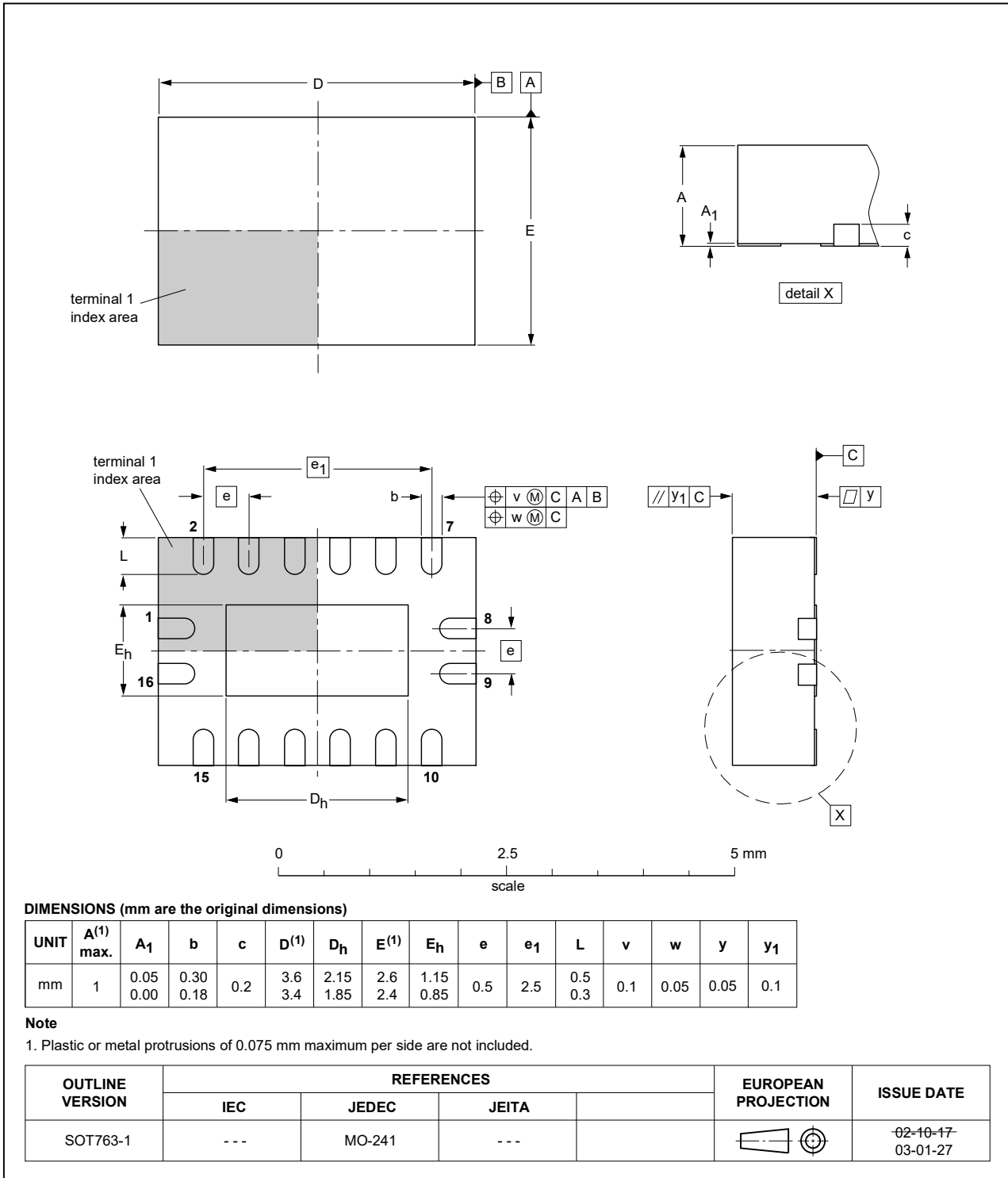


Fig. 13. Package outline SOT763-1 (DHVQFN16)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4020 v.8	20210907	Product data sheet	-	74HC_HCT4020 v.7
Modifications:	<ul style="list-style-type: none"> <li>Type number 74HC4020DB (SOT338-1/SSOP16) removed.</li> </ul>			
74HC_HCT4020 v.7	20200618	Product data sheet	-	74HC_HCT4020 v.6
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type number 74HCT4020DB (SOT338-1/SSOP16) removed.</li> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li><a href="#">Table 4</a>: Derating values for <math>P_{tot}</math> total power dissipation have been updated.</li> </ul>			
74HC_HCT4020 v.6	20160203	Product data sheet	-	74HC_HCT4020 v.5
Modifications:	<ul style="list-style-type: none"> <li>Type numbers 74HC4020N and 74HCT4020N (SOT38-4) removed.</li> </ul>			
74HC_HCT4020 v.5	20120806	Product data sheet	-	74HC_HCT4020 v.4
Modifications:	<ul style="list-style-type: none"> <li>Measurement points added to <a href="#">Fig. 8</a> (errata).</li> </ul>			
74HC_HCT4020 v.4	20111213	Product data sheet	-	74HC_HCT4020 v.3
Modifications:	<ul style="list-style-type: none"> <li>Legal pages updated.</li> </ul>			
74HC_HCT4020 v.3	20100120	Product data sheet	-	74HC_HCT4020 v.2
74HC_HCT4020 v.2	19970901	Product specification	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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