

# SAF360x

## Digital radio and processing system-on-chip

Rev. 3 — 23 January 2015

Product short data sheet



## 1. General description

The SAF360x is a monolithic integrated digital terrestrial radio processor. The SAF360x family includes different chip variants—SAF3600, SAF3601, SAF3602, SAF3604, SAF3606, SAF3607. The SAF360x provides reception, demodulation, audio decoding and application processing for various digital radio standards.

The SAF360x system-on-chip (SoC) is a next generation HD Radio/DAB/DAB+/T-DMB/DRM solution for breakthrough in system integration and cost reduction. The chip is qualified in accordance with AEC-Q100 and includes the following features:

- Next generation HD Radio / DAB / DAB+ / T-DMB / DRM solution for breakthrough in system cost reduction
- Dual channel processing with on-chip dual DAB front-end, memory and source decoding
- End-of-production line programmability
- DAB-FM / DAB-DAB blending
- Advanced reception improvement algorithms
- Integrated antenna splitter enabling antenna diversity
- On chip voltage regulation for performance critical Front-end supply via an external transistor from 3.3 V (SAF3601, SAF3602, SAF3604, SAF3606 only)
- Single system XTAL with optional clock reference output capabilities
- Small PCB footprint using state-of-the-art BGA package

## 2. Features and benefits

### 2.1 HD Radio technology

- HD Radio signal decoding for AM and FM digital audio
- Supports HD Radio single, dual and triple tuner use cases
- HD all-digital mode support
- SAF3604: On-chip FM-tuner for data service reception
- Dual baseband input interface using I<sup>2</sup>S-bus derivative with I/Q
- Secondary baseband interface for dual tuner applications
- Data services support for HD Radio reception
- Electronic Program Guide (EPG)
- Off-chip LOT processing
- Enhanced reception through Maximum Ratio Combining (MRC)



For detailed list of supported features, contact NXP Sales; see [Section 11](#).

## 2.2 DRM

- DRM signal decoding for AM and FM digital audio
- Prepared for dual DRM support with background scanning or data services from second station
- Frontend to baseband interface through serial I<sup>2</sup>S-bus type interface
- Prepared for secondary baseband interface for dual tuner applications
- Channel decoder reception improvements
- Supports xHE-AAC codec
- Prepared for DRM+

## 2.3 DAB, DAB+ and T-DMB radio technology

- Dual reception processing with on-chip dual DAB front-end, ADC, memory and source decoding
- Data service reception and filtering
- Full dual ensemble processing (2 × 1.8 Mbit/s)
- Optional third tuner input via serial I<sup>2</sup>S-bus type interface
- Integrated DAB-FM/ DAB-DAB time alignment and seamless blending
- Integrated support for all actual audio codecs (AAC, HE-AAC, MP2, BSAC)
- (Optional) Additional features:
  - ◆ Reception improvement algorithms for single antenna systems delivering additionally improved BER
  - ◆ Diversity reception improvement through advanced Maximum Ratio Combining (MRC) algorithms leveraging dual antenna diversity
  - ◆ Third external tuner supports enabling background service scan or data services in case of two primary Saturn tuners are used for antenna diversity reception

## 2.4 Digital audio

- Up to 6 channel (5.1) audio support through TDM audio interface or triple I<sup>2</sup>S
- Programmable audio sample rate converter (8 kHz to 48 kHz) for up to 6 channels
- I<sup>2</sup>S audio input for auxiliary processing
- Optional SRC (8 kHz to 48 kHz) for I<sup>2</sup>S-bus input
- Optional support for input and output 96 kHz sample rate conversion
- Basic audio processing for external digital audio sources
- Advanced audio processing (contact NXP for a list of supported audio processing features; see [Section 11](#))

## 2.5 Other peripheral interfaces

- Two I<sup>2</sup>C-bus interfaces
- Two Serial Peripheral Interfaces (SPI)
- One High-Speed Serial Peripheral Interface (HS-SPI)
- One UART interface
- 16 individual GPIO pins for applications and diagnostics

- One JTAG interface for diagnostics

## 2.6 Additional features

- Secure boot, image authentication
- Identical radio architecture with the same chip and specific software for various standards including DAB, HD Radio and DRM
- Radio control reuse from SAF356X with same API
- In field software upgrade possibility
- One internal clock oscillator and two internal Phase-Locked Loops (PLL)
- Powerful signal, audio processing core architecture
- Qualified in accordance with AEC-Q100

**Remark:** Not all features are available on all variants or in all combinations. Contact NXP sales for more information; see [Section 11 “Contact information”](#).

## 3. Applications

- Application depends on usages and reception standard

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Supply voltages</b>						
SAF3601, SAF3602, SAF3604, SAF3606						
V <sub>DDA(VREG)(3V3)</sub>	voltage regulator analog supply voltage		3.0	3.3	3.6	V
V <sub>DDA(ADPLL1)(1V8)</sub>	ADPLL1 analog supply voltage		1.71	1.8	1.89	V
V <sub>DDA(XTAL)(1V8)</sub>	crystal analog supply voltage		1.71	1.8	1.89	V
V <sub>DDA(DCO1)(1V8)</sub>	DCO1 analog supply voltage		1.58	1.8	1.89	V
V <sub>DDA(DIV)(1V8)</sub>	DIV analog supply voltage		1.71	1.8	1.89	V
V <sub>DDA(LVHFA)(1V8)</sub>	LVHFA analog supply voltage		1.71	1.8	1.89	V
V <sub>DDA(VHFM)(1V8)</sub>	VHFM analog supply voltage		1.71	1.8	1.89	V
V <sub>DDA(DCO2)(1V8)</sub>	DCO2 analog supply voltage		1.58	1.8	1.89	V
V <sub>DDA(ADPLL2)(1V8)</sub>	ADPLL2 analog supply voltage		1.71	1.8	1.89	V
V <sub>DDA(ADC)(1V8)</sub>	ADC analog supply voltage		1.71	1.8	1.89	V
V <sub>DDD(ADPLL1)(1V8)</sub>	ADPLL1 digital supply voltage		1.71	1.8	1.89	V
V <sub>DDD(ADPLL2)(1V8)</sub>	ADPLL2 digital supply voltage		1.71	1.8	1.89	V
V <sub>DDD(RFE)(1V8)</sub>	RFE digital supply voltage		1.71	1.8	1.89	V
V <sub>DD(IO)</sub>	input/output supply voltage		3.0	3.3	3.6	V
V <sub>QPS</sub>	OTP programming voltage (2.5 V)		2.25	2.5	2.7	V
V <sub>DD(A)</sub>	analog blocks supply voltage		1.14	1.2	1.26	V
V <sub>DD(C)</sub>	core supply voltage		1.14	1.2	1.26	V

Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>SAF3600, SAF3607</b>						
V <sub>DD(IO)</sub>	input/output supply voltage		3.0	3.3	3.6	V
V <sub>QPS</sub>	OTP programming voltage (2.5 V)		2.25	2.5	2.7	V
V <sub>DD(A)</sub>	analog blocks supply voltage		1.14	1.2	1.26	V
V <sub>DD(C)</sub>	core supply voltage		1.14	1.2	1.26	V
<b>Supply currents</b>						
<b>SAF3601, SAF3602, SAF3604, SAF3606</b>						
I <sub>DDA(XXX)</sub> + I <sub>DDD(XXX)</sub>	combined front-end supply currents	DAB 1.8 SW Stack	-	460	560	mA
I <sub>DD(A)</sub>	analog supply currents	DAB 1.8 SW Stack	-	15	20	mA
I <sub>DD(IO)</sub>	input/output supply current	DAB 1.8 SW Stack	-	40	55	mA
I <sub>DD(C)</sub>	core supply current	DAB 1.8 SW Stack	-	400	460	mA
<b>SAF3600, SAF3607</b>						
I <sub>DD(A)</sub>	analog supply currents	HD 1.5 SW Stack	-	15	20	mA
I <sub>DD(IO)</sub>	input/output supply current	HD 1.5 SW Stack	-	40	55	mA
I <sub>DD(C)</sub>	core supply current	HD 1.5 SW Stack	-	260	310	mA
<b>Power dissipation</b>						
<b>SAF3601, SAF3602, SAF3604, SAF3606</b>						
P <sub>tot</sub>	total power dissipation	DAB 1.8 SW Stack	-	1.53	1.93	W
<b>SAF3600, SAF3607</b>						
P <sub>tot</sub>	total power dissipation	HD 1.5 SW Stack	-	0.46	0.61	W

## 5. Ordering information

**Table 2. Ordering information**

Type number	Package		
	Name	Description	Version
SAF36xxEL/Vyyyz	LFBGA223	plastic low profile fine-pitch ball grid array package; 223 balls	SOT1322-1

**Table 3. Type overview**

Not all variants are commercially released. Please contact NXP Sales for further details.

Type number	Main application	Internal tuners	Clock
<b>HD subtypes</b>			
SAF3600EL/V1040	single tuner use case	No	55.46667 MHz
SAF3600EL/V1041	single tuner use case	No	10.4 MHz – 12.288 MHz
SAF3600EL/V1042	dual and triple tuner use cases	No	55.46667 MHz
SAF3600EL/V1043	dual and triple tuner use cases	No	10.4 MHz – 12.288 MHz
SAF3604EL/V3040	dual tuner use case with one internal tuner	Yes (one FM tuner)	55.46667 MHz
<b>DAB subtypes</b>			
SAF3601EL/V3040	single tuner use case	Yes (one DAB tuner)	55.19220 MHz, 55.46667 MHz
SAF3602EL/V3040	dual and triple tuner use cases	Yes (two DAB tuners)	55.19220 MHz, 55.46667 MHz
<b>DRM subtypes</b>			
SAF3607EL/V1040	single tuner use case	No	55.46667 MHz
SAF3607EL/V1041	single tuner use case	No	10.4 MHz – 12.288 MHz
<b>Premium</b>			
SAF3606EL/V3040	all standards (HD, DAB, DRM); single, dual and triple tuner use cases	Yes (two DAB tuners or one FM tuner)	55.19220 MHz, 55.46667 MHz

6. Block diagram

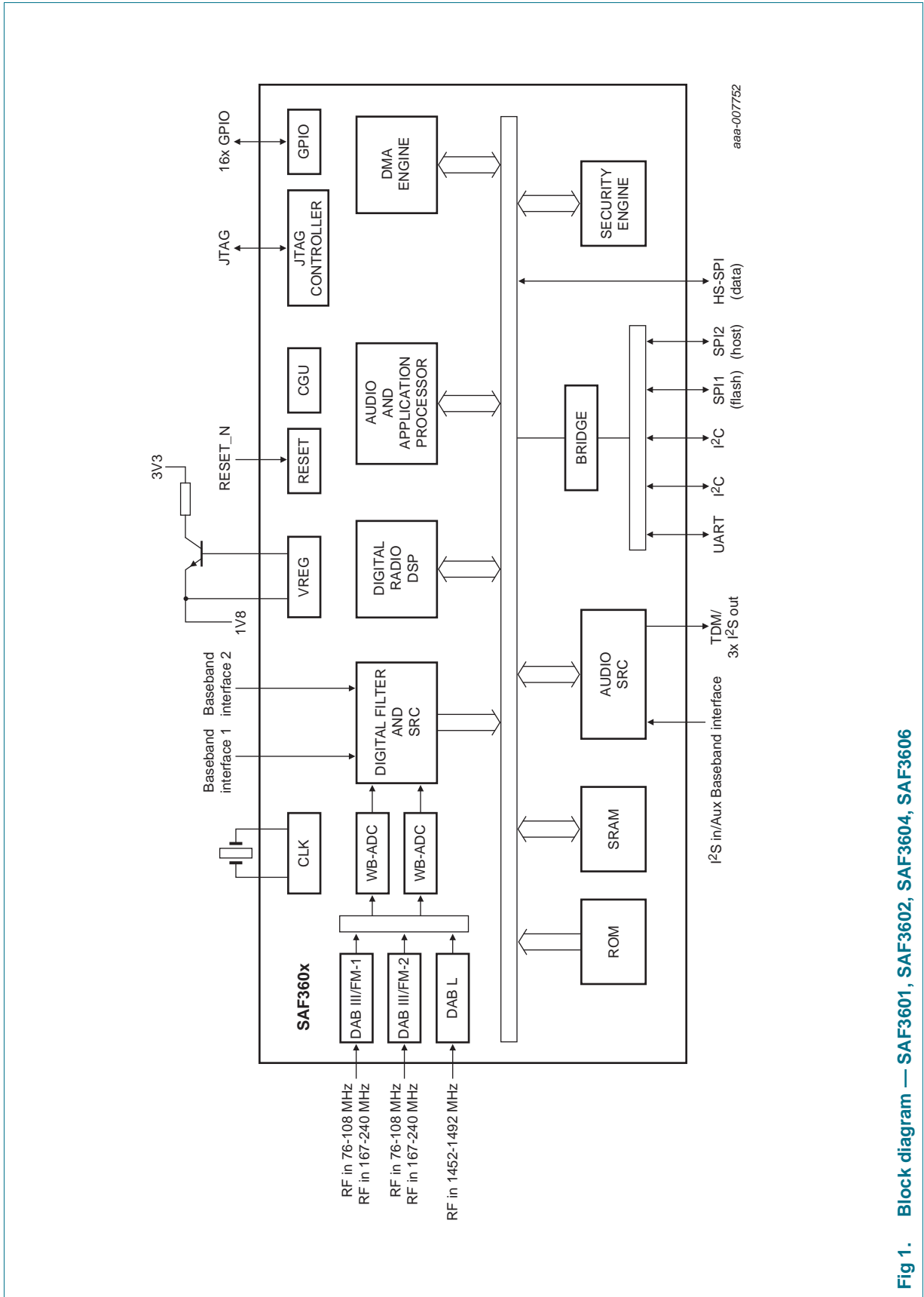


Fig 1. Block diagram — SAF3601, SAF3602, SAF3604, SAF3606

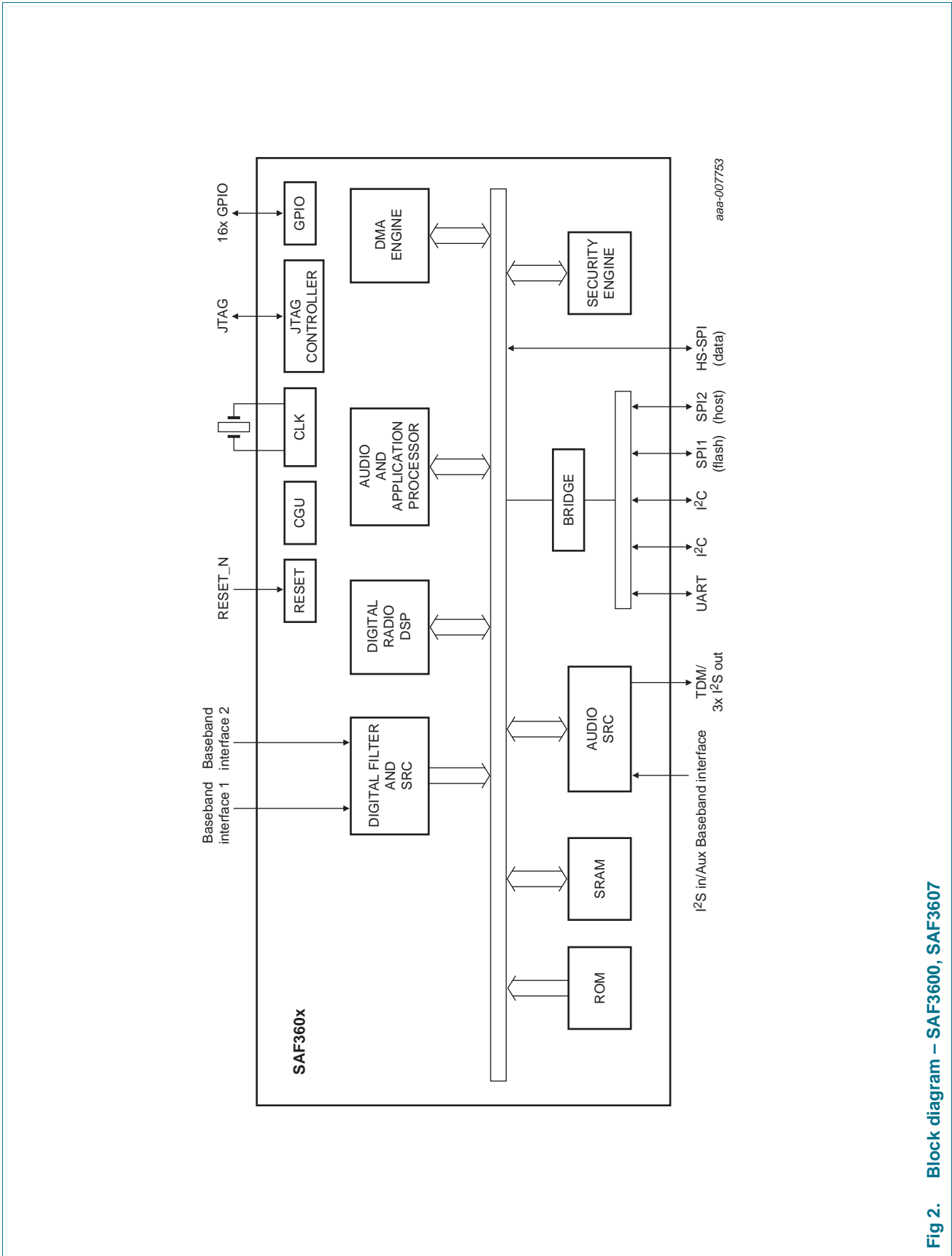


Fig 2. Block diagram – SAF3600, SAF3607

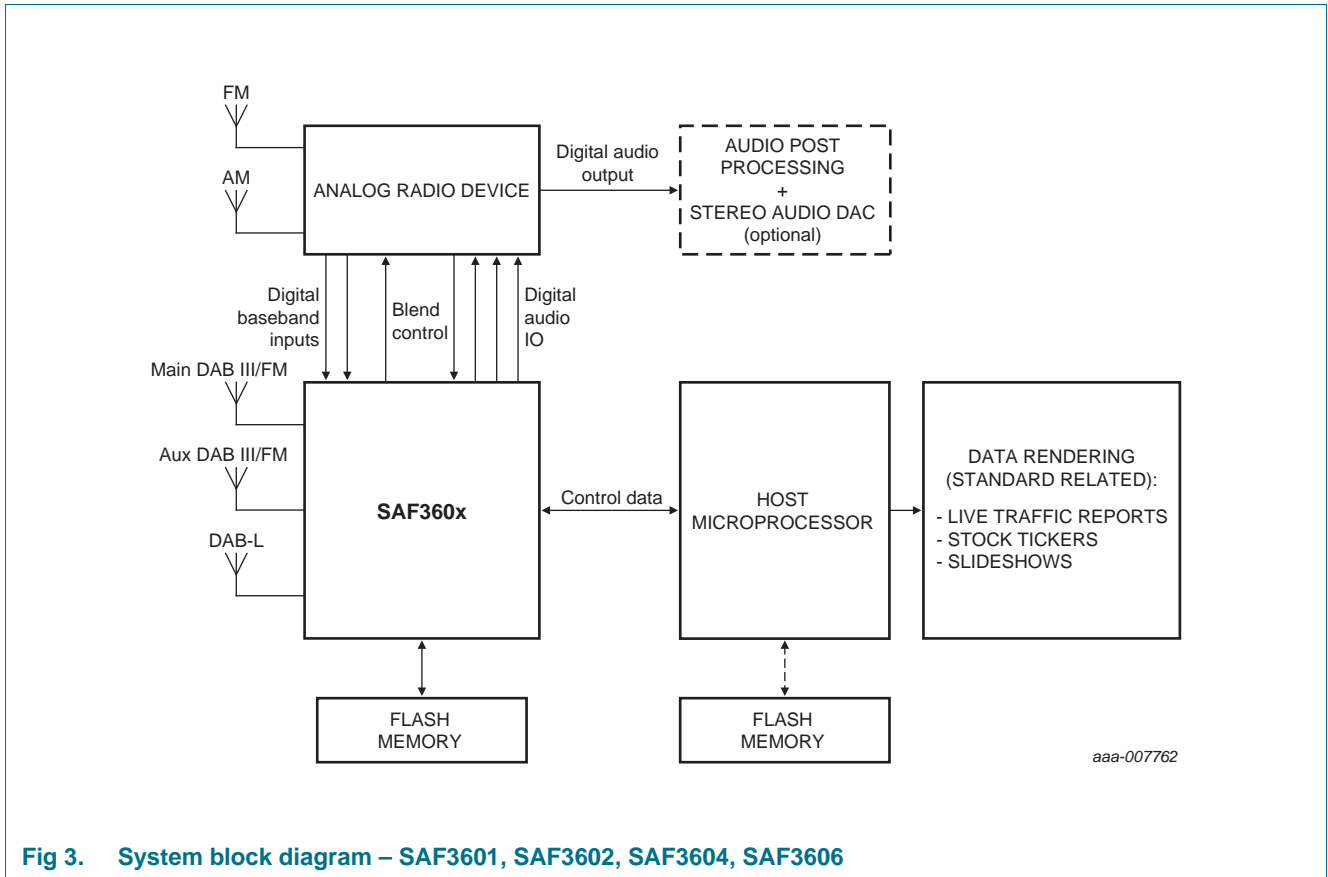


Fig 3. System block diagram – SAF3601, SAF3602, SAF3604, SAF3606

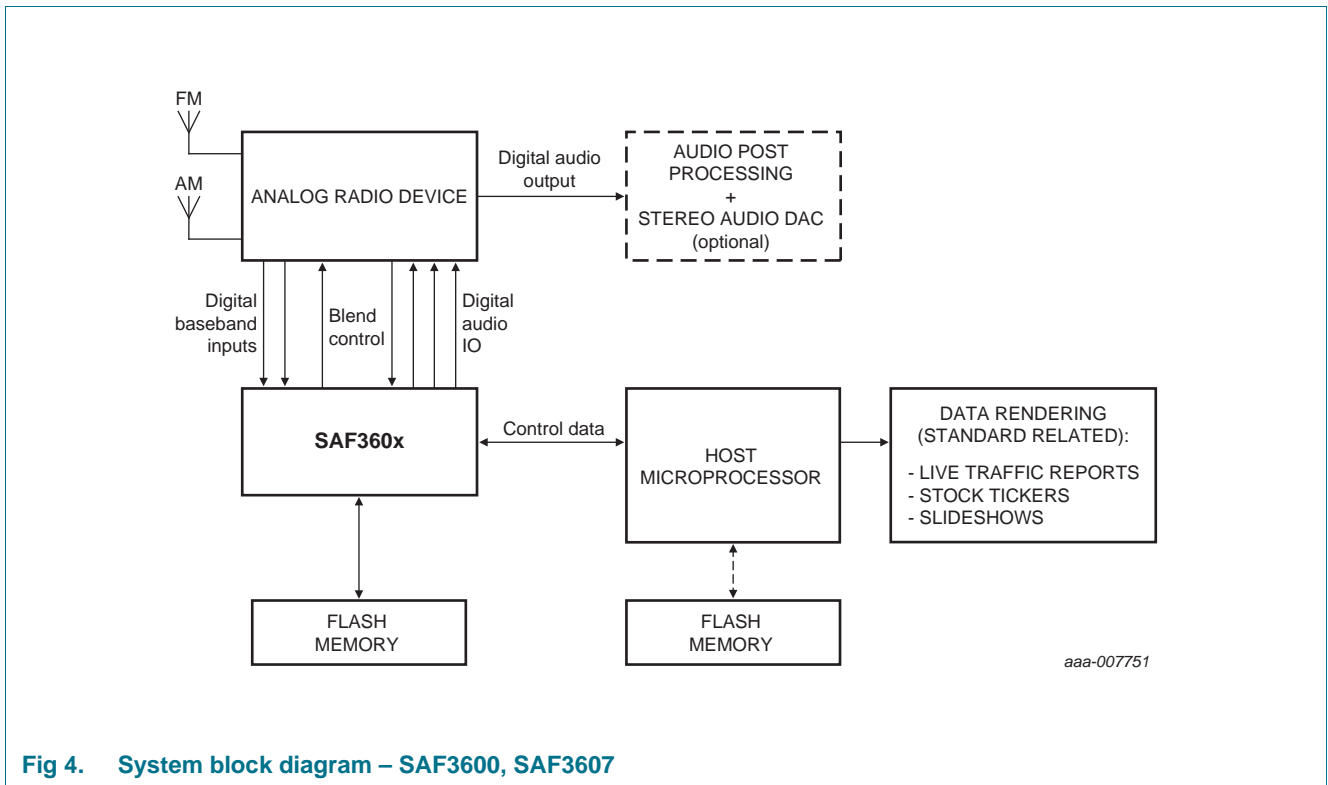


Fig 4. System block diagram – SAF3600, SAF3607



## 7. Limiting values

**Table 4. Limiting values**
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
<b>Voltages</b>					
SAF3601, SAF3602, SAF3604, SAF3606					
V <sub>DDA(VREG)(3V3)</sub>	voltage regulator analog supply voltage (3.3 V)		-0.5	+3.9	V
V <sub>DDA(ADPLL1)(1V8)</sub>	ADPLL1 analog supply voltage		-0.5	+2.4	V
V <sub>DDA(XTAL)(1V8)</sub>	crystal analog supply voltage		-0.5	+2.4	V
V <sub>DDA(DCO1)(1V8)</sub>	DCO1 analog supply voltage		-0.5	+2.4	V
V <sub>DDA(DIV)(1V8)</sub>	DIV analog supply voltage		-0.5	+2.4	V
V <sub>DDA(LVHFA)(1V8)</sub>	LVHFA analog supply voltage		-0.5	+2.4	V
V <sub>DDA(VHFM)(1V8)</sub>	VHFM analog supply voltage		-0.5	+2.4	V
V <sub>DDA(DCO2)(1V8)</sub>	DCO2 analog supply voltage		-0.5	+2.4	V
V <sub>DDA(ADPLL2)(1V8)</sub>	ADPLL2 analog supply voltage		-0.5	+2.4	V
V <sub>DDA(ADC)(1V8)</sub>	ADC analog supply voltage		-0.5	+2.4	V
V <sub>DDD(ADPLL1)(1V8)</sub>	ADPLL1 digital supply voltage		-0.5	+2.4	V
V <sub>DDD(ADPLL2)(1V8)</sub>	ADPLL2 digital supply voltage		-0.5	+2.4	V
V <sub>DDD(RFE)(1V8)</sub>	RFE digital supply voltage		-0.5	+2.4	V
V <sub>DD(IO)</sub>	input/output supply voltage		-0.5	+3.9	V
V <sub>QPS</sub>	OTP programming voltage (2.5 V)		-0.5	+2.7	V
V <sub>DD(A)</sub>	analog blocks supply voltage		-0.5	+1.7	V
V <sub>DD(C)</sub>	core supply voltage		-0.5	+1.7	V
SAF3600, SAF3607					
V <sub>DD(IO)</sub>	input/output supply voltage		-0.5	+3.9	V
V <sub>QPS</sub>	OTP programming voltage (2.5 V)		-0.5	+2.7	V
V <sub>DD(A)</sub>	analog blocks supply voltage		-0.5	+1.7	V
V <sub>DD(C)</sub>	core supply voltage		-0.5	+1.7	V
<b>Input voltages/current</b>					
V <sub>i</sub>	input voltage		-0.5	+V <sub>DD(IO)</sub>	V
SAF3601, SAF3602, SAF3604, SAF3606					
V <sub>i(VHF)(diff)</sub>	peak differential VHF input voltage	between pins VHF_MAIN_IN_P and VHF_MAIN_IN_N or pins VHF_AUX_IN_P and VHF_AUX_IN_N; AC coupling	-	+1.7	V
V <sub>i(L-band)</sub>	peak L-band input voltage	pin LBAND_IN; AC coupling	-	+1.7	V

**Table 4. Limiting values ...continued**  
 In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>ESD</sub>	electrostatic discharge voltage	human body model [1]	-1500	+1500	V
		charged device model			
		corner pins [3]	-750	+750	V
		other pins [4]	-400	+500	V
I <sub>lu</sub>	latch-up current	[5]	-10	+10	mA
<b>SAF3600, SAF3607</b>					
V <sub>ESD</sub>	electrostatic discharge voltage	human body model [2]	-2000	+2000	V
		charged device model			
		corner pins [3]	-750	+750	V
		other pins [4]	-400	+400	V
I <sub>lu</sub>	latch-up current	[5]	-100	+100	mA
<b>Temperature</b>					
T <sub>amb</sub>	ambient temperature		-40	+85	°C
T <sub>stg</sub>	storage temperature		-65	+150	°C

- [1] In accordance with AEC-Q100-002 Rev E, JS-001, 2014, Class C1.
- [2] In accordance with AEC-Q100-002 Rev E, JS-001, 2014, Class 2.
- [3] In accordance with AEC-Q100-011 Rev C1, Class C5.
- [4] In accordance with AEC-Q100-011 Rev C1, Class C3.
- [5] All supply voltages below the maximum values listed in this table.

8. Package outline

LFBGA223: plastic low profile fine-pitch ball grid array package; 223 balls

SOT1322-1

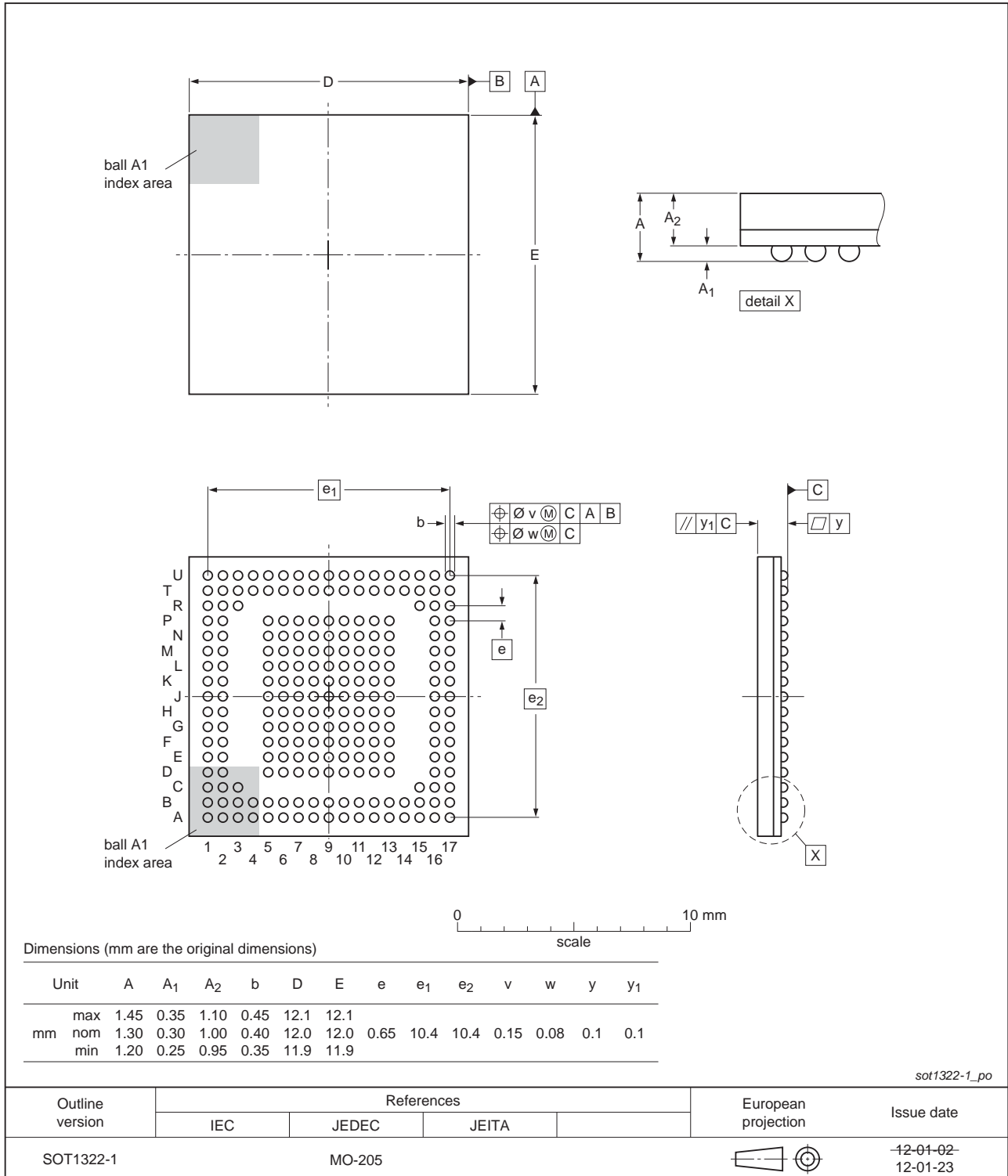


Fig 5. Package outline SOT1322-1 (LFBGA223)

## 9. Revision history

Table 5. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SAF360X_FAM_SDS v.3	20150123	Product short data sheet	-	SAF360X_FAM_SDS v.2
Modifications	• Updated <a href="#">Section 1</a> to <a href="#">Section 7</a> .			
SAF360X_FAM_SDS v.2	20140822	Product short data sheet	-	SAF360X_FAM_SDS v.1
Modifications	• Updated data sheet with SAF3601, SAF3602, SAF3604 and SAF3606 variants			
SAF360X_FAM_SDS v.1	20140716	Product short data sheet	-	-

## 10. Legal information

### 10.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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### ICs with DAB, DAB+ or T-DMB functionality

Use of this product in any manner that complies with the DAB, DAB+ or T-DMB digital radio standards requires a license under applicable patents in the DAB patent portfolio covering mainly the two technologies COFDM radio reception and MPEG audio layer II decoding, which license must be obtained from Koninklijke Philips Electronics N.V. via Philips Intellectual Property and Standards ([www.ip.philips.com](http://www.ip.philips.com)), e-mail: [info.licensing@philips.com](mailto:info.licensing@philips.com).

### ICs with MPEG-2 AAC, MPEG-4 AAC or MPEG-4 BSAC functionality

Use of this product in any manner that complies with the MPEG-2 AAC, MPEG-4 AAC or MPEG-4 BSAC audio compression standards requires a license under applicable patents in the MPEG-2 AAC and MPEG-4 AAC patent portfolio, which license is available from Via Licensing Corporation, 100 Potrero Avenue, San Francisco, CA 94103, USA..

### ICs with T-DMB functionality

Use of this product in any manner that complies with the T-DMB standard, which includes an MPEG-2 transport stream, is expressly prohibited without a license under applicable patents in the MPEG-2 patent portfolio, which license is available from MPEG-LA, L.L.C., 250 Steele Street, Suite 300, Denver, Colorado 80206.

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**HD Radio** — logo is a registered trademark of iBiquity Digital Corporation.

## 11. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

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