

# NX30P0121UK

## High-voltage back-to-back OVP switch

Rev. 1.0 — 19 June 2019

Product data sheet

## 1 General description

---

The NX30P0121UK is an advanced 3A unidirectional power switch. It includes Undervoltage Lockout (UVLO), Overvoltage Lockout (OVLO) in VOUT, OVLO adjustable pin and over-temperature protection circuits. It is designed to automatically isolate the power switch terminals when a fault condition occurs. Both VIN and VOUT pins have 29V tolerance in shutdown mode.

The device has a default internal 14.5V overvoltage protection threshold in VOUT and adjustable OVP threshold by resistor divider from VOUT. ISNS pin is current source output proportional to input current from VIN to VOUT when device is enabled.

The device is enabled by external EN pin. When EN pin is driven LOW, the device is in shutdown mode where all internal circuitries are off and OVP switch is off. When EN pin is driven HIGH and VIN is valid, the OVP switch soft starts after VIN debounce time to limit the inrush current.

NX30P0121UK is offered in a small 12 bumps, 1.65 x 1.25 x 0.525 mm WLCSP package.

## 2 Features and benefits

---

- Wide supply voltage range from 2.5V to 20V
- Switch maximum 3A continuous current
- 29V tolerance on both VIN and VOUT pin
- 54mΩ (typical) Low ON resistance
- Adjustable overvoltage protection threshold, internal 14.5V VOUT OVLO
- Built in slew rate control for inrush current limit
- ISNS to monitor input current from VIN to VOUT
- Protection circuitry
  - Over-temperature protection
  - Overvoltage protection
  - Undervoltage lockout
- ESD protection
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2 kV
  - CDM (JESD22-C101E)
- Specified from -40°C to +85°C

## 3 Applications

---

- Smartphone
- Tablet
- Other portable electronic devices



## 4 Ordering information

Table 1. Ordering information

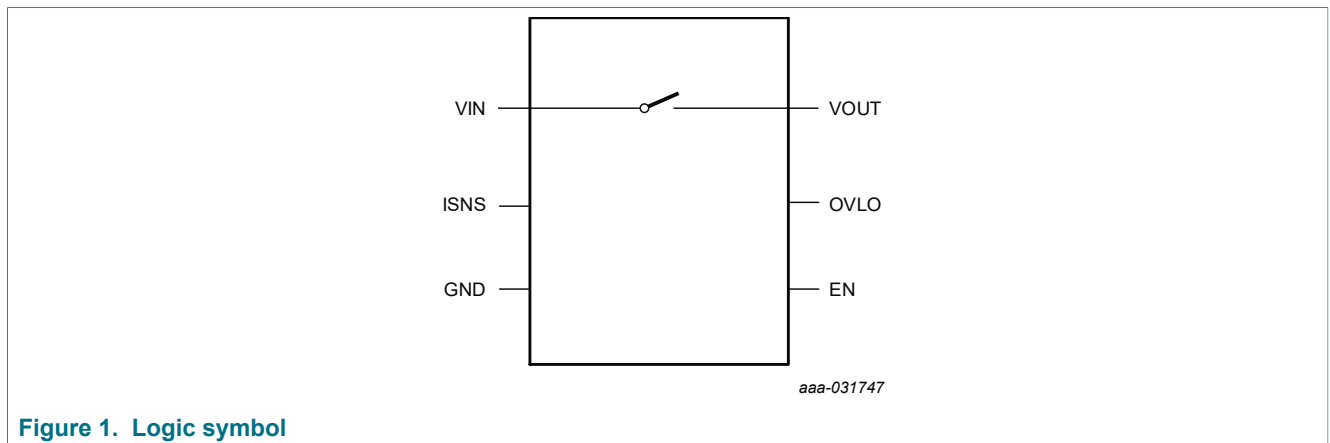
Type number	Topside marking	Package		
		Name	Description	Version
NX30P0121UK	N21	WLCSP12	wafer level chip scale package; 12 bumps; 0.4 mm pitch; 1.65 mm x 1.25 mm x 0.525 mm body (backside coating included)	SOT1390-8

### 4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
NX30P0121UK	NX30P0121UKZ	WLCSP12	REEL 7" Q1 DP CHIPS	4000	T <sub>amb</sub> = -40 °C to +85 °C

## 5 Functional diagram



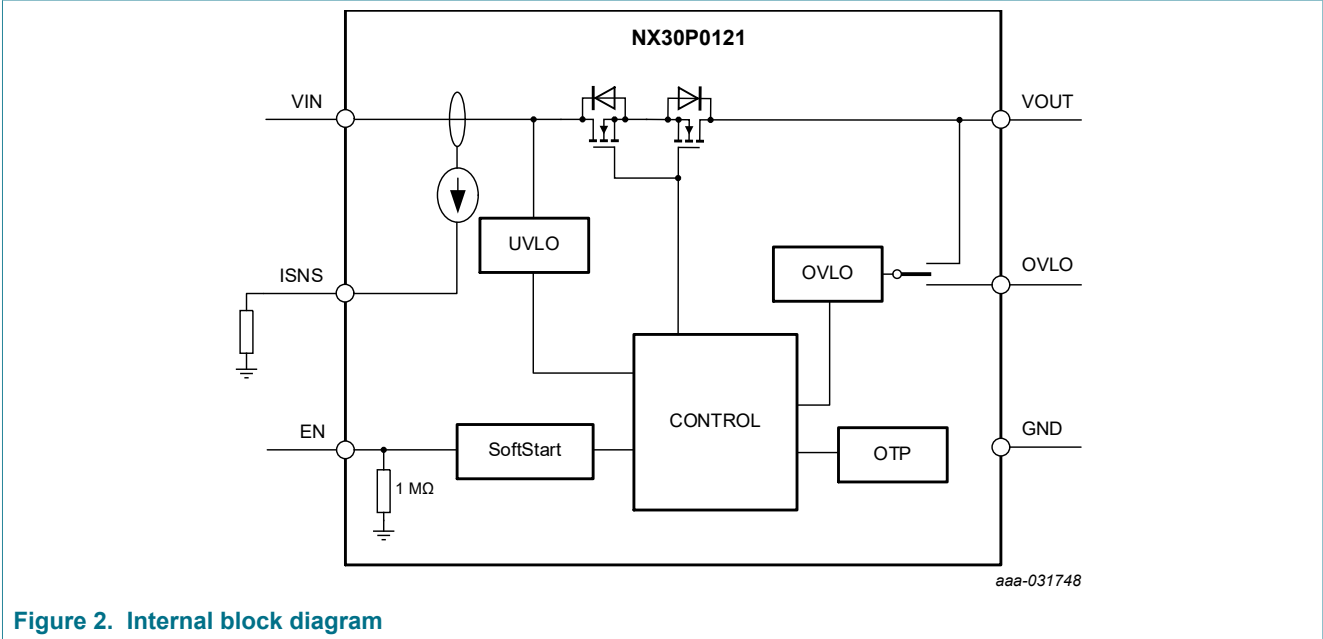


Figure 2. Internal block diagram

## 6 Pinning information

### 6.1 Pinning

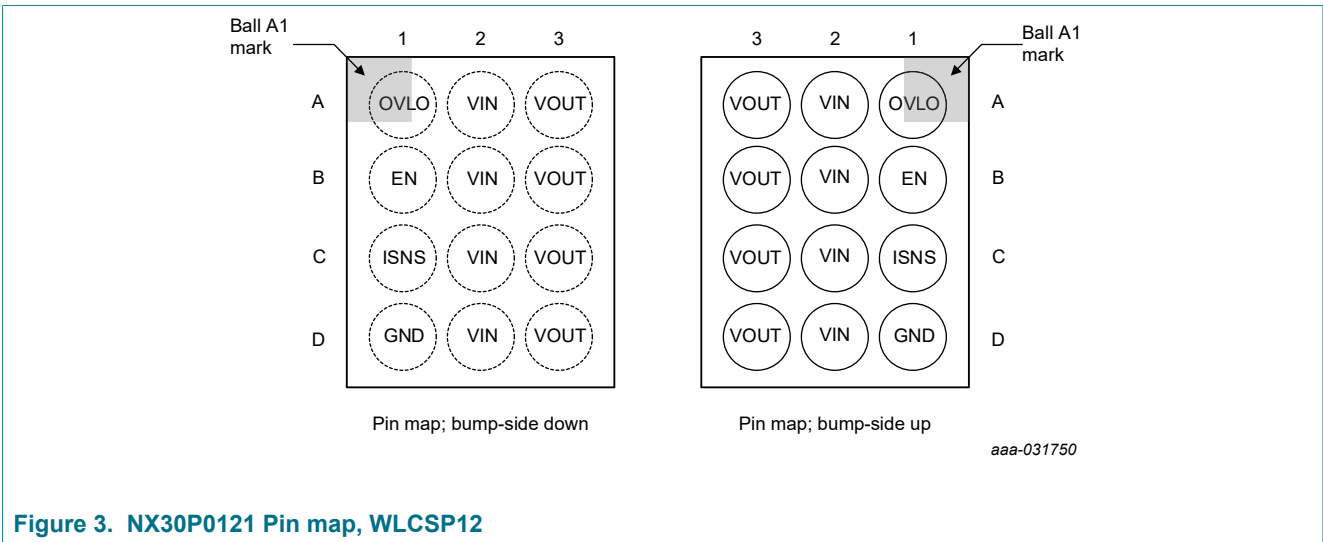


Figure 3. NX30P0121 Pin map, WLCSP12

### 6.2 Pin description

Table 3.

Pin description			
Symbol	Pin	Type	Description
VIN	A2, B2, C2, D2	P	Input power pin. Connect bypass capacitor 1uF to GND

Pin description			
Symbol	Pin	Type	Description
VOUT	A3, B3, C3, D3	P	Output Power pin, Connect bypass capacitor 1uF to GND
EN	B1	DIN	Enable pin. Drive HIGH to enable device.
ISNS	C1	AO	1,053:1 current mirror of input current from VIN to VOUT. Must connect a resistor on ISNS pin to GND to monitor the input current.
OVLO	A1	AIN	Adjustable OVLO threshold with external Resistor divider
GND	D1	P	Ground

## 7 Functional description

Table 4. Function table

EN	VIN	VOUT	Switch	ISNS	Operation
L	X	X	OFF	Hi-Z	Shutdown mode
H	< VIN <sub>UVLO</sub>	X	OFF	Hi-Z	Standby mode, Undervoltage lockout
H	X	> VOUT <sub>OVLO</sub>	OFF	Hi-Z	Standby mode, Overvoltage lockout
H	> VIN <sub>UVLO</sub>	< VOUT <sub>OVLO</sub>	ON	ON	Switch ON mode

### 7.1 EN pin

When EN is driven LOW, the device enters shutdown mode regardless of VIN and VOUT voltage. All internal circuitries are off to minimize current consumption and OVP switch is OFF. When EN is driven HIGH, the OVP switch is ready to turn on depending on VIN and VOUT condition. if VIN is above VIN<sub>UVLO</sub> and VOUT is lower than VOUT<sub>OVLO</sub>, the device soft starts after VIN debounce timer is expired, to reduce in-rush current. There is an internal 1MΩ pull-down resistor in EN pin, which secure EN status in case EN pin is float. This pin has +29V tolerance.

### 7.2 Undervoltage Lockout (UVLO)

When EN is driven HIGH and VIN < VIN<sub>UVLO</sub>, the UVLO circuit disables the power MOSFET. Once VIN exceeds VIN<sub>UVLO</sub> and no other protection circuit is active, the channel MOSFET state is controlled by the EN pin.

### 7.3 Overvoltage Lockout (OVLO)

When EN is driven HIGH and VOUT is above VOUT<sub>OVLO</sub>, the OVLO circuit disables the power MOSFET within t<sub>dis(OVP)</sub>. Once VOUT drops below VOUT<sub>OVLO</sub> and no other protection circuit is active, the power MOSFET resumes operation.

OVLO pin is used to adjust the overvoltage protection threshold. The default overvoltage threshold is 14.5V when OVLO pin is shorted to GND. Connecting a resistor divider to the OVLO pin (see [Figure 4](#)) adjusts the overvoltage threshold from 4V to 20V using below equation.

$$VOUT_{OVLO} = Vth(OVLO) \times (R1 + R2) / (R2)$$

Where  $V_{th}(OVLO) = 1.227V$

R1 is recommended to use 1MΩ resistance.

When the voltage on OVLO pin is below 0.1V, the device defaults to the 14.5V OVP threshold.

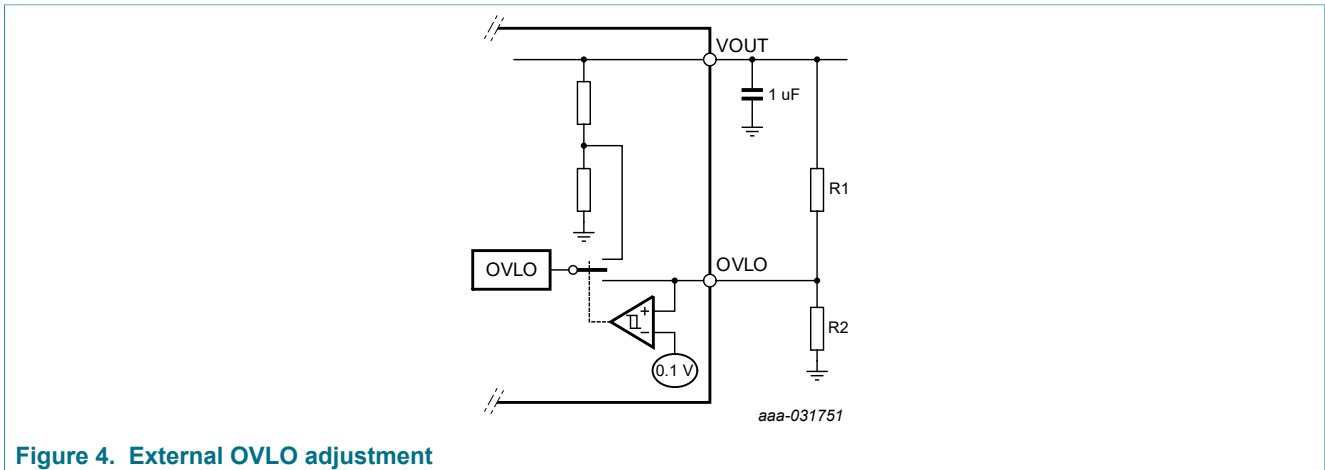


Figure 4. External OVLO adjustment

### 7.4 Over-temperature protection

When EN is HIGH and the device temperature exceeds 145°C the Over-Temperature Protection (OTP) circuit disables the power MOSFET. Once the device temperature decreases below 115 °C and no other protection circuit is active, the state of the OVP MOSFET is controlled by the EN pin again.

### 7.5 ISNS pin

The ISNS pin is current source output having 1,053:1 ratio with input current from VIN to VOUT. It requires a resistor from ISNS to GND to monitor input current. When device is disabled, its output is high impedance. The ISNS voltage is determined by below equation.  $R_{ISNS}$  is recommended to be +/-1% tolerant.

$$V_{ISNS} = ( I_{IN} \times R_{ISNS} ) / 1,053$$

7.6 Timing diagram

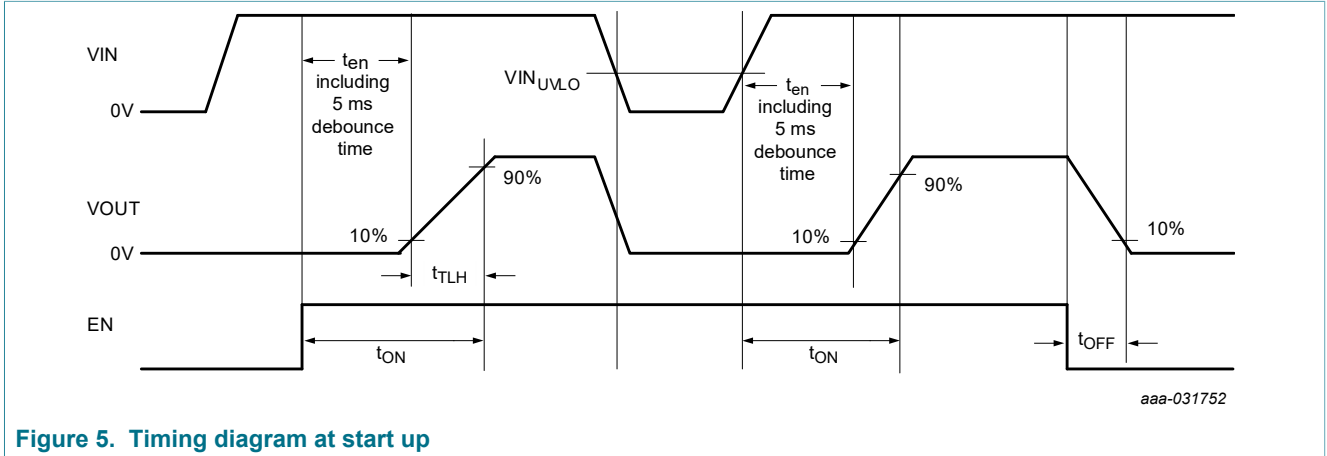


Figure 5. Timing diagram at start up

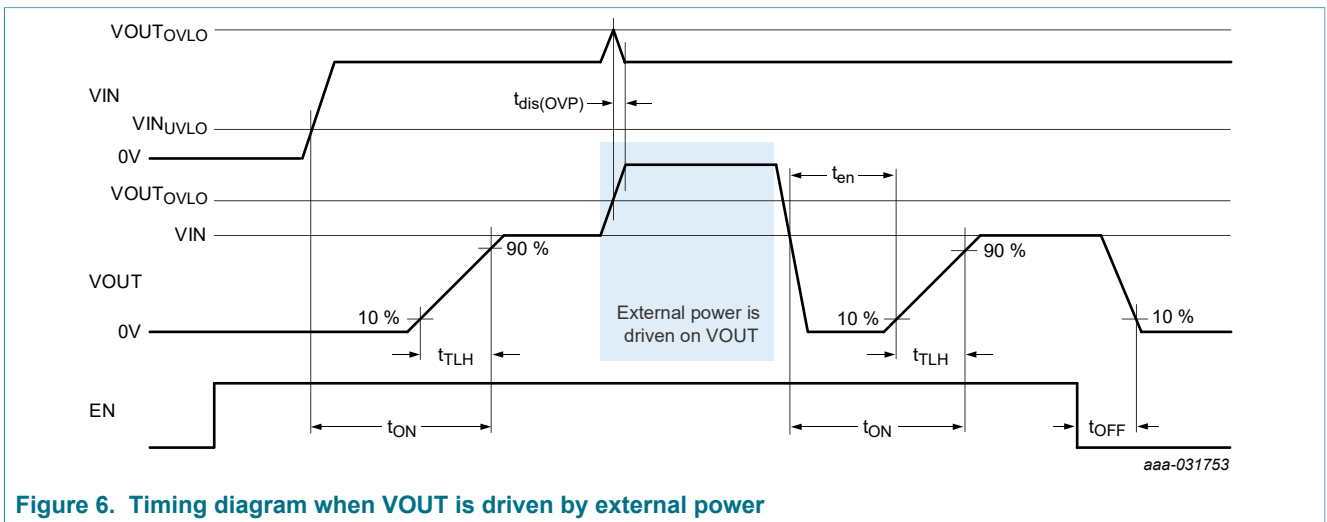


Figure 6. Timing diagram when VOUT is driven by external power

8 Application diagram

The NX30P0121UK is typically used to add wireless charger path in single input switching mode charger application. If wireless charger is used, then NX30P0121UK bridge wireless charger output to the switching mode charger, protecting wireless charger from up to 29V which could be from VBUS.

For best performance, it is recommended to keep input and output traces short and wide, and capacitors as close to the device as possible. Regarding thermal performance, it is recommended to increase the PCB area around VIN and VOUT pins.

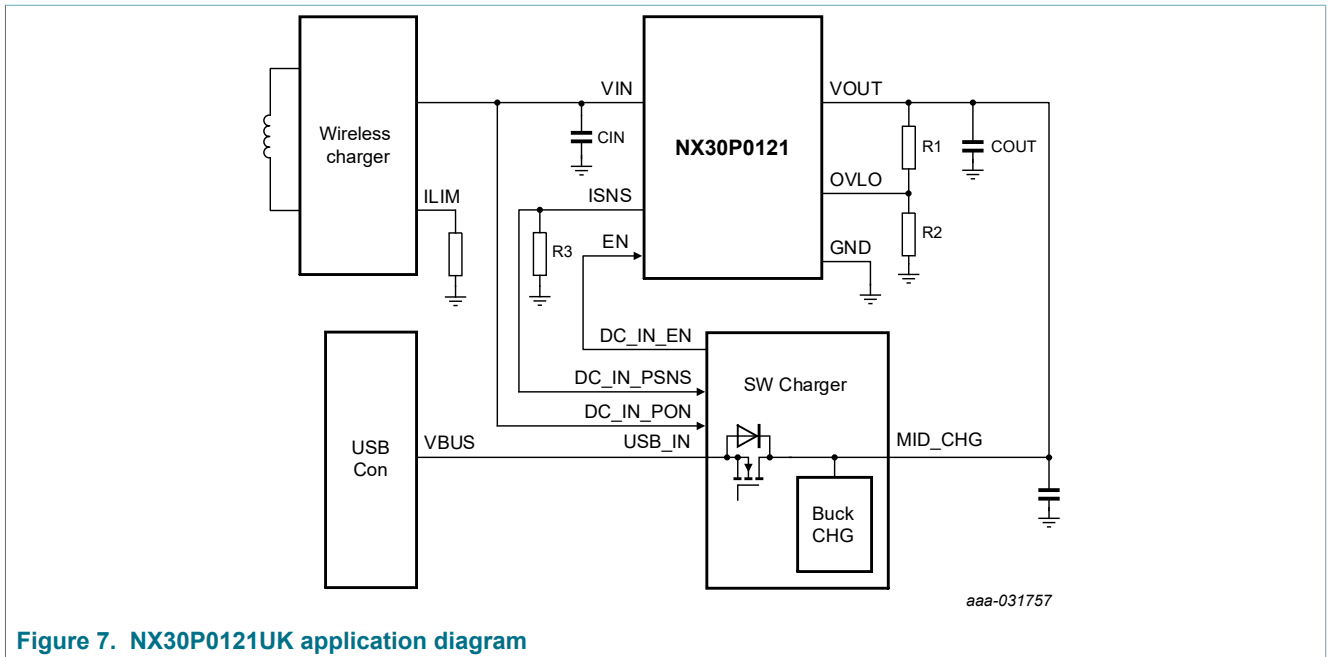


Figure 7. NX30P0121UK application diagram

## 9 Limiting values

Table 5. Limiting values (absolute maximum ratings)

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>I</sub>	Input voltage (with respect to GND)	VIN	-0.5	+29	V
		VOUT	-0.5	+29	V
		OVLO	-0.5	VOUT	V
		EN	-0.5	+29	V
		ISNS	-0.5	+6	V
I <sub>IK</sub>	Input clamping current	EN; V <sub>I</sub> < -0.5 V	-50	-	mA
I <sub>SK</sub>	Switch clamping current	VIN, VOUT; V <sub>I</sub> < -0.5 V	-50	-	mA
I <sub>SW</sub>	Continuous switch current	T <sub>amb</sub> = 85 °C	-	+3.0	A
		T <sub>amb</sub> = 105 °C	-	+3.0	A
	Peak switch current	130µs pulse, 5% duty cycle at 85 °C	-	+10	A
T <sub>stg</sub>	Storage temperature		-65	+150	°C
P <sub>tot</sub>	Total power dissipation	T <sub>amb</sub> = 25 °C	-	1.45	W

## 10 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>I</sub>	input voltage (with respect to GND)	VIN	2.5	20	V
		VOUT	2.5	20	V
		EN	0	20	V

Symbol	Parameter	Conditions	Min	Max	Unit
		ISNS	0	+6	V
$T_{j(max)}$	Maximum junction temperature		-40	+125	°C
$T_{amb}$	Ambient temperature		-40	+85	°C

## 11 Thermal characteristics

**Table 7. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1] [2] 70.8	°C/W

[1] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment

[2] Thermal test board meets JEDEC specification for this package (JESD51-9).

## 12 Electrical characteristics

### 12.1 Static characteristics

**Table 8. Static characteristics**

At recommended input voltages and  $T_{amb} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ; voltages are referenced to GND (ground = 0 V); unless otherwise specified.

Symbol	Parameter	Conditions	$T_{amb} = 25^{\circ}\text{C}$			$T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		Unit
			Min	Typ	Max	Min	Max	
$I_q$	$V_{IN}$ quiescent current	$EN = 1.8\text{V}, V_{IN} = 5\text{V}, IO = 0\text{A}$	-	110	-	-	170	$\mu\text{A}$
		$EN = 1.8\text{V}, V_{IN} = 14\text{V}, IO = 0\text{A}$	-	140	-	-	220	$\mu\text{A}$
$I_{SHDN}$	$V_{IN}$ shutdown leakage current	$EN = 0\text{V}, V_{IN} = 5.0\text{V}; V_{OUT} = 0\text{V}$	-	5	-	2	10	$\mu\text{A}$
	$V_{OUT}$ shutdown Leakage current	$EN = 0\text{V}, V_{OUT} = 5.0\text{V}, V_{IN} = 0\text{V}$	-	1	3	-	5	$\mu\text{A}$
$I_{OVLO}$	OVLO input leakage Current	$V_{OVLO} = V_{th(OVLO)}$	-	0.5	-	-	25	nA
$R_{ON}$	ON resistance	$V_{IN} = 5.0\text{V}$	-	54	66	-	79	m $\Omega$
		$V_{IN} = 14\text{V}$	-	54	66	-	79	m $\Omega$
$V_{INUVLO}$	$V_{IN}$ UVLO voltage	$V_{IN}$ Rising; $EN = 1.8\text{V}$	2.2	2.37	2.55	2.1	2.6	V
$V_{INhys(UVLO)}$	$V_{IN}$ UVLO hysteresis voltage	$V_{IN}$ Falling	-	110	-	-	140	mV
$V_{OUTOVLO}$	Default overvoltage lockout voltage	$V_{OUT}$ Rising; $EN = 1.8\text{V}$ OVLO short to GND	-	14.5	-	13.5	15.3	V



Symbol	Parameter	Conditions	T <sub>amb</sub> = 25 °C			T <sub>amb</sub> = -40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
		V <sub>OUT</sub> Falling; EN = 1.8V OVLO short to GND	-	14.2	-	13.2	15.0	V
V <sub>th(OVLO)</sub>	external OVLO set threshold voltage	V <sub>OUT</sub> = 2.5 V to 20 V; EN = 1.8V	1.163	1.227	1.288	1.16	1.3	V
V <sub>IH</sub>	HIGH-level input voltage	EN pin; V <sub>IN</sub> = 2.5 V to 20 V	1.2	-	-	1.2	-	V
V <sub>IL</sub>	LOW-level input voltage	EN pin; V <sub>IN</sub> = 2.5 V to 20 V	-	-	0.4	-	0.4	V
R <sub>pd</sub>	pull-down resistance	EN	-	1	-	0.7	1.4	MΩ
C <sub>I</sub>	input capacitance	EN pin; V <sub>IN</sub> = 5V	-	2	-	-	-	pF
K	Current sensing ratio	I <sub>IN</sub> / I <sub>ISNS</sub> , I <sub>IN</sub> = 1A, V <sub>IN</sub> = 5V, EN =1.8V		1050		1010	1090	A/A
V <sub>ISNS</sub>	ISNS voltage	I <sub>IN</sub> = 2A, R <sub>ISNS</sub> = 400Ω, V <sub>IN</sub> = 5V, V <sub>IN</sub> > 3.0V		0.762				V
V <sub>ISNS</sub>	ISNS voltage	I <sub>IN</sub> = 1A, R <sub>ISNS</sub> = 806Ω, V <sub>IN</sub> = 5V, V <sub>IN</sub> > 3.0V		0.767				V
V <sub>ISNS</sub>	ISNS voltage	I <sub>IN</sub> = 0.5A, R <sub>ISNS</sub> = 806Ω, V <sub>IN</sub> = 5V, V <sub>IN</sub> > 3.0V		0.384				V
T <sub>th(OTP)</sub>	Over temperature shutdown threshold	EN = 1.8V	-	145	-	-	-	°C
T <sub>th(OTP)Hys</sub>	Over temperature shutdown threshold hysteresis	EN = 1.8V	-	30	-	-	-	°C

**12.2 Dynamic characteristics**

**Table 9. Dynamic characteristics**

Symbol	Parameter	Conditions	T <sub>amb</sub> = 25 °C			T <sub>amb</sub> = -40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
t <sub>en</sub>	Enable Time	From EN to V <sub>OUT</sub> = 10% of V <sub>IN</sub> ; V <sub>IN</sub> = 5 V; C <sub>OUT</sub> =10μF; R <sub>Load</sub> = 100Ω includes 2ms V <sub>IN</sub> debounce time	3.5	5.5	8.0	3.0	11.0	ms
t <sub>TLH</sub>	V <sub>OUT</sub> rise time	V <sub>OUT</sub> from 10% to 90% of V <sub>IN</sub> ; C <sub>OUT</sub> = 10μF; R <sub>OUT</sub> = 100Ω						
		V <sub>IN</sub> = 5 V	-	1.8	-	-	-	ms
		V <sub>IN</sub> =14 V	-	3.0	-	-	-	ms
t <sub>dis(OVP)</sub>	OVP turn off time	From V <sub>OUT</sub> > V <sub>OUT</sub> <sub>OVLO</sub> to V <sub>VIN</sub> = 80% of V <sub>OUT</sub> ; R <sub>load</sub> _V <sub>IN</sub> = 100Ω; C <sub>IN</sub> = 0uF; V <sub>IN</sub> = 12V; OVLO pin short to GND	-	70	-	-	-	ns
t <sub>on</sub>	turn-on time	EN to V <sub>OUT</sub> = 90% of V <sub>IN</sub>						

Symbol	Parameter	Conditions	T <sub>amb</sub> = 25 °C			T <sub>amb</sub> = -40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
		V <sub>IN</sub> = 5.0 V	-	7.5	-	5.0	10.0	ms
		V <sub>IN</sub> = 14.0 V	-	9.0	-	-	-	ms
t <sub>off</sub>	turn-off time	EN to V <sub>OUT</sub> = 10% V <sub>IN</sub>						
		V <sub>IN</sub> = 5.0 V; C <sub>OUT</sub> = 10µF; R <sub>OUT</sub> = 100Ω	-	2.6	4.0	-	4.0	ms
		V <sub>IN</sub> = 14 V; C <sub>OUT</sub> = 10µF; R <sub>OUT</sub> = 100Ω	-	2.6	-	-	-	ms

12.3 Graphs

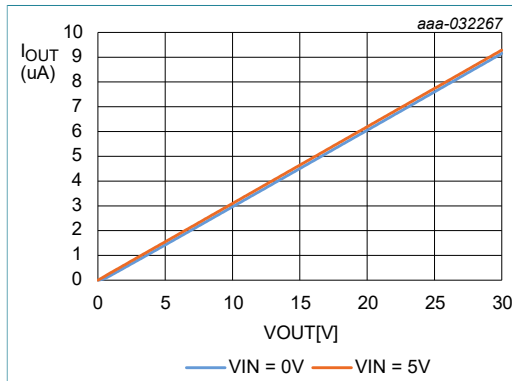


Figure 8. VOUT leakage current (EN = 0V)

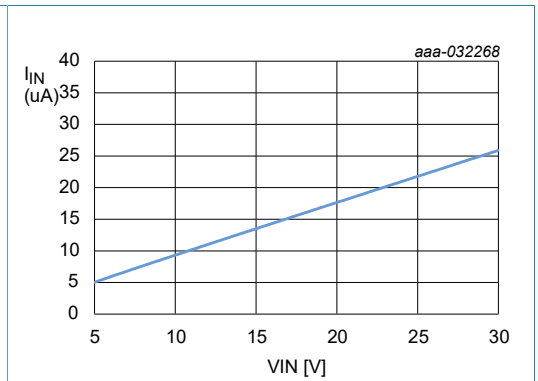


Figure 9. VIN leakage current (EN = 0V)

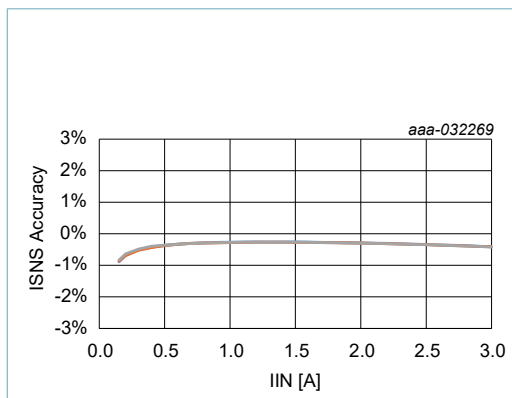


Figure 10. ISNS accuracy (R<sub>ISNS</sub> = 806Ω)

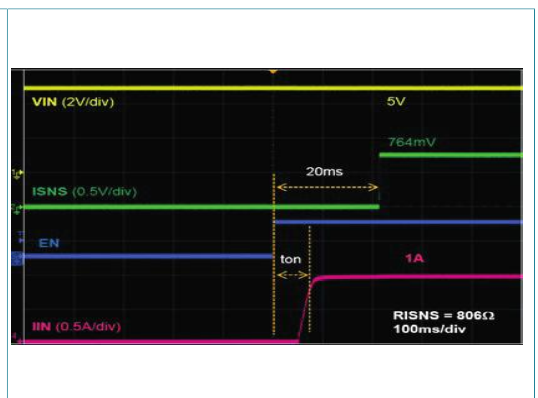
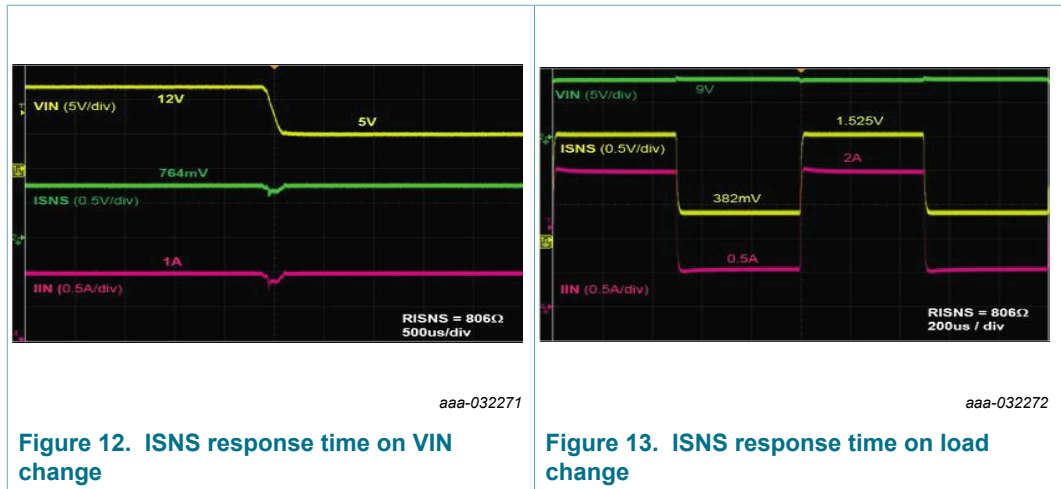


Figure 11. Startup (R<sub>ISNS</sub> = 806Ω)



aaa-032271

aaa-032272

**13 Package outline**

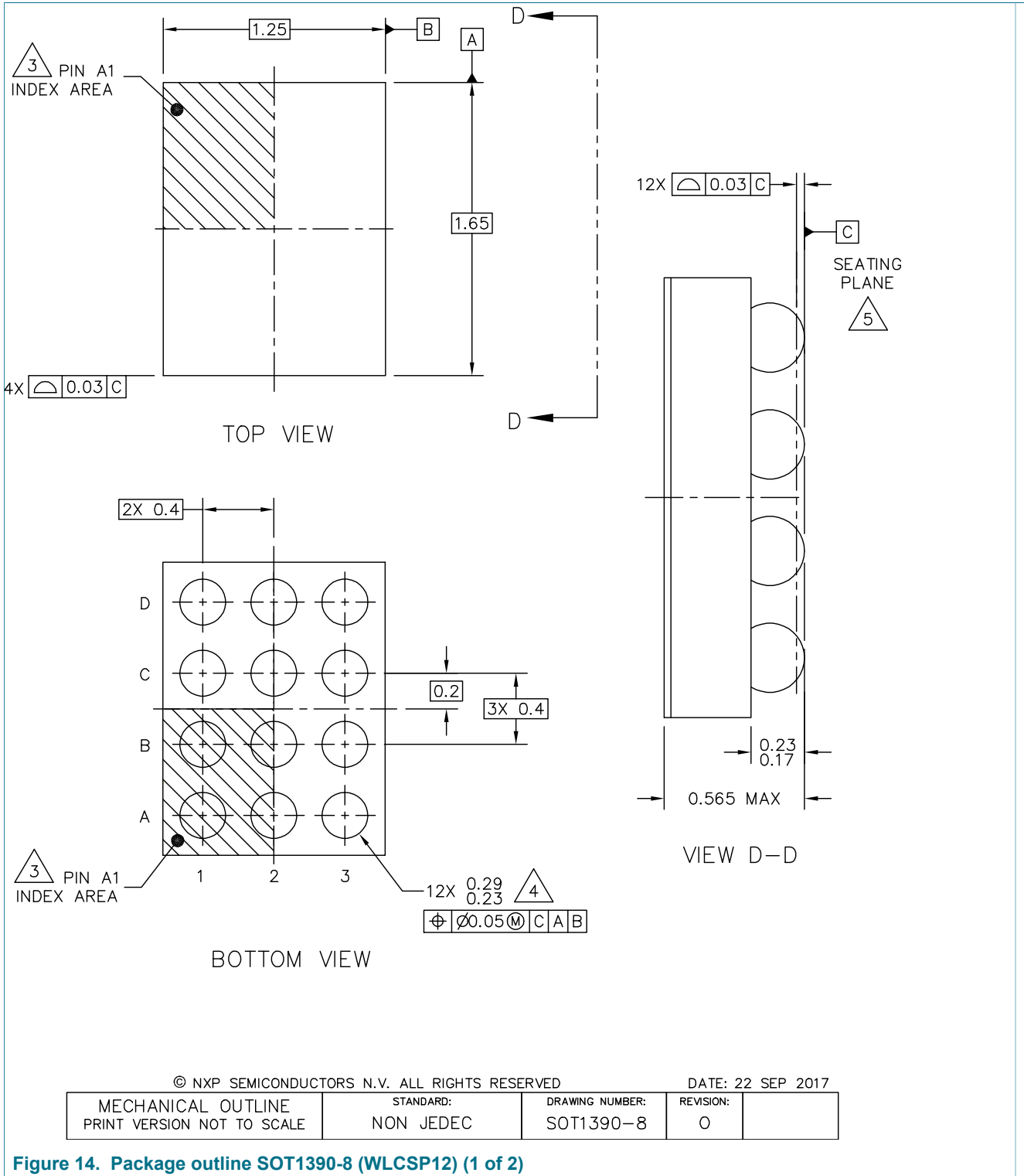


Figure 14. Package outline SOT1390-8 (WLCSP12) (1 of 2)

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

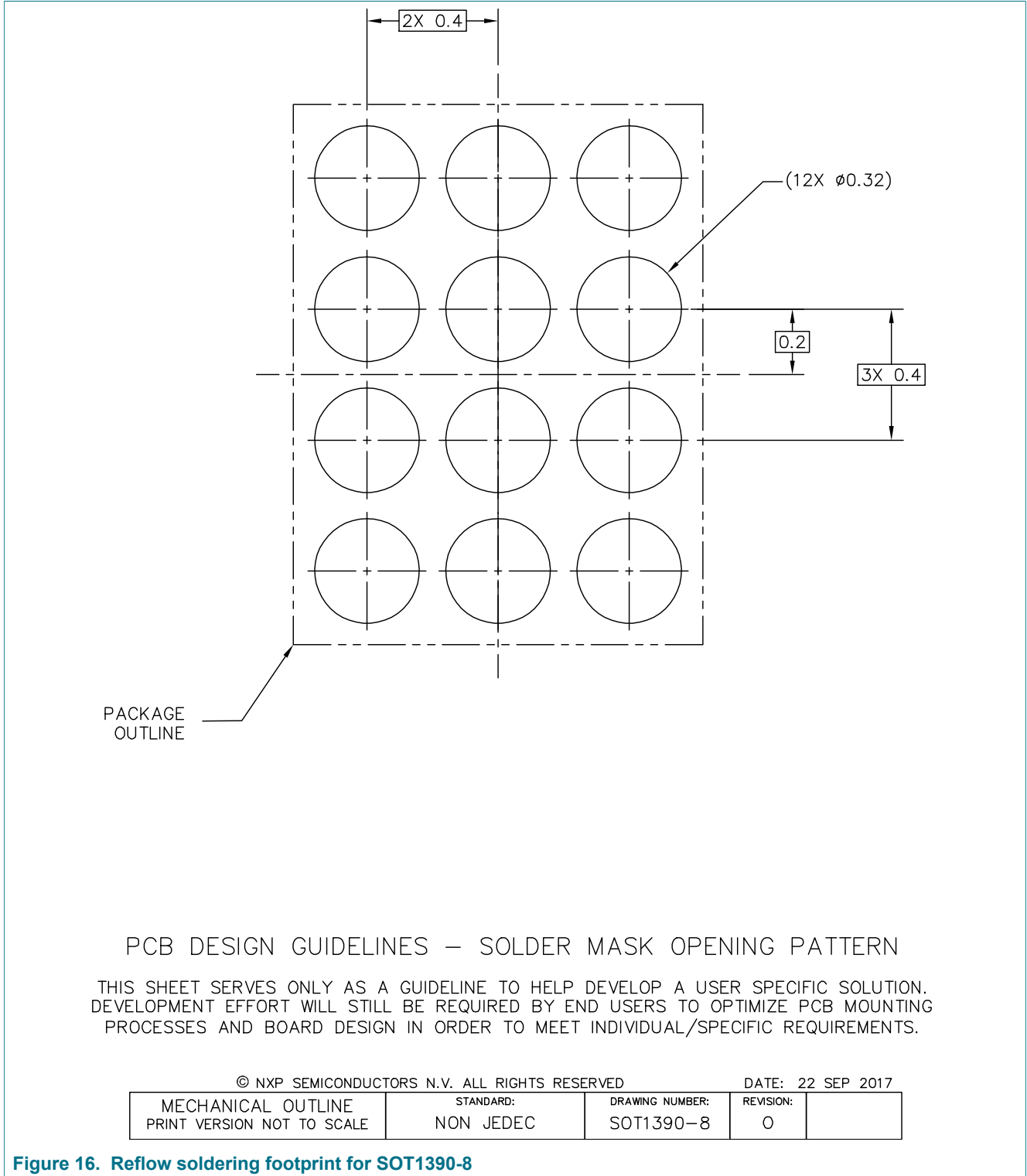
© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED

DATE: 22 SEP 2017

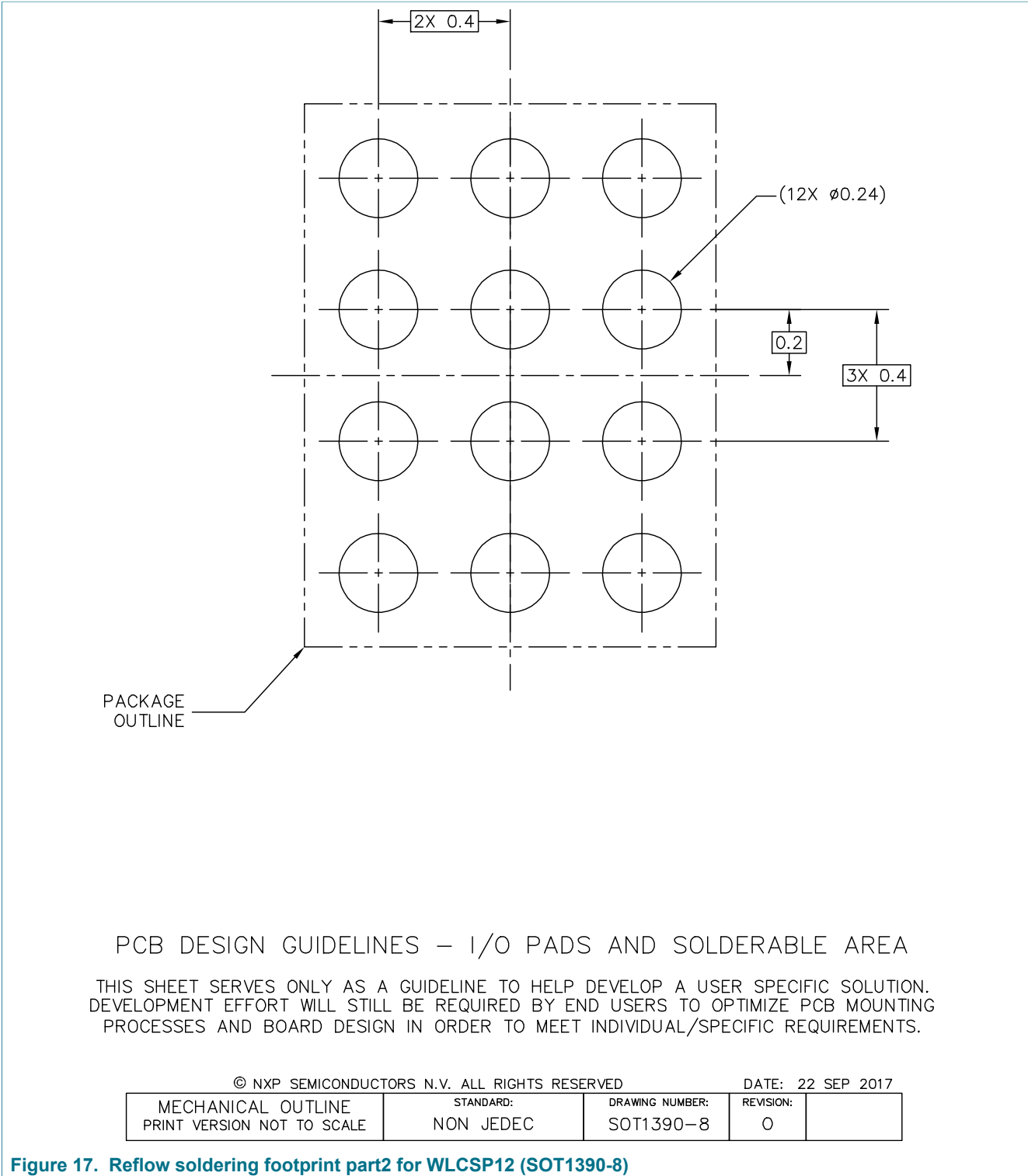
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT1390-8	REVISION: 0	
--	------------------------	------------------------------	----------------	--

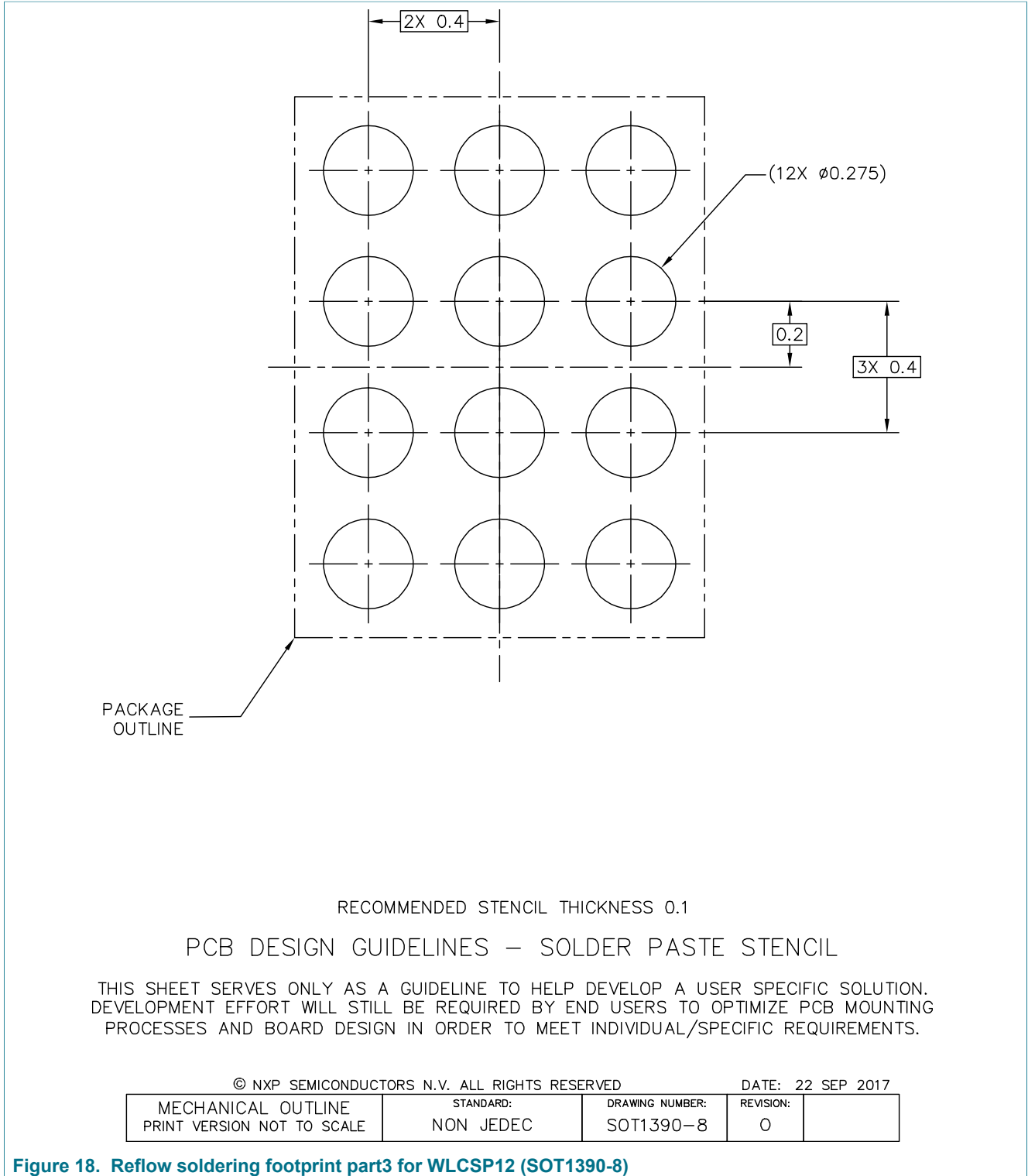
**Figure 15. Package outline SOT1390-8 (WLCSP12) (2 of 2)**

**14 Soldering**



**Figure 16. Reflow soldering footprint for SOT1390-8**





**Figure 18. Reflow soldering footprint part3 for WLCSP12 (SOT1390-8)**



## 15 Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX30P0121 v.1.0	20190619	Product data sheet	-	-

## 16 Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 16.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 16.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without

notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## 16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

**Tables**

Tab. 1.	Ordering information	2	Tab. 6.	Recommended operating conditions	7
Tab. 2.	Ordering options	2	Tab. 7.	Thermal characteristics	8
Tab. 3.		3	Tab. 8.	Static characteristics	8
Tab. 4.	Function table	4	Tab. 9.	Dynamic characteristics	9
Tab. 5.	Limiting values (absolute maximum ratings)	7	Tab. 10.	Revision history	17

**Figures**

Fig. 1.	Logic symbol	2	Fig. 12.	ISNS response time on VIN change	11
Fig. 2.	Internal block diagram	3	Fig. 13.	ISNS response time on load change	11
Fig. 3.	NX30P0121 Pin map, WLCSP12	3	Fig. 14.	Package outline SOT1390-8 (WLCSP12) (1 of 2)	12
Fig. 4.	External OVLO adjustment	5	Fig. 15.	Package outline SOT1390-8 (WLCSP12) (2 of 2)	13
Fig. 5.	Timing diagram at start up	6	Fig. 16.	Reflow soldering footprint for SOT1390-8	14
Fig. 6.	Timing diagram when VOUT is driven by external power	6	Fig. 17.	Reflow soldering footprint part2 for WLCSP12 (SOT1390-8)	15
Fig. 7.	NX30P0121UK application diagram	7	Fig. 18.	Reflow soldering footprint part3 for WLCSP12 (SOT1390-8)	16
Fig. 8.	VOUT leakage current (EN = 0V)	10			
Fig. 9.	VIN leakage current (EN = 0V)	10			
Fig. 10.	ISNS accuracy (RISNS = 806Ω)	10			
Fig. 11.	Startup (RISNS = 806Ω)	10			

**Contents**

1 **General description** ..... 1

2 **Features and benefits** .....1

3 **Applications** .....1

4 **Ordering information** ..... 2

4.1 Ordering options ..... 2

5 **Functional diagram** .....2

6 **Pinning information** ..... 3

6.1 Pinning ..... 3

6.2 Pin description ..... 3

7 **Functional description** .....4

7.1 EN pin .....4

7.2 Undervoltage Lockout (UVLO) .....4

7.3 Overvoltage Lockout (OVLO) ..... 4

7.4 Over-temperature protection .....5

7.5 ISNS pin ..... 5

7.6 Timing diagram .....6

8 **Application diagram** .....6

9 **Limiting values** .....7

10 **Recommended operating conditions** ..... 7

11 **Thermal characteristics** .....8

12 **Electrical characteristics** .....8

12.1 Static characteristics .....8

12.2 Dynamic characteristics .....9

12.3 Graphs ..... 10

13 **Package outline** .....12

14 **Soldering** .....14

15 **Revision history** ..... 17

16 **Legal information** ..... 18

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2019.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 19 June 2019  
 Document identifier: NX30P0121