# TLE6368

## Serial Peripheral Interface (SPI)

Automotive Power

Never stop thinking

**Table of Contents** **Page**

Application Note 2 2010-09-22

# 1 Abstract

This Application Note is intended to provide additional information for operating the Serial Peripheral Interface (SPI) in the TLE6368. The reader should be given a deeper understanding of the architecture and the function of the SPI to avoid undesired programming of the TLE6368.

*Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device*

# 2 Introduction

The TLE6368 is a Multi-Voltage Processor Power Supply with a step down converter as the preregulator supplying a couple of linear voltage regulators. The device delivers the following voltages:

- Linear voltage regulator LDO_1 with 5 V output voltage and 800 mA maximum output current capability.

- Linear voltage regulator LDO_2 with 3.3 or 2.6 V output voltage and 500 mA maximum output current capability.

- Linear voltage regulator LDO_3 with 3.3 or 2.6 V output voltage and 350 mA maximum output current capability.

- Six Trackers T1 to T6 following LDO_1 (5 V output voltage) with a maximum current capability of 17 mA each.

The TLE6368 includes a Reset-Generator monitoring LDO_1, LDO_2 and LDO_3 as well as a Window Watchdog (WWD) to monitor the micro processor.

Communication between the microprocessor and the TLE6368 may be executed using the 16-bit-Serial Peripheral Interface.

Via this interface is possible:

- To control the function of the Trackers T1 to T6 (switch On and Off)

- To send the device to sleep. (Function depends on Wake-Pin (34): If Wake pin is connected to input voltage, the sleep-bit will switch off the device, but it will immediately switch on again. To switch the device off per sleep-bit, the Wake-pin has to be switched to GND. The device will then restart, if Wake-Pin is switched to input voltage.

- To adjust the Reset Delay timing between 8 ms and 64 ms.

- To adjust the Window Watchdog timing between 16 ms and 128 ms.

- To enable or disable the Window Watchdog function.

- To trigger the Window Watchdog.

# 3 SPI Architecture

## 3.1 Principle:

The SPI consists of a daisy chain of D-Flip-Flops to read the information (named command word, please refer to Datasheet 2.12.2. Write mode bit assignment) at pin Data-Input (DI –pin 4) and write the status of the device (named status-word, please refer to Datasheet 2.12.3.1. Read mode bit assignment) at pin Data Output (DO pin 5).

To write a command word into the SPI and receive the status word from the SPI, pin Chip Select (CS – pin 3) has to be low. A clock signal at pin CLK will then make the SPI read the Command Word at pin DI and writes the status of the TLE6368 to pin DO.

- The SPI does not do a validity check of the 16-bit-command word. This means that, that an invalid command-word consisting of less than 16 bit will be accepted. The configuration of the device will then be according to this invalid command-word.

- The SPI is active as soon as the internal power supply of the TLE6368 has started up. This means, that any glitches on the signals CS and CLK may lead to an undesired status.
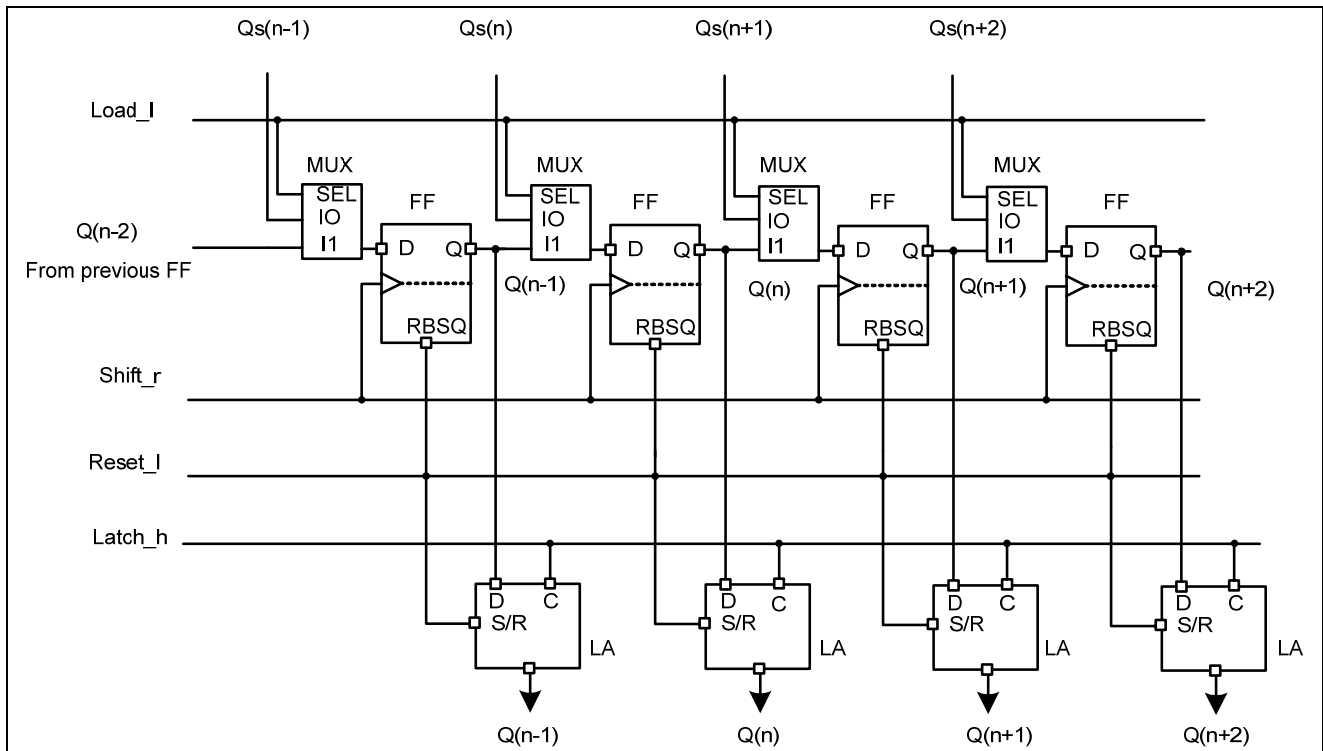
## 3.2 Block Diagram:



**Figure 1 Block Diagram of the SPI**

(Please refer to Signal Flow Diagram (Figure 2), next page)

The meanings of these internal signals are:

- **Qs(n):** Status-bit number n read from actual configuration of the device

- **Q(n):** Command-bit number n read from DI

- **Load_l:** This signal is derived from CLK: As long as it is high, the MUX switches from Input selects the output Q of the previous D-Flip-Flop as the input

- **Shift_r:** This signal is derived from signals CS and CLK. A rising edge of this signal (at a falling edge of CLK) clocks the D-Flip-Flops.

- **Reset_l:** This signal is a combination of three internal signals. As long as Reset_l is low, the SPI does not accept a command word. Reset_l is high as soon as LDO_1 is higher than 2.5 V, which means, that the SPI will then be active.

- **Latch_h**: This signal is derived from Load_l and CS. A high signal loads the outputs of the D-Flip-Flops into the latches (named LA in the block diagram), and then the command word will be executed.
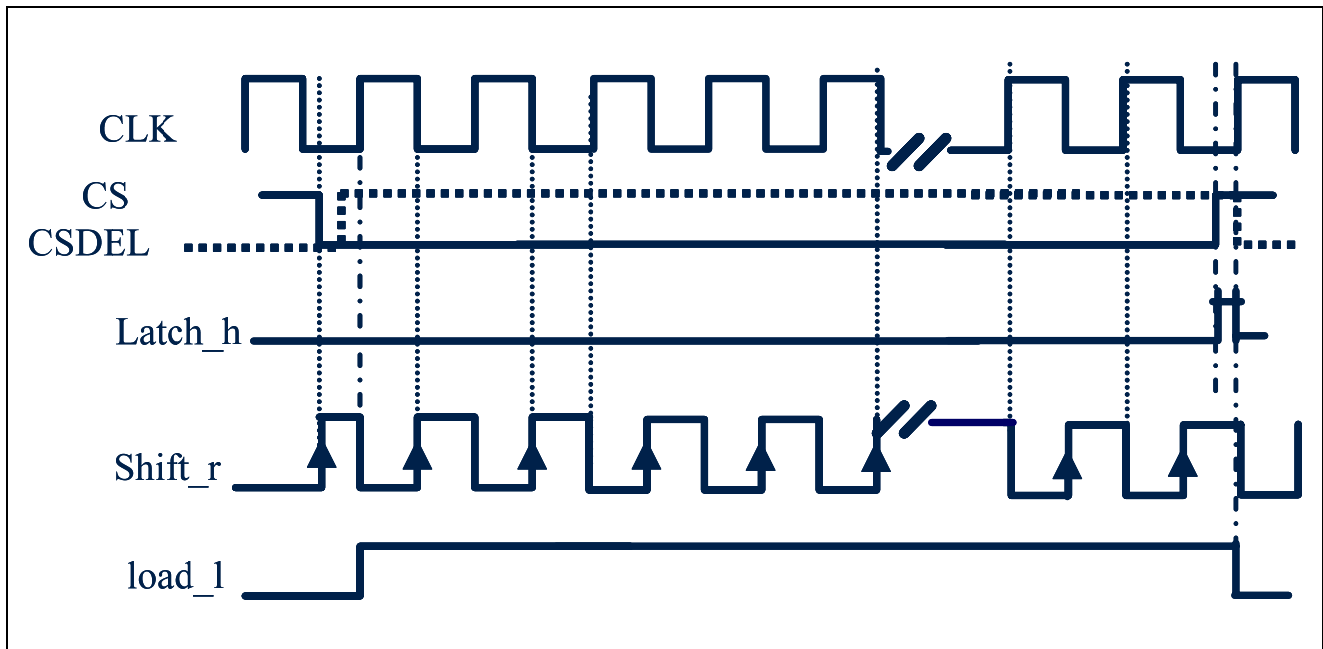
## 3.3    Signal Flow Diagram:



**Figure 2    Signal Flow Diagram of the SPI**

CS and CLK are the external signals, which the SPI receives at pins 3 and 4 from the microprocessor. A low at CS activates the SPI, with a clock signal at CLK the information at pin DI is read, while the SPI writes the status at pin DO (actual status word).

The internal signal CSDEL is derived form CS, but inverted with a 200 ns time delay. It is used to form the signal Load_l together with the next rising edge of CLK.

As soon as CS goes to low, the SPI is active.

CS going to low forms the first Shift_r pulse. At this time, Load_l is low, which means, that the MUX inputs are switched to the internal status bits Qs(n), thus the status of the device is written into the SPI.

Then Load_l goes to high, the MUX inputs are switched to outputs of the previous D-Flip-Flop and the first D-Flip-Flop is switched to Pin DI.

The following falling edge of CLK forms a rising edge of Load_l, which triggers the chain of D-Flip-Flops and the information is shifted to the right. Every falling edge at CLK makes the SPI read the information at pin DI and write the information at the output of the last D-Flip-Flop to pin DO. Thus the new command word is written into the Daisy chain of D-Flip-Flops from the left, while the status of the device present in the Daisy chain of D-Flip-Flops is transferred to the left.

After 16 CLK pulses the new command word is written into the Daisy Chain of D-Flip-Flops and CS returns to high.

CS returning to high and therefore CSDEL going to low 200 ns later forms the Latch-h signal, which loads the outputs of the D-Flip-Flops (RBSQ) into the latches (named LA). The (new) command word is now stable and will be executed.

As there is no validity check included, a command word of less than 16 bit or more than 16 bit will also be accepted, but lead to an undesired configuration of the device.

# 4 Disturbance of SPI Communication:

## 4.1 Glitches on signals CS and CLK during initialization of the microprocessor

Figure 3 shows glitches on the signals CS (green curve) and CLK (blue curve) during the initialization of the microprocessor, the yellow curve is the LDO_1 with 5 V that supplies the microprocessor and the red curve is the preregulator output.
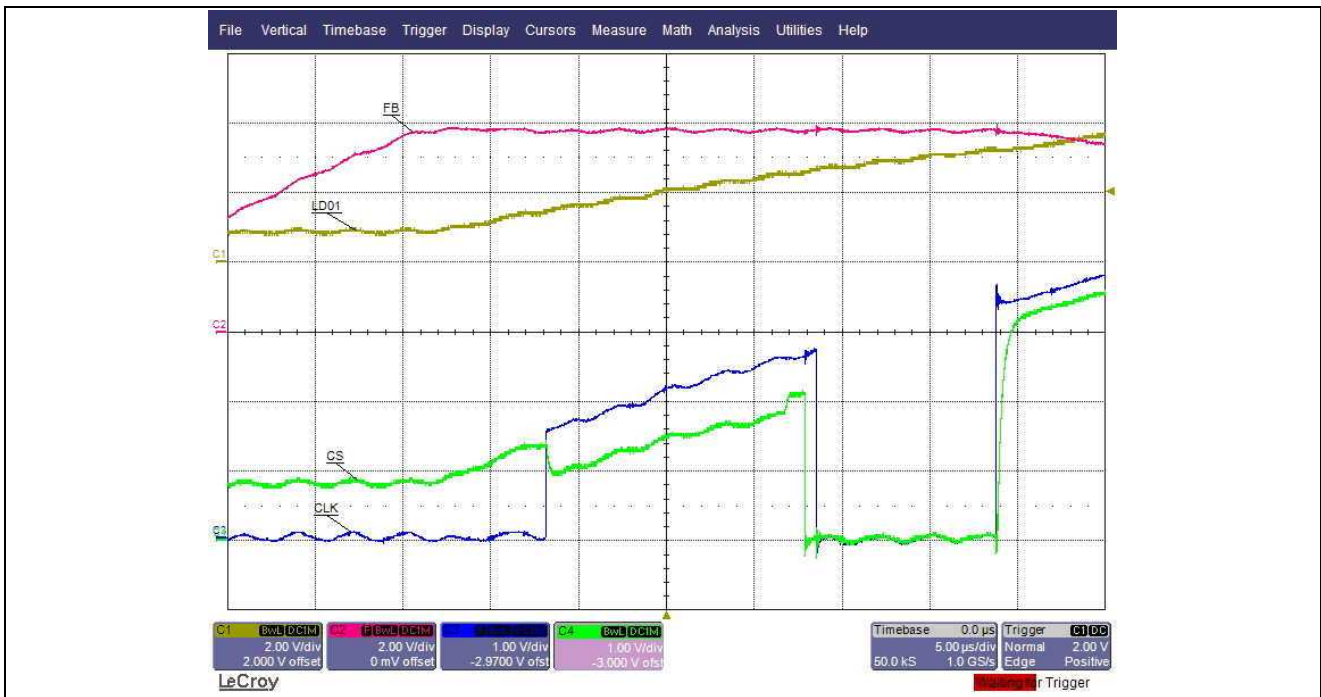


**Figure 3    Glitches on signals CS and CLK**

The microprocessor is emitting these glitches during start up. At this point the SPI is already active. This may lead to a false command word in the daisy chain of D-Flip-Flops. The false command word is generated by the internal status bits which are randomly read as low or high.

In consequence this leads either to an interrupt of the start up, if the sleep bit is activated or to a device configuration which is different from the expected default configuration after the start up.

A false command word may:

- Switch one or more of the trackers off, where they are intended to be on -> tracker voltage missing
- Send the device to sleep -> double start, if Wake pin (pin 34) is connected to input voltage
- Set the Reset delay time to 16, 32 or 64 ms
- Set the Watchdog timing to 64, 32 or 16 ms -> Watchdog failure due to wrong timing
- Switch the watchdog on, where it is intended to be off -> Watchdog failure due to missing trigger

A false command word will not lead to a partial destruction or degradation of the function.

## 4.2     Recommendations:

- Please be aware, that the SPI will be active from the beginning (as soon as LDO_1 output voltage exceeds 2.5 V)

- As there is no validity check included, the SPI will accept any command word.

- Please avoid glitches on CLK and CS signals during initialization of the microprocessor; they may cause an unintended command word in the SPI, which may lead to a configuration different from default.

- If those glitches should be inevitable, please overwrite the actual status with the desired status.

- Make sure that your command word consists of 16 bits.

- A false command word in the TLE6368 will not lead to damage, but will disturb the proper function of the application (i.e. wrong Window Watchdog timing)

# 5        Additional Information

- Please contact your local Infineon representative for further assistance and additional information
- For further information you may also contact **http://www.infineon.com/**

**AP Number**

| **Revision History:** | 2010-10-10 | Rev 1.0 |
|---|---|---|
| Version 1.0: | Initial release | |

| Page | Page |
|---|---|
| | |
| | |
| | |
| | |
| | |
| | |
| | |

**Information**

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

**Warnings**

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.