# TDA8034HN

## Low power smart card interface

Rev. 3.5 — 13 March 2020 Product data sheet

## 1. General description

The TDA8034HN is a cost-effective analog interface for asynchronous and synchronous smart cards operating at 5 V, 3 V or 1.8 V. Using few external components, the TDA8034HN provides all supply, protection and control functions between a smart card and the microcontroller.

## 2. Features and benefits

- Integrated circuit smart card interface in an HVQFN24 package
- 5 V, 3 V or 1.8 V smart card supply
- Very low power consumption in Deep Shutdown mode
- Three protected half-duplex bidirectional buffered I/O lines (C4, C7 and C8)
- $V_{CC}$ regulation:
  - 5 V, 3 V or 1.8 V ± 5 % using two low ESR multilayer ceramic capacitors: one of 220 nF and one of 470 nF
  - current spikes of 40 nA/s ($V_{CC}$ = 5 V and 3 V) or 15 nA/s ($V_{CC}$ =1.8 V) up to 20 MHz, with controlled rise and fall times and filtered overload detection of approximately 120 mA
- Thermal and short-circuit protection for all card contacts
- Automatic activation and deactivation sequences triggered by a short-circuit, card take-off, overheating, falling $V_{DD}$, $V_{DD(INTF)}$ or $V_{DDP}$
- Enhanced card-side ElectroStatic Discharge (ESD) protection of > 8 kV
- External clock input up to 26 MHz connected to pin XTAL1
- Card clock generation up to 20 MHz using pins CLKDIV1 and CLKDIV2 with synchronous frequency changes of $f_{xtal}$, ½ $f_{xtal}$, ¼ $f_{xtal}$ or ⅛ $f_{xtal}$
- Non-inverted control of pin RST using pin RSTIN
- Compatible with ISO 7816, NDS and EMVCo4.3 [1] payment systems
- Supply supervisor for killing spikes during power on and off:
  - using a fixed threshold
  - using an external resistor bridge with threshold adjustment
- Built-in debouncing on card presence contacts (typically 8 ms)
- Multiplexed status signal using pin OFFN

1. For C2 version

## 3. Applications

- Pay TV
- Electronic payment
- Identification
- Bank card readers

## 4. Quick reference data

**Table 1. Quick reference data**

*$V_{DDP}$ = 5 V; $V_{DD}$ = 3.3 V; $V_{DD(INTF)}$ = 3.3 V; $f_{xtal}$ = 10 MHz; GND = 0 V; $T_{amb}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply** | | | | | | |
| $V_{DDP}$ | power supply voltage | pin $V_{DDP}$; regulator input | | | | |
| | | $V_{CC}$ = 5 V | 4.85 | 5 | 5.5 | V |
| | | $V_{CC}$ = 3 V and 1.8 V | 3 | 3.3 | 5.5 | V |
| $V_{DD}$ | supply voltage | pin $V_{DD}$ | 2.7 | 3.3 | 3.6 | V |
| $V_{DD(INTF)}$ | interface supply voltage | pin $V_{DD(INTF)}$ | 1.6 | 3.3 | $V_{DD}$ + 0.3 | V |
| $I_{DD}$ | supply current | shutdown mode | - | - | 35 | µA |
| | | deep shutdown mode | - | - | 12 | µA |
| | | active mode | - | - | 2 | mA |
| $I_{DDP}$ | power supply current | shutdown mode; $f_{xtal}$ stopped | - | - | 5 | µA |
| | | active mode; $f_{CLK}$ = ½ $f_{xtal}$; no load | - | - | 1.5 | mA |
| $I_{DD(INTF)}$ | interface supply current | shutdown mode | - | - | 6 | µA |
| | | active mode | - | - | 2 | mA |
| **Card supply voltage: pin $V_{CC}$**[1] | | | | | | |
| $V_{CC}$ | supply voltage | active mode; $I_{CC}$ < 65 mA DC | | | | |
| | | 5 V card | 4.75 | 5.0 | 5.25 | V |
| | | 3 V card | 2.85 | 3.05 | 3.15 | V |
| | | 1.8 V card | 1.71 | 1.83 | 1.89 | V |
| | | active mode; current pulses of 40 nA/s at $I_{CC}$ < 200 mA; t < 400 ns | | | | |
| | | 5 V card | 4.65 | 5.0 | 5.25 | V |
| | | 3 V card | 2.76 | - | 3.20 | V |
| | | active mode; current pulses of 15 nA/s at $I_{CC}$ < 200 mA, t < 400 ns; 1.8 V card | 1.66 | - | 1.94 | V |
| $V_{ripple(p-p)}$ | peak-to-peak ripple voltage | from 20 kHz to 200 MHz | - | - | 350 | mV |
| $I_{CC}$ | supply current | $V_{CC}$ = 0 V to 5 V, 3 V or 1.8 V | - | - | 65 | mA |
| **General** | | | | | | |
| $t_{deact}$ | deactivation time | see Figure 8 on page 12 | 35 | 90 | 250 | µs |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = −25 °C to +85 °C | - | - | 0.25 | W |
| $T_{amb}$ | ambient temperature | | −25 | - | +85 | °C |

[1] To meet these specifications, $V_{CC}$ should be decoupled to pin GND using two ceramic multilayer capacitors of low ESR with values of either 100 nF or one 220 nF and one 470 nF.

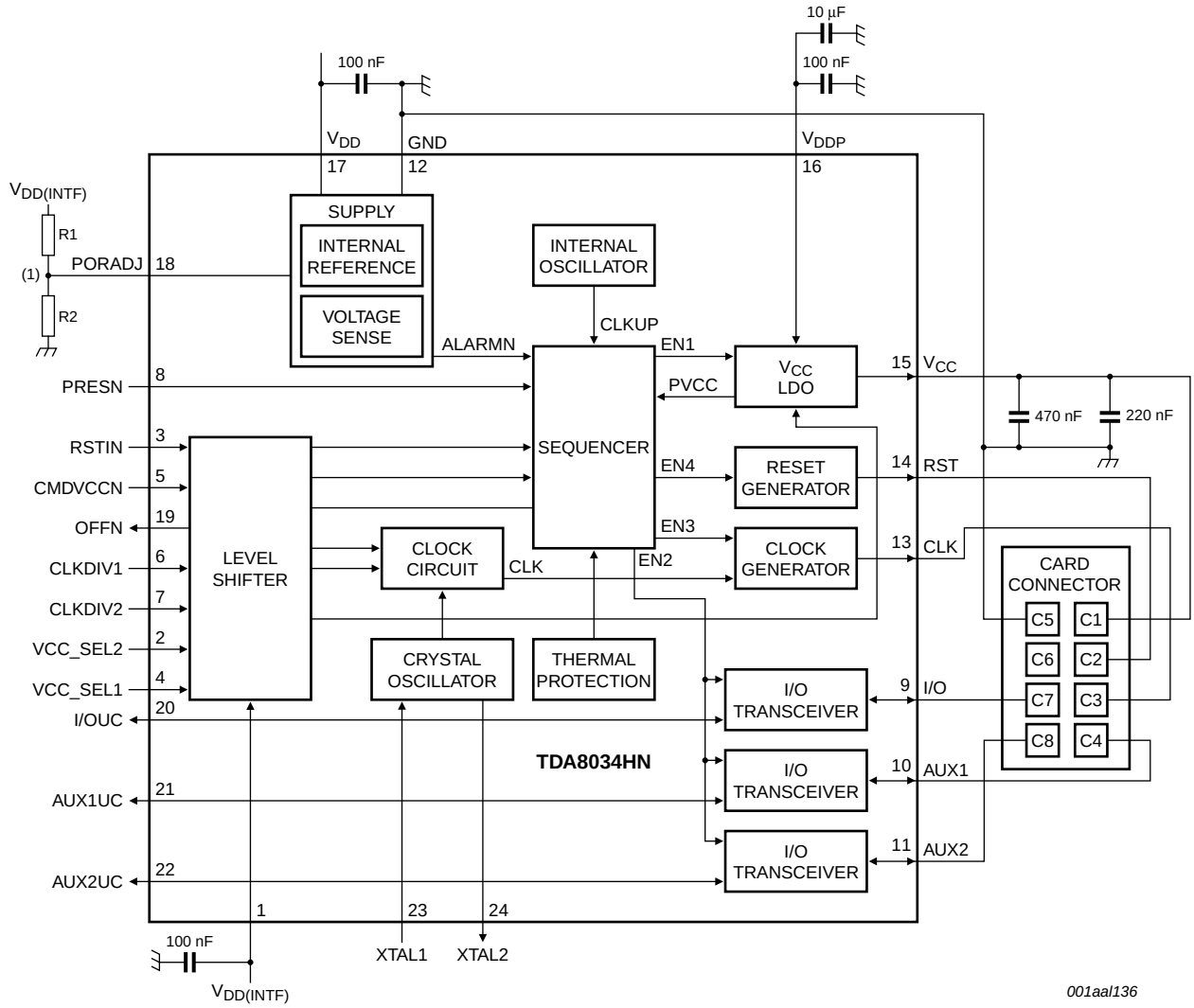
## 5. Ordering information

The TDA8034HN is available in 2 versions. Both have the same functionality. C2 version is compliant with EMVCo 4.3

**Table 2. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| TDA8034HN/C1 | HVQFN24 | plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm | SOT616-1 |
| TDA8034HN/C2 | HVQFN24 | plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm | SOT616-1 |

## 6. Block diagram




ALARMN, CLKUP, EN1, PVCC, EN4, EN3, EN2 and CLK are internal signals.

(1) Optional external resistor bridge, if not required connect pin PORADJ to $V_{DD(INTF)}$

**Fig 1. Block diagram**

# 7. Pinning information

## 7.1 Pinning

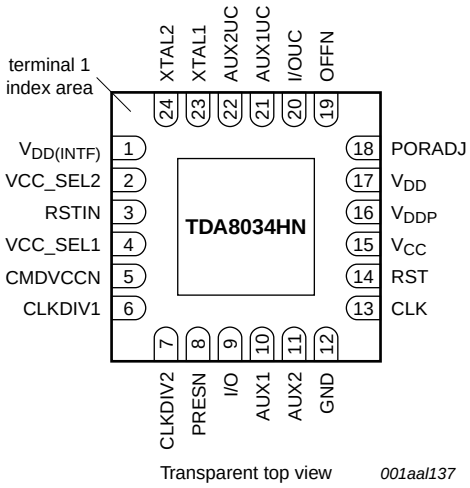



**Fig 2. Pin configuration**

## 7.2 Pin description

**Table 3. Pin description**

| Symbol | Pin | Supply | Type[1] | Description |
|---|---|---|---|---|
| $V_{DD(INTF)}$ | 1 | $V_{DD(INTF)}$ | P | interface supply voltage |
| VCC_SEL2 | 2 | $V_{DD(INTF)}$ | I | 5 V or 3 V $V_{CC}$ voltage selection control signal: |
| | | | | active LOW: $V_{CC}$ = 3 V when pin VCC_SEL1 is HIGH |
| | | | | active HIGH: $V_{CC}$ = 5 V |
| RSTIN | 3 | $V_{DD(INTF)}$ | I | microcontroller card reset input; active HIGH |
| VCC_SEL1 | 4 | $V_{DD(INTF)}$ | I | 1.8 V $V_{CC}$ voltage selection control signal: |
| | | | | active LOW: $V_{CC}$ = 1.8 V |
| | | | | active HIGH: disables 1.8 V selection |
| CMDVCCN | 5 | $V_{DD(INTF)}$ | I | microcontroller start activation sequence input; active LOW |
| CLKDIV1 | 6 | $V_{DD(INTF)}$ | I | sets the clock frequency on pin CLK in association with pin CLKDIV2; see Table 4 |
| CLKDIV2 | 7 | $V_{DD(INTF)}$ | I | sets the clock frequency on pin CLK in association with pin CLKDIV1; see Table 4 |
| PRESN | 8 | $V_{DD(INTF)}$ | I | card presence contact input; active LOW[2] |
| I/O | 9 | $V_{CC}$ | I/O | card input/output data line (C7)[3] |
| AUX1 | 10 | $V_{CC}$ | I/O | auxiliary card input/output data line (C4)[3] |
| AUX2 | 11 | $V_{CC}$ | I/O | auxiliary card input/output data line (C8)[3] |
| GND | 12 | - | G | ground |
| CLK | 13 | $V_{CC}$ | O | card clock (C3) |
| RST | 14 | $V_{CC}$ | O | card reset (C2) |
| $V_{CC}$ | 15 | $V_{CC}$ | P | card supply (C1); decouple to pin GND using one 470 nF capacitor close to pin $V_{CC}$ and one 220 nF capacitor close to card socket contact C1 with an ESR < 100 mΩ |

**Table 3. Pin description** *...continued*

| Symbol | Pin | Supply | Type[1] | Description |
|---|---|---|---|---|
| $V_{DDP}$ | 16 | $V_{DDP}$ | P | low-dropout regulator input supply voltage |
| $V_{DD}$ | 17 | $V_{DD}$ | P | digital supply voltage |
| PORADJ | 18 | $V_{DD(INTF)}$ | I | power-on reset threshold adjustment input using an optional external resistor bridge |
| OFFN | 19 | $V_{DD(INTF)}$ | O | NMOS interrupt to microcontroller[4]; active LOW; see Section 8.10 on page 12 |
| I/OUC | 20 | $V_{DD(INTF)}$ | I/O | microcontroller input/output data line[5] |
| AUX1UC | 21 | $V_{DD(INTF)}$ | I/O | auxiliary microcontroller input/output data line[5] |
| AUX2UC | 22 | $V_{DD(INTF)}$ | I/O | auxiliary microcontroller input/output data line[5] |
| XTAL1 | 23 | $V_{DD}$ | I | crystal connection input |
| XTAL2 | 24 | $V_{DD}$ | O | crystal connection output |

[1] I = input, O = output, I/O = input/output, G = ground and P = power supply.

[2] If pin PRESN is LOW, the card is considered to be present. During card insertion, debouncing can occur on these signals. To counter this, the TDA8034HN has a built-in debouncing timer (typically 8 ms).

[3] Uses an internal 11 kΩ pull-up resistor connected to pin $V_{CC}$.

[4] Uses an internal 20 kΩ pull-up resistor connected to pin $V_{DD(INTF)}$.

[5] Uses an internal 10kW pull-up resistor connected to pin $V_{DD(INTF)}$

# 8. Functional description

**Remark:** Throughout this document the ISO 7816 terminology conventions have been adhered to and it is assumed that the reader is familiar with these.

## 8.1 Power supplies

The power supply voltage ranges are as follows:

- $V_{DDP}$: 4.85 V to 5.5 V when VCC_SEL2 is HIGH ($V_{CC}$ = 5 V)
- $V_{DDP}$: 3 V to 5.5 V when VCC_SEL2 is LOW ($V_{CC}$ = 3 V) or when VCC_SEL1 is LOW ($V_{CC}$ = 1.8 V)
- $V_{DD}$: 2.7 V to 3.6 V

All interface signals to the system controller are referenced to $V_{DD(INTF)}$. All card contacts remain inactive during power up or power down. After powering up the device, pin OFFN remains LOW until pin CMDVCCN is set HIGH and pin PRESN is LOW. During power down, pin OFFN goes LOW when $V_{DDP}$ falls below the falling threshold voltage ($V_{th}$).

The internal oscillator frequency ($f_{osc(int)}$) is only used during the activation sequences. When the card is not activated (pin CMDVCCN is HIGH), the internal oscillator is in low frequency mode to reduce power consumption.

This device has a Low Drop-Off (LDO) voltage regulator connected to pin $V_{CC}$, and is used instead of a DC-to-DC converter. It ensures a minimum $V_{CC}$ of 4.75 V and that the power supply voltage on pin $V_{DDP}$ does not fall below 4.85 V when pin VCC_SEL2 is HIGH, for a maximum load current of 65 mA.

In case the 3  power supply VDD, VDDP, VDD(INTF) are connected together (VDD =VDDP= VDD(INTF)) and if the power up slope is faster than 1ms (10%-90% slope<1ms), a deep shutdown sequence  must be performed once the supplies have  reached steady state; this means CMDVCCN is set high while VCC_SEL1 and VCC_SEL2 forced to low level (see Section 8.6 “Deep shutdown mode”).

## 8.2 Voltage supervisor

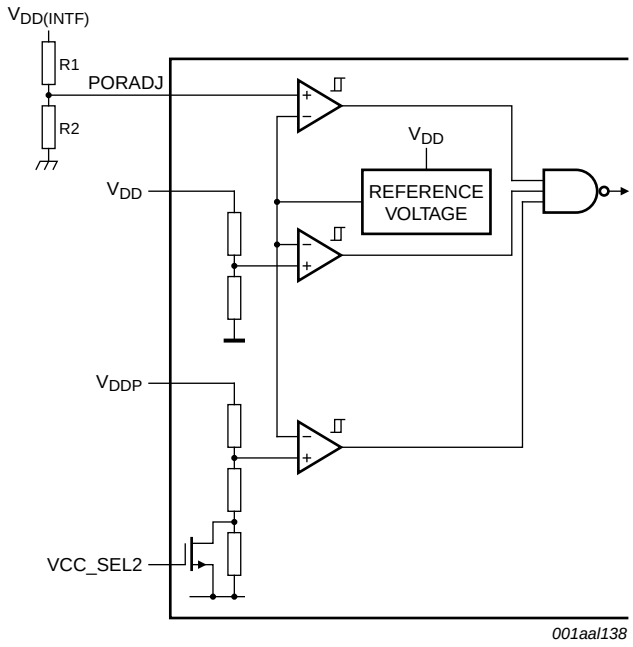



**Fig 3. Voltage supervisor circuit**

The voltage supervisor monitors the voltage of the $V_{DDP}$, $V_{DD}$ and $V_{DD(INTF)}$ supplies providing both Power-On Reset (POR) and supply drop-out detection during a card session. The supervisor threshold voltages for $V_{DDP}$ and $V_{DD}$ are set internally, and for $V_{DD(INTF)}$ externally by pin PORADJ. As long as $V_{DD}$ is less than $V_{th} + V_{hys}$, the IC remains inactive irrespective of the command line levels. After $V_{DD}$ has reached a level higher than $V_{th} + V_{hys}$, the IC remains inactive for the duration of $t_w$. The output of the supervisor is sent to a digital controller in order to reset the TDA8034HN. This defined reset pulse of approximately 8 ms, i.e. ($t_w = 1024 \times {}^{1}/_{f_{osc(int)low}}$), is used internally to maintain the IC in the Shutdown mode during the supply voltage power on; see Figure 4. A deactivation sequence is performed when either $V_{DD}$, $V_{DDP}$ or $V_{DD(INTF)}$ falls below $V_{th}$.

**Remark:** $f_{osc(int)low}$ is the low frequency (or inactive) mode of the defined $f_{osc(int)}$ parameter.

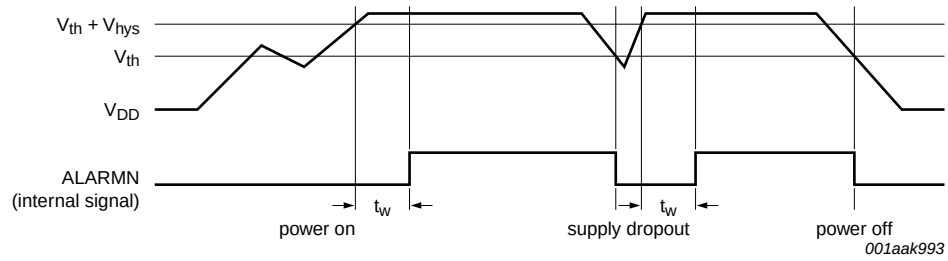
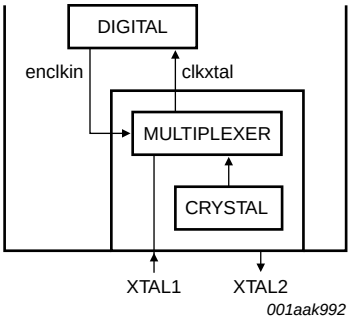



**Fig 4. Voltage supervisor waveforms**

## 8.3 Clock circuits

The clock signal from pin CLK to the card is either supplied by an external clock signal connected to pin XTAL1 or generated using a crystal connected between pins XTAL1 and XTAL2. The TDA8034HN automatically detects if an external clock is connected to XTAL1, eliminating the need for a separate pin to select the clock source.

Automatic clock source detection is performed on each activation command (falling edge of the signal on pin CMDVCCN). The presence of an external clock on pin XTAL1 is checked during a time window defined by the internal oscillator. If a clock is detected, the internal crystal oscillator is stopped. If a clock is not detected, the internal crystal oscillator is started. When an external clock is used, it is mandatory that the clock is applied to pin XTAL1 before the falling edge of the signal on pin CMDVCCN.




enclkin and clkxtal are internal signal names.

**Fig 5. Basic layout for using an external clock**

The clock frequency is selected using pins CLKDIV1 and CLKDIV1 to be either $f_{xtal}$, $\frac{1}{2}$ $f_{xtal}$ or $\frac{1}{4}$ $f_{xtal}$ or $\frac{1}{8}$ $f_{xtal}$ as shown in Table 4.

**Remark:** The levels on both pins must not be allowed to change simultaneously but should be separated by a minimum of 10 ns.

The frequency change is synchronous and as such during transition, no pulse is shorter than 45 % of the smallest period. In addition, only the first and last clock pulse around the change has the correct width. When dynamically changing the frequency, the modification is only effective after 10 clock periods on pin XTAL1.

The duty cycle of $f_{xtal}$ on pin CLK should be between 45 % and 55 %. If an external clock is connected to pin XTAL1, its duty cycle must be between 48 % and 52 %.

When the frequency of the clock signal on pin CLK is either $f_{xtal}$, $\frac{1}{2} f_{xtal}$, $\frac{1}{4} f_{xtal}$ or $\frac{1}{8} f_{xtal}$, the frequency dividers guarantee a duty cycle between 45 % and 55 %.

**Table 4. Clock configuration**

| Pin CLKDIV1 level | Pin CLKDIV2 level | Pin CLK frequency |
|---|---|---|
| LOW | LOW | $\frac{1}{8} f_{xtal}$ |
| LOW | HIGH | $\frac{1}{4} f_{xtal}$ |
| HIGH | HIGH | $\frac{1}{2} f_{xtal}$ |
| HIGH | LOW | $f_{xtal}$ |

## 8.4 Input and output circuits

When pins I/O and I/OUC are pulled HIGH using an 11 kΩ resistor between pins I/O and $V_{CC}$ and/or between pins I/OUC and $V_{DD(INTF)}$, both lines enter the idle state. Pin I/O is referenced to $V_{CC}$ and pin I/OUC to $V_{DD(INTF)}$, thus allowing operation at $V_{CC} \neq V_{DD(INTF)}$.

The first side on which a falling edge occurs becomes the master. An anti-latch circuit disables falling edge detection on the other line, making it the slave. After a time delay $t_d$, the logic 0 present on the master-side is sent to the slave-side. When the master-side returns logic 1, the slave-side sends logic 1 during time delay ($t_{w(pu)}$). After this sequence, both master and slave sides return to their idle states.

The active pull-up feature ensures fast LOW-to-HIGH transitions making the TDA8034HN capable of delivering more than 1 mA, up to an output voltage of $0.9V_{CC}$, at a load of 80 pF. At the end of the active pull-up pulse, the output voltage is dependent on the internal pull-up resistor value and load current. The current sent to and received from the card's I/O lines is limited to 15 mA at a maximum frequency of 1 MHz.

## 8.5 Shutdown mode

After a power-on reset, if pin CMDVCCN is HIGH, the circuit enters the Shutdown mode, ensuring only the minimum number of circuits are active while the TDA8034HN waits for the microcontroller to start a session.

- all card contacts are inactive. The impedance between the contacts and GND is approximately 200 Ω.
- pins I/OUC, AUX1UC and AUX2UC are high-impedance using the 11 kΩ pull-up resistor connected to $V_{DD(INTF)}$
- the voltage generators are stopped
- the voltage supervisor is active
- the internal oscillator runs at its lowest frequency ($f_{osc(int)low}$)

## 8.6 Deep shutdown mode

When the smart card reader is inactive, the TDA8034HN will enter Deep shutdown mode if pin CMDVCCN is forced HIGH and pins VCC_SEL1 and VCC_SEL2 are LOW. In Deep shutdown mode, all circuits are disabled and pin OFFN follows the status of pin PRESN. Changing the status of either pin CMDVCCN, VCC_SEL1 or VCC_SEL2 exits Deep shutdown mode; see Figure 6.

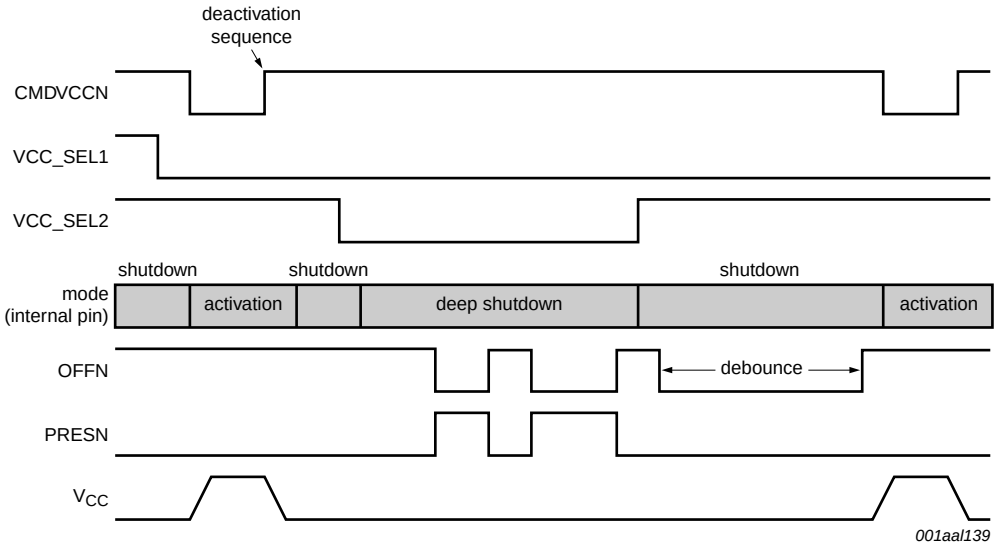



**Fig 6. Shutdown and Deep shutdown mode activation/deactivation**

## 8.7 Activation sequence

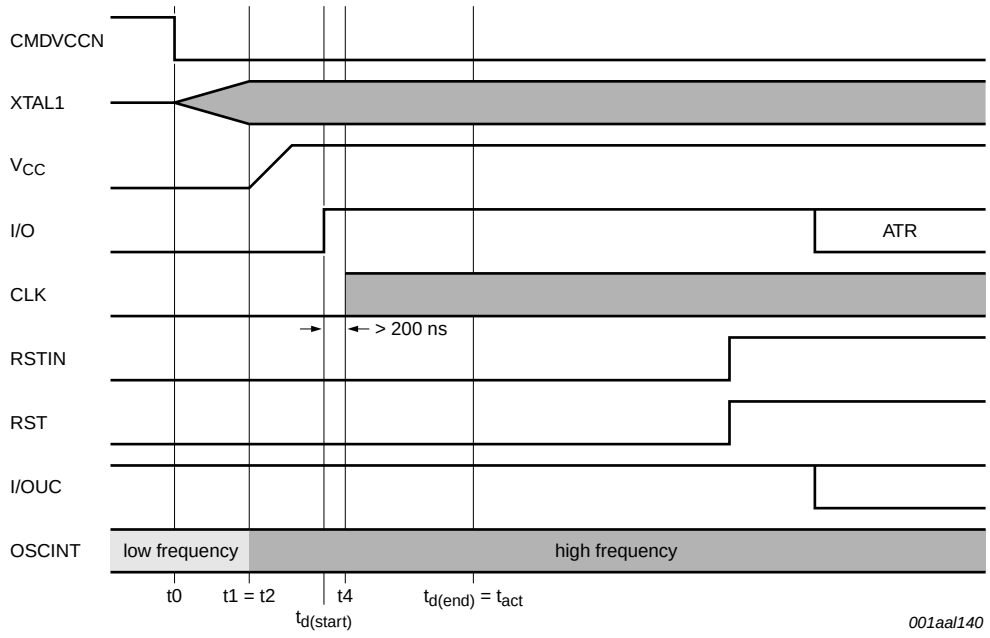
The following device activation sequence is applied when using an external clock; see Figure 7:

1. Pin CMDVCCN is pulled LOW (t0).
2. The internal oscillator is triggered (t0).
3. The internal oscillator changes to high frequency (t1).
4. $V_{CC}$ rises from either 0 V to 3 V or 0 V to 5 V on a controlled slope (t2).
5. Pins I/OUC, AUX1UC and AUX2UC are driven HIGH (t3).
6. The clock on pin CLK is applied to the C3 contact (t4).
7. Pin RST is enabled (t5).

Calculation of the time delays is as follows:

- t1 = t0 + 384 × $^{1}/_{f_{osc(int)low}}$
- t2 = t1
- t3 = t1 + 17T / 2
- t4 = driven by host controller; > t3 and < t5
- t5 = t1 + 23T / 2

**Remark:** The value of period T is 64 times the period interval of the internal oscillator at high frequency ($^{1}/_{f_{osc(int)high}}$); t3 is called $t_{d(start)}$ and t5 is called $t_{d(end)}$.




OSCINT = internal oscillator.

**Fig 7. Activation sequence at t3**

## 8.8 Deactivation sequence

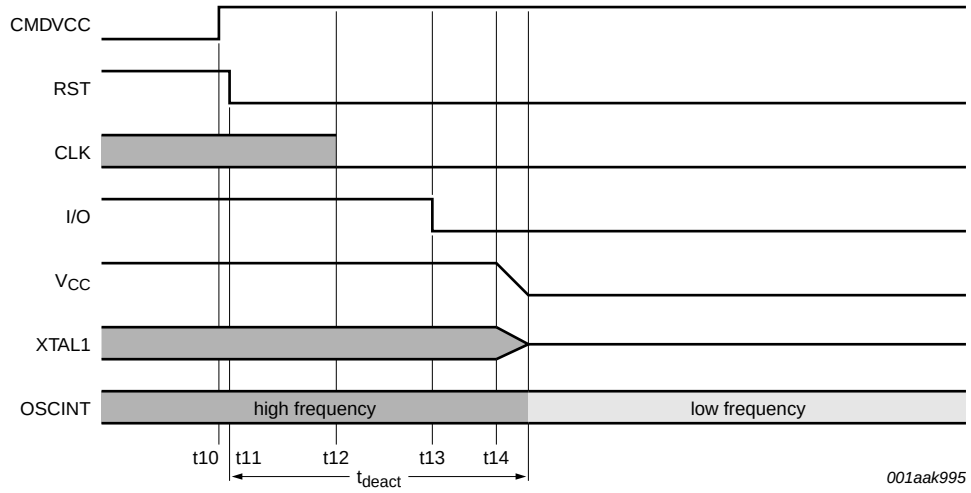
When a session ends, the microcontroller sets pin CMDVCCN HIGH. The TDA8034HN then executes an automatic deactivation sequence by counting the sequencer back to the inactive state (see Figure 8) as follows:

1. Pin RST is pulled LOW (t11).
2. The clock is stopped, pin CLK is LOW (t12).
3. Pins I/OUC, AUX1UC and AUX2UC are pulled LOW (t13).
4. $V_{CC}$ falls to 0 V (t14). The deactivation sequence is completed when $V_{CC}$ reaches its inactive state.
5. $V_{CC}$ < 0.4 V ($t_{deac}$)
6. All card contacts become low-impedance to GND. However, pins I/OUC, AUX1UC and AUX2UC remain pulled up to $V_{DD}$ using the 11 kΩ resistor.
7. The internal oscillator returns to its low frequency mode.

Calculation of the time delays is as follows:

- t11 = t10 + 3T / 64
- t12 = t11 + T / 2
- t13 = t11 + T
- t14 = t11 + 3T / 2
- $t_{deac}$ = t11 + 3T / 2 + $V_{CC}$ fall time

**Remark:** The value of period T is 64 times the period interval of the internal oscillator (i.e. ± 25 μs).




OSCINT = internal oscillator.

**Fig 8. Deactivation sequence**

## 8.9 $V_{CC}$ regulator

The $V_{CC}$ buffer is able to continuously deliver up to 65 mA at $V_{CC}$ = 5 V, 3 V, or 1.8 V.

The $V_{CC}$ buffer has an internal overload protection with a threshold value of approximately 120 mA. This detection is internally filtered, enabling spurious current pulses up to 200 mA with a duration of a few milliseconds to be drawn by the card without causing deactivation. However, the average current value must stay below maximum; see Table 8.

## 8.10 Fault detection

The following conditions are monitored by the fault detection circuit:

- Short-circuit or high current on pin $V_{CC}$
- Card removal during transaction
- $V_{DDP}$ falling
- $V_{DD}$ falling
- $V_{DD(INTF)}$ falling
- Overheating

Fault detection monitors two different situations:

- Outside card sessions, pin CMDVCCN is HIGH: pin OFFN is LOW if the card is not in the reader and HIGH if the card is in the reader. Any voltage drop on $V_{DD}$ is detected by the voltage supervisor. This generates an internal power-on reset pulse but does not act upon the pin OFFN signal. The card is not powered-up and short-circuits or overheating are not detected.

- In card sessions, pin CMDVCCN is LOW: when pin OFFN goes LOW, the fault detection circuit triggers the automatic emergency deactivation sequence (see Figure 9). When the microcontroller resets pin CMDVCCN to HIGH, after the deactivation sequence, pin OFFN is rechecked. If the card is still present, pin OFFN returns to HIGH. This check identifies the fault as either a hardware problem or a card removal incident.

On card insertion or removal, bouncing can occur in the PRESN signal. This depends on the type of card presence switch in the connector (normally open or normally closed) and the mechanical characteristics of the switch. To correct for this, a debouncing feature is integrated in to the TDA8034HN. This feature operates at a typical duration of 8 ms ($t_{deb}$ = 640 × ($^{1}/_{f_{osc(int)low}}$). Figure 10 on page 14 shows the operation of the debouncing feature.

On card insertion, pin OFFN goes HIGH after the debounce time has elapsed. When the card is extracted, the automatic card deactivation sequence is performed on the first HIGH/LOW transition on pin PRESN. After this, pin OFFN goes LOW.

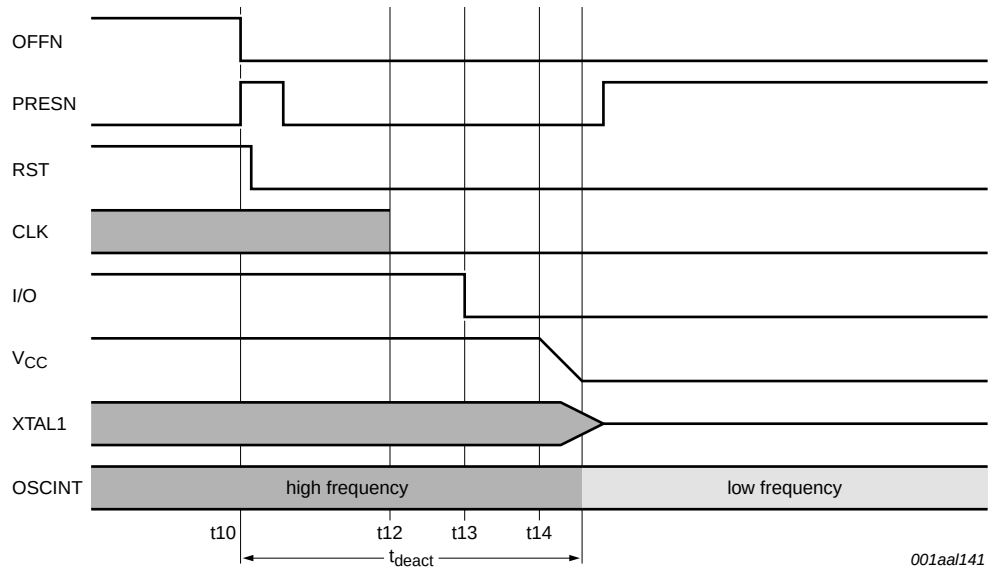
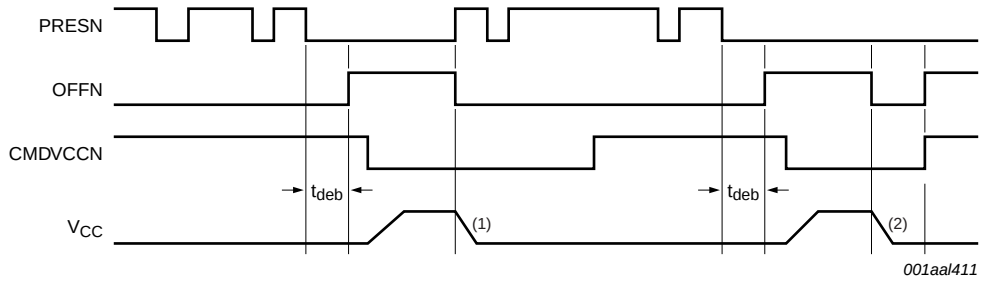



**Fig 9. Emergency deactivation sequence after card removal**




(1) Deactivation caused by card withdrawal.

(2) Deactivation caused by short-circuit.

**Fig 10. Operation of debounce feature with pins OFFN, CMDVCCN, PRESN and $V_{CC}$**

# 9. Limiting values

**Remark:** All card contacts are protected against any short-circuit to any other card contact. Stress beyond the levels indicated in Table 5 can cause permanent damage to the device. This is a short-term stress rating only and under no circumstances implies functional operation under long-term stress conditions.

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DDP}$ | power supply voltage | pin $V_{DDP}$ | –0.3 | +6 | V |
| $V_{DD}$ | supply voltage | pin $V_{DD}$ | –0.3 | +4.6 | V |
| $V_{DD(INTF)}$ | interface supply voltage | pin $V_{DD(INTF)}$ | –0.3 | +4.6 | V |
| $V_I$ | input voltage | pins CMDVCCN, CLKDIV1, CLKDIV2, VCC_SEL1, VCC_SEL2, RSTIN, OFFN, PORADJ, XTAL1, XTAL2, I/OUC, AUX1UC, AUX1UC | –0.3 | +4.6 | V |
| | | card contact pins PRESN, I/O, RST, AUX1, AUX2 and CLK | –0.3 | +6 | V |
| $T_{stg}$ | storage temperature | | –55 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = –25 °C to +85 °C | - | 0.25 | W |
| $T_j$ | junction temperature | | - | +125 | °C |
| $T_{amb}$ | ambient temperature | | –25 | +85 | °C |
| $V_{ESD}$ | electrostatic discharge voltage | Human Body Model (HBM) on card pins I/O, RST, $V_{CC}$, AUX1, AUX2, CLK; within typical application | –8 | +8 | kV |
| | | Human Body Model (HBM); all other pins[1] | –2 | +2 | kV |
| | | Machine Model (MM); all pins | –200 | +200 | V |
| | | Field Charged Device Model (FCDM); all pins | –500 | +500 | V |

[1] The PRESN pin supports ESD HBM discharge up to 7kV

## 10. Thermal characteristics

**Table 6. Thermal characteristics**

| Symbol | Package name | Parameter | Conditions | | Typ | Unit |
|---|---|---|---|---|---|---|
| $R_{th(j-a)}$ | HVQFN24 | thermal resistance from junction to ambient | in free air | | 53 | K/W |

## 11. Characteristics

**Table 7. Characteristics of IC supply voltage**

*$V_{DDP}$ = 5 V; $V_{DD}$ = 3.3 V; $V_{DD(INTF)}$ = 3.3 V; $f_{xtal}$ = 10 MHz; GND = 0 V; $T_{amb}$ = 25 °C; for C1 and C2 versions; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply** | | | | | | |
| $V_{DDP}$ | power supply voltage | pin $V_{DDP}$ | | | | |
| | | $V_{CC}$ = 5 V | 4.85 | 5 | 5.5 | V |
| | | $V_{CC}$ = 3 V or 1.8 V | 3 | 3.3 | 5.5 | V |
| $V_{DD}$ | supply voltage | pin $V_{DD}$ | 2.7 | 3.3 | 3.6 | V |
| $V_{DD(INTF)}$ | interface supply voltage | pin $V_{DD(INTF)}$ | 1.6 | 3.3 | $V_{DD}$ + 0.3 | V |
| $I_{DD}$ | supply current | shutdown mode | - | - | 35 | µA |
| | | deep shutdown mode | - | - | 12 | µA |
| | | active mode | - | - | 2 | mA |
| $I_{DDP}$ | power supply current | shutdown mode | | | | |
| | | $f_{xtal}$ stopped | - | - | 5 | µA |
| | | active mode | | | | |
| | | $f_{CLK}$ = ½ $f_{xtal}$; no load | - | - | 1.5 | mA |
| | | $f_{CLK}$ = ½ $f_{xtal}$; $I_{CC}$ = 65 mA | - | - | 70 | mA |
| $I_{DD(INTF)}$ | interface supply current | shutdown mode | - | - | 6 | µA |
| | | active mode | - | - | 2 | mA |
| $V_{th}$ | threshold voltage | no external resistors on pin PORADJ | | | | |
| | | pin $V_{DD}$ falling | 2.30 | 2.40 | 2.50 | V |
| | | pin $V_{DDP}$ falling; $V_{CC}$ = 5 V | 3.00 | 4.10 | 4.40 | V |
| | | external resistors on pin PORADJ | 1.20 | 1.24 | 1.29 | V |
| $V_{hys}$ | hysteresis voltage | no external resistors on pin PORADJ | | | | |
| | | pin $V_{DD}$ | 50 | 100 | 150 | mV |
| | | pin $V_{DDP}$; $V_{CC}$ = 5 V | 100 | 200 | 350 | mV |
| $t_w$ | pulse width | | 5.1 | 8 | 10.2 | ms |
| $I_L$ | leakage current | pin PORADJ < 0.5 V | −0.1 | +4 | +10 | µA |
| | | pin PORADJ > 1 V | −1 | - | +1 | µA |
| **Card supply voltage: pin $V_{CC}$[1]** | | | | | | |
| $C_{dec}$ | decoupling capacitance | connected to $V_{CC}$ [2] | 550 | - | 830 | nF |

**Table 7. Characteristics of IC supply voltage** *...continued*

*$V_{DDP}$ = 5 V; $V_{DD}$ = 3.3 V; $V_{DD(INTF)}$ = 3.3 V; $f_{xtal}$ = 10 MHz; GND = 0 V; $T_{amb}$ = 25 °C; for C1 and C2 versions; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_o$ | output voltage | Shutdown mode | | | | |
| | | no load | −0.1 | - | +0.1 | V |
| | | $I_o$ = 1 mA | −0.1 | - | +0.3 | V |
| $I_o$ | output current | Shutdown mode; pin $V_{CC}$ connected to ground | - | - | −1 | mA |
| $V_{CC}$ | supply voltage | 5 V card; Active mode : $I_{CC}$ < 65 mA DC | 4.75 | 5.0 | 5.25 | V |
| | | 3 V card; Active mode : $I_{CC}$ < 65 mA DC | 2.85 | 3.05 | 3.15 | V |
| | | 1.8 V card; Active mode : $I_{CC}$ < 35 mA DC | 1.71 | 1.83 | 1.89 | V |
| | | 5 V card; active mode; current pulses of 40 nA/s at $I_{CC}$ < 200 mA; t < 400 ns | 4.65 | 5.0 | 5.25 | V |
| | | 3 V card; active mode; current pulses of 40 nA/s at $I_{CC}$ < 200 mA; t < 400 ns | 2.76 | - | 3.20 | V |
| | | 1.8 V card; active mode; current pulses of 15 nA/s at $I_{CC}$ < 200 mA, t < 400 ns; | 1.66 | - | 1.94 | V |
| $V_{ripple(p-p)}$ | peak-to-peak ripple voltage | 20 kHz to 200 MHz | - | - | 350 | mV |
| $I_{CC}$ | supply current | $V_{CC}$ = 0 V to 5 V, 3 V or 1.8 V | - | - | 65 | mA |
| | | $V_{CC}$ shorted to ground | 90 | 120 | 150 | mA |
| SR | slew rate | 5 V card | 0.055 | 0.18 | 0.3 | V/µs |
| | | 3 V card | 0.040 | 0.18 | 0.3 | V/µs |
| | | 1.8 V card | 0.025 | 0.18 | 0.3 | V/µs |
| **Crystal oscillator: pins XTAL1 and XTAL2** | | | | | | |
| $C_{ext}$ | external capacitance | pins XTAL1 and XTAL2 (depending on the crystal or resonator specification) | - | - | 15 | pF |
| $f_{xtal}$ | crystal frequency | card clock reference; crystal oscillator | 2 | - | 26 | MHz |
| $f_{ext}$ | external frequency | external clock on pin XTAL1 | 0 | - | 26 | MHz |
| $V_{IL}$ | LOW-level input voltage | crystal oscillator | −0.3 | - | $+0.3V_{DD}$ | V |
| | | external clock | −0.3 | - | $+0.3V_{DD(INTF)}$ | V |
| $V_{IH}$ | HIGH-level input voltage | crystal oscillator | $0.7V_{DD}$ | - | $V_{DD}$ + 0.3 | V |
| | | external clock | $0.7V_{DD(INTF)}$ | - | $V_{DD(INTF)}$ + 0.3 | V |
| **Data lines: pins I/O, I/OUC, AUX1, AUX2, AUXIUC and AUX2UC** | | | | | | |
| $t_d$ | delay time | falling edge on pins I/O and I/OUC or vise versa | - | - | 200 | ns |

**Table 7. Characteristics of IC supply voltage** *...continued*

*$V_{DDP}$ = 5 V; $V_{DD}$ = 3.3 V; $V_{DD(INTF)}$ = 3.3 V; $f_{xtal}$ = 10 MHz; GND = 0 V; $T_{amb}$ = 25 °C; for C1 and C2 versions; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{w(pu)}$ | pull-up pulse width | | 200 | - | 400 | ns |
| $f_{io}$ | input/output frequency | on data lines | - | - | 1 | MHz |
| $C_i$ | input capacitance | on data lines | - | - | 10 | pF |
| **Data lines to the card: pins I/O, AUX1and AUX2[3]** | | | | | | |
| $V_o$ | output voltage | Shutdown mode | | | | |
| | | no load | 0 | - | 0.1 | V |
| | | $I_o$ = 1 mA | 0 | - | 0.3 | V |
| $I_o$ | output current | Shutdown mode; pin I/O grounded | - | - | −1 | mA |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 1 mA- C1 version | 0 | - | 0.3 | V |
| | | $I_{OL}$ = 1 mA- C2 version | 0 | - | 0.15 $V_{CC}$ | V |
| | | $I_{OL} \geq$ 15 mA | $V_{CC}$ − 0.4 | - | $V_{CC}$ | V |
| $V_{OH}$ | HIGH-level output voltage | no DC load | 0.9$V_{CC}$ | - | $V_{CC}$ + 0.1 | V |
| | | $I_{OH} \geq$ −15 mA | 0 | - | 0.4 | V |
| | | C1 version | | | | |
| | | $I_{OH}$ < −40 µA; 5 V or 3 V | 0.75$V_{CC}$ | - | $V_{CC}$ + 0.1 | V |
| | | $I_{OH}$ < −20 µA; 1.8 V | 0.75$V_{CC}$ | - | $V_{CC}$ + 0.1 | V |
| | | C2 version | | | | |
| | | $I_{OH}$ < −40 µA; 5 V or 3 V | 0.8 $V_{CC}$ | - | $V_{CC}$ + 0.1 | V |
| | | $I_{OH}$ < −20 µA; 1.8 V | 1.28 | - | $V_{CC}$ + 0.1 | V |
| $V_{IL}$ | LOW-level input voltage | C1 version | −0.3 | - | +0.8 | V |
| | | C2 version | −0.3 | - | 0.2 $V_{CC}$ | V |
| $V_{IH}$ | HIGH-level input voltage | C1 version | | | | |
| | | $V_{CC}$ = 5 V | 0.6$V_{CC}$ | - | $V_{CC}$ + 0.3 | V |
| | | $V_{CC}$ = 3 V or 1.8 V | 0.7$V_{CC}$ | - | $V_{CC}$ + 0.3 | V |
| | | C2 version | | | | |
| | | $V_{CC}$ = 5 V or 3V | 0.6$V_{CC}$ | - | $V_{CC}$ + 0.3 | V |
| | | $V_{CC}$ = 1.8 V | 1.55 | - | $V_{CC}$ + 0.3 | V |
| $V_{hys}$ | hysteresis voltage | pin I/O | - | 50 | - | mV |
| $I_{IL}$ | LOW-level input current | pin I/O; $V_{IL}$ = 0 V | - | - | 600 | µA |
| $I_{IH}$ | HIGH-level input current | pin I/O; $V_{IH}$ = $V_{CC}$ | - | - | 10 | µA |
| $t_{r(i)}$ | input rise time | $V_{IL}$ maximum to $V_{IH}$ minimum | - | - | 1.2 | µs |
| $t_{r(o)}$ | output rise time | $C_L \leq$ 80 pF; 10 % to 90 %; 0 V to $V_{CC}$ | - | - | 0.1 | µs |
| $t_{f(i)}$ | input fall time | $V_{IL}$ maximum to $V_{IH}$ minimum | - | - | 1.2 | µs |
| $t_{f(o)}$ | output fall time | $C_L \leq$ 80 pF; 10 % to 90 %; 0 V to $V_{CC}$ | - | - | 0.1 | µs |
| $R_{pu}$ | pull-up resistance | connected to $V_{CC}$ | 7 | 9 | 11 | kΩ |

**Table 7. Characteristics of IC supply voltage** *...continued*

*$V_{DDP}$ = 5 V; $V_{DD}$ = 3.3 V; $V_{DD(INTF)}$ = 3.3 V; $f_{xtal}$ = 10 MHz; GND = 0 V; $T_{amb}$ = 25 °C; for C1 and C2 versions; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{pu}$ | pull-up current | $V_{OH}$ = 0.9$V_{CC}$; C = 80 pF | –8 | –6 | –4 | mA |
| **Data lines to the system: pins I/OUC, AUX1UC and AUX2UC[4]** | | | | | | |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 1 mA | 0 | - | 0.3 | V |
| $V_{OH}$ | HIGH-level output voltage | no DC load | 0.9$V_{DD(INTF)}$ | - | $V_{DD(INTF)}$ + 0.1 | V |
| | | $I_{OH} \leq$ 40 µA; $V_{DD(INTF)}$ > 2 V | 0.75$V_{DD(INTF)}$ | - | $V_{DD(INTF)}$ + 0.1 | V |
| | | $I_{OH} \leq$ 20 µA; $V_{DD(INTF)}$ < 2 V | 0.75$V_{DD(INTF)}$ | - | $V_{DD(INTF)}$ + 0.1 | V |
| $V_{IL}$ | LOW-level input voltage | | –0.3 | - | +0.3$V_{DD(INTF)}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | 0.7$V_{DD(INTF)}$ | - | $V_{DD(INTF)}$ + 0.3 | V |
| $V_{hys}$ | hysteresis voltage | pin I/OUC | - | 0.14$V_{DD(INTF)}$ | - | V |
| $I_{IH}$ | HIGH-level input current | $V_{IH}$ = $V_{DD(INTF)}$ | - | - | 10 | µA |
| $I_{IL}$ | LOW-level input current | $V_{IL}$ = 0 V | - | - | 600 | µA |
| $R_{pu}$ | pull-up resistance | connected to $V_{DD(INTF)}$ | 8 | 10 | 12 | kΩ |
| $t_{r(i)}$ | input rise time | $V_{IL}$ maximum to $V_{IH}$ minimum | - | - | 1.2 | µs |
| $t_{r(o)}$ | output rise time | $C_L \leq$ 30 pF; 10 % to 90 %; 0 V to $V_{DD(INTF)}$ | - | - | 0.1 | µs |
| $t_{f(i)}$ | input fall time | $V_{IL}$ maximum to $V_{IH}$ minimum | - | - | 1.2 | µs |
| $t_{f(o)}$ | output fall time | $C_L \leq$ 30 pF; 10 % to 90 %; 0 V to $V_{DD(INTF)}$ | - | - | 0.1 | µs |
| $I_{pu}$ | pull-up current | $V_{OH}$ = 0.9$V_{DD}$; C = 30 pF | –1 | - | - | mA |
| **Internal oscillator** | | | | | | |
| $f_{osc(int)}$ | internal oscillator frequency | Shutdown mode | 100 | 150 | 200 | kHz |
| | | active state | 2 | 2.7 | 3.2 | MHz |
| **Reset output to the card: pin RST** | | | | | | |
| $V_o$ | output voltage | Shutdown mode | | | | |
| | | no load | 0 | - | 0.1 | V |
| | | $I_o$ = 1 mA | 0 | - | 0.3 | V |
| $I_o$ | output current | Shutdown mode; pin RST grounded | - | - | –1 | mA |
| $t_d$ | delay time | between pins RSTIN and RST; RST enabled | - | - | 2 | µs |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 200 µA; $V_{CC}$ = 5 V | 0 | - | 0.3 | V |
| | | $I_{OL}$ = 200 µA; $V_{CC}$ = 3 V or 1.8 V | 0 | - | 0.2 | V |
| | | current limit $I_{OL}$ = 20 mA | $V_{CC}$ – 0.4 | - | $V_{CC}$ | V |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH}$ = –200 µA | 0.9$V_{CC}$ | - | $V_{CC}$ | V |
| | | current limit $I_{OH}$ = –20 mA | 0 | - | 0.4 | V |

**Table 7. Characteristics of IC supply voltage** *...continued*

*$V_{DDP}$ = 5 V; $V_{DD}$ = 3.3 V; $V_{DD(INTF)}$ = 3.3 V; $f_{xtal}$ = 10 MHz; GND = 0 V; $T_{amb}$ = 25 °C; for C1 and C2 versions; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_r$ | rise time | $C_L$ = 100 pF | - | - | 0.1 | µs |
| $t_f$ | fall time | $C_L$ = 100 pF | - | - | 0.1 | µs |
| **Clock output to the card: pin CLK** | | | | | | |
| $V_o$ | output voltage | Shutdown mode | | | | |
| | | no load | 0 | - | 0.1 | V |
| | | $I_o$ = 1 mA | 0 | - | 0.3 | V |
| $I_o$ | output current | Shutdown mode; pin CLK grounded | - | - | −1 | mA |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 200 µA - C1 version | 0 | - | 0.3 | V |
| | | $I_{OL}$ = 200 µA - C2 version | 0 | - | 0.15 $V_{CC}$ | V |
| | | current limit $I_{OL}$ = 70 mA | $V_{CC}$ − 0.4 | - | $V_{CC}$ | V |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH}$ = −200 µA | 0.9$V_{CC}$ | - | $V_{CC}$ | V |
| | | current limit $I_{OH}$ = −70 mA | 0 | - | 0.4 | V |
| $t_r$ | rise time | $C_L$ = 30 pF [5] | - | - | 16 | ns |
| $t_f$ | fall time | $C_L$ = 30 pF [5] | - | - | 16 | ns |
| $f_{CLK}$ | frequency on pin CLK | operational | 0 | - | 20 | MHz |
| δ | duty cycle | $C_L$ = 30 pF [5] | 45 | - | 55 | % |
| SR | slew rate | rise and fall; $C_L$ = 30 pF | | | | |
| | | $V_{CC}$ = 5 V | 0.2 | - | - | V/ns |
| | | $V_{CC}$ = 3 V or 1.8 V | 0.12 | - | - | V/ns |
| **Control inputs: pins CLKDIV1, CLKDIV2, RSTIN, VCC_SEL1 and VCC_SEL2[6]** | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | −0.3 | - | 0.3$V_{DD(INTF)}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | 0.7 $V_{DD(INTF)}$ | - | $V_{DD(INTF)}$ + 0.3 | V |
| $V_{hys}$ | hysteresis voltage | control input | - | 0.14$V_{DD(INTF)}$ | - | V |
| $I_{IL}$ | LOW-level input current | $V_{IL}$ = 0 V | - | - | 1 | µA |
| $I_{IH}$ | HIGH-level input current | $V_{IH}$ = $V_{DD(INTF)}$ | - | - | 1 | µA |
| **Control input: pin CMDVCCN[6]** | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | −0.3 | - | 0.3$V_{DD(INTF)}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | 0.7$V_{DD(INTF)}$ | - | $V_{DD(INTF)}$ + 0.3 | V |
| $V_{hys}$ | hysteresis voltage | control input | - | 0.14$V_{DD(INTF)}$ | - | V |
| $I_{IL}$ | LOW-level input current | $V_{IL}$ = 0 V | - | - | 1 | µA |
| $I_{IH}$ | HIGH-level input current | $V_{IH}$ = $V_{DD(INTF)}$ | - | - | 1 | µA |
| $f_{CMDVCCN}$ | frequency on pin CMDVCCN | | - | - | 100 | Hz |

**Table 7. Characteristics of IC supply voltage** *...continued*

*$V_{DDP}$ = 5 V; $V_{DD}$ = 3.3 V; $V_{DD(INTF)}$ = 3.3 V; $f_{xtal}$ = 10 MHz; GND = 0 V; $T_{amb}$ = 25 °C; for C1 and C2 versions; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_w$ | pulse width | 5 V card | 30 | - | - | ms |
| | | 3 V card | - | - | 15 | ms |
| **Card detection input: pin PRESN[6][7]** | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | −0.3 | - | $0.3V_{DD(INTF)}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | $0.7V_{DD(INTF)}$ | - | $V_{DD(INTF)}$ + 0.3 | V |
| $V_{hys}$ | hysteresis voltage | pin PRESN | - | $0.14V_{DD(INTF)}$ | - | V |
| $I_{IL}$ | LOW-level input current | 0 V < $V_{IL}$ < $V_{DD(INTF)}$ | - | - | 5 | µA |
| $I_{IH}$ | HIGH-level input current | 0 V < $V_{IH}$ < $V_{DD(INTF)}$ | - | - | 5 | µA |
| **OFFN output[8]** | | | | | | |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 2 mA | 0 | - | 0.3 | V |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH}$ = −15 µA | $0.75V_{DD(INTF)}$ | - | - | V |
| $R_{pu}$ | pull-up resistance | connected to $V_{DD(INTF)}$ | 16 | 20 | 24 | kΩ |

[1] To meet these specifications, $V_{CC}$ should be decoupled to pin GND using two ceramic multilayer capacitors of low ESR with values of one 220 nF and one 470 nF.

[2] Using decoupling capacitors of one 220 nF ±20 % and one 470 nF ±20 %.

[3] Using the integrated 9 kΩ pull-up resistor connected to $V_{CC}$.

[4] Using the integrated 10 kΩ pull-up resistor connected to $V_{DD(INTF)}$.

[5] The transition time and the duty factor definitions are shown in Figure 11 on page 21; δ = t1 / (t1 + t2).

[6] Pins PRESN and CMDVCCN are active LOW; pin RSTIN is active HIGH; see Table 4 for states of pins CLKDIV1 and CLKDIV2.

[7] Pin PRESN has an integrated current source of 1.25 µA to $V_{DD(INTF)}$.

[8] Pin OFFN is an NMOS drain, using an internal 20 kΩ pull-up resistor connected to $V_{DD(INTF)}$.

**Table 8. Protection characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{Olim}$ | output current limit | pin I/O | −15 | - | +15 | mA |
| | | pin $V_{CC}$ | 135 | 175 | 225 | mA |
| | | pin CLK | −70 | - | +70 | mA |
| | | pin RST | −20 | - | +20 | mA |
| $I_{sd}$ | shutdown current | pin $V_{CC}$ | 90 | 120 | 150 | mA |
| $T_{sd}$ | shutdown temperature | at die | - | 150 | - | °C |

**Table 9. Timing characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{act}$ | activation time | see Figure 7 on page 11 | 2090 | - | 4160 | µs |
| $t_{deact}$ | deactivation time | see Figure 8 on page 12 | 35 | 90 | 250 | µs |

**Table 9. Timing characteristics** *…continued*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_d$ | delay time | CLK sent to card using an external clock | | | | |
| | | $t_{d(start)}$ = t3; see Figure 7 on page 11 | 2090 | - | 4112 | µs |
| | | $t_{d(end)}$ = t5; see Figure 7 on page 11 | 2120 | - | 4160 | µs |
| $t_{deb}$ | debounce time | pin PRESN | 3.2 | 4.5 | 6.4 | ms |

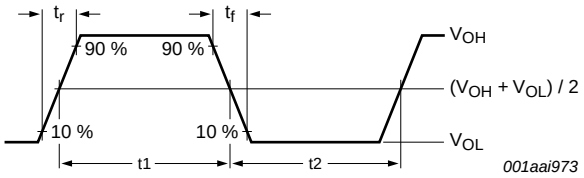



**Fig 11. Definition of output and input transition times**

## 12. Application information

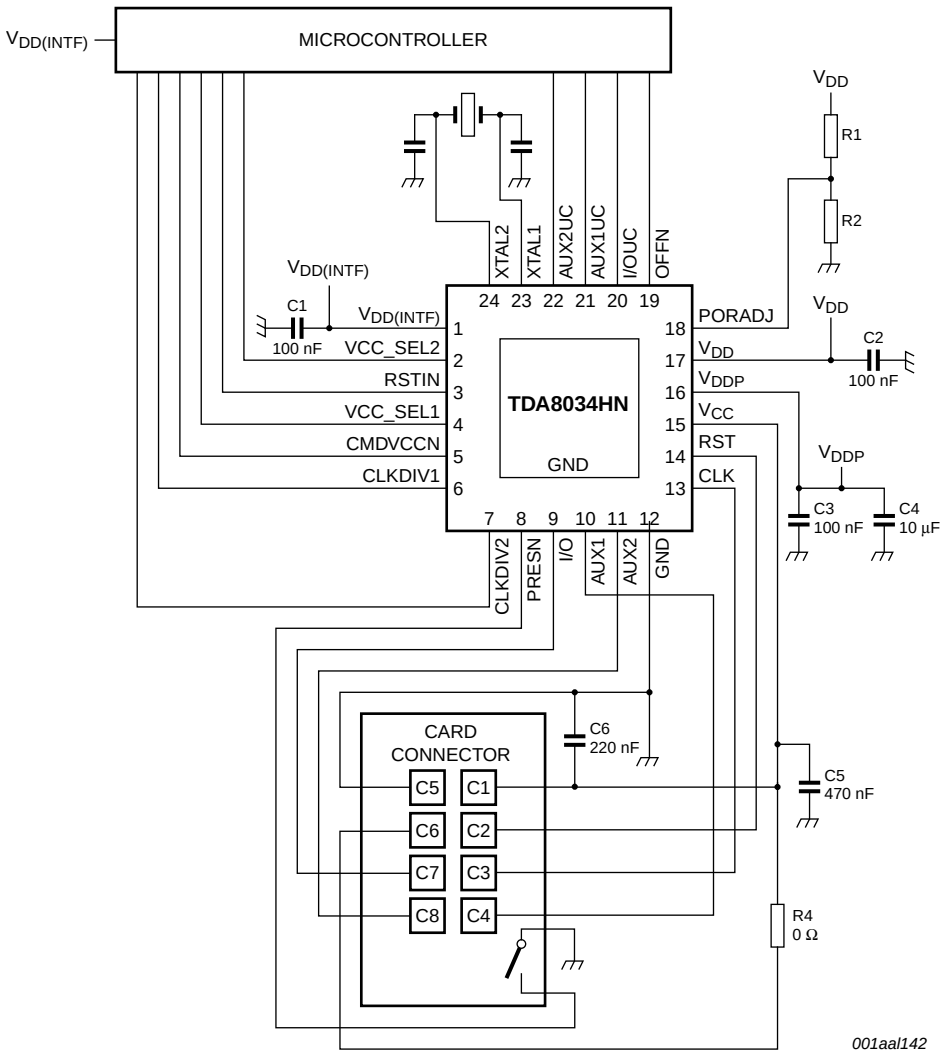
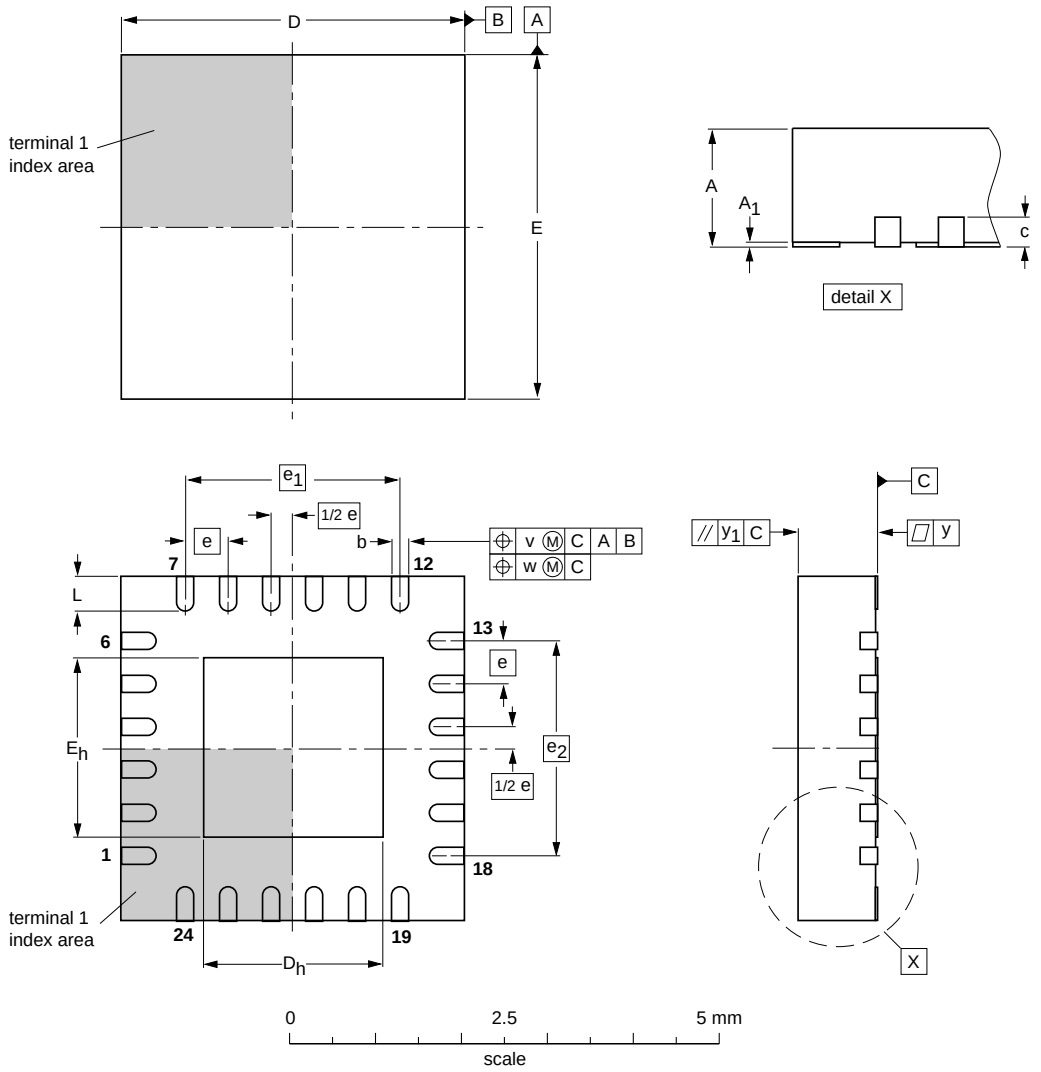



**Fig 12. Application diagram**

## 13. Package outline

**HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm** **SOT616-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | $A^{(1)}$ max. | $A_1$ | b | c | $D^{(1)}$ | $D_h$ | $E^{(1)}$ | $E_h$ | e | $e_1$ | $e_2$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1 | 0.05<br>0.00 | 0.30<br>0.18 | 0.2 | 4.1<br>3.9 | 2.25<br>1.95 | 4.1<br>3.9 | 2.25<br>1.95 | 0.5 | 2.5 | 2.5 | 0.5<br>0.3 | 0.1 | 0.05 | 0.05 | 0.1 |

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT616-1 | - - - | MO-220 | - - - | | | ~~01-08-08~~<br>02-10-22 |

**Fig 13. Package outline SOT616-1 (HVQFN24)**

# 14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

## 14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

## 14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

## 14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 14) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 10 and 11

**Table 10. SnPb eutectic process (from J-STD-020D)**

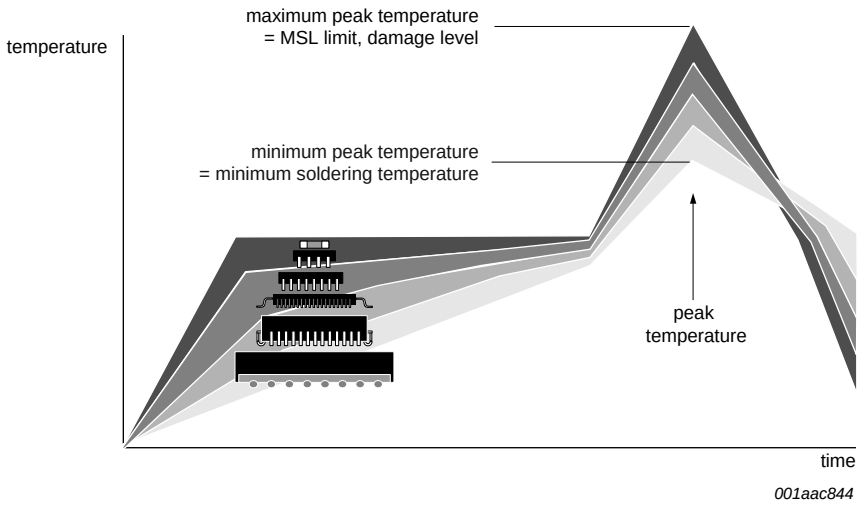
| Package thickness (mm) | Package reflow temperature (°C) | |
|---|---|---|
| | Volume ($mm^3$) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

**Table 11. Lead-free process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) | | |
|---|---|---|---|
| | Volume ($mm^3$) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 14.




MSL: Moisture Sensitivity Level

**Fig 14. Temperature profiles for large and small components**

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

## 15. Abbreviations

**Table 12. Abbreviations**

| Acronym | Description |
|---|---|
| EMV | Europay MasterCard VISA |
| ESD | ElectroStatic Discharge |
| ESR | Equivalent Series Resistor |
| FCDM | Field Charged Device Model |
| HBM | Human Body Model |
| LDO | Low Drop-Out |
| MM | Machine Model |
| NMOS | Negative-channel Metal-Oxide Semiconductor |
| POR | Power-On Reset |

# 16. Revision history

**Table 13. Revision history**

| Document ID | Release date | Data sheet status | Change notice- | Supersedes |
|---|---|---|---|---|
| TDA8034HN v.3.5 | 20200313 | Product data sheet | - | TDA8034HN v.3.4 |
| Modifications: | • Section 8.1 “Power supplies”: Last paragraph added | | | |
| TDA8034HN v.3.4 | 20160629 | Product data sheet | - | TDA8034HN v3.3 |
| Modifications: | • Section 5 “Ordering information”: C2 version added (EMVCo 4.3 compliant)<br>• Table 7 “Characteristics of IC supply voltage”: values for C2 version added | | | |
| TDA8034HN v.3.3 | 20150520 | Product data sheet | - | TDA8034HN v3.2 |
| Modifications: | • Section 2 “Features and benefits”: ESD value updated<br>• Table 5 “Limiting values”: $V_{ESD}$ values updated | | | |
| TDA8034HN v.3.2 | 20140325 | Product data sheet | - | TDA8034HN v.3.1 |
| Modifications: | • Change of descriptive title<br>• Section 2 “Features and benefits”: typos corrected | | | |
| TDA8034HN v.3.1 | 20110905 | Product data sheet | - | TDA8034HN v.3.0 |
| Modifications: | • Table 1 “Quick reference data”: values added<br>• Table 7 “Characteristics of IC supply voltage”: values added<br>• Figure 1 “Block diagram”: Figure note (1) changed | | | |
| TDA8034HN v.3.0 | 20110117 | Product data sheet | - | TDA8034HN v.2.0 |
| Modifications: | • Table 2 “Ordering information”: type number updated into TDA8034HN/C1<br>• Table 3 “Pin description”: Table note [2] corrected | | | |
| TDA8034HN v.2.0 | 20101112 | Product data sheet | - | TDA8034HN_1 |
| Modifications: | • Table 3 “Pin description”:<br>Table note [4] $V_{DD}$ changed into $V_{DD(INTF)}$<br>Table note [5] added<br>IOUC, AUX1UC, AUX2UC referenced to new note [5] | | | |
| TDA8034HN_1 | 20100205 | Product data sheet | - | - |

# 17. Legal information

## 17.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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# 19. Tables

## 20. Figures

## 21. Contents





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