

NXP I²C-bus and SMBus controller PCA9564

Easy interfacing between serial I²C-bus and 8-bit parallel communication bus

This simple-to-use bus controller makes it easy to create a bidirectional interface between the serial I²C-bus and the 8-bit parallel bus system used by most standard microcontrollers and microprocessors.

Key features

- ▶ Compatible with I²C-bus and SMBus
- ▶ Compatible with Intel 8051 and NXP 80C51 architectures
- ▶ Four internal registers for device configuration
- ▶ Status register
- ▶ Tx and Rx modes for master and slave
- ▶ Bus error detection and recovery function
- ▶ Fully internal timeout function
- ▶ Interrupt control to initiate interrupt routine
- ▶ Built-in Power On Reset
- ▶ Glitch-free operation at power-up and power-down, for hot insertion
- ▶ ESD protection exceeds 2000V HBM per JESD22-A114, 200V MM per JESD22-A115, and 1000V CDM per JESD22-C101
- ▶ JEDEC Standard JESD78 latch-up testing exceeds 100 mA
- ▶ Operating temperature range = -40 to +85 °C
- ▶ High-volume CMOS process
- ▶ 20-pin SO (D), TSSOP (PW), and HVQFN (BS)

Applications

- ▶ Microcontroller and microprocessor-based systems

Manufactured in a high-volume CMOS process, the NXP PCA9564 provides the interface between the serial I²C-bus or SMBus and most standard parallel-bus microcontrollers or microprocessors. It enables bidirectional communication between the 8-bit parallel-bus system and the I²C-bus.

The PCA9564 can operate as a master or a slave and can act as a transmitter or a receiver. Communication with the I²C-bus is conducted on a byte basis using interrupts or polled handshakes. Without using any external timing elements, the PCA9564 controls all the sequences, protocols, arbitration, bus errors, and timing issues that are specific to the I²C-bus.

Four registers configure device operation: timeout information, address information, data, and mode of operation. A status register is also included.

The PCA9564 is similar to the popular NXP PCF8584, which supports Intel 8049/8051, Motorola 6800/68000 and Xicor Z80 devices. The PCA9564 operates at lower voltages and higher I²C-bus frequencies than the PCF8584.

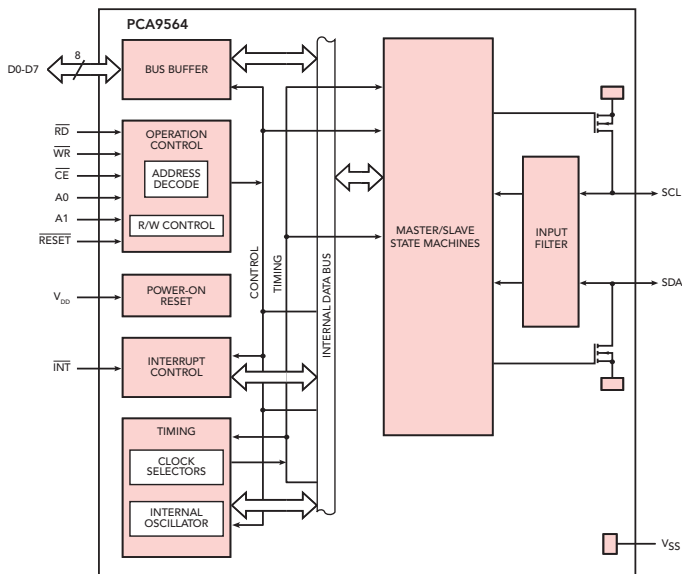


The voltage range of the PCA9564 is 2.3 to 3.6 V (the range for the PCF8584 is from 4.5 to 5.5 V), and the PCA9564 has I/O that are tolerant to 5.5 V. The maximum I²C-bus frequency for the PCA9564 is 360 kHz (400 kHz in slave mode), while the PCF8584 has a maximum of 90 kHz.

The PCA9564 is compatible with faster processors because it has a faster parallel interface. It also provides a more cost-effective and flexible solution because it uses an internal clock that can regulate an oscillator to within ±10%.

The PCA9564 is compatible with the Intel 8051 architecture and is designed to be very similar to the I²C-bus hardware used in the NXP 80C51 microcontrollers, so existing code can be used with only a few modifications. Support for bus monitor "snoop" mode is not included.

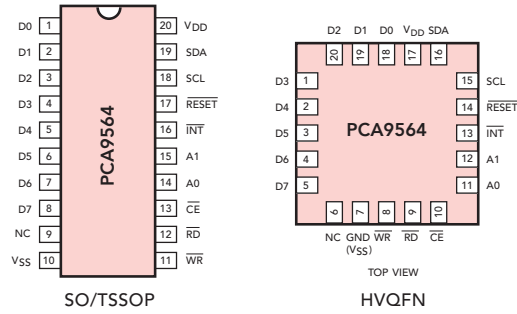
The PCA9665 is an improved version of the PCA9564 that offers frequencies up to 1 MHz with more master frequency selections, 68 byte buffer to reduce loading on the microcontroller and ability to directly drive > 1500 pF buses.



PCA9564 block diagram

Ordering information

| Package | Container | PCA9564 |
|---------|-------------|-------------|
| SO | Tube | PCA9564D |
| | Tape & Reel | PCA9564D-T |
| TSSOP | Tube | PCA9564PW |
| | Tape & Reel | PCA9564PW-T |
| HVQFN | Tape & Reel | PCA9564BS-T |



Pin configuration

| Symbol | Pin type | Name and function |
|-----------------|----------|--|
| D0-D7 | I/O | Data Bus: Bidirectional, 3-state data bus used to transfer commands, data, and status between the controller and the CPU. D0 is the least-significant bit. |
| NC | | No connect: Must be left floating. |
| V _{SS} | Pwr | Ground. |
| WR | I | Write Strobe: When this and CE are low, the contents of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of the signal. |
| RD | I | Read Strobe: When this and CE are low, the contents of the addressed register are presented to the data bus. The read cycle begins on the falling edge of RD. |
| CE | I | Chip Enable: Active-low input signal. When low, data transfer between the CPU and the controller are enabled on D0-D7, as controlled by the WR, RD, and A0-A1 inputs. When high, the D0-D7 lines are placed in the 3-state condition. |
| A0,A1 | I | Address Inputs: Selects the internal registers and ports for read/write operations. |
| INT | O | Interrupt Request: Active low, open-drain output. Requires a pull-up device. |
| RESET | I | Reset: When low, clears internal registers and resets the I ² C-bus state machine. |
| SCL | I/O | I ² C-bus serial clock input/output (open-drain) |
| SDA | I/O | I ² C-bus serial drain input/output (open-drain) |
| V _{DD} | Pwr | Power Supply: +2.3 to +3.6 V |



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