# 74HC112; 74HCT112

## Dual JK flip-flop with set and reset; negative-edge trigger

Rev. 4 — 11 January 2021 Product data sheet

## 1. General description

The 74HC112; 74HCT112 is a dual negative-edge triggered JK flip-flop. It features individual J and K inputs, clock ($n\overline{CP}$) set ($n\overline{SD}$) and reset ($n\overline{RD}$) inputs. It also has complementary nQ and $n\overline{Q}$ outputs. The set and reset are asynchronous active LOW inputs and operate independently of the clock input. The J and K inputs control the state changes of the flip-flops as described in the mode select function table. The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of $V_{CC}$.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

## 2. Features and benefits

- Input levels:
  - For 74HC112: CMOS level
  - For 74HCT112: TTL level
- Asynchronous set and reset
- Specified in compliance with JEDEC standard no. 7A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74HC112D | -40 °C to +125 °C | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| 74HCT112D | | | | |
| 74HC112PW | -40 °C to +125 °C | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |
| 74HCT112PW | | | | |

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## 4. Functional diagram

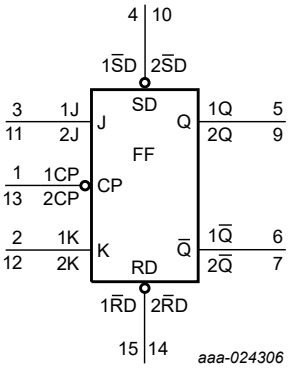


Fig. 1. Logic symbol

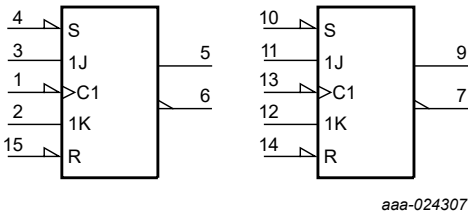


Fig. 2. IEC logic symbol

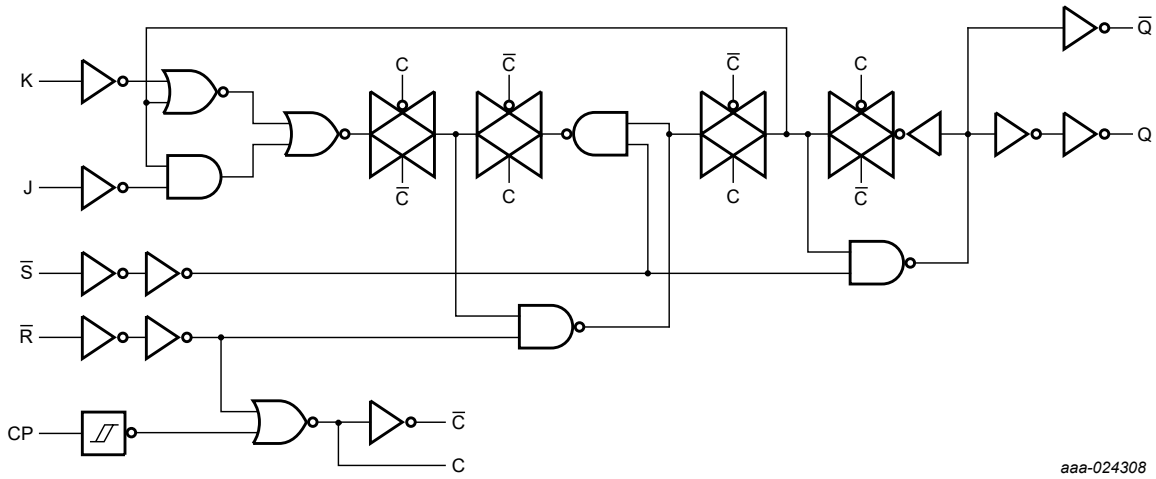


Fig. 3. Logic diagram (one flip-flop)

## 5. Pinning information

### 5.1. Pinning

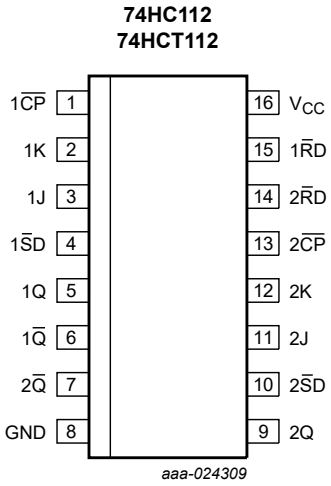


Fig. 4. Pin configuration SOT109-1 (SO16)

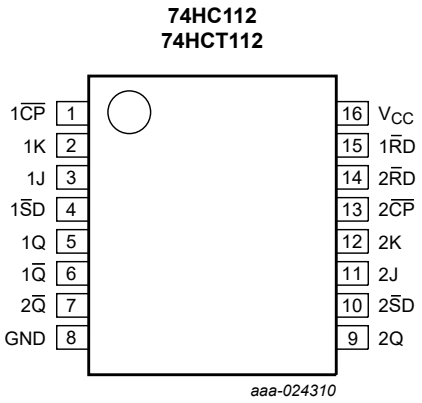


Fig. 5. Pin configuration SOT403-1 (TSSOP16)


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### 5.2. Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| 1$\overline{CP}$, 2$\overline{CP}$ | 1, 13 | clock input (HIGH-to-LOW; edge-triggered) |
| 1K, 2K | 2, 12 | data input |
| 1J, 2J | 3, 11 | data input |
| 1$\overline{SD}$, 2$\overline{SD}$ | 4, 10 | set input (active LOW) |
| 1Q, 2Q | 5, 9 | true flip-flop output |
| 1$\overline{Q}$, 2$\overline{Q}$ | 6, 7 | complement flip-flop output |
| GND | 8 | ground (0 V) |
| 1$\overline{RD}$, 2$\overline{RD}$ | 15, 14 | reset input (active LOW) |
| $V_{CC}$ | 16 | supply voltage |

## 6. Functional description

**Table 3. Function selection**

*If n$\overline{SD}$ and n$\overline{RD}$ simultaneously go from LOW-to-HIGH, the output states are unpredictable.*
*H = HIGH voltage level; h = HIGH voltage level one set-up time before the HIGH-to-LOW clock transition;*
*L = LOW voltage level; l = LOW voltage level one set-up time before the HIGH-to-LOW clock transition;*
*q = lowercase letters indicate the state of the referenced output one set-up time before the HIGH-to-LOW clock transition;*
*X = don't care; ↓ = HIGH-to-LOW clock transition.*

| Operating modes | Input | | | | | Output | |
|---|---|---|---|---|---|---|---|
| | n$\overline{SD}$ | n$\overline{RD}$ | n$\overline{CP}$ | nJ | nK | nQ | n$\overline{Q}$ |
| Asynchronous set | L | H | X | X | X | H | L |
| Asynchronous reset | H | L | X | X | X | L | H |
| Undetermined | L | L | X | X | X | H | L |
| Toggle | H | H | ↓ | h | h | $\overline{q}$ | q |
| Load 0 (reset) | H | H | ↓ | l | h | L | H |
| Load 1 (set) | H | H | ↓ | h | l | H | L |
| Hold no change | H | H | ↓ | l | l | q | $\overline{q}$ |


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# 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | -0.5 | +7 | V |
| $I_{IK}$ | input clamping current | $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V | - | ±20 | mA |
| $I_{OK}$ | output clamping current | $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V | - | ±20 | mA |
| $I_O$ | output current | $-0.5$ V $< V_O < V_{CC} + 0.5$ V | - | ±25 | mA |
| $I_{CC}$ | supply current | | - | +50 | mA |
| $I_{GND}$ | ground current | | -50 | - | mA |
| $T_{stg}$ | storage temperature | | -65 | +150 | °C |
| $P_{tot}$ | total power dissipation | [1] | - | 500 | mW |

[1] For SOT109-1 (SO16) package: $P_{tot}$ derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: $P_{tot}$ derates linearly with 8.5 mW/K above 91 °C.

# 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

*Voltages are referenced to GND (ground = 0 V)*

| Symbol | Parameter | Conditions | 74HC112 | | | 74HCT112 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{CC}$ | supply voltage | | 2.0 | 5.0 | 6.0 | 4.5 | 5.0 | 5.5 | V |
| $V_I$ | input voltage | | 0 | - | $V_{CC}$ | 0 | - | $V_{CC}$ | V |
| $V_O$ | output voltage | | 0 | - | $V_{CC}$ | 0 | - | $V_{CC}$ | V |
| $T_{amb}$ | ambient temperature | | -40 | +25 | +125 | -40 | +25 | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | $V_{CC}$ = 2.0 V | - | - | 625 | - | - | - | ns/V |
| | | $V_{CC}$ = 4.5 V | - | 1.67 | 139 | - | 1.67 | 139 | ns/V |
| | | $V_{CC}$ = 6.0 V | - | - | 83 | - | - | - | ns/V |

# 9. Static characteristics

**Table 6. Static characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| **74HC112** | | | | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 2.0 V | 1.5 | 1.2 | - | 1.5 | - | 1.5 | - | V |
| | | $V_{CC}$ = 4.5 V | 3.15 | 2.4 | - | 3.15 | - | 3.15 | - | V |
| | | $V_{CC}$ = 6.0 V | 4.2 | 3.2 | - | 4.2 | - | 4.2 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 2.0 V | - | 0.8 | 0.5 | - | 0.5 | - | 0.5 | V |
| | | $V_{CC}$ = 4.5 V | - | 2.1 | 1.35 | - | 1.35 | - | 1.35 | V |
| | | $V_{CC}$ = 6.0 V | - | 2.8 | 1.8 | - | 1.8 | - | 1.8 | V |


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| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| $V_{OH}$ | HIGH-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | $I_O$ = -20 µA; $V_{CC}$ = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | $I_O$ = -20 µA; $V_{CC}$ = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O$ = -20 µA; $V_{CC}$ = 6.0 V | 5.9 | 6.0 | - | 5.9 | - | 5.9 | - | V |
| | | $I_O$ = -4.0 mA; $V_{CC}$ = 4.5 V | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| | | $I_O$ = -5.2 mA; $V_{CC}$ = 6.0 V | 5.48 | 5.81 | - | 5.34 | - | 5.2 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | $I_O$ = 20 µA; $V_{CC}$ = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 20 µA; $V_{CC}$ = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 20 µA; $V_{CC}$ = 6.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 4.0 mA; $V_{CC}$ = 4.5 V | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| | | $I_O$ = 5.2 mA; $V_{CC}$ = 6.0 V | - | 0.16 | 0.26 | - | 0.33 | - | 0.4 | V |
| $I_I$ | input leakage current | $V_I = V_{CC}$ or GND; $V_{CC}$ = 6.0 V | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| $I_{CC}$ | supply current | $V_I = V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 6.0 V | - | - | 4.0 | - | 40 | - | 80 | µA |
| $C_I$ | input capacitance | | - | 3.5 | - | - | - | - | - | pF |
| **74HCT112** | | | | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | 2.0 | 1.6 | - | 2.0 | - | 2.0 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | - | 1.2 | 0.8 | - | 0.8 | - | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I = V_{IH}$ or $V_{IL}$; $V_{CC}$ = 4.5 V | | | | | | | | |
| | | $I_O$ = -20 µA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O$ = -4.0 mA | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{IH}$ or $V_{IL}$; $V_{CC}$ = 4.5 V | | | | | | | | |
| | | $I_O$ = 20 µA; $V_{CC}$ = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 4.0 mA; $V_{CC}$ = 5.5 V | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| $I_I$ | input leakage current | $V_I = V_{CC}$ or GND; $V_{CC}$ = 5.5 V | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| $I_{CC}$ | supply current | $V_I = V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 5.5 V | - | - | 4.0 | - | 40 | - | 80 | µA |
| $\Delta I_{CC}$ | additional supply current | per input pin; $V_I = V_{CC}$ - 2.1 V; other inputs at $V_{CC}$ or GND; $V_{CC}$ = 4.5 V to 5.5 V | | | | | | | | |
| | | $n\overline{SD}$ inputs | - | 50 | 180 | - | 225 | - | 245 | µA |
| | | nK inputs | - | 60 | 216 | - | 270 | - | 294 | µA |
| | | $n\overline{RD}$ inputs | - | 65 | 236 | - | 293 | - | 319 | µA |
| | | nJ, and $n\overline{CP}$ inputs | - | 100 | 360 | - | 450 | - | 490 | µA |
| $C_I$ | input capacitance | | - | 3.5 | - | - | - | - | - | pF |


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## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

*Voltages are referenced to GND (ground = 0 V); $C_L$ = 50 pF unless otherwise specified; for test circuit, see Fig. 8.*

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | Min | Max | |
| **74HC112** | | | | | | | | | | |
| $t_{pd}$ | propagation delay | $n\overline{CP}$ to nQ; see Fig. 6 [2] | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | - | 55 | 175 | - | 220 | - | 265 | ns |
| | | $V_{CC}$ = 4.5 V | - | 20 | 35 | - | 44 | - | 53 | ns |
| | | $V_{CC}$ = 5 V; $C_L$ = 15 pF | - | 17 | - | - | - | - | - | ns |
| | | $V_{CC}$ = 6.0 V | - | 16 | 30 | - | 37 | - | 45 | ns |
| | | $n\overline{CP}$ to $n\overline{Q}$; see Fig. 6 | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | - | 55 | 175 | - | 220 | - | 265 | ns |
| | | $V_{CC}$ = 4.5 V | - | 20 | 35 | - | 44 | - | 53 | ns |
| | | $V_{CC}$ = 5 V; $C_L$ = 15 pF | - | 17 | - | - | - | - | - | ns |
| | | $V_{CC}$ = 6.0 V | - | 16 | 30 | - | 37 | - | 45 | ns |
| | | $n\overline{RD}$ to nQ, $n\overline{Q}$; see Fig. 7 | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | - | 58 | 180 | - | 225 | - | 270 | ns |
| | | $V_{CC}$ = 4.5 V | - | 21 | 36 | - | 45 | - | 54 | ns |
| | | $V_{CC}$ = 5 V; $C_L$ = 15 pF | - | 18 | - | - | - | - | - | ns |
| | | $V_{CC}$ = 6.0 V | - | 17 | 31 | - | 38 | - | 46 | ns |
| | | $n\overline{SD}$ to nQ, $n\overline{Q}$; see Fig. 7 | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | - | 50 | 155 | - | 295 | - | 235 | ns |
| | | $V_{CC}$ = 4.5 V | - | 18 | 31 | - | 39 | - | 47 | ns |
| | | $V_{CC}$ = 5 V; $C_L$ = 15 pF | - | 15 | - | - | - | - | - | ns |
| | | $V_{CC}$ = 6.0 V | - | 14 | 26 | - | 33 | - | 40 | ns |
| $t_t$ | transition time | nQ, $n\overline{Q}$; see Fig. 6 [3] | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | - | 19 | 75 | - | 95 | - | 110 | ns |
| | | $V_{CC}$ = 4.5 V | - | 7 | 15 | - | 19 | - | 22 | ns |
| | | $V_{CC}$ = 6.0 V | - | 6 | 13 | - | 16 | - | 19 | ns |
| $t_W$ | pulse width | $n\overline{CP}$ HIGH or LOW; see Fig. 6 | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | 80 | 22 | - | 100 | - | 120 | - | ns |
| | | $V_{CC}$ = 4.5 V | 16 | 8 | - | 20 | - | 24 | - | ns |
| | | $V_{CC}$ = 6.0 V | 14 | 6 | - | 17 | - | 20 | - | ns |
| | | $n\overline{SD}$, $n\overline{RD}$ LOW; see Fig. 7 | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | 80 | 22 | - | 100 | - | 120 | - | ns |
| | | $V_{CC}$ = 4.5 V | 16 | 8 | - | 20 | - | 24 | - | ns |
| | | $V_{CC}$ = 6.0 V | 14 | 6 | - | 17 | - | 20 | - | ns |


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| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | Min | Max | |
| $t_{rec}$ | recovery time | $n\overline{RD}$ to $n\overline{CP}$; see Fig. 7 | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | 80 | 22 | - | 125 | - | 150 | - | ns |
| | | $V_{CC}$ = 4.5 V | 16 | 8 | - | 25 | - | 30 | - | ns |
| | | $V_{CC}$ = 6.0 V | 14 | 6 | - | 21 | - | 26 | - | ns |
| | | $n\overline{SD}$ to $n\overline{CP}$; see Fig. 7 | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | 80 | -19 | - | 100 | - | 120 | - | ns |
| | | $V_{CC}$ = 4.5 V | 16 | -7 | - | 20 | - | 24 | - | ns |
| | | $V_{CC}$ = 6.0 V | 14 | -6 | - | 17 | - | 20 | - | ns |
| $t_{su}$ | set-up time | nJ and nK to $n\overline{CP}$; see Fig. 6 | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | 80 | 19 | - | 100 | - | 120 | - | ns |
| | | $V_{CC}$ = 4.5 V | 16 | 7 | - | 20 | - | 24 | - | ns |
| | | $V_{CC}$ = 6.0 V | 14 | 6 | - | 17 | - | 20 | - | ns |
| $t_h$ | hold time | nJ and nK to $n\overline{CP}$; see Fig. 6 | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | 0 | -11 | - | 0 | - | 0 | - | ns |
| | | $V_{CC}$ = 4.5 V | 0 | -4 | - | 0 | - | 0 | - | ns |
| | | $V_{CC}$ = 6.0 V | 0 | -3 | - | 0 | - | 0 | - | ns |
| $f_{max}$ | maximum frequency | $n\overline{CP}$; see Fig. 6 | | | | | | | | |
| | | $V_{CC}$ = 2.0 V | 6 | 20 | - | 4.8 | - | 4.0 | - | MHz |
| | | $V_{CC}$ = 4.5 V | 30 | 60 | - | 24 | - | 20 | - | MHz |
| | | $V_{CC}$ = 5 V; $C_L$ = 15 pF | - | 66 | - | - | - | - | - | MHz |
| | | $V_{CC}$ = 6.0 V | 35 | 71 | - | 28 | - | 24 | - | MHz |
| $C_{PD}$ | power dissipation capacitance | $C_L$ = 50 pF; f = 1 MHz; $V_I$ = GND to $V_{CC}$ [4] | - | 27 | - | | | - | - | pF |
| **74HCT112** | | | | | | | | | | |
| $t_{pd}$ | propagation delay | $n\overline{CP}$ to nQ; see Fig. 6 [2] | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | - | 21 | 35 | - | 44 | - | 53 | ns |
| | | $V_{CC}$ = 5 V; $C_L$ = 15 pF | - | 19 | - | - | - | - | - | ns |
| | | $n\overline{CP}$ to $n\overline{Q}$; see Fig. 6 | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | - | 23 | 40 | - | 50 | - | 60 | ns |
| | | $V_{CC}$ = 5 V; $C_L$ = 15 pF | - | 19 | - | - | - | - | - | ns |
| | | $n\overline{RD}$ to nQ, $n\overline{Q}$; see Fig. 7 | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | - | 22 | 37 | - | 46 | - | 56 | ns |
| | | $V_{CC}$ = 5 V; $C_L$ = 15 pF | - | 19 | - | - | - | - | - | ns |
| | | $n\overline{SD}$ to nQ, $n\overline{Q}$; see Fig. 7 | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | - | 18 | 32 | - | 40 | - | 48 | ns |
| | | $V_{CC}$ = 5 V; $C_L$ = 15 pF | - | 15 | - | - | - | - | - | ns |
| $t_t$ | transition time | nQ, $n\overline{Q}$; see Fig. 6 [3] | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | - | 7 | 15 | - | 19 | - | 22 | ns |
| $t_W$ | pulse width | $n\overline{CP}$ HIGH or LOW; see Fig. 6 | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | 16 | 8 | - | 20 | - | 24 | - | ns |
| | | $n\overline{SD}$, $n\overline{RD}$ LOW; see Fig. 7 | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | 18 | 10 | - | 23 | - | 27 | - | ns |


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| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | Min | Max | |
| $t_{rec}$ | recovery time | $n\overline{RD}$ to $n\overline{CP}$; see Fig. 7 | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | 20 | 11 | - | 25 | - | 30 | - | ns |
| | | $n\overline{SD}$ to $n\overline{CP}$; see Fig. 7 | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | 20 | -8 | - | 25 | - | 30 | - | ns |
| $t_{su}$ | set-up time | nJ and nK to $n\overline{CP}$ ; see Fig. 6 | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | 16 | 7 | - | 20 | - | 24 | - | ns |
| $t_h$ | hold time | nJ and nK to $n\overline{CP}$; see Fig. 6 | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | 0 | -7 | - | 0 | - | 0 | - | ns |
| $f_{max}$ | maximum frequency | $n\overline{CP}$; see Fig. 6 | | | | | | | | |
| | | $V_{CC}$ = 4.5 V | 30 | 64 | - | 24 | - | 20 | - | MHz |
| | | $V_{CC}$ = 5 V; $C_L$ = 15 pF | - | 70 | - | - | - | - | - | MHz |
| $C_{PD}$ | power dissipation capacitance | $C_L$ = 50 pF; f = 1 MHz; $V_I$ = GND to $V_{CC}$ [4] | - | 30 | - | - | - | - | - | pF |

[1] All typical values are measured at $T_{amb}$ = 25 °C.
[2] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$.
[3] $t_t$ is the same as $t_{THL}$ and $t_{TLH}$.
[4] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
$f_i$ = input frequency in MHz;
$f_o$ = output frequency in MHz;
$C_L$ = output load capacitance in pF;
$V_{CC}$ = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.


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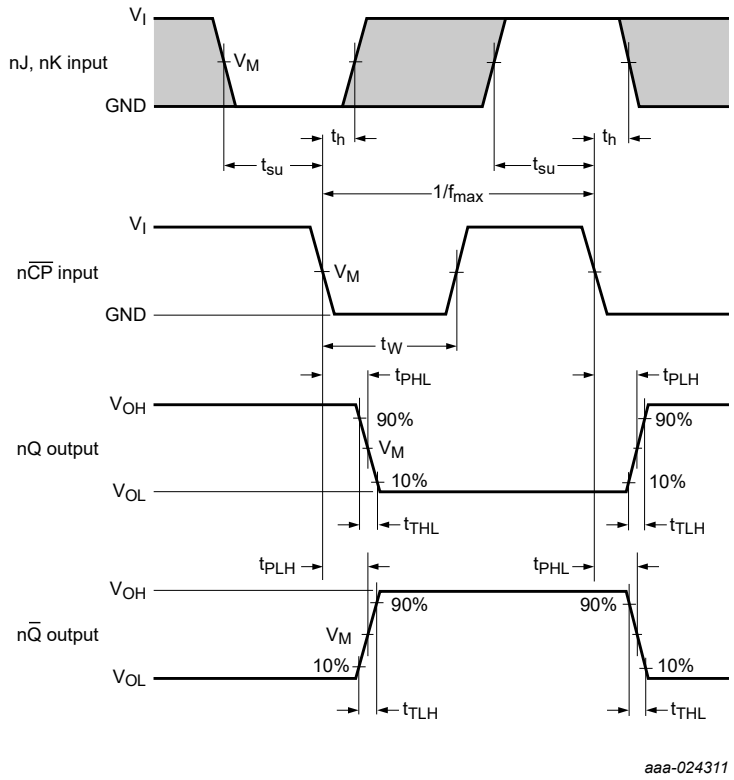
## 10.1. Waveforms and test circuit




Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

**Fig. 6. Clock propagation delays, output transition time, pulse width, set-up, hold times, and maximum frequency**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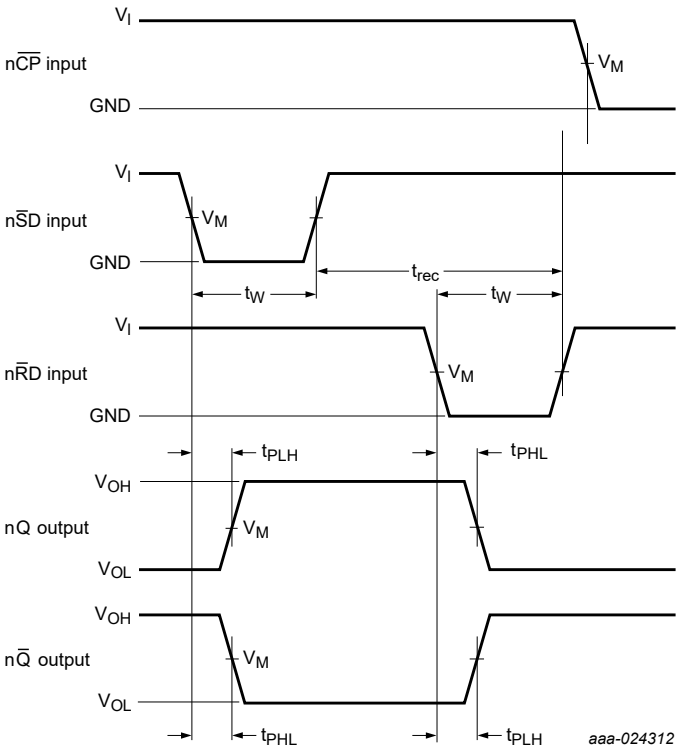


Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

**Fig. 7. Set and reset propagation delays, pulse widths and recovery time**

**Table 8. Measurement points**

| Type | Input | Output |
|---|---|---|
| | $V_M$ | $V_M$ |
| 74HC112 | $0.5V_{CC}$ | $0.5V_{CC}$ |
| 74HCT112 | 1.3 V | 1.3 V |


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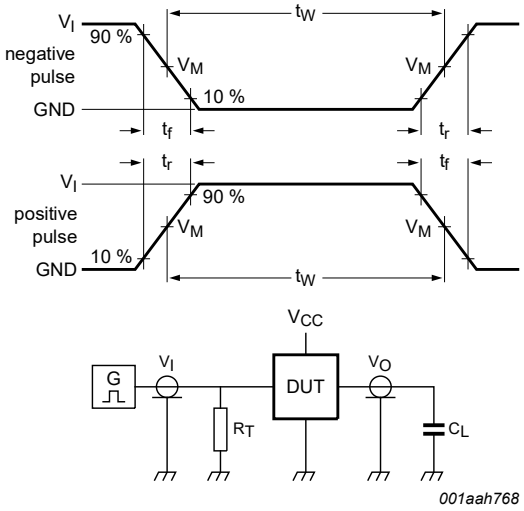


Test data is given in Table 9.

Definitions test circuit:

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$C_L$ = Load capacitance including jig and probe capacitance.

**Fig. 8. Test circuit for measuring switching times**

**Table 9. Test data**

| Type | Input | | Load | Test |
|---|---|---|---|---|
| | $V_I$ | $t_r$, $t_f$ | $C_L$ | |
| 74HC112 | $V_{CC}$ | 6 ns | 15 pF, 50 pF | $t_{PLH}$, $t_{PHL}$ |
| 74HCT112 | 3 V | 6 ns | 15 pF, 50 pF | $t_{PLH}$, $t_{PHL}$ |


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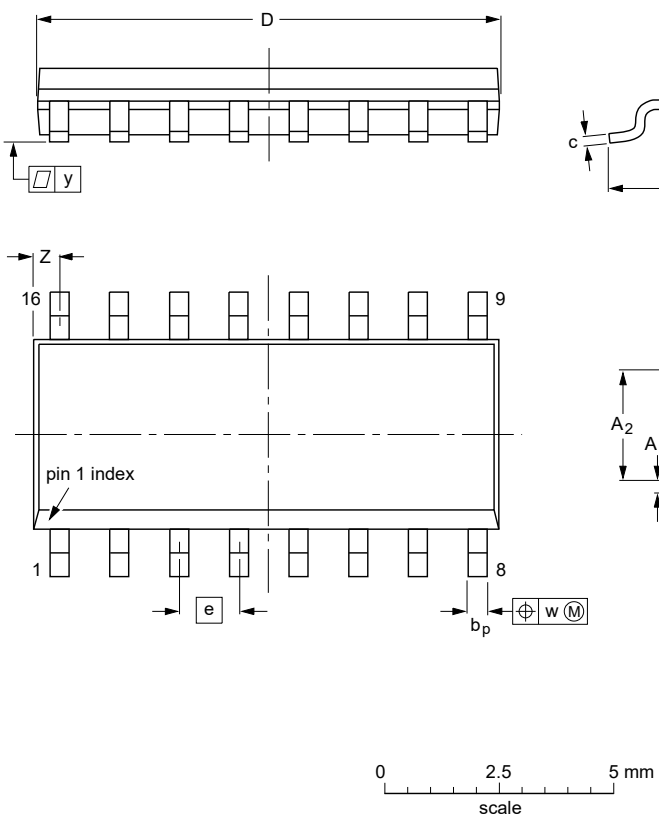
## 11. Package outline

**SO16: plastic small outline package; 16 leads; body width 3.9 mm** **SOT109-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 10.0<br>9.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | 8°<br>0° |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.39<br>0.38 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.020 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT109-1 | 076E07 | MS-012 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig. 9. Package outline SOT109-1 (SO16)**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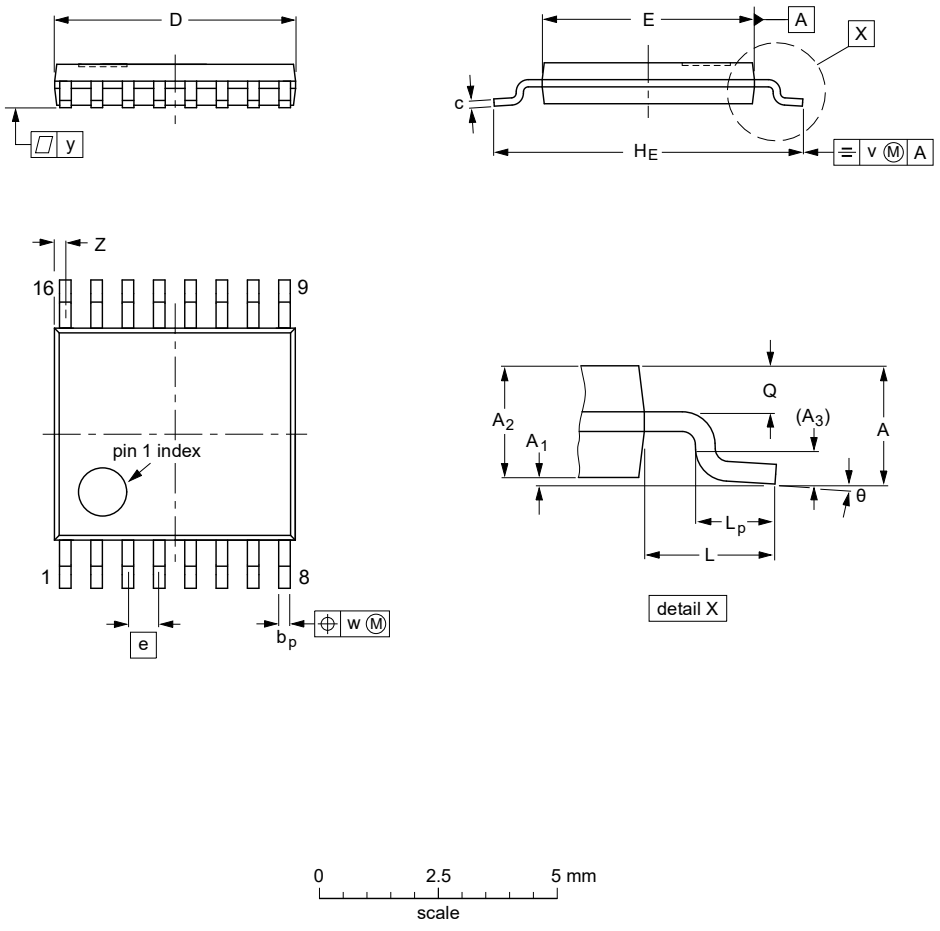
**TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm** **SOT403-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 5.1<br>4.9 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.40<br>0.06 | 8°<br>0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT403-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-18 |

**Fig. 10. Package outline SOT403-1 (TSSOP16)**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## 12. Abbreviations

**Table 10. Abbreviations**

| Acronym | Description |
|---|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

## 13. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74HC_HCT112 v.4 | 20210111 | Product data sheet | - | 74HC_HCT112 v.3 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• Type numbers 74HC112DB and 74HCT112DB (SOT338-1 / SSOP16) removed.<br>• Section 7: Derating values for $P_{tot}$ total power dissipation have been updated. | | | |
| 74HC_HCT112 v.3 | 20160809 | Product data sheet | - | 74HC_HCT112_CNV v.2 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• Type numbers 74HC112N and 74HCT112N removed. | | | |
| 74HC_HCT112_CNV v.2 | 19980610 | Product specification | - | - |


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# 14. Legal information

## Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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