DATASHEET

OL2381

Integrated UHF Transceiver

Rev 1.3

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NXP
founded by Philips

Integrated UHF Transceiver

CONTENTS

Integrated UHF Transceiver

Integrated UHF Transceiver

Integrated UHF Transceiver

Integrated UHF Transceiver

1 General Information

1.1 Features

- Highly integrated solution for the 315 / 434 / 868 / 915 MHz band

- Very few external components required.

- Complies with ETSI EN300-220 / FCC part 15 Standards.

- Near Zero-IF RX architecture

- On-chip channel filtering with automatic calibration supported to provide stable cut-off frequencies and filter roll-off.

- Multi channel TX and RX operation by fully integrated Frac-N $\Sigma\Delta$ PLL with on-chip loop filter.

- Automatic VCO sub band selection and calibration to reduce PLL loop bandwidth variation.

- Programmable ASK/FSK modulation with Manchester Codec.

- Programmable transmitter output power (-20 to +10dBm), stabilised with onboard PA regulator.

- Digital RSSI with a configurable threshold.

- Onboard Signal Signature Recognition Unit with Preamble Pattern Recognition.

- Configurable Rx polling timer with 2% absolute accuracy.

- Level Sensitive Data slicer with self-adjusting threshold

- Low power Consumption (Rx 16mA, Tx 13mA @6dBm), with ultra Low 0.5µA standby current and configurable polling timer.

- Single Lithium cell operation (2.1V). Operation up to 3.6V fully supported.

- 32-Pin HVQFN32 Pb-free package

1.2 General Description

A highly integrated single chip transceiver solution, the OL2381 is ideally suited to telemetry applications operating in the ISM/SRD bands. The small form factor, low power consumption and wide supply voltage range make this device suitable for use in battery powered, handheld devices and their counter parts.
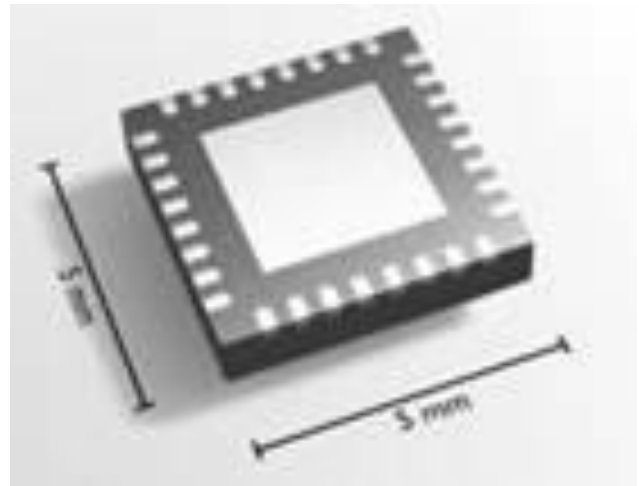
The device utilises a fully integrated, programmable Fractional-N PLL (including loop filter) to control the Local Oscillator, thus supporting multi channel operation and frequency hopping schemes. This feature also allows programmable frequency steps for XTAL drift compensation.

The device can employ ASK, FSK or GFSK like modulations. The ASK modulation characteristics are fully programmable by varying the power amplifier output power in accordance with the transmit data. The FSK modulation utilizes the Fractional-N PLL capability to precisely modulate the Local Oscillator frequency with the transmit data (in loop modulation). Relaxed narrow band applications can utilize an on-chip GFSK like modulation to improve the spectral occupancy.

The device is based on a low IF Direct Conversion receiver architecture, with on-chip IF filtering and programmable channel bandwidth. After filtering and amplification the quadrature signals are digitized, demodulated and processed in the digital domain.

Base-band processing of the receive signal comprises of a demodulator, a data-slicer and clock recovery followed by a Manchester decoder. Automated signal signature recognition units are available to allow simple, fast and reliable data reception.

The device is controlled via a three wire serial interface (SPI) with data input and output, data clock and interface enable. The interface can be configured to a full SPI interface with separate data and clock pins. Additional pins are available to access internal signals in real-time.

6

Integrated UHF Transceiver

1.3 Ordering Information

EXTENDED TYPE NUMBER	DESCRIPTION	PACKAGE		TEMPERATURE RANGE (°C)
		NAME	OUTLINE VERSION	
OL2381AHN/C0B	315MHz , 434MHz, 868MHz, 915MHz Transceiver	HVQFN32	SOT617-3	-25 to +85°C

2 Pin Information

2.1 Pin Configuration
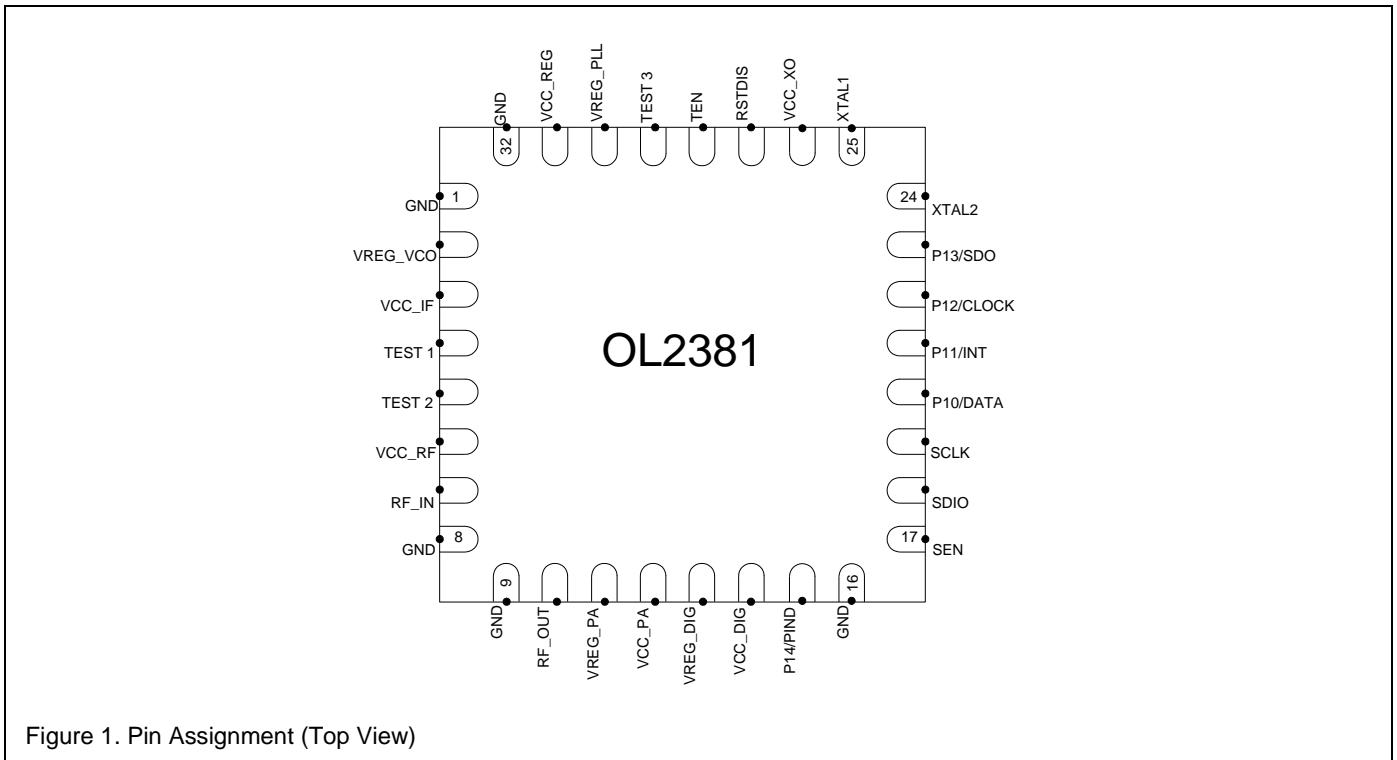
Figure 1. Pin Assignment (Top View)

7

Integrated UHF Transceiver

2.2 Pin Description

Pin	Symbol	Pad Type	Equivalent Circuit	Description	Reset state
1	GND	---		Ground (please refer exposed heatsink as ground reference)	---
2	VREG_VCO	A		VCO regulator output voltage (for decoupling capacitor)	Z
3	VCC_IF	A		IF part power supply	A
4	TEST1	A		RX test I output	Z
5	TEST2	A		RX test Q output	Z
6	VCC_RF	A		LNA power supply	A
7	RF_IN	A		Received RF signal input	A
8	GND	---		Ground (please refer exposed heatsink as ground reference)	---
9	GND	---		Ground (please refer exposed heatsink as ground reference)	---
10	RF_OUT	A		Transmitted RF signal output	Z
11	VREG_PA	A		PA regulator output voltage (for decoupling capacitor)	Z
12	VCC_PA	A		PA power supply	A
13	VREG_DIG	A		Digital regulator output voltage (for decoupling capacitor)	A
14	VCC_DIG	A		Digital part supply voltage	A
15	P14/PIND	DO		Digital output port with increased drive capability (for PIN diode control)	Z
16	GND	---		Ground (please refer exposed heatsink as ground reference)	---
17	SEN	DI		Serial interface enable	DI
18	SDIO	DIO		Serial interface input/output	DI
19	SCLK	DIO		Serial interface clock	DI
20	P10/DATA	DIeO		Digital output port, Transmitter data input, Received data output, Data output of debug interface	Z
21	P11/INT	DO		Digital output port, Interrupt output, Several status indicators, reference clock output, Frame indicator of debug interface	POR, interrupt output
22	P12/CLOCK	DO		Digital output port, TX/reference clock out, RX Data clock, Clock of debug interface	1 MHz reference clock
23	P13/SDO	DO		Digital output port, Status indicators, Serial interface data output	Z
24	XTAL2	A		XTAL pin, reference frequency input	A
25	XTAL1	A		XTAL pin	A
26	VCC_XO	A		Crystal oscillator supply voltage	A
27	RSTDIS	DI		Reset disable signal	DI
28	TEN	DI		Test enable input	DI
29	TEST3	A		PLL test output	Z
30	VREG_PLL	A		PLL regulator output voltage (for decoupling capacitor)	Z
31	VCC_REG	A		PLL, VCO regulators power supply	A

Integrated UHF Transceiver

Pin	Symbol	Pad Type	Equivalent Circuit	Description	Reset state
32	GND	---		Ground (please refer exposed heatsink as ground reference)	---
Exp.die pad	GND	A		Ground connection	Ground

Pad
Types: A   analogue
         DI   digital input
         DO   digital output (with enable signal)
         DIO   digital input (without enable signal) and output (with enable signal)
         DIeO   digital input and output (both with enable signal)

Table 1: Frequency Control register FCxL

Integrated UHF Transceiver

3 General Architecture Overview

3.1.1 Functional Block Diagram
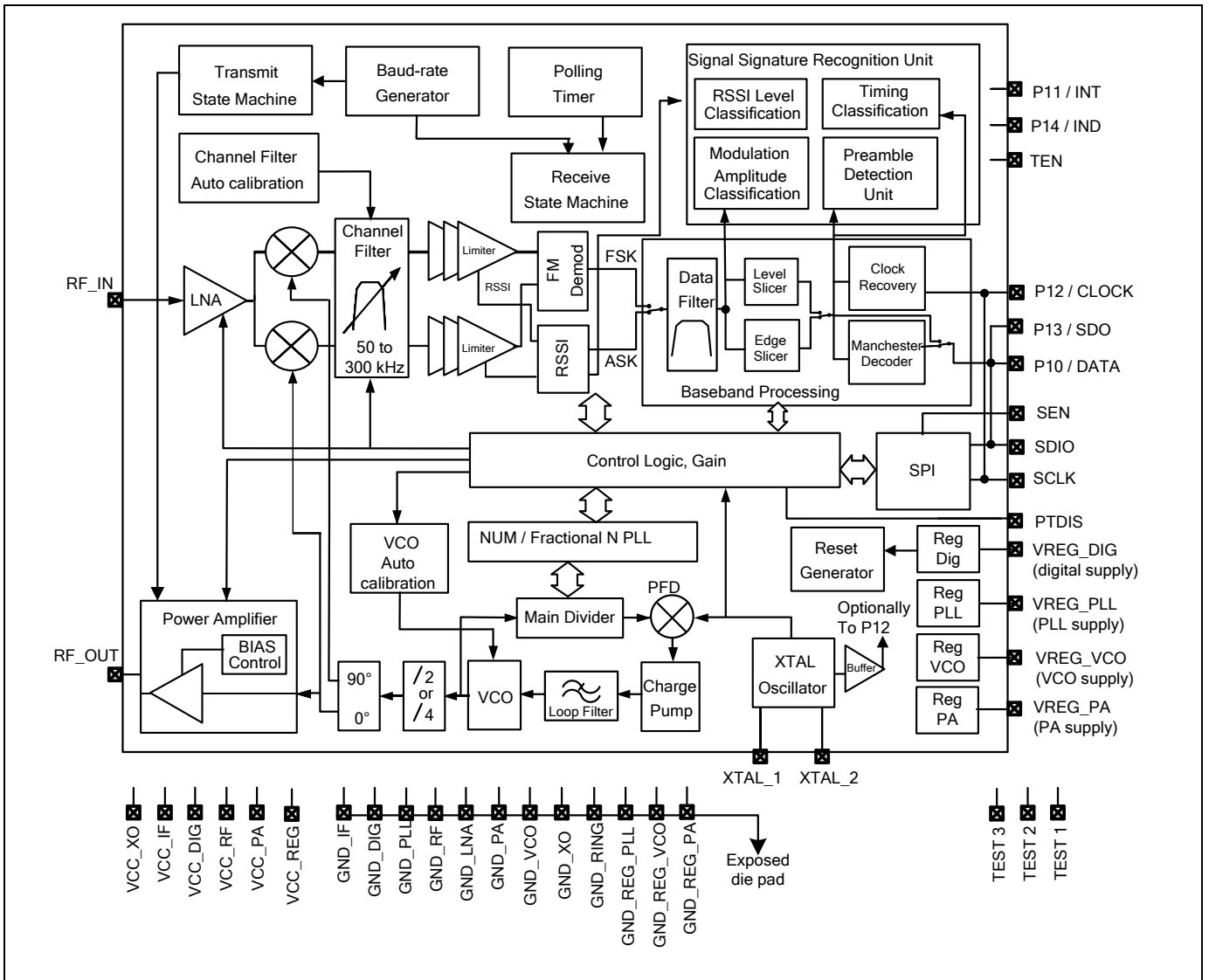
Figure 2. Functional block diagram

10

Integrated UHF Transceiver

3.1.2 TX block diagram:
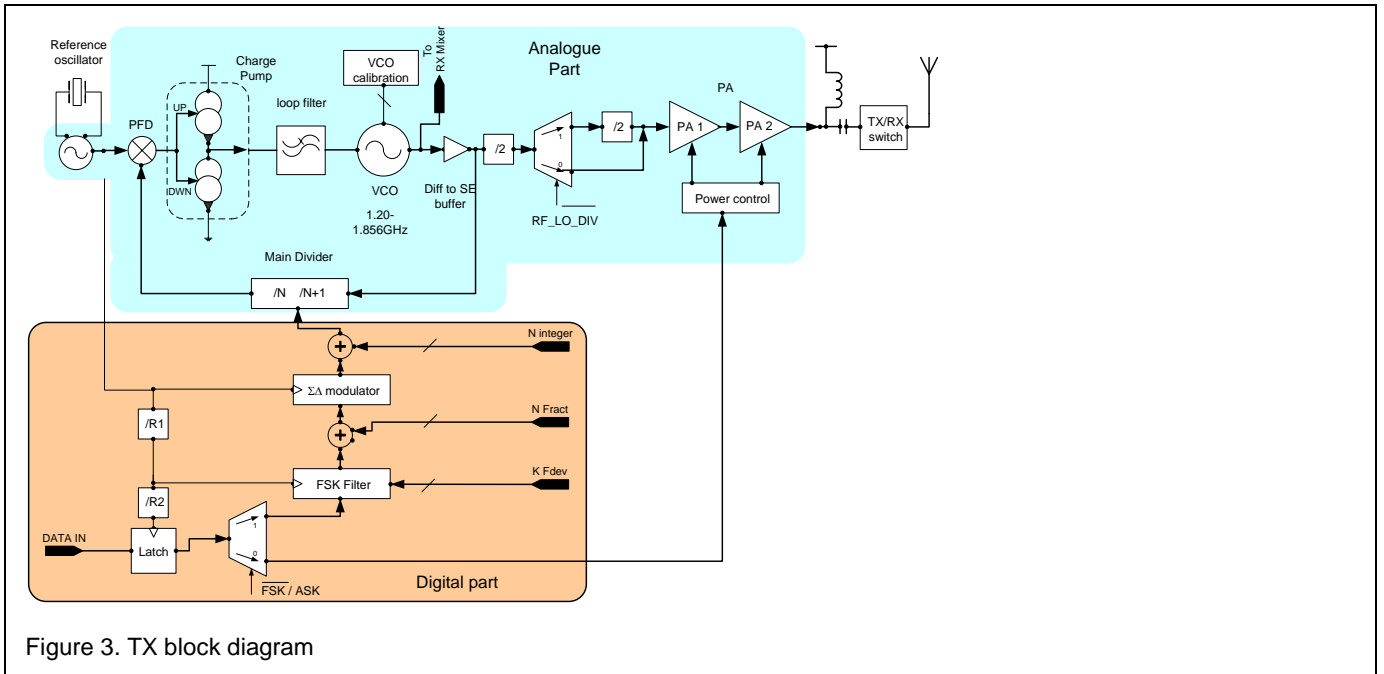
Figure 3. TX block diagram

3.1.3 RX block diagram:
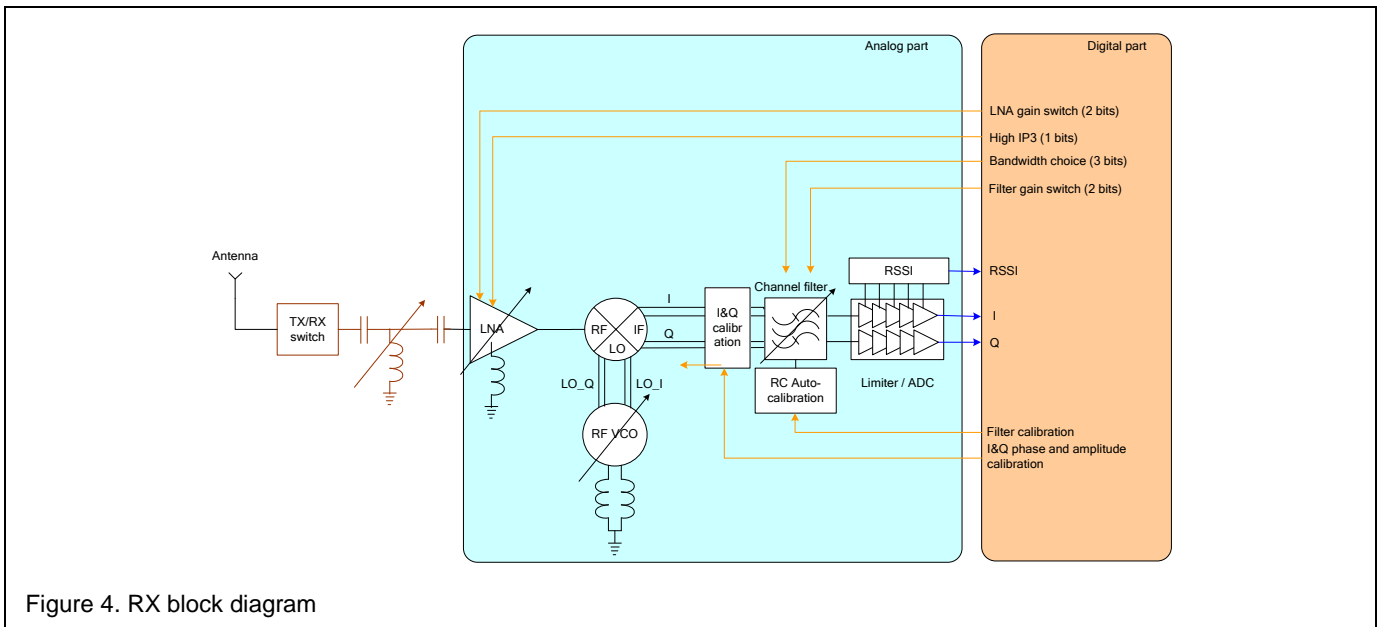
Figure 4. RX block diagram

Integrated UHF Transceiver

3.2 General Architecture description

The OL2381 transceiver is designed for use in both complex base-stations, when paired with powerful microcontrollers, and low component count remote units with low pin-count micros. The IC features unique configuration possibilities via external pin-level configuration or SFR bit manipulation. Several automatic sequences are implemented to ease device operation, all of which can be manually influenced or overridden by control-bits.

Power-management

The device contains a configurable power-on reset block. The device control registers are reset as the external voltage rises, to ensure that the device state is in "stand-by mode". This is implemented by ensuring that all blocks are off except the SPI and the digital regulator. It should be noted that the digital regulator is operating in clamp mode at this time.

XTAL Oscillator

The main time-reference is derived from an amplitude controlled XTAL oscillator. This 16MHz reference is used as a reference clock for the PLL and as a timing reference for various analogue calibration purposes.

Polling timer

Several base-station applications require a low-power polling timer for periodic device wake-up. This feature is essential to enable listening in pre-programmed time-windows when the OL2381 is used in receive mode applications. Internal configuration and trimming registers allow the setting of a wide range of different timer-intervals while achieving an average timing accuracy of 2%.

TX block:

The TX section is able to operate within all ISM bands (315MHz, 434MHz, 868MHz and 900MHz). The device provides a high degree of flexibility and is capable of ASK/FSK modulation, Output power control and on-chip baud-rate generation with data rates up to 112kchip/s. The device features multi-channel operation and enables carrier frequency adjustment and compensation of XTAL frequency offsets due its high resolution Fractional-N PLL architecture. The TX block features a high degree of integration, employing an on-chip VCO and PLL loop Filter.

VCO calibration:

On chip calibration is available in order to reduce the VCO input voltage range, and thus reduce the PLL loop bandwidth variation. The variation in system parameters such as locking time and LO phase noise can therefore be maintained within a tight window.

Calibration is carried out by selecting the proper VCO sub-band according to the desired channel frequency. VCO sub-band selection and the PLL start-up sequence can be triggered by command and are supported by an automatic flow sequence. This flow can be overridden if required. It should be noted that if the incorrect sub-band is chosen the VCO calibration will be unable to tune to the desired frequency.

Transmit Command

Tx Parameters (Frequency, Modulation, Output-Power,etc) can be predefined to enable fast and simple entry into transmit mode (PA switched on).

RX block:

The RX path of the device consists of a broadband resistive-feedback LNA, a mixer (mixing down the input signal to an IF of 300kHz), a channel-filter, a limiter, an RSSI stage (AM demodulation) and a base-band signal processing block used for FM and AM data and clock recovery. The LNA, Limiter and channel-filter gain-settings can be configured via control-bits. The bandwidth of the channel-filter can also be adapted.

Channel filter auto calibration

Channel bandwidth accuracy requirements vary between applications. The modulation bandwidth changes with different bit rates. Data rates can be chosen from 0.5 to 112 kchip/s and the IF channel filter bandwidth has to be set accordingly (50kHz – 300kHz).

In order to maintain constant performance Auto-calibration of the channel bandwidth is implemented. This ensures stable cut-off frequencies and filter roll-off over process and temperature variations. This calibration is included in the receive command.

I&Q calibration

In order to improve the channel image rejection for certain applications, an I/Q calibration can be implemented. The purpose of this calibration is to improve amplitude mismatch and phase quadrature between I and Q signals.

Both parameters can be trimmed by injecting an external RF signal operating in the image channel. The RSSI can then be used to determine the optimum settings to have the minimal remaining signal. This calibration is required for each frequency band.

The I/Q calibration settings are made available and must be stored by an external micro-controller.

Receive Command

The predefined set of Rx Parameters (Center Frequency, Modulation, etc.) enables Receive Mode (Receiver and LO-Buffers switched on) to be entered quickly after receipt of the receive command. Several means of signal signature recognition are implemented. These modes of semi-automatic signal processing can be pre-selected by the receive command.

Integrated UHF Transceiver

Signal Signature Recognition Unit

Several signal recognition units are implemented in order to provide fast and accurate signal detection. Signal signatures such as signal level (RSSI), modulation depth or baud-rate and coding can be automatically detected as wakeup criteria during the wakeup search phase.

Preamble detection

A configurable 1–32 bit pattern recognition unit can be implemented to aid power saving and avoid unintended wake-up due to ambient noise.

3.3 General Operation

The OL2381 is a state machine based transceiver and will therefore be used in conjunction with a microcontroller. In order to choose the appropriate configuration of the OL2381 for a specific application this datasheet should be studied carefully. First of all the interface to the micro-controller has to be defined, see section 4. The next step shall be the identification of the correct 'basic' settings. The operational frequency band has to be chosen, all relevant registers have to be programmed for Tx and Rx mode (exact setting of desired frequency, modulation, modulation depth, IF-bandwidth, baseband-filtering, etc). It is strongly recommended to study every aspect of this datasheet in detail and to verify correct operation of the device by measuring available debug-signals. The optimum operation and the highest performance of the device will be achieved by fine-tuning and verification of all device settings. After determining the optimum device configuration the automatic operation sequences should be used. Generally the first operation would be to bring the device from stand-by to power-up state (precondition for any operation). This can be done manually (triggered by the external micro-controller) or automatically by the built-in polling timer. In this device mode, the XTAL-oscillator is operational. SFR register bits (configuration data) can be changed. This mode can be left by issuing transmit or receive commands. To save power and operation time the commands can be prepared by the 'prepare transmit' or 'prepare receive' commands.

13

Integrated UHF Transceiver

4 Interface Description

4.1 Port Connections

The minimum connection between a host controller and the OL2381 comprises of three SPI lines; SDIO, SCLK and SEN only. SPI communication and TX / RX data transfer can be achieved by multiplexing the SPI data and clock lines. The SPI of the host controller must be set in slave mode after the RX / TX Command is sent, the SCKL then shifts the out / in data via the SPI of the host controller.
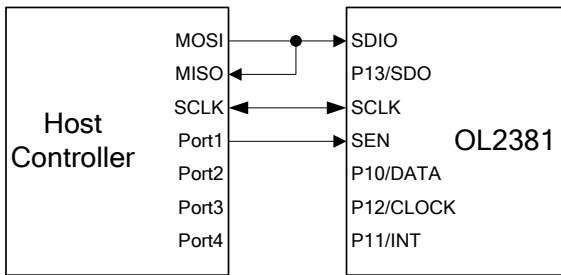
Figure 5: Minimum port connections for transmit and receive mode.

The device also supports full four-line SPI mode, the line SDIO serving as data input and P13/SDO as data output.

Alternatively, the device can be configured for separate data inputs and outputs. The lines SDIO, SCLK and, if selected, P13/SDO can be reserved for SPI command handling. In this case, Transmit and receive data is handled by the port pin P10/DATA, the clock is carried by port P12/CLOCK. The OL2381's remaining ports can be used for additional status information.
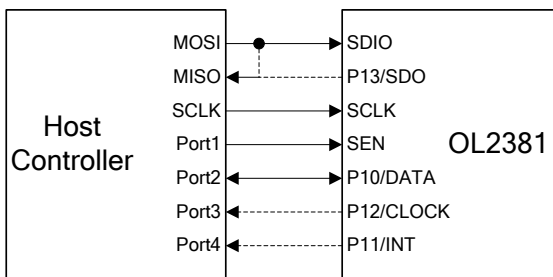
Figure 6: Full port connections between host controller and the OL2381.

4.2 Special Ports

4.2.1 TEN

Test enable input: **this pin has to be connected to GND!** This pin is only required for a factory test and has no user operable functionality.

4.2.2 TEST1, TEST2, and TEST3

Test pins for internal analog test-signals. These pins have to be left open in the application.

4.2.3 RSTDIS

The RSTDIS defines the state of the polling timer enable bit after power on. When the pin is set to low the device is initialised with the polling timer enable bit set to 1.

4.3 General Purpose Ports

The device features five general purpose ports P10 to P14 (see PWRMODE register), with selectable dedicated user functions. The port function is controlled by the bits P1xCx. The width of these control bits for every port depends on the number of selectable signals.

All general purpose ports except P11/INT and P12/CLOCK are in tri-state after power-on reset. Port P11/INT is initialized as an output driving the low-active POR interrupt. Notice that this interrupt is non-maskable.

Port P12/CLOCK is initialized to provide a 1 MHz reference clock as the default output.

4.3.1 P10/DATA

Priority of functionalities:

1) Output signal of receiver debug interface.

2) RX data output, if bit SEP_RX_OUT = 1 and the receiver is activated

OR

TX data input when bit SEP_TX_LINES = 1 and the transmitter is activated

If the bit SEP_TX_LINES in PORTCON2 is set and P12C is equal to 010b, the port delivers the transmit clock as specified through register TXCON. This clock is activated after the ninth SCLK pulse of the transmit command and it runs until the power amplifier is turned off. This clock indicates the timing of the transmitter and informs the controller when the device samples the input data from the P10/DATA line.

If the bit SEP_RX_OUT in PORTCON2 is set and if P12C equals 010b, the port delivers the receive clock associated with the data provided at P10/DATA. This clock is activated after the ninth SCLK pulse of the receive DATA command. If the receive command is a PRDA, this clock is activated after successful detection of the preamble. In both cases the clock continues as long as the receiver state machine is in its DATA state. This clock is recovered from the timing of the received signal and informs the controller when it shall sample the data delivered at the P10/DATA line.

Please note that in contrast to P10/DATA, where setting the SEP_TX_LINES or the SEP_RX_OUT bit overrules the

14

Integrated UHF Transceiver

normal port function, this is not the case for P12/CLOCK. The clock is only output if selected with P12C = 010b.

The inversion bit P10INV inverts output data (including RX data). If an inversion of transmit data is desired, the bit INV_TX_DATA (TXCON Register) must be used.

4.3.2 P11, P12

P11 and P12 together with P10, form the serial interface when the Receiver debug mode is activated, please refer to section 13 RXD Debug Interface.

4.3.3 P14

P14 can be used to control an external circuit, eg a Tx / Rx switch or an LNA.

4.4 Serial configuration interface description

4.4.1 General SPI Information

The chip is configured via a three or 4 wire serial interface, consisting of an 8-bit shift register and 80 8-bit registers holding the configuration data.

Data can be exchanged with multiple 8-bit frames (auto-increment) or in portions of 8 bits (1 byte), which provides an advantage when using a hardware SPI-Interface. Data in the shift register is loaded into the addressed register on the last edge of SCLK within the last bit of the transferred byte.

4.4.2 SEN

A logic low applied to the SEN pin disables the SPI interface. The internal state machine is halted and every activity on the pins SDIO and SCLK is ignored.

If the device is in POWER DOWN mode, a positive edge of pin SEN activates the device. The crystal oscillator is always on, unless the device is in POWER DOWN mode. The watchdog is cleared with a high level of pin SEN (see section 6.2).

After the transmit command the SEN pin has an additional function: At the falling edge of the SEN pin the level of the SDIO pin is latched and frozen.

4.4.3 SCLK

SCLK is the clock pin for the serial interface. Every edge of SCLK shifts data into or gets data from the SPI register-set. The second clock edge (SCLK) is used for data capturing and the direction switching of SDIO between input and output is accomplished with the first clock edge of the ninth bit. An additional clock edge is necessary at the beginning of a transmit or receive command.

The polarity of the clock for an SPI command can be selected (see section 4.4.5).

If desired, the pin SCLK can carry the baud-rate clock during a transmit command and the recovered receiver clock during a receive command.

4.4.4 SDIO

SDIO is the bi-directional data input / output pin of the serial interface. Data In or Data Out operation is adapted automatically during SPI communication sequences.

If desired, the pin SDIO can be used to input data if a transmit command is executed or for received data if a receive command is active.

4.4.5 General SFR access information

If SCLK is high at the rising edge of SEN, the data is transferred with the rising edge of SCLK (like shown in the write and read-access diagrams), if SCLK is low at the rising edge of SEN, the data is transferred with the falling edge of SCLK.

For continuity, all figures and examples included herewith assume EN is low at the rising edge of SCLK (unless otherwise stated). The first edge of SCLK is referred to as the rising edge and the second as the falling edge.

15

Integrated UHF Transceiver

4.5 Write and Read access to SFR

Write access to SFR

Figure 7. Write Serial Interface Timing diagram

Read access to SFR

Figure 8. Read Serial Interface Timing diagram
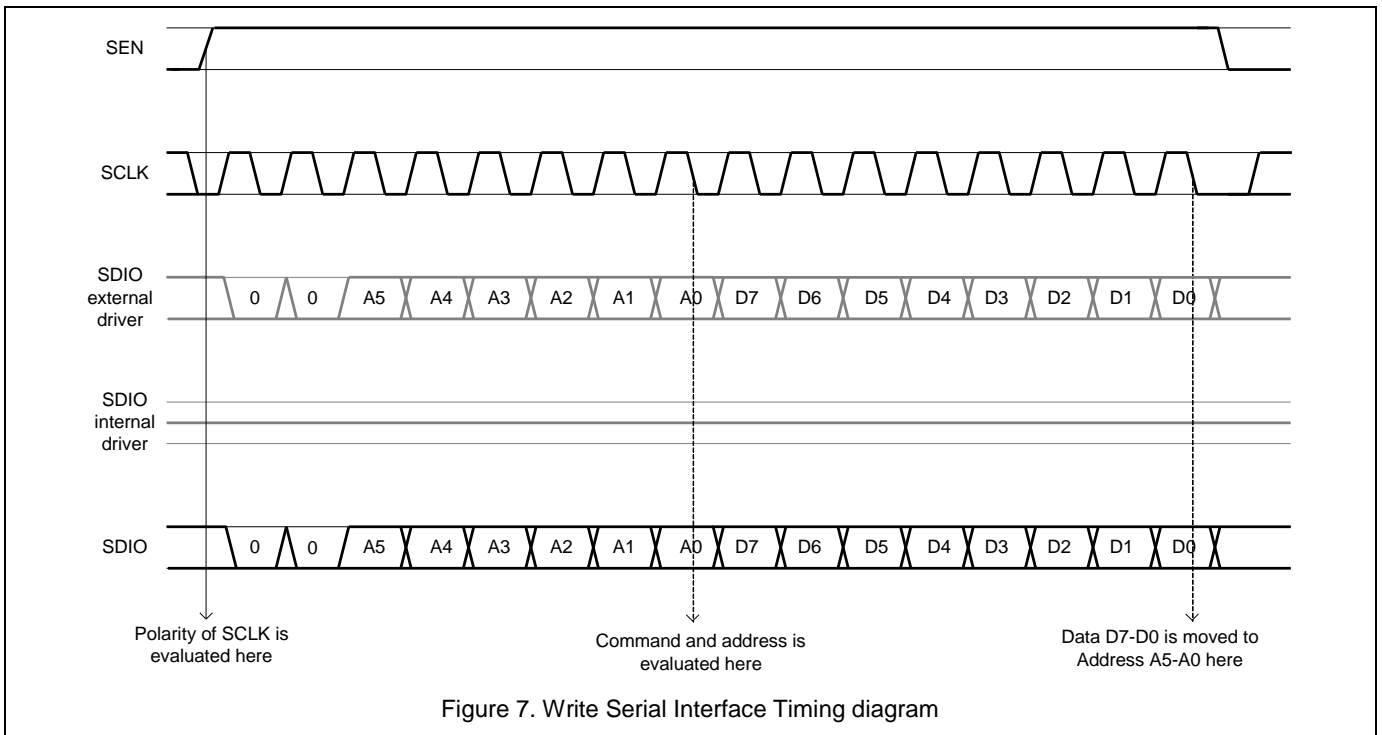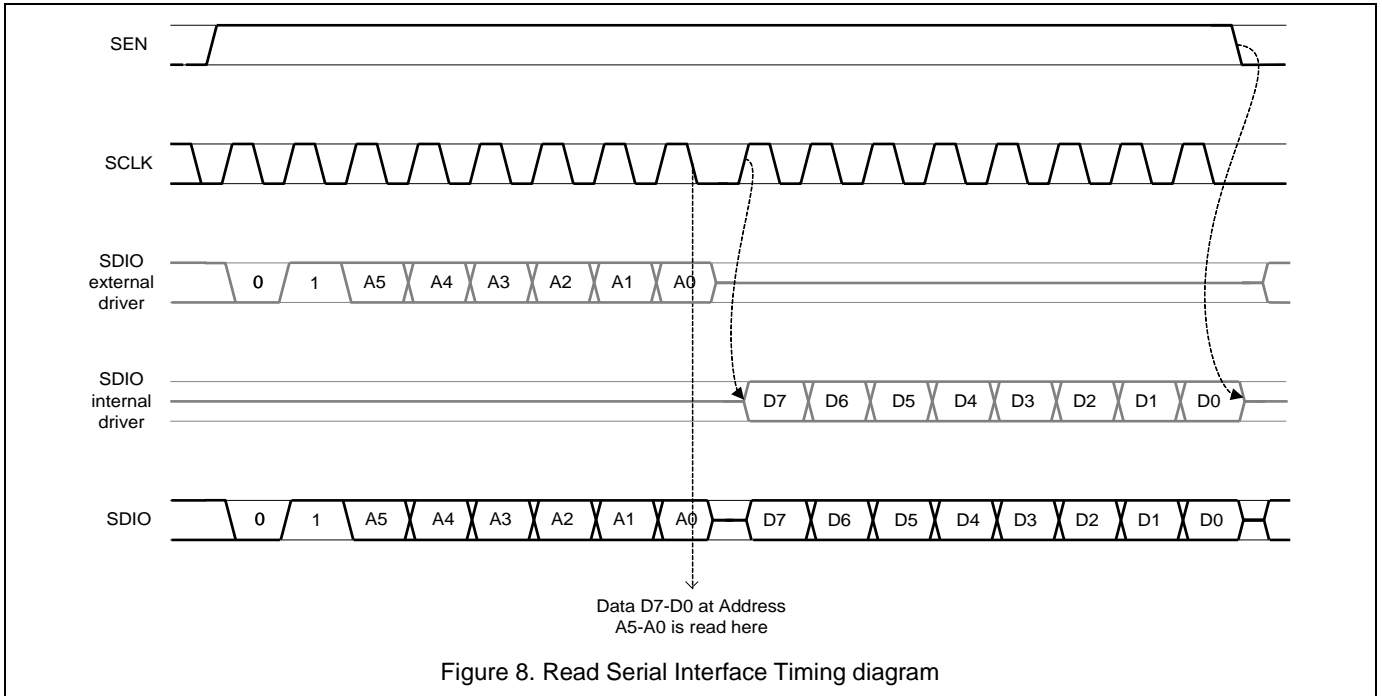
4.5.1 Separation of SDI and SDO Line

In order to use a four-wire SPI interface it is possible to use pin SDIO as MOSI pin and pin P13/SDO as MISO pin. Timing and output control of pin SDO is the same as for the internal SDIO driver.

16

Integrated UHF Transceiver

Read access to SFR with separate SDO line

Figure 9. Read Serial Interface Timing diagram (SEP_SDO = 1)
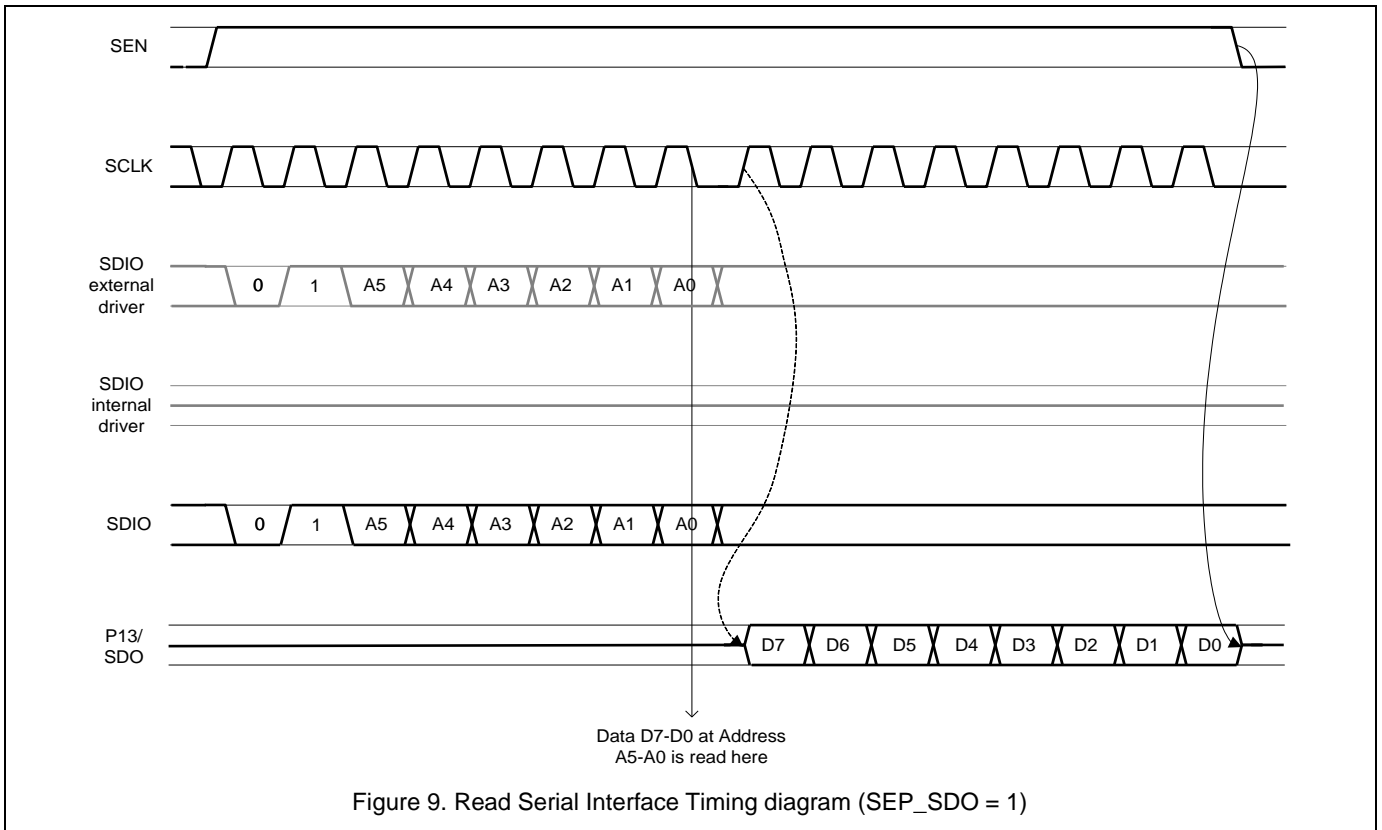
4.5.2 Read and Write Access to SFR with Auto-Increment Function

If the SPI clock SCLK is still applied after the first transferred 8 data bits, the auto-increment function automatically increases the address for the following next 8 data bits by one. This enables writing data to a continuous range of bytes without having to set the address for every single data-byte. The auto-increment function is terminated with the falling edge of SEN.

If the address reaches the end of the address range (i.e. 3Fh) an additional increment causes the address to start at 00h again. This wrap around is accomplished in the current address bank. The auto-increment function has no influence on the bank selection.

Integrated UHF Transceiver

Write access to SFR with auto-increment function

Figure 10. Write Serial Interface auto-increment Timing diagram
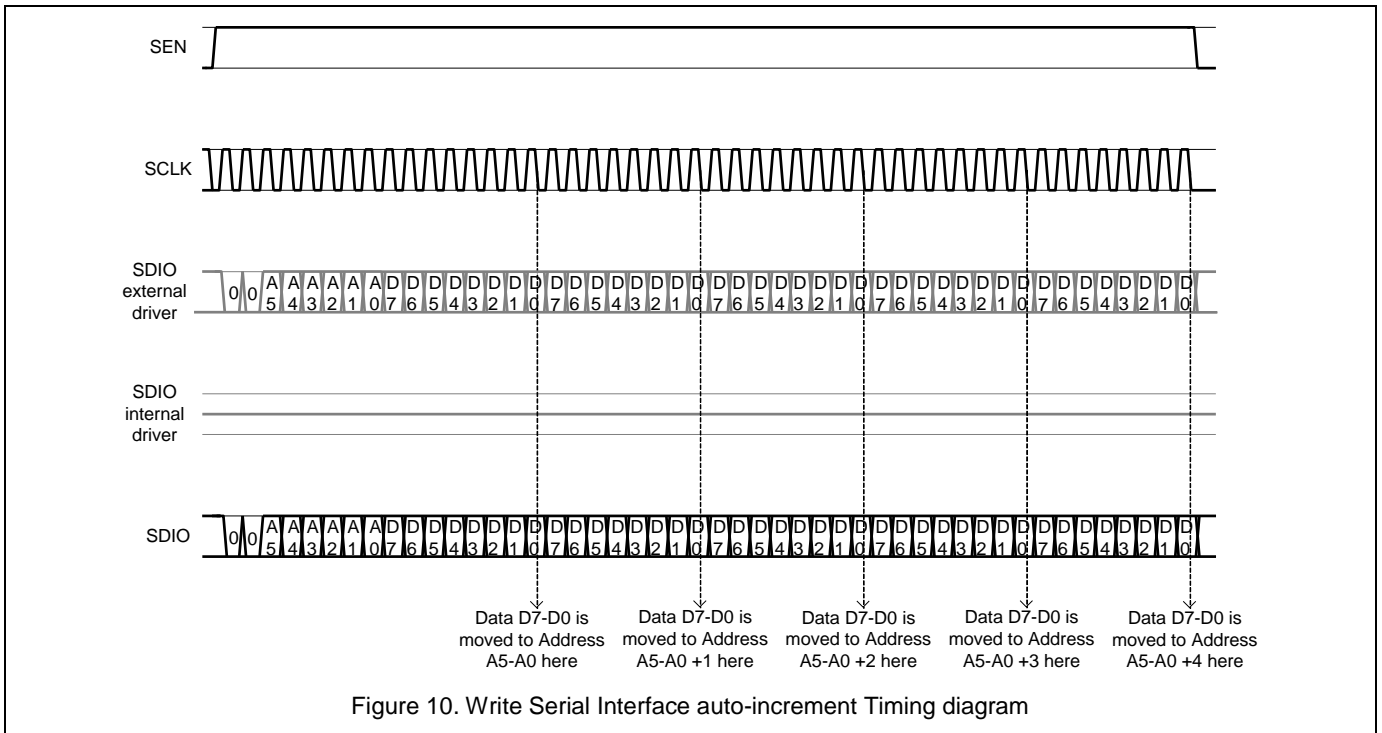
SEN must be forced low after registers have been written in order to signal end of Write. The diagram shows an example, where 5 successive bytes are stored

Read access to SFR with auto-increment function

Figure 11. Read Serial Interface auto-increment Timing diagram (SEP_SDO = 0)
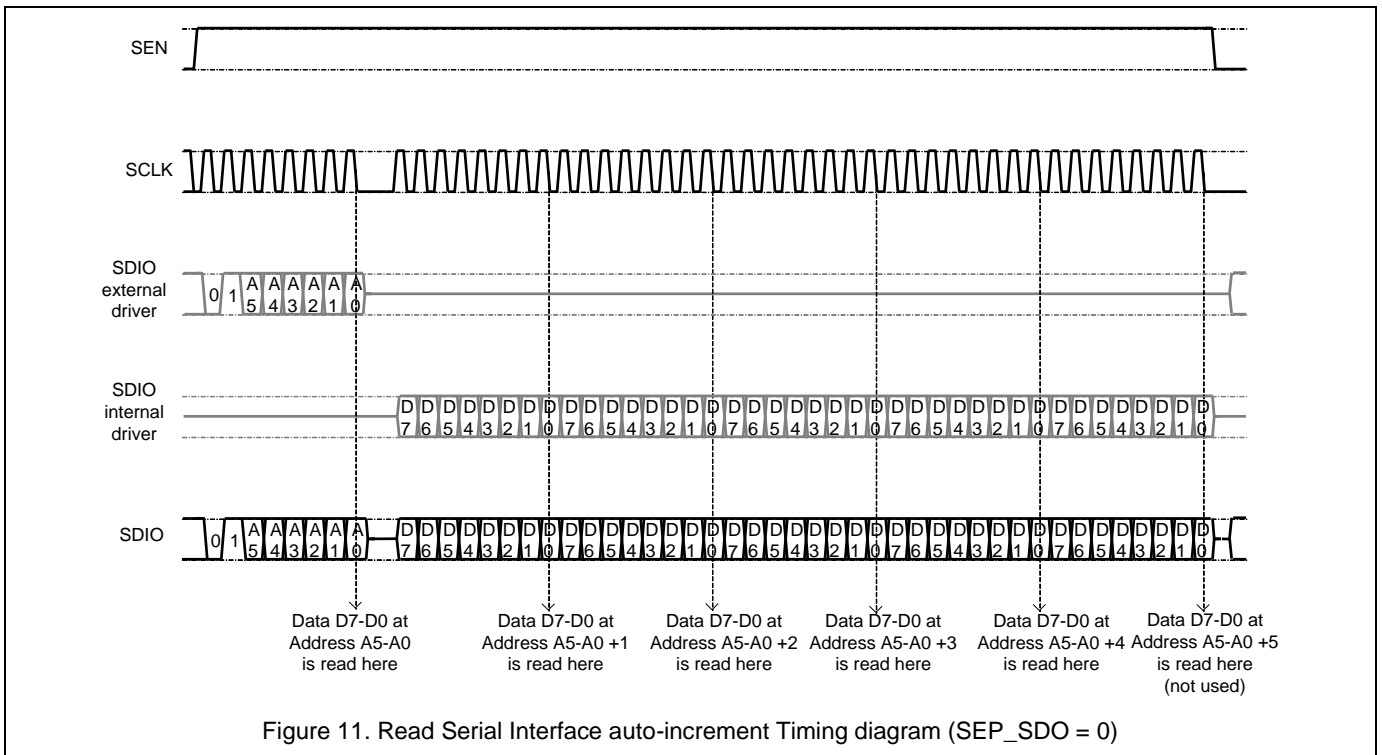
SEN must be forced low after registers have been read in order to signal end of Read. The diagram shows an example, where 5 successive bytes are read.

18

Integrated UHF Transceiver

5 Device Mode Description

Automatic Start-Up Procedures

The device features the following automatic start-up procedures in order to ease device handling and configuration:

- Power-on and crystal oscillator start-up
- PLL and VCO start-up including calibration
- Preparation for transmit mode
- Preparation for receive mode
- VCO auto calibration at every change of the centre frequency
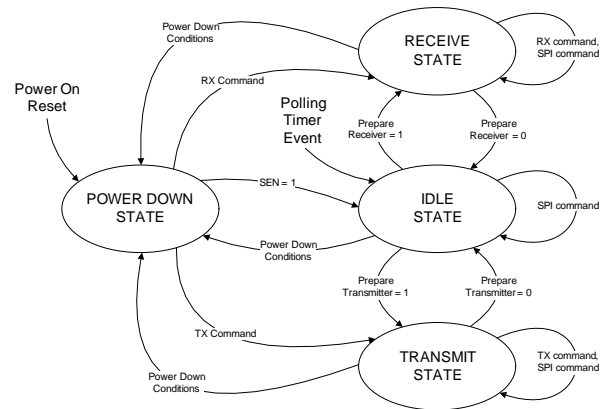
Figure 12: Simplified state diagram

General Description

The automatic start-up procedures are implemented to aid the quick and easy transition between operational states. Most procedures are controlled by changing bits in the PWRMODE register. Certain configurations can be directly entered by the transmit or receive commands.

5.1 The Reset and Power Mode Register

The PWRMODE register acts as the 'main power on/off/standby switch' of the device. Setting the RESET bit of this register brings the device into the reset condition equal to the power-on reset state. This power down state is also reached automatically at first power-on (battery insertion). If this bit is set with a write command the effect on all registers with a reset condition is a 'hard-reset'. If, with the same SPI write command, other bits are simultaneously written to the PWRMODE register their content will be changed automatically to the power-on reset state.

First power-on reset

The non maskable interrupt flag IF_POR is set when the initial power on reset takes place (battery insertion).

Power-down

Setting the PD bit brings the device into the low current consumption standby mode. All analogue receive and transmit circuitry including the crystal oscillator are turned off and all dynamic digital activity is stopped. Only the SPI and the polling timer (if enabled) are active. The PD bit is also under automatic device control and is set under the following conditions:

- power-on reset or setting the RESET (setting the reset bit overrides all other) bit
- the watchdog timer times out

Three important static device internal enable signals are decoded from the DEV_MODE: PLLEN, TXEN and RXEN.

- PLLEN is set whenever the DEV_MODE is not 00.

- RXEN is set only if DEV_MODE is 10.
- TXEN is set only if DEV_MODE is 11.

An important implication of this is that a Transmit operation is immediately aborted if the active mode is switched to anything except Transmit Mode. For example, switching the device into Receive mode immediately shuts down the power amplifier without smoothly ramping down the RF power.

Conversely, entering Transmit mode immediately aborts any receive operation.

The DEV_MODE bits can be either set directly by writing the PWRMODE register or by sending a Receive or a Transmit command, where a Receive command sets the DEV_MODE to 10 and a Transmit command sets the DEV_MODE to 11.

Setting the RESET bit or setting the PD (power-down) bit resets the DEV_MODE to 00, where only the crystal oscillator is (potentially) enabled.

An alternative to setting the device mode can be to send a Transmit command and delay the '9th Edge'. This has the effect of setting the frequency and iniating the device as if in Transmit mode. The PA is then switched on with the '9th Edge' of the Transmit command.

5.1.1 Flow Description

The following actions are performed if the device leaves POWER DOWN state and enters ACTIVE state. These internal control signals are explained in more detail in later sections.

POWER DOWN state indicator is cleared.

Digital Regulator Startup

The digital voltage regulator is turned on whenever the device leaves the power down state.

19

Integrated UHF Transceiver

XTAL Oscillator Startup

The crystal oscillator or the buffer for the external clock is turned on depending upon XO_DIS and EXT_CLK_BUF_EN bits of the CLOCKCON register.

Bit XO_RDY = 1 once the crystal oscillator has settled. The device waits for number of clock periods until the frequency and the duty cycle of the clock output have fully settled to within the required specification. The end of this waiting period is indicated with REFCLK_RDY going to 1. This enables the master clock gate at the root of the clock distribution tree and if applicable, the reference clock for the digital part is enabled. A (re-)calibration of the polling timer is also initiated at this point.

PLL Start-Up

This sequence is controlled by the internal control signal PLLEN. The voltage regulators for the PLL and VCO (REG_VCO_ON, REG_PLL_ON) are turned on.

Wait until the voltage regulators have settled. This sequence is finished, if LO_PWR_RDY = 1

Turn on VCO

The phase frequency detector (PFD_ON), prescaler (PRESC_ON), clock for the PLL (CLK_PLL_ON) and PLL lock detection are turned on with the next clock cycle.

Perform VCO calibration

This sequence is complete once the PLL is locked (LO_RDY is set). A manual VCO calibration immediately stops any Tx or Rx command.

Preparation for Transmit Mode

This mechanism is invoked by by issuing device mode 11 (prepare for Tx) or by sending a Transmit Command.

The voltage regulator for the power amplifier (REG_PA_ON) and the VCO clock divider for transmitter path (TXON) are enabled.

This sequence is finished, if the regulator of the power amplifier has started properly (brown-out detection not active).

Preparation for Receive Mode

This mechanism is invoked by issuing device mode 10 (prepare for RX) or by sending a Receive Command.

The bandgap reference circuit for the receiver part (RX_GAP_ON), VCO clock divider for the receiver part (PLL_LOCK), reference clock for the receiver path (CLK_RXA_ON), and the analogue part of receiver (RXA_ON) are enabled.

Perform channel filter calibration

The channel filter calibration is performed every time the device enters receive mode. This sequence is finished, if the channel filter calibration is finished.

5.2 Changing device modes

Intermediate device modes may be required in an operation sequence e.g. start digital regulator and XTAL to initialize / change SFR contents or to re-trim the polling timer. This can be carried out by changing the corresponding registers. However, the direct commands may be more useful if the only operation required is the entering of Tx or Rx mode. The corresponding sequences will be automatically started and operation will be enabled after all internal settling times have been met.

5.3 Interrupts

TheOL2381 can generate various interrupts which can be enabled by the IEN register and read from the IFLAG register. The IFLAG register is always cleared after it is read. Certain pins can also be configured to present the these interrupts, as documented in the interface description section.

5.4 Power Supply and Reset

Each main functional block is equipped with its' own dedicated supply voltage pin. For this reason several supply pins are available on the package and all have to be connected. Note that all ground connections of these functional blocks are bonded to the exposed die pad of the package (metal plate underneath the die). Some blocks are supplied via dedicated integrated low-dropout voltage-regulators. Note that for all regulators the output voltage is available both internally and externally on a pin in order to connect a decoupling capacitor. The following blocks have regulated supplies.

Block	Regulator supply pin	Pin to Decouple
PLL	VCC_REG	VREG_PLL
VCO	VCC_REG	VREG_VCO
Digital	VCC_DIG	VREG_DIG

Table 2: Blocks with regulated supplies

5.5 Operation of the Voltage Regulators

All regulators are operated automatically by selecting the corresponding device modes. The device modes are set by the two DEV_MODE bits in the PWRMODE register. Detailed information can be found in section 5.1.

The regulators can also be independently controlled by the control-bits located inside the TEST registers. Individual

Integrated UHF Transceiver

operation of the voltage regulators can be necessary for debug or measurement purposes. The following paragraphs describe each individual regulator and its purpose.

Digital Regulator

In order to operate the device the digital regulator has to be switched on. In stand-by state (power-down state) the digital regulator is by-passed and supplies the digital part with a low supply voltage in order to guarantee data-retention in the configuration registers. If the digital regulator is switched on the voltage will reach its stabilized value of approx. 1.8V. The digital regulator can be activated or deactivated by the bit REG_DIG_DIS in the TEST1 register. Clearing the bit enables the regulator depending on the selected device mode, setting the bit always disables the regulator.

PLL Regulator

To start any PLL operation the PLL-regulator has to be switched on. This happens automatically with operation of the bit REG_PLL_ON in the TEST2 register. Note: this bit only starts the PLL regulator, all functional blocks of the PLL are enabled individually by separate control-bits.

VCO Regulator

For stability and immunity reasons the VCO is supplied via an independent voltage regulator. This regulator can be manually controlled via the REG_VCO_ON bit in the TEST2 register. Note: this bit only starts the VCO regulator, the VCO operation is enabled individually by a separate control-bit.

PA Regulator

This regulator is enabled if PA operation is desired. This can be manually controlled by setting the REG_PA_ON bit. Note: this bit only starts the PA regulator, the TX operation has to be enabled by setting the corresponding command on the SPI interface.

5.6 Device reset

A device reset occurs whenever the supply voltage is applied on the VCC-pins (battery insertion). The device utilises two power-on detection mechanisms, one digital and one analogue. These reset circuits constantly monitor the supply voltage. Setting the bit RESET in the PWRMODE register performs the same operation by software. This is equivalent to a power-on reset. If the RESET bit is set via a command, it automatically will be cleared when the SPI signal SEN goes low after the next Write Register command.

21

Integrated UHF Transceiver

6 Main Control and Timing Blocks

6.1 Crystal Oscillator

6.1.1 Circuit Description

The crystal oscillator is the source of the reference clock for the PLL, the digital part and the mixed signal blocks in the receiver chain. A complete diagram of the crystal oscillator is shown below.
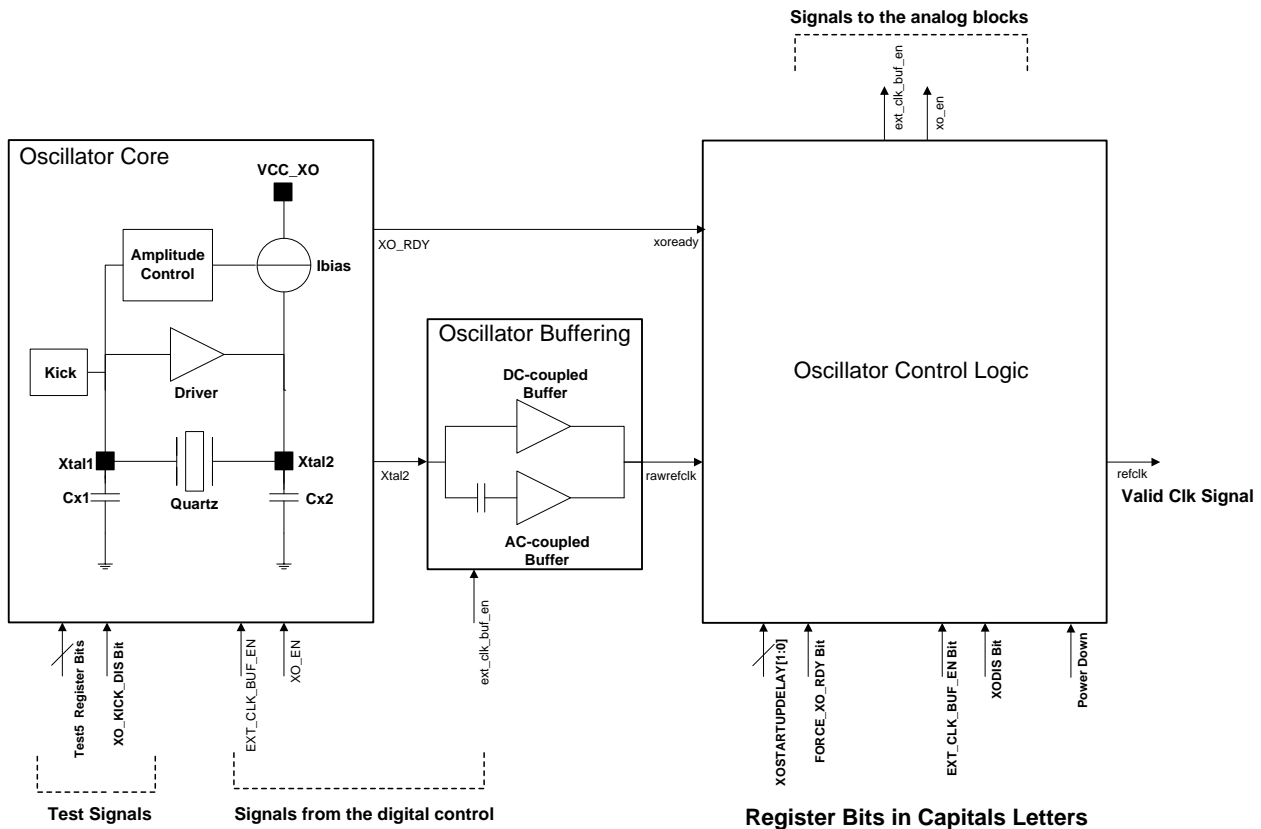
Figure 13: Crystal Oscillator Circuit

The Crystal Oscillator consists of three main blocks: the Oscillator Core, the Oscillator Buffer and the Oscillator Control Logic.

The Oscillator Core is a low power Quartz based Pierce Oscillator. The oscillation frequency is defined by the Quartz and the tuning capacitors CX1 and CX2. The low capacitance of the driver has negligible impact on the frequency value. The Oscillator Core is supplied by VCC_XO pin.

When the oscillation has started and the amplitude has been successfully detected, the Amplitude Control releases the signal XO_RDY to the Oscillator Control Logic for validation. This signal does not mean that the Oscillator is settled but that the Amplitude Control Loop has entered in regulation mode. An extra delay is still needed to ensure

the frequency accuracy (refer to XOSTARTUPDELAY in section 14.5.2 Register EXPERT1 at address 32h)

After start-up, the Amplitude Control avoids clipping and excessive driving power in the crystal unit.

The Oscillator Control Logic has the role to validate the oscillator signal and provide configuration facilities. The Oscillator Control Logic is supplied by the digital regulator to the level VREG_DIG.

The Oscillator Buffer consists on two amplifiers connected in parallel: One low-noise AC-coupled amplifier for crystal operation and one high-input-voltage DC-couple amplifier for testing purposes only. The Buffer plays the role of LevelShifter for the signals in PLL and Digital supply domains. The Buffer circuitry is supplied by the PLL and Digital regulators accordingly.

Integrated UHF Transceiver

Alternatively, an external clock signal can be applied at pin XTAL2. (Refer to External Clock Buffer in section 7.1.2). The applied signal has to comply with the logic levels in the digital core (0V for LOW and 1.8V for HIGH). With the OL2381 properly configured, the DC-couple amplifier replaces the low noise AC-couple amplifier. This provides the possibility to skip the start-up sequence of the internal Oscillator and allows the customer to stop the clock sequence for test purposes as well.

Caution:

The use of an external clock signal requires a special care in the hardware configuration. The Oscillator Core circuitry connected at XTAL2 can not stand higher levels than 2.8V. Therefore, the use of this test mode with supply voltages higher than 2.8V requires a hardware modification for VCC_XO. The recommended solution is the connection of VCC_XO pin together with VREG_DIG pin. In that configuration the integrity of the circuit is ensured but the digital noise needs to be considered.

The Crystal Oscillator is always active either in oscillator mode or in external clock buffer mode when the device is not in POWER DOWN state.
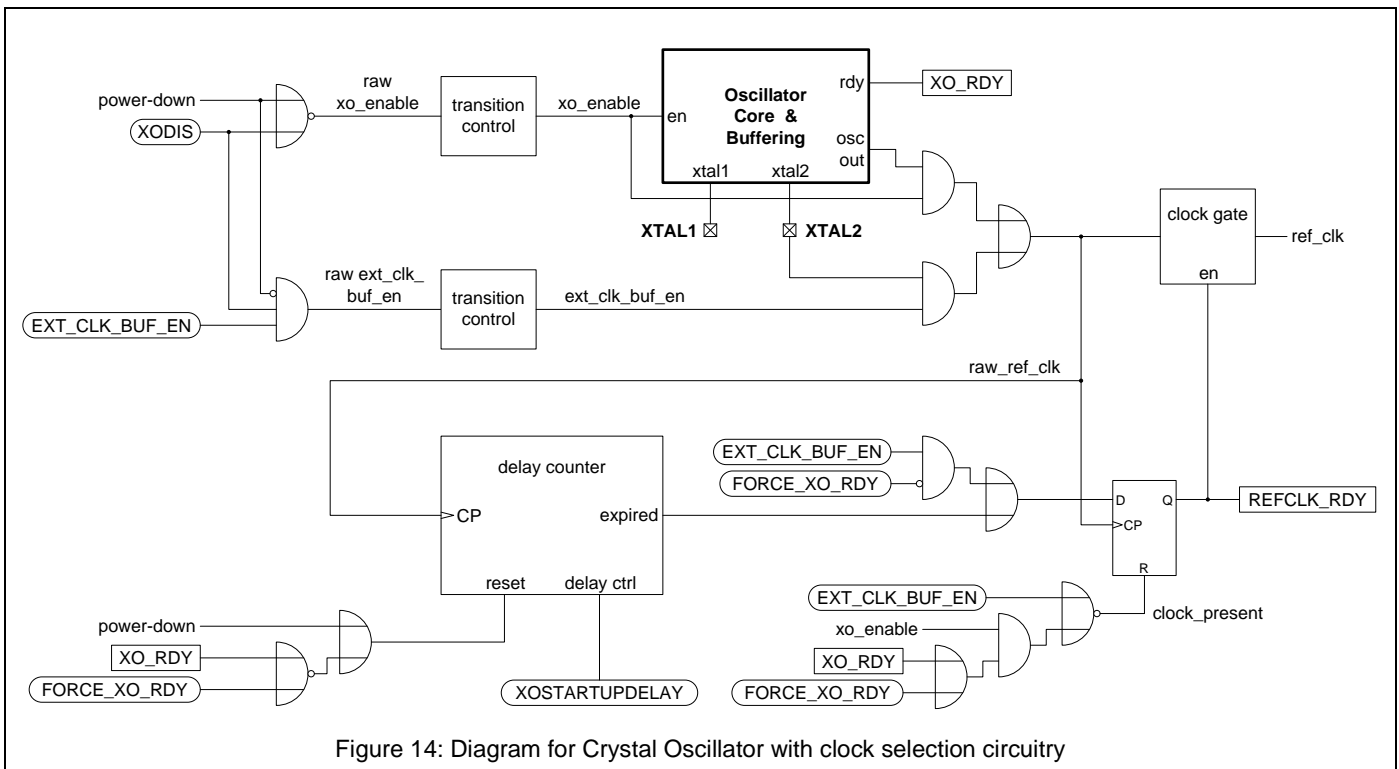
Figure 14: Diagram for Crystal Oscillator with clock selection circuitry

6.1.2 Oscillator Control and Control Bits

The Oscillator Control Logic is described in Figure 14. The signal labels enclosed in a rounded shape denote control bits in the register set of the OL2381, signal labels enclosed in rectangles denote (internal and 'official') status signals and signal labels with no boundary denote internal signals.

The enable logic is visible at the top left corner for both modes, the crystal oscillator mode and the external clock buffer mode. The crystal oscillator is turned on when both, power-down and XODIS, are false. The transition control ensures that no glitches can be generated when turning the

oscillator on and off. The external clock buffer is turned on when the device is not in power-down mode and both control bits, XO_DIS and EXT_CLK_BUF_EN are set (CLOCKCON Register). As a consequence of this bringing the device into power-down mode disables all clock activity and turning the crystal oscillator on has priority over turning the external clock buffer on.

If the crystal oscillator is turned on (xo_enable becomes true) and a crystal is connected to the oscillator, the raw clock becomes available after the oscillation has reached a significant amplitude, which is then signalled with the internal XO_RDY status signal. This internal status signal

Integrated UHF Transceiver

can be routed to P12/CLOCK for observation. While the crystal oscillator is disabled, it is ensured that the clock from this clock source is held at the zero level.

If the external clock buffer is turned on (ext_clk_buf_en becomes true) the signal connected to the XTAL2 pin is taken as the clock source. While the external clock buffer is disabled, it is ensured that the clock from this clock source is held at the zero level.

Since only one clock source can deliver a clock at a given time they can be easily merged. But only when the clock gate is enabled the clock is actually passed on into the circuit. The following paragraphs explain the conditions for enabling this clock gate separately for each clock source.

When using the crystal oscillator the delay counter, drawn at the bottom of the diagram, is held in reset state during power-down mode or if both, the internal status signal XO_RDY and the expert control bit FORCE_XO_RDY, are false. If the oscillator signals XO_RDY after start-up (or if the FORCE_XO_RDY is set), the delay counter is released from reset, which lets it count the raw clock pulses from the oscillator. Please notice that counting does not occur if the oscillation amplitude is too low or if the clock pulses are too 'thin' (duty cycle near 0% or near 100%). Therefore it is ensured that the delay counting does not start before the raw clock has a usable shape. After a programmable count (see the following table) has been reached, the counter stops and signals the expiration of the delay.

The digital oscillator start-up delay can be controlled by the two bits XOSTARTUPDELAY[1:0] of the EXPERT1 Register.

After the expiration status of the delay counter has reached the REFCLK_RDY flip-flop, which is shown at the lower, right corner of the diagram, it is sampled by the raw clock, which has now stabilized, and this declares the reference clock ready. This also enables the clock gate which passes the clock on to the circuit beginning with the following clock pulse. The REFCLK_RDY status flip-flop is immediately reset when the raw clock is no longer present, which happens when the crystal oscillator is turned off or XO_RDY becomes false due to any reason which may have stopped the oscillation.

Please notice that special care is needed when non-recommended crystals are used. The use of non-recommended crystals and resonators could have a negative impact on the start-up behaviour, on the frequency stability and on the PLL noise performance.

For recommended crystals the oscillation amplitude is always large enough, so the Amplitude Control can properly detect the start-up and the noise generated by the AC-couple buffering is appropriate for operation of the PLL.

If the crystal is replaced by a resonator with a low Q factor, the resulting amplitude may not become large enough, so

that the XO_RDY status may not be properly detected, although the generated clock could be still usable. In order to use the OL2381 in such conditions, the XO_RDY status must be overridden by using the expert control bit FORCE_XO_RDY. Please notice that the delay counting mechanism does not start counting before the raw clock has reached a certain quality.

If the external clock buffer is used, it is assumed that the clock source, which is connected to XTAL2, provides a stable clock with a duty cycle near 50% at the time when the EXT_CLK_BUF_EN bit is set. Therefore the delay counter is not needed in this case. But even without the delay counter the circuit provides a well-controlled startup sequence, which is enforced by the REFCLK_RDY flip-flop and the clock gate, so that no glitches are generated when the clock buffer is turned on or off. Please notice that not using the delay counter in this normal case requires the FORCE_XO_RDY expert control bit to be in the cleared state.

However, if the FORCE_XO_RDY bit is set when using the external clock buffer the delay mechanism is put into effect. This is how the delay counter is tested in the production test but it may also help to overcome start-up problems in the external clock source. The XO_RDY, REFCLK_RDY signals can be observed for oscillator testing via the test buffer. The resulting clock can be probed at the CLOCK pin.

6.2 Watchdog

The device features a watchdog timer to recover from situations when activation is not desired. The watchdog timer runs with the reference clock and it is activated, if the device is not in POWER DOWN mode.

The watchdog is cleared and temporarily stopped under the following circumstances:

- The pin SEN is high.

- A terminating wakeup search is executed, i.e. either a pessimistic wakeup search is activated (WUPSMODE = 0) or the timer for the wakeup search is activated during an optimistic wakeup search (WUPSMODE = 1 and WUPSTIMEOUT not equal to 0).

- A terminating preamble detection is executed, i.e. the timeout for the preamble must be activated (EN_PREADET_TIMEOUT = 1 and WUPSTIMEOUT not equal to 0).

Bit EN_PREADET_TIMEOUT can be found in register WUPSMODE. Bit WUPSTIMEOUT can be found in register WUPSTO.

The watchdog timeout can be adjusted according the following formula:

24

Integrated UHF Transceiver

$$Watchdog\,timeout = \frac{2^{15+WATCHDOG\_TIME}}{CLK_{REF}}, \quad with \;\; CLK_{REF} = 16\,MHz$$

It is not possible to turn off the watchdog completely. Only if pin SEN is fixed to high, the watchdog can be disabled for an arbitrary period.

6.3 Polling and Wakeup Timer

The device features a low power oscillator, which can be used to generate wakeup events. An overflow of the polling

timer always generates an interrupt request. Moreover, if selected, the device can be automatically released from the POWER DOWN state and it can enter the receive state.

The low power oscillator has a nominal period of 40 µs and a tolerance of ±50 % over the entire temperature and supply voltage range and over process dependent device spread.
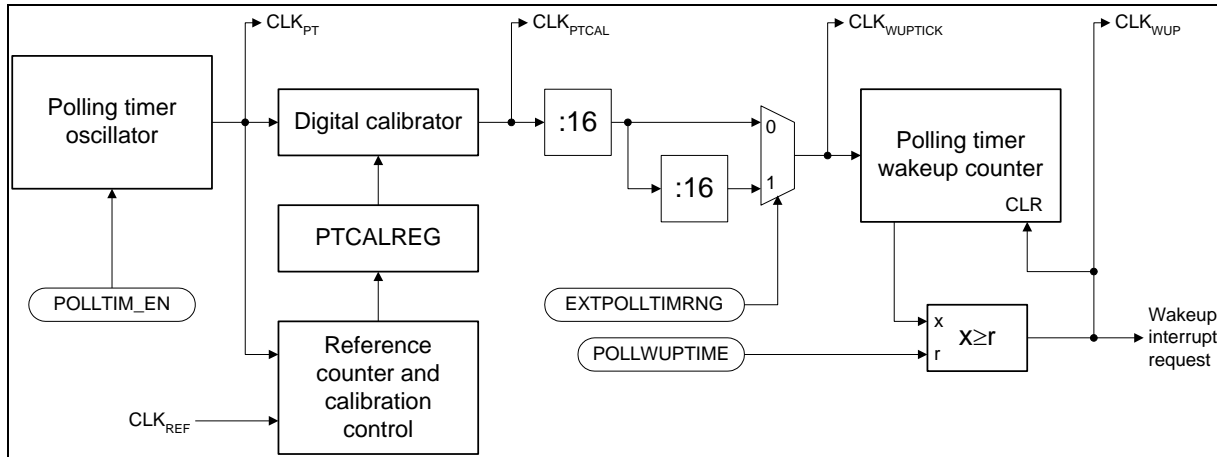
Figure 15: Polling Timer Block Diagram

The polling timer employs a digital calibration with a modulo counter. The crystal oscillator clock CLK_{REF} is used as a reference clock for the calibration. The calibration procedure measures one period of the polling timer clock CLK_{PT} and determines the appropriate calibration value for the modulo counter. The output clock CLK_{PTCAL} has a nominal period of 62.5 µs.

The polling timer can be turned on and off with the bit POLLTIM_EN in the PWRMODE register. The state of this bit after a master reset is determined by the RSTDIS bits.

Please note that due to the absence of the reference clock it is not possible to trim the polling timer directly after a master reset. The calibration register PTCALREG is set to its nominal value after a master reset.

The calibration of the polling timer is triggered automatically upon exit from POWER DOWN mode, providing the crystal oscillator has started properly. It is also possible to trigger a manual calibration by setting the bit MANUALPTCAL. Setting this bit generates a short pulse, which starts the calibration routine. Reading of bit MANUALPTCAL will always yield zero. The manual calibration is only executed if the polling timer and the crystal oscillator are running, otherwise the request is ignored. Setting bit MANUALPTCAL at the same time as POLLTIM_EN is not supported. The calibration shall only be performed after the polling timer oscillator has settled.

The value in the calibration register will be consistent under all circumstances. This must also be the case if a running

calibration is interrupted. Direct read or write access to register PTCALREG is not supported.

The wakeup time of the polling timer can be set with the 8 bit control register POLLWUPTIME. The wakeup time calculates to:

$$T_{WUP} = (POLLWUPTIME + 1) \cdot T_{WUPTICK}$$

The achievable resolution and wakeup times can be selected in two different ranges, a normal and an extended polling timer range according to the setting of the EXTPOLLTIMRNG bit in the CLOCKCON register.

It is possible to change the register POLLWUPTIME while the polling timer is running. If the new value is greater than the current content of the polling timer counter the running period is not interrupted and the newly set wakeup time is seamlessly adjusted. This mechanism allows the setting of a new wakeup time with respect to the last wakeup event. If the newly set value in register POLLWUPTIME is smaller than the current content of the polling timer counter the counter is reset immediately.

The digital calibration is implemented so that the accuracy of wakeup times greater than 10 ms is better than 1 %. This allows an overall timing error of less than 2 % for the given range.

6.3.1 Actions at polling timer wakeup

The POLLACTION register defines which action the device carries out after a polling timer event.

25

Integrated UHF Transceiver

The 2-bit POLL_MODE setting defines what the operating mode of the device shall be after a polling timer event.

The two RX_GAIN bits have the same meaning as the Receive flags RE and RF (gain step/switch selection bits). The RX_CMD bit has the same meaning as the Receive flag RC. It allows choosing between a WUPS (0) and a PRDA command (1). The RX_FREQ bits have the same meaning as the Receive flags RA and RB (frequency selection).

The last bit in the POLLACTION register, SET_RX_FLAGS, defines whether the current contents of the RX flag register is used for the automatically initiated Receive command (if 0) or whether the Receive flags RA, RB, RC, RE and RF flags are overwritten with the contents of the RX_FREQ, RX_CMD and RX_GAIN settings of this register, respectively, before the command is actually launched (if 1). If the flags are overwritten, the Receive flag RD is set to 1 in order to make the sub-command either a WUPS or a PRDA command. More information to the receive command can be found in section 9.10 Receive Command

6.4 Baud Rate Generator for the Receiver and the Transmitter

The baud rate generator generates the nominal, unsynchronized chip clock according to the following formula

$$baud\,rate = \frac{16\,MHz}{2^{PRESC}} \cdot \frac{2^{11} + MAINSC}{2^{12}} \cdot \frac{1}{128}$$

where PRESC is an exponent in the range from 0 through 7 and $2^{11} + MAINSC$ is the mantissa in the range 2048 through 4095. The resulting baud rate clock can jitter by one prescaler clock cycle CLK_{PSC}.

The lower bits of the mainscaler MAINSCL can be found in register TIMING0.

The divider by 128 is used as a 'clock' for several other blocks to measure the sub-timing within one chip interval.

This baud-rate generator is used as the time reference for an synchronized transmit operation and as time reference for the clock-recovery in receive mode.
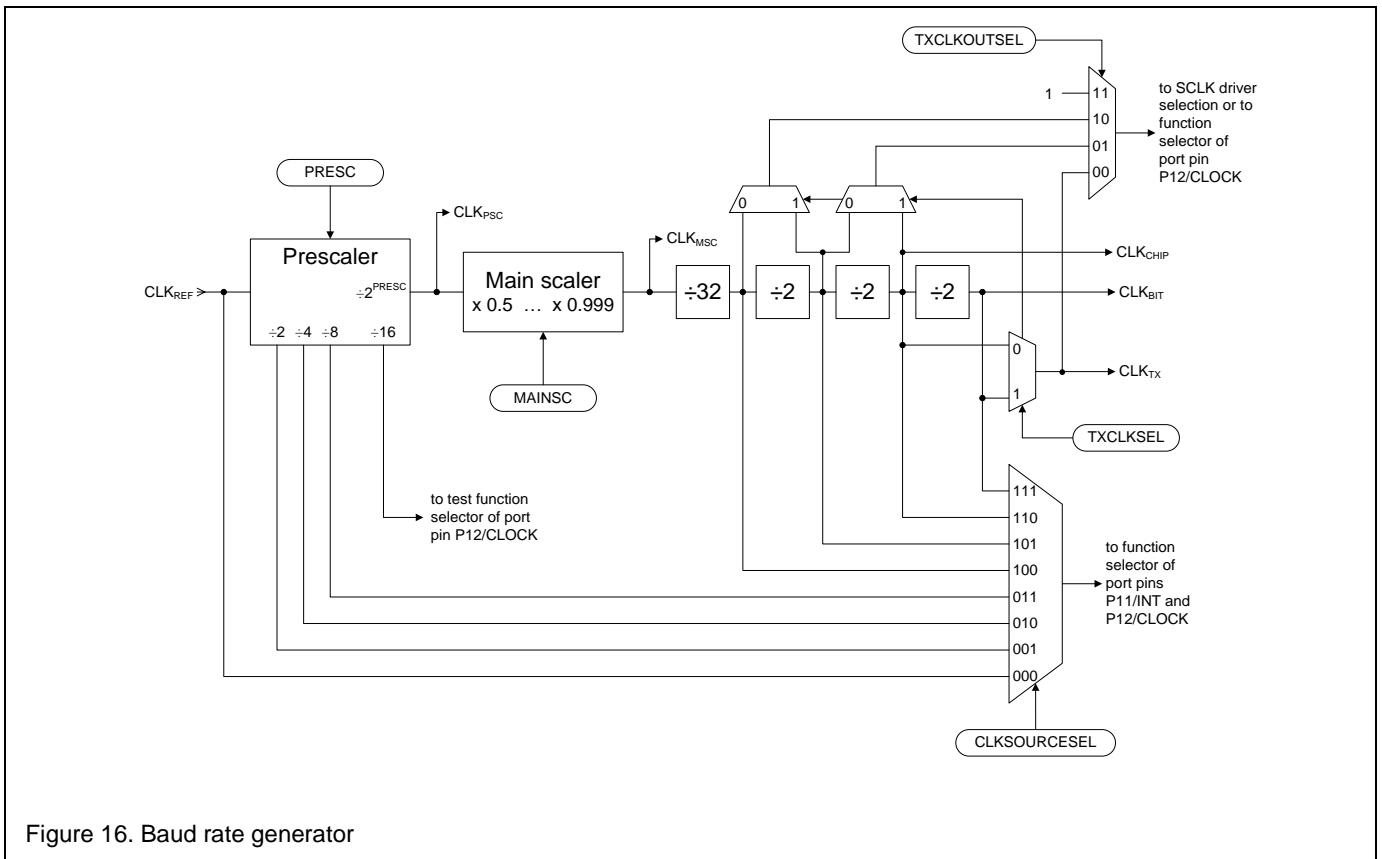
Figure 16. Baud rate generator

Calculation of clock in transmit mode:

$$CLK_{TX} = \frac{CLK_{REF}}{2^{PRESC}} \cdot \frac{2^{11} + MAINSC}{2^{12}} \cdot \frac{1}{128} \cdot \frac{1}{2^{TXCLKSEL}}$$

26

Integrated UHF Transceiver

with $CLK_{REF} = 16$ MHz.

With bit TXCLKSEL it can be selected whether the chip clock CLK_{Chip} or the bit clock CLK_{Bit} shall be used as transmit clock. If automatic Manchester generation is required the bit clock must be selected.

The bits CLKSOURCESEL can be found in register CLOCKCON.

The bit TXCLKSEL can be found in register TXCON.

6.5 Clock recovery for receive mode

The clock-recovery for receive mode is dependent on the accuracy of the baud rate. If the absolute correct baud rate cannot be selected then the next available integer value should be chosen. The clock recovery is able to cope with a 1% tolerance to be able to operate correctly with standard XTAL cutting and temperature inaccuracies. The clock-recovery is implemented as a digital phase control loop with a fixed operating frequency (determined by the baud-rate generator setting). The mainscaler clock of the baud-rate generator acts as the reference clock for the clock-recovery PLL (128 times the actual chip-clock). The clock recovery PLL is programmable with regards to its settling speed. The settling of the clock-recovery speed can be set to reach its final state within 3, 7, 15 or 31 chips. If the clock-recovery is locked to the bit-stream the actual possible phase-error is proportional to the selected settling speed setting. (highest settling speed (settling within 3 chips) produces the smallest actual phase error due to fast regulation; slowest speed (settling within 31 chips), allows for the largest phase error due to the slowest regulation time constant.

Note that the decoding of NRZ signals with long constant bit-periods is directly influenced by the accuracy of the selected baud-rate. Proper coding can significantly improve sensitivity and the BER of NRZ decoding.

Integrated UHF Transceiver

7 Phase Locked Loop

A complete on-chip PLL is available in order to provide an RF carrier both in RX and TX mode. The PLL is realized as 4th order fractional-N PLL. The analogue part of the PLL is described in section 8.1, the digital part in section 8.2.
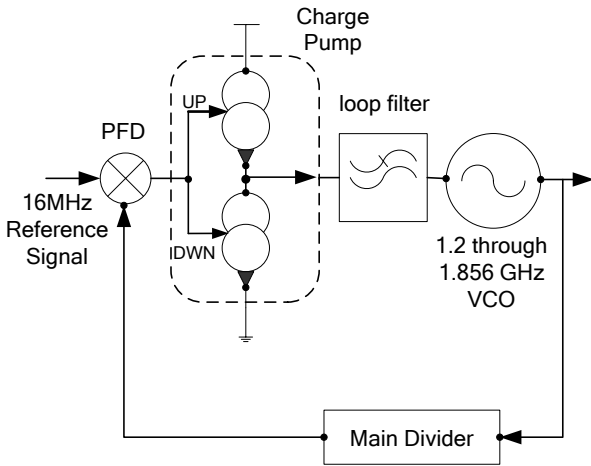
Figure 17. PLL block diagram

7.1 PLL Building Blocks

All PLL building blocks except VCO_BAND and the charge pump reference current (PLL_ICP settings) are automatically configured and operated by selecting the corresponding device modes. The following paragraphs describe the function of the internal control signals. These control signals can be influenced, if desired, by operating control-bits located in the EXPERT and TEST registers.

7.1.1 PLL and VCO regulators

In order to operate the whole PLL both regulators have to be switched on. See section 0.

7.1.2 General PLL operation

The following blocks are enabled after switching on the regulators, if the entire PLL is to be operational: VCO (VCO_ON), phase-detector (PFD_ON) prescaler (PRESC_ON) and reference clock buffer (CLK_PLL_ON). Dependent of the selected mode of operation (Rx or Tx mode, selected via device mode or command) also eventually RX_ON has to be set. If this bit is set to 1, the RX LO dividers are activated.

7.1.3 Charge pump

This block delivers the charge to the loop filter. The polarity and amount of the charge are proportional to the phase error reported by the phase detector.

The peak current of this charge pump is automatically adjusted. It can be overridden through the PLL_ICP control bits located in the EXPERT0 register. The charge pump peak current is a function of the icp control bits:

$$icp[0]*15\mu A + icp[1]*30\mu A + icp[2]*60\mu A + icp[3]*120\mu A + icp[4]*240\mu A$$

This means that a value from 15µA up to 465µA can be selected. The purpose of this programmability is to compensate for other blocks' gain variation (especially RF VCO) in order to keep a constant PLL loop bandwidth.

7.1.4 RF VCO

The very low phase-noise on-chip RF oscillator is based on an LC oscillator.

A capacitor bank is integrated in order to centre the resonant frequency of the LC-tank on the desired RF frequency. The VCO auto-calibration routine automatically trims the VCO to the correct sub-band. Whenever a different frequency setting is used for Tx or Rx operation the VCO auto-calibration is carried out automatically. Automatic trimming can be blocked by setting the bit SKIP_VCO_CAL in the LOCON register except during the PLL start-up. The trimming (sub-band selection) can be manually modified by the VCO_SUBBAND control-bits located in the VCOCON register. Frequency sub-band setting 0 corresponds to the maximum frequency, and 3Fh to the minimum frequency.

Note that this RF VCO is running at twice (868 and 928MHz band) or four times (313 and 434MHz bands) the chosen frequency bands.

Setting the VCO_BAND bit selects the appropriate operating mode for the VCO. For RF frequency bands below 400MHz, this bit has to be set to 1. For all other bands it should be set to 0.

7.1.5 PLL loop bandwidth setting

It is recommended that the PLL loop bandwidth should set to just above 150kHz (-3dB closed loop bandwidth) as this gives the best trade off between noise behavior and locking time. The loop bandwidth can be set by the PLL_ICP, recommended value for ICP=2.

7.2 Delta-Sigma modulator for fractional-N synthesis

The operating frequency is set by the content of the frequency control registers FC0 to FC3, which each have a width of 20 bits. The selection of the 'active' frequency control register is done directly with the transmit or receive command.

Integrated UHF Transceiver
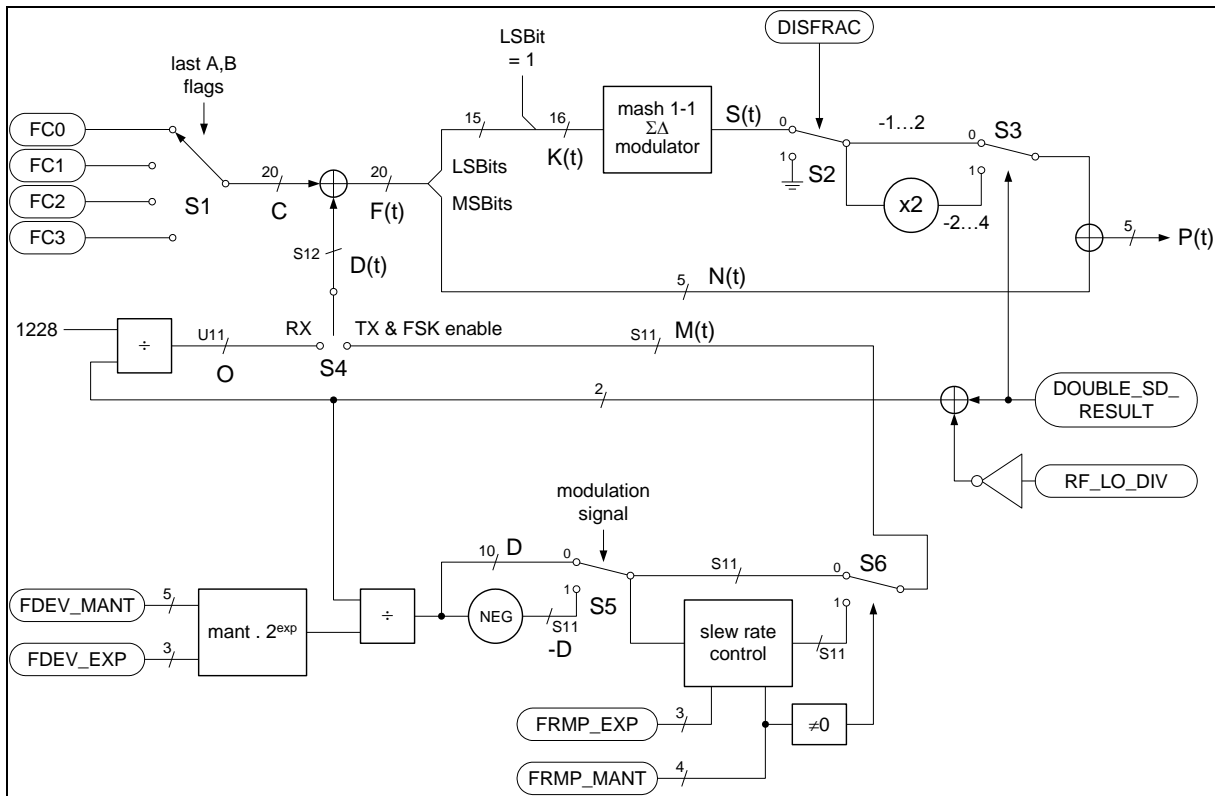
Figure 18: Computing the frequency divider control word

7.2.1 PLL operation frequency f0

From the diagram above, the integer (Nt) is forwarded directly to the adder which produces the relevant control word (Pt) for the PLL. The remaining fractional values cannot be handled by the frequency divider directly and are therefore converted into a pseudo-random sequence of integers. This conversion is implemented by the sigma-delta modulator. It produces numbers in the range from –1 to 2, whose average over time equals the given fractional part.

The spectral purity of the resulting RF signal is highly dependent on the randomness of the sequence generated by the fractional part. If this contained short repetitive patterns you could observe unwanted spurious in the RF spectrum. In order to guarantee that the produced sequences are always of maximal length, we append a constant 1 bit to the given fractional part, which resolves the issue. The weight of this 16th bit is $1/2^{16} = 1/65536$, which is very low. It creates a tiny frequency offset, which can be taken into account when calculating the centre frequency control value FCx for a given centre frequency.

When the fractional part approaches 0 or 1 the low-frequency noise components in the pseudo-random sequence become more dominant and can no longer be sufficiently suppressed by the transfer function of the PLL. The visible effect is then an increase of the phase noise in

the RF output near the carrier. To counteract this effect, the OL2381 has the DOUBLE_SD_RESULT bit (double sigma delta result). If this bit is set the fractional contribution to the PLL control word is doubled. So when increasing the frequency control value F(t) linearly, each RF output frequency is now produced twice; once with a fractional value that is closer to zero or one (between 0 and ¼ or between ¾ and 1) and a second time with a fractional value which is closer to the mid value ½ (between ¼ and ¾). The latter value produces a good pseudo-random sequence.

The fractional part of the frequency control value is processed differently depending on the DOUBLE_SD_RESULT bit, and the center frequency changes accordingly. Therefore the formulas, which convert between a given FC value and the RF center frequency, change with the state of the DOUBLE_SD_RESULT bit.

In normal mode the expression is straightforward.

$$f_{RF} = f_{ref} \cdot \left(64 + 2 \cdot \frac{2 \cdot FCx + 1}{65536} \right) \cdot \frac{1}{2 + 2 \cdot RF\_LO\_DIV} \quad (1)$$

- At the left side of the expression there is the reference frequency. The output frequency varies proportional with the reference.
- The parenthesised expression (64 + 2*…) is the characteristics of the frequency divider in the PLL.

29

Integrated UHF Transceiver

- The right term in the parenthesised expression accounts for the number interpretation of C and F(t) and the constant 1 LSBit, which has been added to guaranteed maximum length sequences from the sigma-delta modulator.
- The fraction at the right is the output division ration, which is either ½ or ¼, depending on the setting of the RF_LO_DIV bit.

After simplifying the expression a bit further we get

$$f_{RF} = f_{ref} \cdot \left(32 + \frac{2.FCx + 1}{65536} \right) \cdot \frac{1}{1 + RF\_LO\_DIV}$$

(2)

For the inverse we solve the above expression for FCx and then we round the result to the nearest integer number.

$$FCx = round\left(\left(\frac{f_{RF}}{f_{ref}} . (1 + RF\_LO\_DIV) - 32 \right) . 32768 - 0.5 \right)$$

(3)

Using the floor function this becomes

$$FCx = \left\lfloor \left(\frac{f_{RF}}{f_{ref}} . (1 + RF\_LO\_DIV) - 32 \right) . 32768 \right\rfloor$$

(4)

If the bit DOUBLE_SD_RESULT is set, the integer part and the fractional part of the centre frequency setting must be considered separately. In this case the expression for the output frequency is

$$f_{RF} = f_{ref} \cdot \left(64 + 2.\left(FCx[19:15] + 2.\frac{2.FCx[14:0]+1}{65536} \right) \right) \cdot \frac{1}{2 + 2.RF\_LO\_DIV}$$

You can see that in the inner parenthesised expression the integer part has been taken as is, where the term, which contains the fractional part, has got an additional factor of 2. After cancelling certain factors of 2 we get

$$f_{RF} = f_{ref} \cdot \left(32 + FCx[19:15] + \frac{2.FCx[14:0]+1}{32768} \right) \cdot \frac{1}{1 + RF\_LO\_DIV}$$

(5)

The inverse of this function is a bit trickier, because the function for the output frequency is not monotonous. But we know that each output frequency is exactly produced

twice and we know also that we want the solution where the average of the sigma-delta output S(t) is closest to ½. Let us convert Equation 5 such that the integer part of the frequency control value has no factor and the term containing the fractional part of the frequency control value becomes isolated on one side of the equation.

$$\frac{f_{RF}}{f_{ref}} . (1 + RF\_LO\_DIV) - 32 - FCx[19:15] = \frac{2.FCx[14:0]+1}{32768} = 2.fract$$

Now we ask for the integer part for which the fractional part becomes a value in the range from ¼ to ¾, which is equivalent that twice the fractional part lies in the between ½ and 1½.

$$\frac{f_{RF}}{f_{ref}} . (1 + RF\_LO\_DIV) - 32 - FCx[19:15] \geq 0.5$$

$$\frac{f_{RF}}{f_{ref}} . (1 + RF\_LO\_DIV) - 32 - FCx[19:15] < 1.5$$

Now we can isolate the integer part from both inequalities such that the right sides are the same.

$$FCx[19:15] \leq \frac{f_{RF}}{f_{ref}} . (1 + RF\_LO\_DIV) - 32 - 0.5$$

$$FCx[19:15] + 1 > \frac{f_{RF}}{f_{ref}} . (1 + RF\_LO\_DIV) - 32 - 0.5$$

And then, knowing that   stands for the two inequalities and   , we can combine both inequalities to a single expression for the integer part.

$$FCx[19:15] = \left\lfloor \frac{f_{RF}}{f_{ref}} . (1 + RF\_LO\_DIV) - 32.5 \right\rfloor$$

(6)

Now we can enter the integer part, which we have just found, into Equation 5 and then we can solve for the fractional part. We get the result for the settings after rounding it to the nearest integer number.

$$FCx[14:0] = round\left(\left(\frac{f_{RF}}{f_{ref}} . (1 + RF\_LO\_DIV) - 32 - FCx[19:15] \right).16384 - 0.5 \right)$$

30

Integrated UHF Transceiver

When using the floor function this becomes

$$FCx[14:0] = \left\lfloor \left(\frac{f_{RF}}{f_{ref}} \cdot (1 + RF\_LO\_DIV) - 32 - FCx[19:15] \right) \cdot 16384 \right\rfloor$$
(7)

From equations 1 and 5 we can also see which frequency resolution can be achieved in which mode. If DOUBLE_SD_RESULT is set to 0, we get

$$f_{RF,res}(0) = f_{ref} \cdot 2 \cdot \frac{2}{65536} \cdot \frac{1}{2 + 2.RF\_LO\_DIV} = \frac{f_{ref}}{32768} \cdot \frac{1}{1 + RF\_LO\_DIV}$$
(8)

If DOUBLE_SD_RESULT is set to 1, the resolution becomes

$$f_{RF,res}(1) = f_{ref} \cdot 2 \cdot 2 \cdot \frac{2}{65536} \cdot \frac{1}{2 + 2.RF\_LO\_DIV} = \frac{f_{ref}}{16384} \cdot \frac{1}{1 + RF\_LO\_DIV}$$

Taking the bit DOUBLE_SD_RESULT into the formula, the above two equations can be combined into.

$$f_{RF,res} = \frac{f_{ref}}{32768} \cdot \frac{1 + DOUBLE\_SD\_RESULT}{1 + RF\_LO\_DIV}$$

7.2.2 RX frequency offset

Because the OL2381 receiver implements a super-heterodyne architecture with an intermediate frequency at 300 kHz. The local oscillator is automatically tuned to 300 kHz above the wanted receive centre frequency in receive mode.

This is accomplished by adding an offset value O to the centre frequency setting C (please refer to Figure 18: Computing the frequency divider control word

). This offset value is automatically adjusted such that it matches the LO frequency resolution, which changes with the RF_LO_DIV and DOUBLE_SD_RESULT settings.

The following table shows that the resulting RX frequency offset is independent from the RF_LO_DIV and DOUBLE_SD_RESULT settings. It is always 195 Hz below the nominal IF of 300 kHz, which is accurate enough in all cases.

7.3 PLL LOCK detection

A lock detection circuit is implemented in order to support the shortest PLL power-on time. The lock-detection circuit monitors phase and frequency difference of the PLL and the reference clock. If the phase-difference of the two clock signals is settled within a defined window an internal LOCK_DETECT signal is triggered. After a specified time LOCK_DET_TIME (EXPERT1 register) the status bit LO_RDY is set in the DEVSTATUS register. Since the lock detect circuit consumes additional power, it is only enabled during the start-up phase of the PLL and whenever a different sub-band setting is applied. The lock detect circuit can be manually controlled by the bit LOCK_DET_ON in the LOCON register.

7.4 VCO Auto Calibration

The VCO calibration is performed every time the centre frequency of the VCO is changed. The following internal sequences are started:

Start VCO calibration and turn on PLL lock detection. The output of the lock detection must be gated low as long as the calibration is running.

With the next clock cycle: Turn on phase frequency detector (PFD_ON), prescaler (PRESC_ON), clock for PLL (CLK_PLL_ON) and PLL lock detection

Perform VCO calibration (select best possible sub-band for desired frequency setting)

Check PLL lock detection + lock detect time.

31

Integrated UHF Transceiver

8 Tx Operation

8.1 Transmit Mode

8.1.1 Preparation for Transmit Mode

Transmit mode is initiated by setting the device mode bits DEV_MODE to 11b or by sending a transmit command. The necessary VCO, PLL and PA start-up is accomplished by the internal state machine. Bit TX_RDY in the special function register DEVSTATUS signals completion of the start-up sequence.

8.2 Transmit Command

The power amplifier is activated with the first active edge of the ninth bit of the transmit command. Therefore, the active edge for the power amplifier start-up differs from the active edge of the remaining SPI communication. This must be considered for the data set-up time of the transmitted bit.

Predefined configurations (description of the configuration bits, see below.) can be chosen for the transmit-sequence.

TA	TB	TC	TD	TE	TF
Transmitter frequency selection bits		Data and power amplifier synchronisation bit	Power amplifier control bit	Manch. generation bit	Amplitude selection bit

Table 3 Transmit Command Bits

D0	D1	D2	D3	D4	D5	D6	D7
1	1	TA	TB	TC	TD	TE	TF

Table 4 Transmit Command Packet

Bit TC	Bit TE	Effect	Note
0	0	Transmitted data is unsynchronised (only synchronisation to CLK_{REF}).	
1	0	Transmitted data is synchronised with the baud rate clock (CLK_{TX})	
X	1	Transmitted data is synchronised and XORed with the baud rate clock (CLK_{TX}), hence Manchester generation is applied.	1

Table 5 Control of transmitted data (bits TC, TE)

Bit TC	Bit TD	Effect
X	0	Power amplifier stays on after falling edge of SEN.
0	1	Power amplifier is turned off with the falling edge of SEN (PA off-ramping supported).
1	1	Power amplifier is turned off synchronously with the baud rate clock (CLK_{TX}) after the falling edge of SEN (PA off-ramping supported).

Table 6 Power amplifier control and synchronisation (bits TC, TD)

TC	TD	TE	Function
0	0	0	Unsynchronised TX Data and PA stays on.
0	0	1	Manchester Coded Data and PA stays on.
0	1	0	Unsynchronised TX Data and falling edge of SEN turns off PA.
0	1	1	Manchester Coded Data and falling edge of SEN turns off PA.
1	0	0	Synchronised TX Data and PA stays on.
1	0	1	Manchester Coded Data and PA stays on.
1	1	0	Synchronised TX Data and PA turns off synchronously (CLK_{TX}) after the falling edge of SEN.
1	1	1	Manchester Coded Data and PA turns off synchronously (CLK_{TX}) after the falling edge of SEN.

Table 7 Summary of combined TC, TD and TE bits.

BitTF	Effect
0	Modulation and amplitude/power settings are applied according to register ACON0.
1	Modulation and amplitude/power settings are applied according to register ACON1.

Table 8 Amplitude selection (bit TF)

Bit TA	Bit TB	Selected frequency band
0	0	FC0L, FC0M, FC0H
0	1	FC1L, FC1M, FC1H
1	0	FC2L, FC2M, FC2H
1	1	FC3L, FC3M, FC3H

Table 9 Frequency band selection (bits TA, TB)

Note:

1) If bit TE = 1, the value of bit TC is ignored and data is always synchronised with the baud rate clock. However, bit TC has an effect if bit TD = 1. Therefore, bit TC must be properly set even if TE = 1.

32

Integrated UHF Transceiver

Transmission command
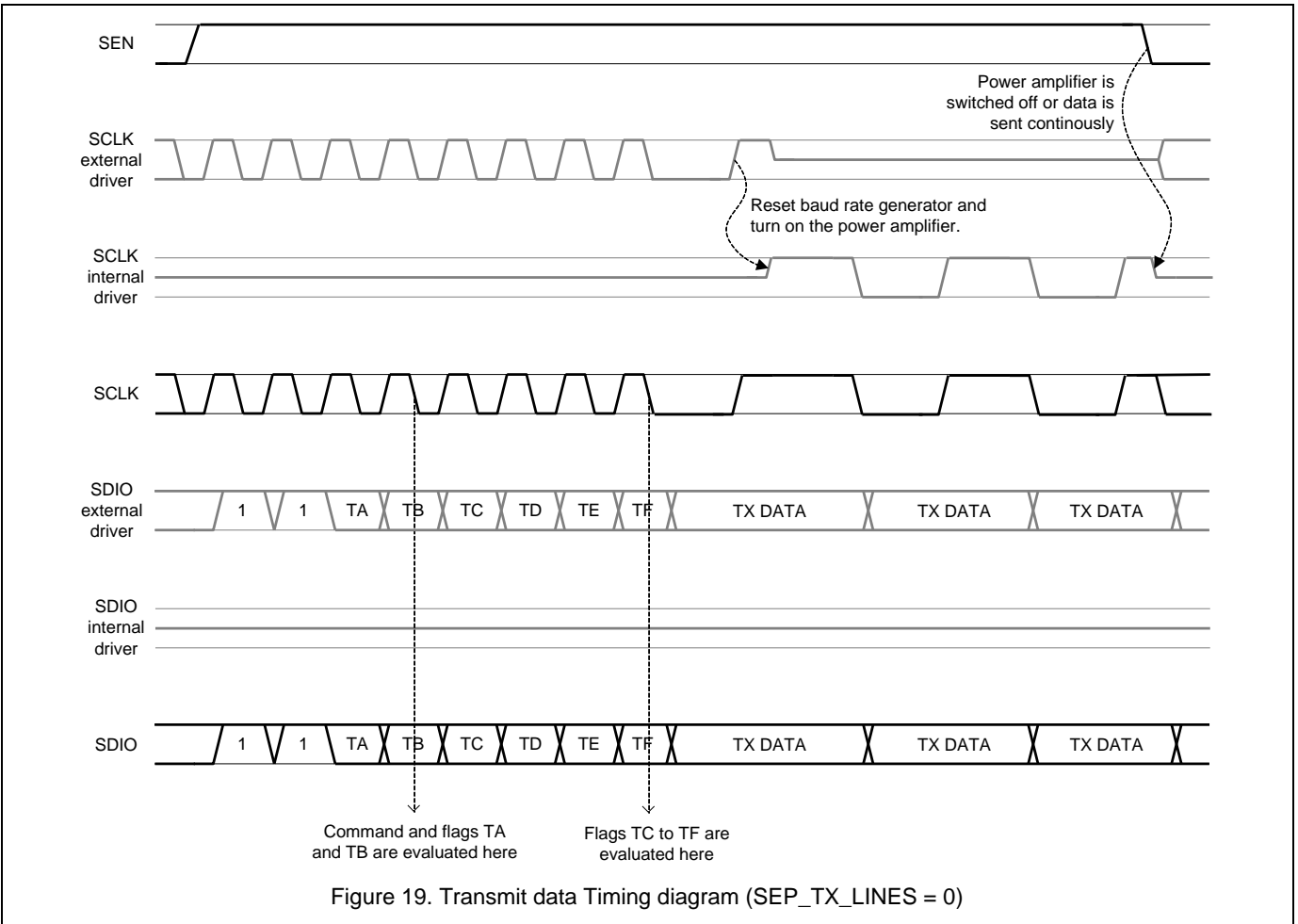
SEN

Power amplifier is
switched off or data is
sent continously

SCLK
external
driver

Reset baud rate generator and
turn on the power amplifier.

SCLK
internal
driver

SCLK

SDIO
external
driver

| 1 | 1 | TA | TB | TC | TD | TE | TF | TX DATA | TX DATA | TX DATA |

SDIO
internal
driver

SDIO

| 1 | 1 | TA | TB | TC | TD | TE | TF | TX DATA | TX DATA | TX DATA |

Command and flags TA
and TB are evaluated here

Flags TC to TF are
evaluated here

Figure 19. Transmit data Timing diagram (SEP_TX_LINES = 0)

TA to TF contains configuration information for the transmit-operation.

Integrated UHF Transceiver
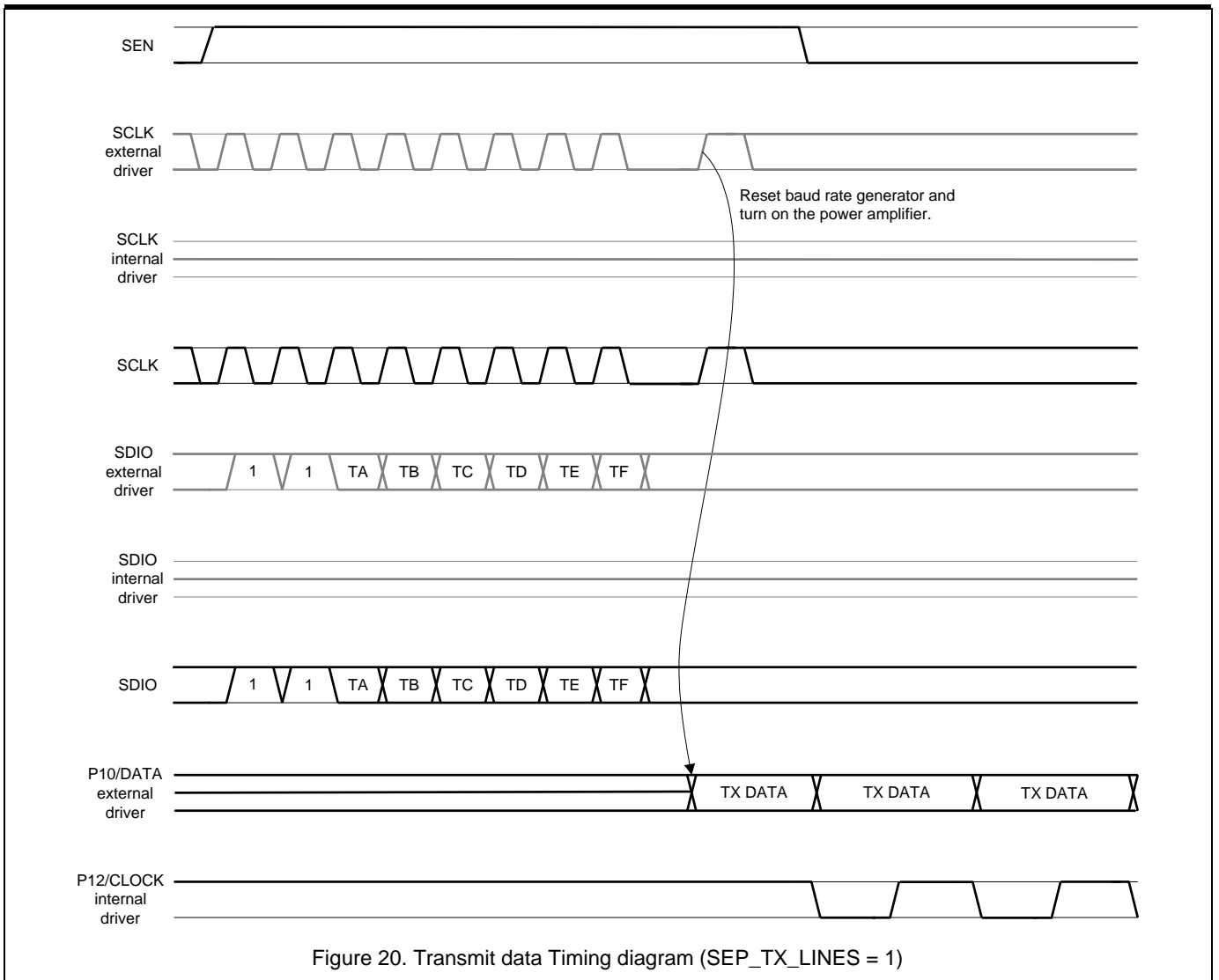
Figure 20. Transmit data Timing diagram (SEP_TX_LINES = 1)

TA to TF contains configuration information for the transmit-operation.

Integrated UHF Transceiver

Example of synchronized data transmission

Phase 1: Data transmission

D0	D1	D2	D3	D4	D5	D6	D7
1	1	0	0	1	0	1	0
		Selection of frequency configuration register FC0		Synch. of TX-data with the positive edge of the transmitter clock CLK_{TX}.	PA stays on after falling edge of SEN. TX data is stored and continuously sent.	Manchester code generation is selected.	Modulation and amplitude / power settings of ACON0 are applied.

Phase 2: End of data transmission

D0	D1	D2	D3	D4	D5	D6	D7
1	1	0	0	1	1	1	0
		Selection of frequency configuration register FC0		Synch. of TX-data with the positive edge of the transmitter clock CLK_{TX}.	PA is turned off in synch. with TX clock CLK_{TX} after the falling edge of SEN.	Manchester code generation is selected.	Modulation and amplitude / power settings of ACON0 are applied.
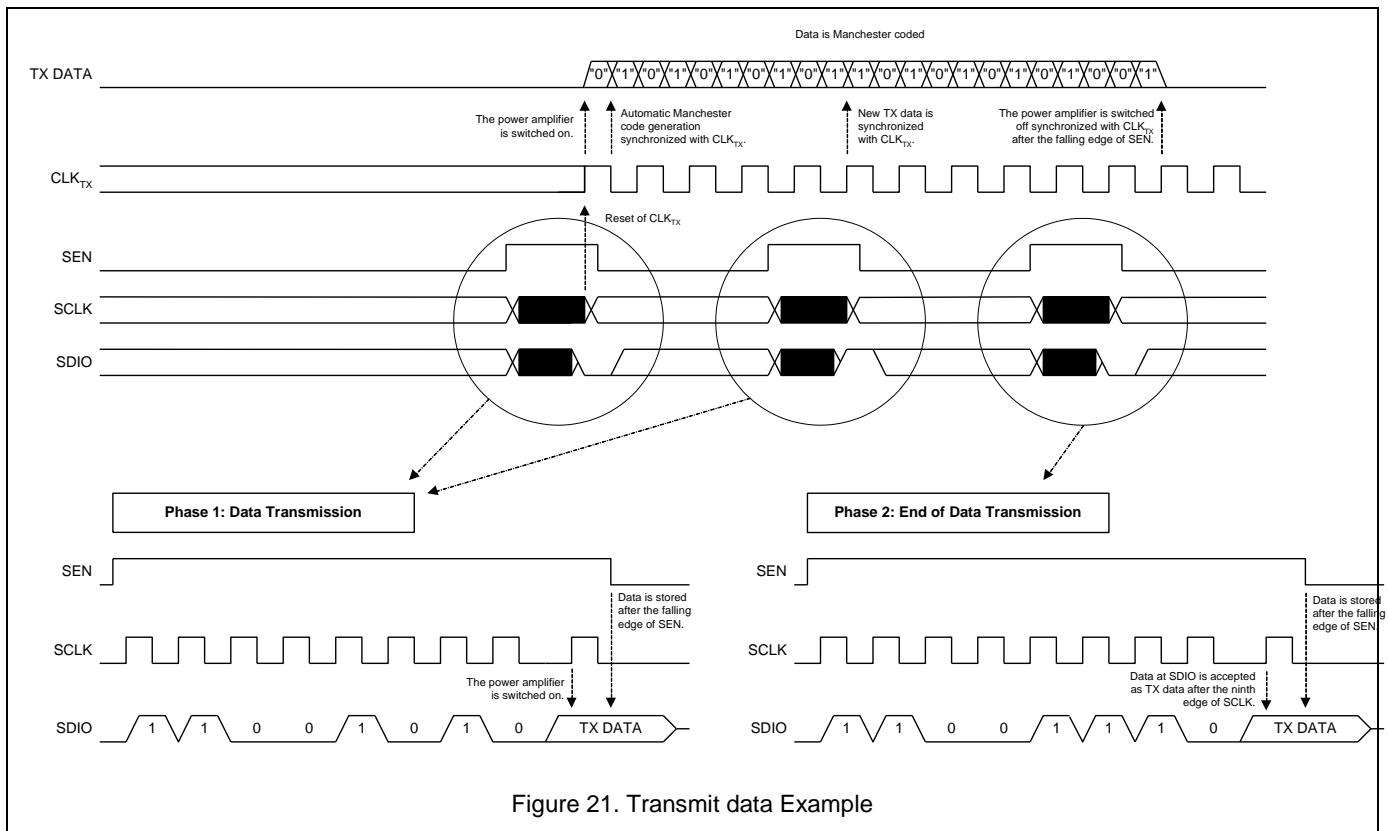
Figure 21. Transmit data Example

35

Integrated UHF Transceiver

8.2.1 Clock Output Selection for the Transmit Command

The clock output at port pin SCLK or P12/CLOCK respectively, can be selected with the special function bits TXCLKOUTSEL. With this mechanism it is possible to provide a faster clock than the actual transmitter clock CLK_{TX}.

If no clock is selected, hence TXCLKOUTSEL = 11b, the device behaves as follows:

- SEP_TX_LINES = 0: The output driver of SCLK is never activated.

- SEP_TX_LINES = 1: The line P12/CLOCK drives a constant high level.

8.3 Power Amplifier

The power amplifier is driven from the PLL synthesizer and operates in single ended fashion.

The power amplifier consists of six binary weighted output stages which are connected in parallel and are operated according to the amplifier control register settings ACON0, ACON1 and ACON2. Though the supply-voltage of the PA is configurable to 3 different voltage settings, it is advised to use only the PAM 0 setting for the majority of applications.

The device features several control bits controlling the output amplitude and ASK modulation characteristics of the power amplifier. The control registers ACON0-ACON2 control the power amplifier stage, for either amplitude fine-tuning or ASK modulation means. ASK0 located in ACON0 and ASK1 located in ACON1 determine ASK or FSK operation.

The lower 5 bits of the control registers ACON0, ACON1 and ACON2 allow to set two different high levels (AMH0 and AMH1) and one low level (AML), respectively, which define the modulation depth during amplitude modulation of the UHF carrier. Which of the two available AMHx registers will be actually used is selected with the flag bit TF of the Transmit command. Amplitude modulation is achieved by switching between the selected high low levels in accordance with the internal signal AMOUT, which is derived from the TX data stream.
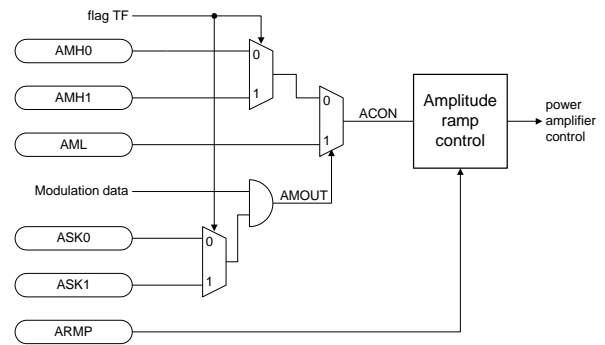
Figure 22. Power Amplifier Control
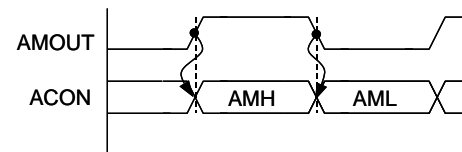
Figure 23. ASK Modulation Timing

8.4 Soft ASK, Ramp Control

To achieve a more narrow spectral occupation of the ASK signal Gaussian ASK like modulation is implemented. The time constant defined in the ARMP register defines the up and down ramping time-constant of the ASK signal. This feature is also used for switching on the carrier in FSK applications to achieve best possible electro magnetic radiation values.

The ARMP register sets the number of 16MHz clock cycles to be used to ramp the ASK amplitude from the lower AML value to the higher AMH value and vice versa. The number of clocks is calculated as follows:

Number of Clocks = ARMP_MANT * 2 $^{ARMP\_EXP}$

If ARMP_MANT is zero, then no amplitude ramping is done.
Inverse function:

$$ARMP\_EXP = max\left(0, \left\lfloor \log_2\left(\frac{ARMP}{15.75}\right)\right\rfloor\right)$$

$$ARMP\_MANT = \left\lfloor 0.5 + \frac{ARMP}{2^{ARMP\_EXP}} \right\rfloor$$

For power-on / power-off ramping the value is changed between zero and the current AMH or AML value.

The total duration of the ramp is ARMP * (|AMH-AML|-1) / fref, where ARMP = 2^ARMP_EXP * ARMP_MANT.

The supply-voltage of the PA is configurable to 3 different voltage settings to achieve the best possible power

36

Integrated UHF Transceiver

resolution for low power, medium power and high power applications. The actual stabilized voltage of the PA regulator can be selected with the PAM bits located in the TXCON register. The only recommended PAM setting is PAM 0 (D1=0, D0=0), with Class E matching (please see application note.

8.5 PLL frequency deviation (FSK)

8.5.1 Frequency modulation

FSK and GFSK-like modulation is accomplished by adding a time varying sequence to the centre frequency control value. This variation in the total frequency control value is slow enough to pass the transfer function of the PLL and the resulting RF is modulated in frequency. Please refer to the PLL section for a detailed description of operation.

The FSK path starts by computing the frequency deviation value D from the given FDEV_EXP and FDEV_MANT values.

The RF_LO_DIV and DOUBLE_SD_RESULT bits have been included in this expression in order to compensate for the influence of these bits on the frequency resolution. If the argument of the floor function is an integer, which is the case for all but 72 of the 1024 possible combinations of the settings, then the result of the floor function equals its argument. In these cases the resulting frequency deviation is independent from the RF_LO_DIV and DOUBLE_SD_RESULT bits.

$$f_{dev} = 2^{FDEV\_EXP}.\,FDEV\_MANT\,.\,\frac{1}{2}.\frac{1+RLD}{1+DSR}.\frac{f_{ref}}{32768}.\frac{1+DSR}{1+RLD}$$

Note: in the above formula DSR and RLD stand for the bits DOUBLE_SD_RESULT and RF_LO_DIV, respectively. After cancelling out the dependency from these bits we get the following simple result.

$$\boxed{f_{dev} = \frac{2^{FDEV\_EXP}.\,FDEV\_MANT}{65536}\,.\,f_{ref}}$$

If the argument of the floor function is not an integer, the result should be multiplied with the current frequency resolution, which is equivalent to rounding the result from equation above down to the next available frequency step.

The modulation signal controls the RF output such that a 0 produces +D (the high frequency, $f_{RF} = f_{center} + f_{dev}$) and 1 selects –D (the low frequency, $f_{RF} = f_{center} - f_{dev}$). If FRMP_MANT is zero the resulting squarewave shaped sequence is the modulating sequence M(t).

8.5.2 Soft-FSK

In order to achieve a narrower signal bandwidth of the FSK spectrum a GFSK like modulation scheme is implemented. The GFSK shape is modelled by a linear interpolation approach. The FSK frequency shifting is done in a linear way between $F_{RF} - F_{DEV}$ and $F_{RF} + F_{DEV}$. The linear ramp is implemented by stepping the frequency control value between +D and –D at a step rate sr, using a step increment of si. Both variables are controlled with the settings FRMP_EXP and FRAMP_MANT according to the following two expressions.

$$sr = \frac{f_{ref}}{2^{\min(0,FRMP\_EXP-4)}.\,FRMP\_MANT}$$

increments/s

$$si = 2^{\min(0,4-FRMP\_EXP)}\ steps$$

When FRMP_EXP has the value 4, the scaling factor for the step rate is 1 and so is the step increment si. When FRMP_EXP is greater than 4, the step rate is decreased in powers of two and the step increment is kept at 1. Likewise, when FRMP_EXP is smaller than 4 the step increment is increased in powers of two and the step rate scaling factor is kept at 1. These two dependencies taken together result in a continuous scaling of the slew rate of the ramp.

When we multiply these two expressions together, we get the slew rate of the ramp in steps/s.

$$slew\,rate = f_{ref}\,.\,\frac{2^{\min(0,4-FRMP\_EXP)}}{2^{\min(0,FRMP\_EXP-4)}.\,FRMP\_MANT}$$

$$slew\,rate = f_{ref}\,.\,\frac{2^{\min(0,4-FRMP\_EXP)-\min(0,FRMP\_EXP-4)}}{FRMP\_MANT}$$

In order to find out what the slew rate of the Soft FSK ramp is in terms of Hz/s, we have to multiply the expression the equation above with the frequency resolution, as follows.

$$slew\,rate = f_{ref}\,.\,\frac{2^{4-FRMP\_EXP}}{FRMP\_MANT}.\frac{f_{ref}}{32768}.\frac{1+DOUBLE\_SD\_RESULT}{1+RF\_LO\_DIV}$$

$$\boxed{slew\,rate = \frac{f_{ref}^{\,2}}{2048\,.\,FRMP\_MANT\,.\,2^{FRMP\_EXP}}.\frac{1+DOUBLE\_SD\_RESULT}{1+RF\_LO\_DIV}}$$

Integrated UHF Transceiver

If we want to get the FRMP settings from a given slew rate, we need the inverse function.

$$FRMP\_MANT.2^{FRMP\_EXP} = \frac{f_{ref}^2}{2048 \cdot slewrate} \cdot \frac{1 + DOUBLE\_SD\_RESULT}{1 + RF\_LO\_DIV}$$

8.6 Oscillator and divider settings

In order to allow operation for all ISM bands different oscillator divider and PLL divider settings can be selected. The configuration information is located in the LOCON register.

The bit RF_LO_DIV controls the output frequency divider of the local oscillator. If this bit is 0, the divider divides the VCO frequency by 2 in which case the LO produces RF frequencies above 500 MHz; if the bit is 1, the divider divides by 4 in which case the LO produces frequencies below 500 MHz.

8.7 Modulation Data Generation

Either SDIO or P10/DATA act as the data input depending on the setting of SEP_TX_LINES. Input data is synchronised to the reference clock CLK_{REF}. This flip-flop serves also as storage for the input data. Input data is sampled under the following conditions:

- SEP_TX_LINES = 0: Input data sampling starts with the ninth bit of the transmit command and stops when the command finishes, hence, SEN goes to low level. The last input state is stored.

- SEP_TX_LINES = 1: Input data sampling starts with the ninth bit of the transmit command that turns on the power amplifier and stops when the power amplifier is turned off again. Intermediate SPI read, write or transmit commands which do not alter the state of the power amplifier will not influence data sampling.

The sampled input data is either provided transparently, synchronised to the baud rate or Manchester coded, depending on the current transmitter flags TC and TE. Baud rate synchronisation and Manchester code generation runs with the transmitter clock CLK_{TX}. Data is updated with every positive clock edge of CLK_{TX} and, if Manchester coding is selected, it is inverted with the negative clock edge of CLK_{TX}.

The data stream can be optionally inverted by setting bit INV_TX_DATA. This inversion is located after the storage elements. If the stored data is constant, it is possible to alter modulation data just by an SPI write access to INV_TX_DATA.

8.8 Transmitter operating mode

8.8.1 Power-Down

In this mode the device has very low current consumption. Also, the registers will not change, all transmitting, receiving, clock generating, and amplifying blocks will be switched off.

When the power-down state is left (by rising edge of EN) the PD bit is cleared.

8.8.2 Idle-Mode

In this mode the device is powered up. The crystal oscillator or the external clock buffer is enabled and after the stabilization of the crystal oscillator (if selected) the device is supplied with the reference clock.

8.8.3 Active-Mode

Active mode is entered when the device mode bits are set to anything other than '00'. The digital regulator and XTAL are always activated. If active mode 01 is chosen the VCO and the PLL are also started. If SPI state is entered, communication between a microcontroller and the registers is enabled via the SPI interface. The Active state can be left by programming a register indicating another state or by setting EN low for more than 4ms.

8.8.3.1 PLL-Active Mode

8.8.3.2 Transmit

The transmit-mode is entered on reception of a valid Transmit command, providing the PLL is settled. Depending on the content of the transmit command, exit of transmit mode either directly when is EN set low, or in a synchronized way with the edge of the last data-bit when EN is set low or upon direct SPI register setting. The power amplifier is turned on with the first active edge of the ninth bit of the transmit command. Therefore, the active edge for the power amplifier start-up differs from the active edge of the remaining SPI communication. This must be considered for the data set-up time of the transmitted bit. Any SPI clock following the ninth bit shall be ignored by the SPI interface. If during a transmit-sequence a POR or power fail condition occurs, the XTAL-Active mode is entered. More information can be found in section 8.2.

8.8.4 Baud rate generation

The baud-rate for the Tx data is generated by the baud-rate generator. This baud-rate generator is used for Tx and Rx operation at the same time. For a detailed explanation see section 6.4.

8.8.5 Clock selection for Tx mode

Depending on the bit TXCLKSEL in the register TXCON different clock sources can be selected. TXCLKSEL = 1

Integrated UHF Transceiver

selects the bit-clock of the baud-rate generator, TXCLKSEL = 0 selects the chip-clock. If Manchester Modulation is desired, the bit clock is selected. The bit INV_TX_DATA is used to invert the Tx data-stream.

Integrated UHF Transceiver

9 Rx Operation

9.1 Rx Signal diagram
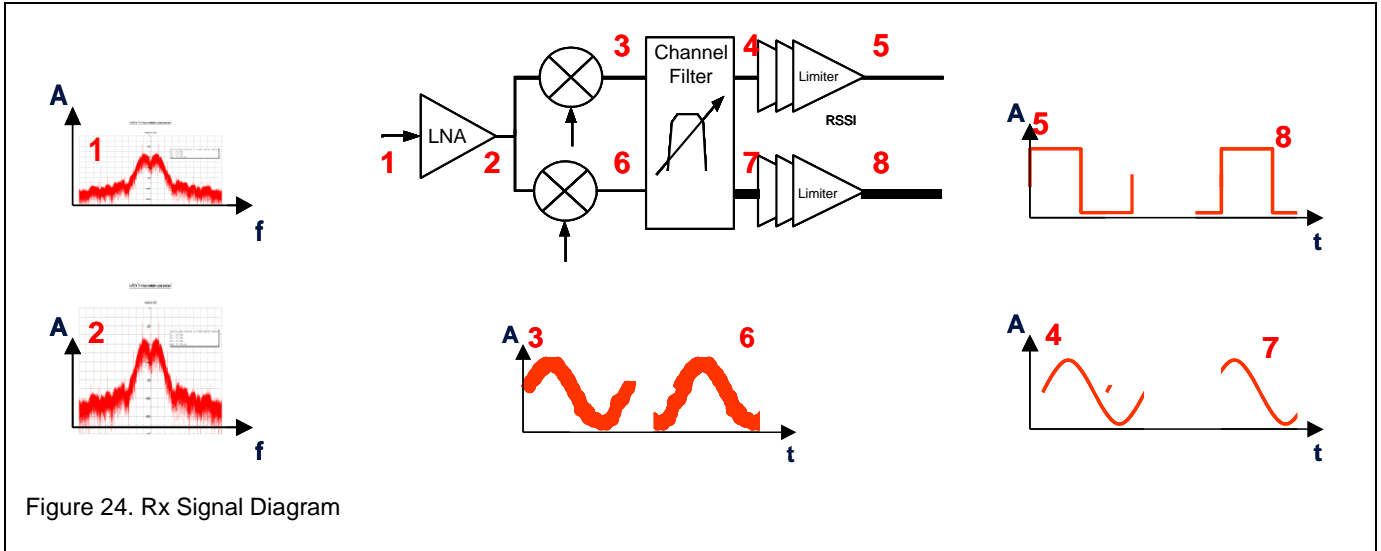
Figure 24. Rx Signal Diagram

The Figure 24. Rx Signal Diagram visualizes internal signal shapes inside the Rx block. Signal 1 represents the signal input spectrum (sketched in the frequency domain) The frequency spectrum is centred to the desired Rx frequency. Signal 2 represents the amplified spectrum of the input signal (Signal 1). Signal 2 is with the LO frequency (should be set to 300kHz above the Rx frequency) mixed down from the Rx input frequency with the I and the Q mixer to the IF (300kHz). Signal 3 and signal 6 represent the IF signals of the I and the Q channel (90deg phase difference) in the time domain. Signals 4 and 7 represent the I and Q signals after the channel filter. Signals 5 and 8 are the amplified and limited I and Q signals at the output of the limiter. It is possible to switch some of these internal analogue signals to the pins TEST1, TEST2 via the ANA_TEST_SEL-bits of register TEST1. The digital IQ-signals of the limiter output, along with other digital baseband signals can be accessed via the alternative port functions of P11C and P12C with the appropriate setting of the DIG_TEST_SEL-bits. Please see section 67 for further details.

9.2 General Operation

The Rx-Block consists of a fully analogue front-end including an analogue channel-filter. The mixer together with the channel filter demodulates only one sideband to the IF. The LO frequency (frequency of the RF VCO) has to be set 300kHz above the expected frequency of the Rx signal. The receiver mixes down the lower side-band of the

Rx signal. The gain settings of the LNA and the channel-filter are adjustable to achieve a high dynamic operating range. Field-strength detection, automatic gain-selection and AM demodulation are implemented via the RSSI information. The RSSI is derived from a limiter. Details of the automatic gain selection can be found in sections 9.6 LNA and Channel-filter gain settings.

Data demodulation is realized in the digital part of the Rx-chain. The circuit is capable of demodulating ASK and FSK signals. FSK demodulation is applied directly with the analogue IF signal coming from the channel filter. This signal is directly fed into the digital FM demodulator where it is processed further. ASK demodulation employs the RSSI signal. This signal is decoded in the digital part and then also further processed. The Data-slicer and clock-recovery mechanisms regenerate the bit-stream for both, ASK and FSK signals.

The OL2381 is able to cope with a 1% data rate tolerance to be able to operate correctly with standard XTAL cutting and temperature inaccuracies.

9.3 LNA

The feed from the single-ended antenna is converted to a differential signal at the input of the mixer. The intrinsic voltage gain (from Rx input pin to unloaded LNA) is adjustable to typically 4dB, 17dB, 23dB or 25.5dB. Two gain settings can be programmed in order to meet the dynamic range requirements of the receiver chain. In

40

Integrated UHF Transceiver

parallel to the LNA gain, the channel-filter gain can also be adjusted. The selection of the appropriate gain-setting (Hi-gain or Lo-gain) is executed automatically by the gain-control loop. The individual gain setting is programmed by the control-bits located in the RXGAIN register. See section 9.6.

9.4 Mixer

The Mixer is realized as an active I/Q mixer. It mixes down the amplified signal from the LNA to the IF frequency of 300kHz.

9.5 Channel filter

Channel filter gain and bandwidth can be selected independently with control bits. Auto-calibration features are implemented in order to achieve a well defined filter bandwidth. The Filter bandwidth itself can be configured by setting the CF_BW bits in the RXW register. The different adjustable bandwidth settings of the IF channel-filter can be found in the table below. The bandwidth of the channel-filter should be set as close as possible to the bandwidth occupied by the modulated Rx Signal in order to achieve the best noise-performance.

9.5.1 Channel filter auto-calibration

An auto-calibration of the channel-filter is implemented in order to achieve a well centred filter roll-off characteristic in the filter pass-band. This feature can compensate for process and temperature dependent parameter mismatches. Filter auto-calibration is performed automatically before every Rx operation.

The calibration can be blocked by setting the bit SKIP_CF_RC_CAL, and can be forced at any time by setting the bit FORCE_CF_RC_CAL.

Status information of the channel-filter calibration can be accessed by reading the CFRCCAL register. All bits inside the CFRCCAL register are read-only.

After channel-filter calibration is started the bit CF_RC_CAL_RUNNING can be probed. This bit is set to 1 when the RC calibration algorithm is running.

This status bit CF_RC_CAL_OK is set to one when a channel-filter calibration has been correctly performed. This indicates that the data of the CF_RC_CAL_RES control bits are valid.

These 4 bits, CF_RC_CAL_RES, indicate the result of the channel RC calibration. These bits are applied directly to the internal RC components of the channel-filter.

In order to manually influence the channel-filter auto-calibration a special register (TEST4) is available. Via the bits inside the TEST4 register the auto-calibration can be over-ridden. The control-bits CF_RC_ADJUSTCAL allow to cross-check the accuracy of the channel-filter auto-calibration routine.

Setting the bit SKIP_CF_RC_CAL by-passes the on-chip RC-calibration. Setting the bit FORCE_CF_RC_CAL triggers an RC auto-calibration. The corresponding RC calibration values (values achieved after auto-calibration inside the 4 bits CF_RC_CAL_RES, CFRCCAL register) have to be entered into the MAN_CF_RC_CALVAL bits.

The CF_RC_ADJUSTCAL control bits can be used to evaluate the on chip channel filter RC calibration block accuracy.

By changing the value of these two bits, the R part of the RC reference is trimmed. Knowing the adjusted R variation, we can verify that the output of the CF_RC_CAL_RES control bits is changing accordingly. In this way the complete RC measurement mechanism can be validated.

An I/Q calibration is implemented in order to achieve a high image frequency rejection. This calibration is intended to be used once during production of the final application PCB as part of an end-of-line test. It requires an external signal at the image frequency of the desired receive frequency to be applied to the Rx pin. The I/Q calibration routine automatically calculates the best I/Q trimming configuration for the optimum image rejection (>50dBc). This result has to be read and stored by the external microcontroller. The calibration value is valid for the whole frequency band over all supply voltages and temperatures.

The I/Q calibration should be performed as follows:

A signal at the image frequency of the receive frequency should be applied. The level of the signal has to be chosen in a way that the RSSI is still able to measure the damped image: e.g: -40dBm -> image would be at -90dBm, still sufficient RSSI operation margin.

The I/Q calibration is enabled by setting the bit START_CF_IQ_CAL in the CFIQCAL register. The status bit CF_IQ_CAL_RUNNING indicates an active calibration cycle. All possible I/Q offset combinations are run in a sequential way, at every combination an RSSI measurement is performed. The combination with the minimum RSSI reading is stored in the CF_IQ_CALVAL register. This information has to be stored by the external micro-controller. This register should be initialized every time with the stored values. If no IQ calibration is required, the CF_IQ_CALVAL bits should be set to 0.

Figure 25 shows the effect of I/Q calibration in a simulation result. With this calibration an image rejection of 50dB is achievable.

41

Integrated UHF Transceiver
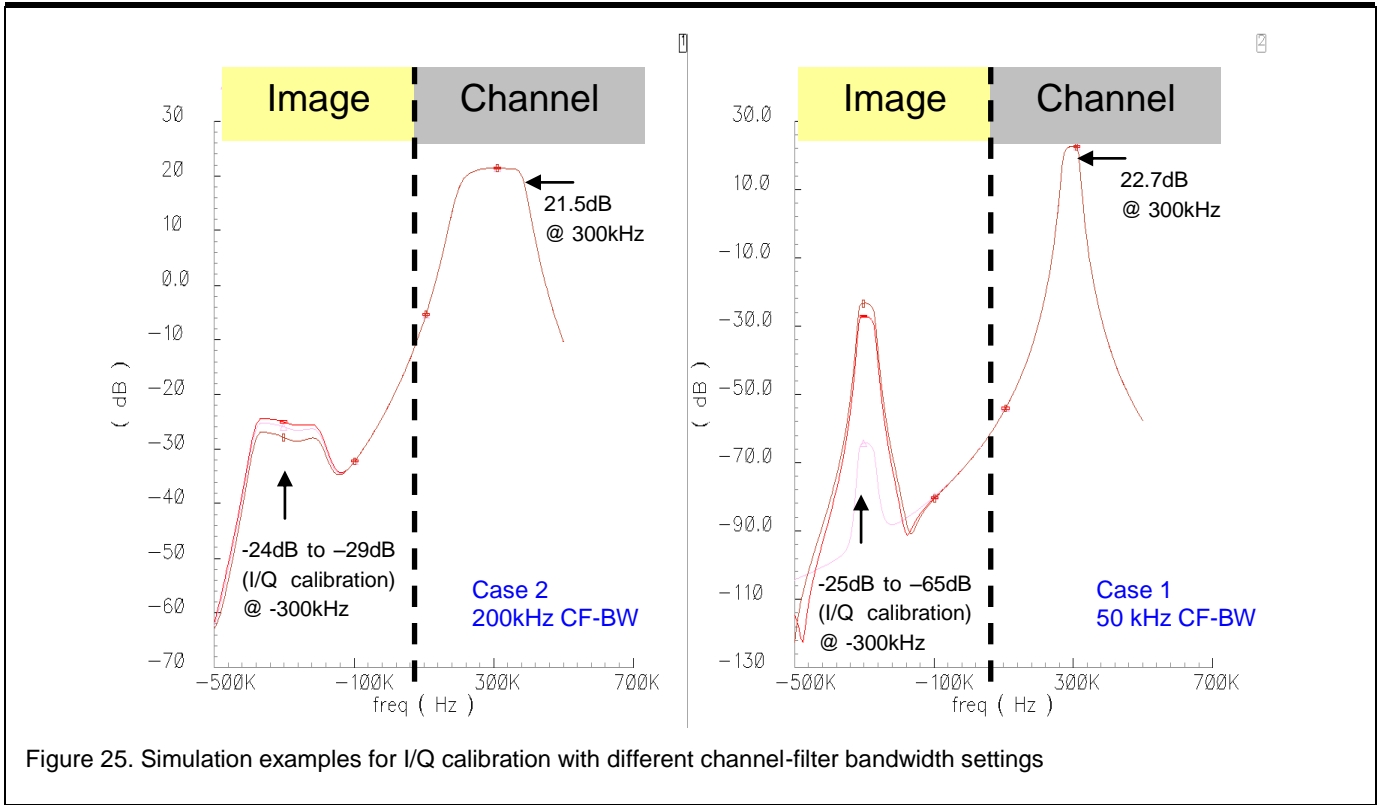
Figure 25. Simulation examples for I/Q calibration with different channel-filter bandwidth settings

9.6 LNA and Channel-filter gain settings

The following table gives the intrinsic voltage gain of the LNA circuit. LNA voltage gain is programmable and this table indicates incremental ICC steps impacting RX Front end current consumption in the same amount.

CF-Gain 1	CF-Gain 0	Voltage Gain
0	0	-2dB
0	1	17dB
1	0	22dB
1	1	27dB

Table 10 Channel-Filter Gain setting

LNA-Gain 1	LNA-Gain 0	Gain (dB)	LNA input stage typical current
0	0	4 *	0.55 mA
0	1	17	0.55 mA
1	0	23	1.1 mA
1	1	25.5	1.65mA

Table 11: RX Gain Control

* LNA low gain stage.

Notes:

1- Voltage gain induced by impedance transformation network (from antenna to RX input pin) needs to be added to these figures (e.g. 6dB extra gain in case of ideal 50Ω to 200Ω impedance transformation) to compute the overall RX FE voltage gain.

2- Voltage gain of the RX analogue chain (before limiter) can then be performed by adding these values to those of the Channel Filter given in the table 63 hereafter.

The following diagrams illustrate the field-strength dependent gain-switching graphically.
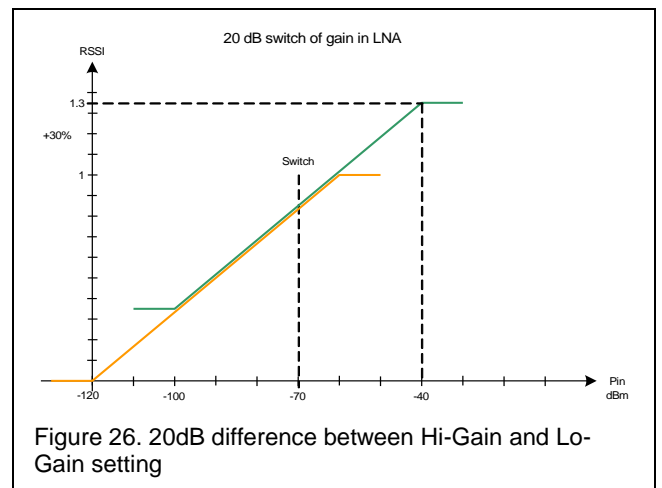
Figure 26. 20dB difference between Hi-Gain and Lo-Gain setting

42

Integrated UHF Transceiver
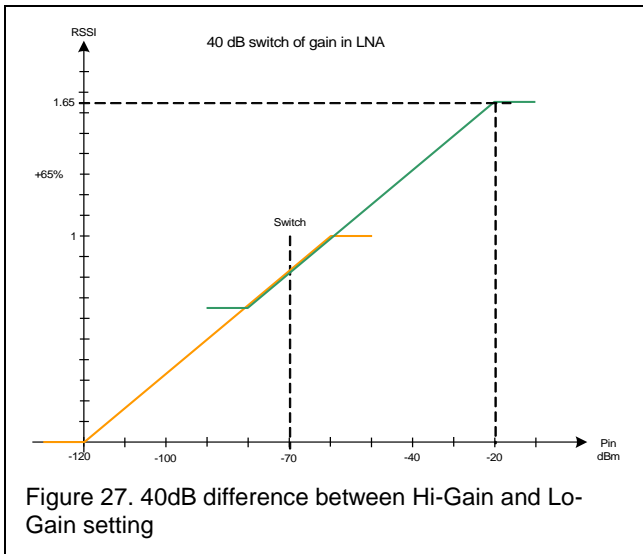
Figure 27. 40dB difference between Hi-Gain and Lo-Gain setting

9.7 Limiter

The function of the limiter is to amplify or limit the input signal in a way that the output voltage of the last stage of the limiter is always constant. This applies for both very small signals at the sensitivity limit and very large input signals. The limiter block consists of 5 individual gain stages for each channel (I and Q). The Limiter output signal of the last stage can be seen as a rail-to-rail square signal. Two limiter chains are implemented. One chain limits the I-signal, the other one is used to limit the Q-channel. These square wave signals are used for FM demodulation in the base-band signal processing part. Therefore the limiter can be interpreted as a one bit ADC directly connected to the digital part. The analogue output signal levels of the individual limiter stages are used in conjunction with the RSSI block to measure the received signal strength on a logarithmic scale.

Filter cut-off frequency for the Limiter-block

Taking into account the IF frequency of 300 KHz, and a maximum bandwidth of 300 KHz the following cut-off frequencies have been selected:

- high pass cut-off frequency < 100 KHz
- low pass cut-off frequency > 500 KHz.
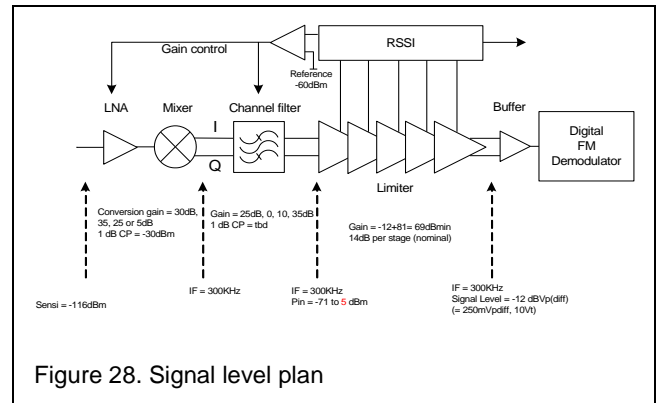
Figure 28. Signal level plan

9.8 RSSI

The RSSI function is implemented by the adding of the tail currents used in the individual limiter-stages. This does not apply for levels higher than the compression point. In this case the gain of the LNA and the Channel-filter will be lowered to increase the linearity and the dynamic range of the RSSI.

Note: As the RSSI is proportional to the input voltage level, which has a frequency of 300 kHz, it has to be filtered to ensure a stable result as the input voltage. The RSSI itself has a frequency of 600kHz due to the nature of the RSSI detector principle.

Dynamic Range and Operation

The dynamic operation of the RSSI is needed for ASK demodulation and carrier detection. For this purpose an overall dynamic range of 130dB is required (-120dBm minimum sensitivity up to +10dBm max. signal strength). The gain of the front-end can be switched. It is recommended to have an overlap of the dynamic ranges of 20dB to guarantee continuous ASK demodulation. This results in a single 'range' of 70dB. The RSSI reading also could be used to reduce the power output for a Tx operation. The RSSI value could be included in the handshaking information and appropriate Tx power settings thus applied.

Resolution

The resolution is set to +/-2dB in all conditions. For process variation and temperature variation reasons a 6 bit converter is implemented.

43

Integrated UHF Transceiver
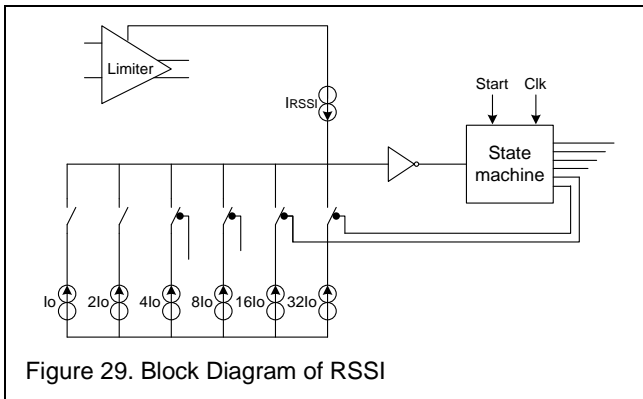
Figure 29. Block Diagram of RSSI

RSSI low-pass filtering

The filter integration time-constant of the analogue RSSI signal can be adapted to achieve a more stable digital RSSI reading (RSSI raw value) as an input to the digital filtering and interpolation. This analogue filter (RC-type) is used in addition to the digital filters implemented in the base-band digital signal processing unit. This first order low-pass filter is applied directly at the summed output of the limiter tail-currents. It does not affect the gain-bandwidth characteristics of the limiter itself.

RSSI digital filtering

The raw RSSI value is fed to a digital filtering and interpolation circuit. The output of the digital circuit is the cooked RSSI value. The digital RSSI filter cut-off frequency can be selected by the RSSI_FILTER_FC bits.

The first order low-pass filter, which is mentioned above, has a cut of frequency, which can be calculated according to following formula:

$$f_c = \frac{f_{ref}}{2\pi \cdot 2^{5+RSSI\_FILTER\_FC}}$$

where f_{ref} is the reference frequency and RSSI_FILTER_FC is a 4 bit value in the RXBW register.

Low level signal detection

The RSSI is used to detect the start of a communication sequence. Carriers at a sensitivity level down to -110dBm are detected properly.

9.8.1 RSSI Gain Control

The switching threshold of the automatic front-end gain selection is controlled via the output signal of the RSSI.

The principle of this is to decrease the front-end gain (and, if necessary, the channel filter), when the input level is significantly greater than the reference sensitivity level. This gain switching increases the linearity of the overall chain and the robustness for large signal behavior as well increasing the dynamic range of the RSSI.

The HIGAINLIM register contains the 8 bits of the HI_GAIN_LIMIT control word. At powerup the front-end gain is always set to RX_HI_GAIN, the RSSI therefore operating in its' 'most sensitive' mode. If the gain switching is enabled during wakeup-search, the gain will be lowered to the RX_LO_GAIN settings providing the RSSI threshold set by HI_GAIN_LIMIT is exceeded. The RSSI reading is performed automatically during the wakeup-search detection.

NOTE: If the input signal level is above the switching threshold and the gain-switching is initiated, two bits are lost due to the switching event. The length of the wake-up and the preamble has to be chosen accordingly to guarantee safe operation. The minimum length of preamble should be 8 bits; the bit time of two bits is necessary to start-up the receiver and to perform the necessary RSSI measurement, 2 bits may be lost due to the RSSI switching, and a minimum of 4 bits are required to detect the preamble correctly and to synchronize the clock-recovery).This is true only for the when using the edge slicer, more time may be required when using the level sensitive slicer.

The result of the RSSI conversion can be retrieved in the RSSILEVEL status register.

A compensation value can be set in the GAINSTEP register in order to achieve a continuous RSSI reading when the gain of the front-end is changed. RSSI_GAIN_STEP_ADJ is the representation of the difference in gain-setting between RX_HI_GAIN and RX_LO_GAIN in the corresponding RSSI-reading value. The RSSI_GAIN_STEP_ADJ value is added to the RSSI conversion result when the RX_LO_GAIN is activated. This yields in an overall dynamic range of the RSSI of more than 120dB.

Integrated UHF Transceiver

9.9 Receive Mode

9.9.1 Preparation for Receive Mode

The device initiates Receive mode upon the correct setting of the DEV_MODE bits. This, in turn, sets the internal enable bits PLLEN and RXEN.
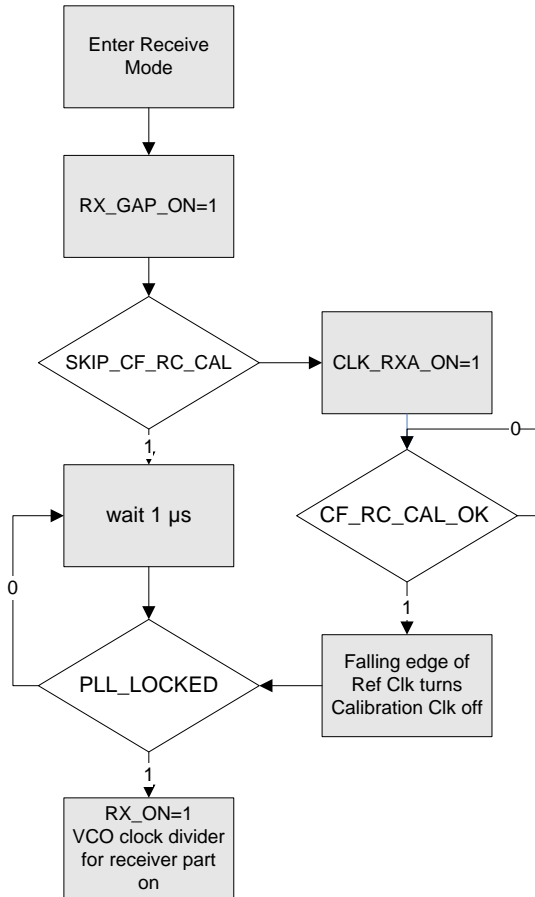
Figure 30: Preparation for Receive Mode

1) Turn on the bandgap reference circuit for the receiver part (RX_GAP_ON). and the clock for the channel filter RC calibration (CLK_RXA_ON) with the negative edge of the reference clock. The latter shall be done only if the channel filter RC calibration is not skipped (SKIP_CF_RC_CAL). Then wait 1 µs until the bandgap has stabilized.

2) If the channel filter RC calibration is enabled, start it and then and wait until its completion. Then turn the clock for the RC calibration off with the next falling edge of the reference clock.

3) Wait until the PLL control state machine has reached the state PLL_LOCKED and then turn the receiver on (RX_ON), which also turns the VCO clock divider for receiver part on.

This sequence finishes with the channel filter RC calibration, if enabled. Once this is complete the Receiver has been turned on.

9.10 Receive Command

The device features a receive command comparable to the transmit command. The command includes the six command bits RA, RB, RC, RD, RE and RF.

- Bits RA, RB: Receive frequency selection bits

- Bits RC, RD: sub-command bits

- Bits RE, RF: gain step/switch selection bits

D0	D1	D2	D3	D4	D5	D6	D7
1	0	RA	RB	RC	RD	RE	RF

Table 12 Receive Command Packet

Bit RA	Bit RB	Selected frequency band
0	0	FC0L, FC0M, FC0H
0	1	FC1L, FC1M, FC1H
1	0	FC2L, FC2M, FC2H
1	1	FC3L, FC3M, FC3H

Table 13 Frequency selection (bits RA, RB)

Note: in Receive mode a frequency offset of +300 kHz is automatically added to the resulting centre frequency in order to account for the necessary LO frequency offset. If this is the first Receive command after a Transmit operation or whenever these flags change from one Receive command to another, an LO sub-band calibration (VCO calibration) is initiated.

Bit RC	Bit RD	Selected Receive sub-command
0	0	CONT (continue)
0	1	WUPS (wakeup search)
1	0	PRDA (preamble detection followed by data reception)
1	1	DATA (data reception without preamble detection)

Table 14 Sub-command selection bits RC, RD)

With a CONT Receive command the µC can continue any previously initiated WUPS, DATA or PRDA command. If the frequency selection bits RA and RB are the same as in the previous receive command and if the flags RE and RF are both 0, then, with the next rising edge of the SCLK line, only the receive clock and the receive data lines are switched onto the SPI SCLK and D(I)O pins, respectively. This provides the µC with the possibility to interlace SPI Read and Write commands with receiving data, provided that the SPI communication rate is much faster than the data reception rate. If there is currently no Receive operation in progress, the CONT Receive command does not initiate anything, it just switches the SPI lines with the next SPI clock edge and delivers the internal receiver result (this could be the recovered chip clock and the transparent slicer signal or just a constant level, depending on the

45

Integrated UHF Transceiver

current receiver output configuration and depending on the receiver state).

With a WUPS Receive command a wakeup search operation is initiated. This command has restart characteristics, which means that it interrupts any other Receive operation. During this command the RXDCON0 configuration is applied as the dynamic configuration for the slicer and signal classification and detection means. During the command the receive clock and data result can be observed with the SPI lines, which is a constant HI on the clock line and a constant LO on the data line in cooked mode. This output (not the wakeup search operation itself) can be interrupted with Read and Write commands and can be continued with a CONT Receive command. The WUPS command finishes after either a WAKEUP_FOUND or a WAKEUP_NOT_FOUND decision has been made. In both cases the status of the detection means is sampled. After finishing the WUPS command the WUPS_FOLLOWUP configuration dictates how the device should proceed.

With a PRDA Receive command a preamble detection is initiated. This command has restart characteristics, which means that it interrupts any other Receive operation. During this command the RXDCON1 configuration is applied as the dynamic configuration for the slicer and signal classification and detection means. During the command the receive clock and data result can be observed with the SPI lines, which is a constant HI on the clock line and a constant HI on the data line during preamble detection in cooked mode. This output (not the preamble detection operation itself) can be interrupted with Read and Write commands and can be continued with a CONT Receive command. When the correct preamble is detected, the receiver switches automatically into data reception mode. This switch does not influence the signal processing part of the receiver, which means that there is a seamless transition from the preamble detection mode to the data reception mode. But what changes with the switch is the dynamic part of the configuration and the state of the signal detection and classification means. The dynamic configuration for the signal detection and classification means is switched to the RXDCON2 set and the detection means are restarted.

If the preamble detection finishes with a PREAMBLE_-NOT_FOUND status (after running into a timeout), the PREA_FOLLOWUP configuration decides whether and how the receiver proceeds automatically. Regardless of the outcome of the preamble detection phase (found or timeout) the status of the detection means is sampled when the preamble detection is finished.

If the cooked receive output format is selected for the receive clock and data, both are held constant as long as the preamble detection is in progress. After the preamble has been detected the receive clock is started up and the associated receive data bits are delivered with each receive clock pulse. In transparent mode the output signals are always available.

With a DATA Receive command the reception of frame data is initiated skipping the preamble detection phase. This command uses always the RXDCON1 set as the dynamic configuration for the slicer and the signal detection and classification means and after initializing the slicer it behaves like the PRDA command after successful preamble detection.

Both the PRDA command in data reception mode and the DATA command do not finish automatically on any selectable criteria. They can be terminated with either a Transmit command or another restarting Receive command or by turning the receiver off.

Bit RE	Bit RF	Selected gain step/switch config.
0	0	keep the receiver gain as it is
0	1	gain switch (WUPS sub-command only), same as 00 for other sub-commands
1	0	use the low gain settings
1	1	use the high gain settings

Table 15 Gain switch selection (bits RE, RF)

The combination 01 (gain switch) is only applicable with the wakeup search (WUPS) Receive command. If this is chosen, the wakeup search starts with the high gain settings. If the received RF signal strength is always below the limit given by the HI_GAIN_LIMIT settings, then the low gain settings are used throughout the whole wakeup search. But if the RF amplitude exceeds this limit, the receiver automatically switches to the low gain settings and continues with the wakeup search. Note: the wakeup search timer is not influenced by the gain switch.

Integrated UHF Transceiver

Figure 31: Example of a Receive command (SEP_SDO = 0, SEP_RX_OUT = 0)

Figure 32: Example of a Receive command (SEP_SDO = 0, SEP_RX_OUT = 1)
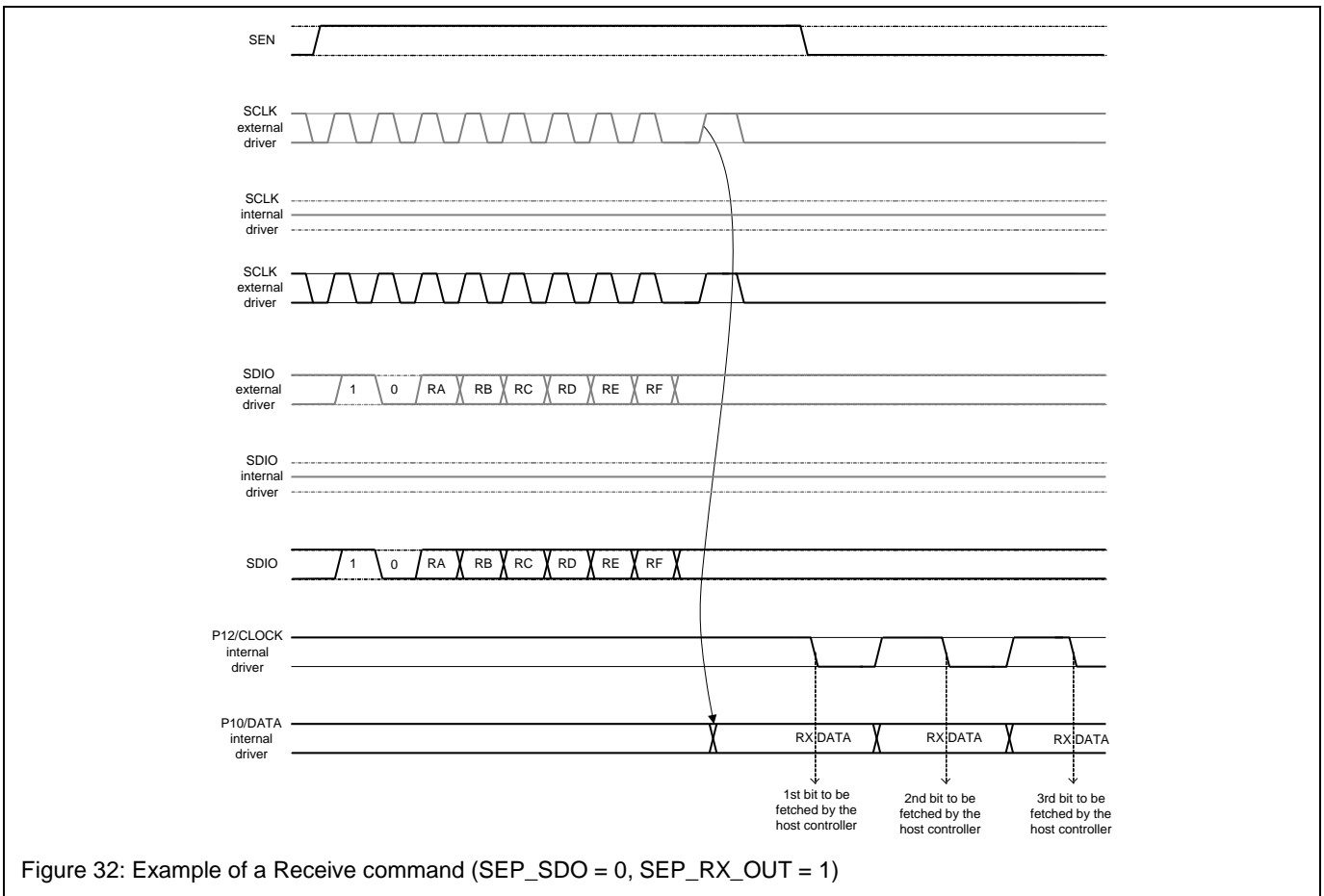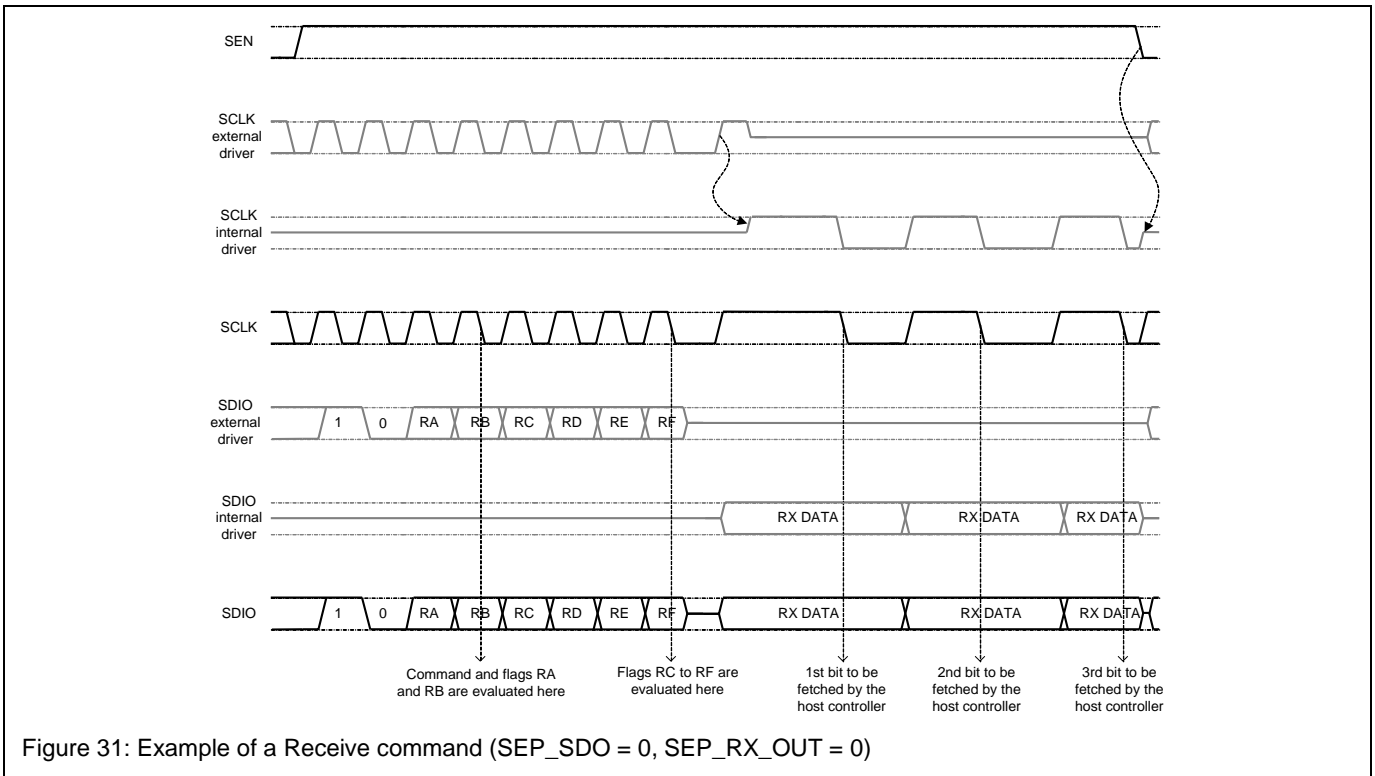
From a sequence and timing point of view the Receive command behaves as follows:

The DEV_MODE is set to 10 (RX mode) with the falling edge of the SPI clock after receiving the 4th bit (flag bit RB)

47

Integrated UHF Transceiver

of the command. The new frequency setting is applied according to the flag bits RA and RB, which is shared with the Transmit command. The LO will be initialised for this frequency and the receiver will remain switched on even if the receive command is aborted. A four bit command can be used to turn the receiver on and to switch the LO frequency. A new calibration of the VCO sub-band, providing it is enabled, and a new lock-in of the PLL will occur under the following conditions.

- upon receipt of the first Receive command after a Transmit operation

- the first Receive command after powering up the device

- the frequency settings are changed with respect to a previous Receive command

The next relevant action occurs upon receiving the 8th bit (flag bit RF) of the command with the falling edge of the SPI clock. This latches the remaining flags (RC through RF) into the Receive flag register. Please notice that the Receive state machine is still not influenced after having received the full command byte. This gives the µC the chance to wait until the analog part of the receiver has fully settled before the execution of the command is actually started from a sequence point of view.

The command is actually initiated with the next rising edge of the SPI clock. In the case of a WUPS, a PRDA or a DATA Receive command this brings the receiver state machine to the respective starting point of the sub-command. If a CONT Receive command is issued the receiver state machine is not influenced. The rising edge of the SPI clock also switches the receive clock onto the SCLK line after a programmable delay (CLK2SCLK_DELAY) and the receive data output is immediately switched onto the SD(I)O line. This delay takes effect when switching the SPI line SCLK with a Transmit or Receive command into the mode, where it changes its direction to output. In this mode it delivers the transmit or receive clock, respectively. The delay starts with the next positive edge of the reference clock following the 9th edge of SCLK (activation edge). After the delay the output driver of SCLK is activated.

The delay value is (CLK2SCLK_DELAY + 1) / fref, where CLK2SCLK_DELAY (a 4-bit value) can be set to a value in the range 0,…,15. So if the 9th edge of SCLK occurs just before the positive edge of the reference clock and if CLK2SCLK_DELAY is set to 0, the minimum delay is 1 reference clock cycle (62.5 ns @ 16 MHz). If the 9th edge of SCLK occurs just after the positive edge of the reference clock and if CLK2SCLK_DELAY is set to 15, the maximum delay is 17 reference clock cycles (1062.5 ns @ 16 MHz).

If cooked receiver output mode is configured, the clock output will deliver a constant HI state during wakeup search and during preamble detection. The output will start toggling during data reception according to the recovered receive clock. The data output will behave in a similar way if in cooked mode, the only difference being that it will be in the low state during wakeup search operations.

If transparent receiver output is configured, the clock and data output will always deliver the recovered chip clock and the deglitched slicer output, respectively.

9.10.1 Dynamic receiver configuration

It is not always appropriate to have a fixed setting for all aspects of the receiver configuration for a given protocol. This is illustrated in the following two examples.

1. If the transmitter sends its frames continuously without RF interruption, then it makes sense to initialize the slicer at the beginning of the wakeup search but to skip the slicer initialization at the beginning of the preamble detection in order to save time.

2. If Manchester encoded data is to be received then the modulation amplitude detection must be configured to allow single signal gaps, which occur at data bit transitions (01 or 10). But if the wakeup pattern is a constant Manchester encoded 000… or 111… pattern, allowing no signal gaps increases discrimination precision.

To be able to manage these scenarios whilst minimising the loading of the external microcontroller a so called dynamic device configuration can be implemented. This dynamic device configuration is controlled with the following control bytes.

Register	Nomenclature
RXDCON0	Wake-Up Search Settings
RXDCON1	Preamble-Detection Settings
RXDCON2	Data Reception Settings

Table 74: RXDCON Registers

The relevant register is automatically selected depending on whether the receiver is in wakeup search mode, preamble detection mode or in data reception mode. For the SLICERINITSEL and the INIT_ACQ_BITS two individual alternative configuration sets are available, because for the combined preamble detection and data reception operation only one slicer initialization is necessary.

Integrated UHF Transceiver

It is possible to chain all these device modes together, employing individual device configuration settings automatically. This is especially useful when the first command is initiated from a polling timer event where the receiver can work in parallel to the wakeup of the µC.

first operation	after wakeup search				after preamble detection			
initated by	polling timer		command		polling timer		Command	
success(+)/fail(-)	+	−	+	−	+	−	+	−
power-down		✓		✓		✓		✓
stop	✓!	✓!	✓	✓		✓!		✓
DATA	✓!		✓		✓!		✓	
PRDA	✓		✓					
bit (field) name	WUPS_ FU_TS	WUPS_ FU_TF	WUPS_ FU_CS	WUPS_ FU_CF		PREA_ FU_TF		PREA_ FU_CF
follow up config name	WUPS_FOLLOWUP				PREA_FOLLOWUP			

Table 16: Receiver operating mode transitions

In the above table a '✓' symbol indicates a possible operating mode transition and a '!' symbol indicates where a non-maskable interrupt is generated. The above table can be used to determine the configuration of the RXFOLLOWUP register. Note: An interrupt may be generated when finishing a wakeup search or a preamble detection. All other interrupts can be enables with the interrupt enable register.

Integrated UHF Transceiver

10 Signal Signature Recognition Unit

The purpose of the signal signature recognition unit is to provide a user friendly and easy means to support quick and configurable receive tools. The basic challenge in receive mode is to distinguish noise or unwanted disturbers from the wanted receive signal. This 'signal quality' decision has to be taken within the shortest time possible to save system power consumption. After successful 'signal quality' detection the receive process has to be

started. The receive process basically consists of data and clock regeneration. In order to make the system even more robust to ambient noise and/or disturbers the data and clock recovery can be gated by additional means. If the baud-rate and the coding of the receive signal is known, a 'wake-up' pattern matching unit can be activated. The following Table provides a comprehensive overview of the various available units. All units are individually selected and configured.

Recognition Unit	block name	processes the signal	started by	Purpose
RSSI level classification	RSSI level classification	cooked RSSI		Determine correct signal strength (upper and lower limit can be defined)
Modulation amplitude classification	Modulation amplitude classification	demodulated baseband	start of wakeup search	Determine correct FSK/ASK modulation amplitude
Data classification	Slicer	demodulated baseband	start of wakeup search, only if initial acquisition is enabled	Enable selection for different data-slicer behaviour (fast settling, long averaging, hold of previously acquired levels)
	Chip Timing verification and code checker	slicer output	slicer output valid after start of wakeup search	Decode and search for correct Manchester coding and special coding sequences
	Baud rate checker	slicer output	FIRST_SYNC or RESYNC of the Timing verification after start of wakeup search	Check for correct Baud rate
	Preamble detection	Slicer output	End of wakeup search	Configurable 1-32 bit preamble pattern matching
Wakeup search timer	Wakeup search timer		start of wakeup search	start /end of recognition sequence

Table 17: Overview of the Signal Signature Recognition Unit

10.1 RSSI level classification

The RSSI circuit is used for ASK demodulation, for determining the front-end gain switch threshold and for signal level detection. Two different application scenarios can be supported by a level-detection circuit

1. Check for a carrier signal strength within a given threshold, i.e. above a minimum level or below a maximum level or between minimum and maximum.

2. Check for a carrier signal strength outside a given threshold, i.e. below a minimum level or above a maximum level.

The first scenario can be used to determine the presence of a carrier as precondition for other demodulation or classification measures. The second scenario is useful to quickly check for occupied channels in a multi channel system.

The RSSI classification unit is realized as a window comparator with programmable threshold values.

Functional Block diagram:
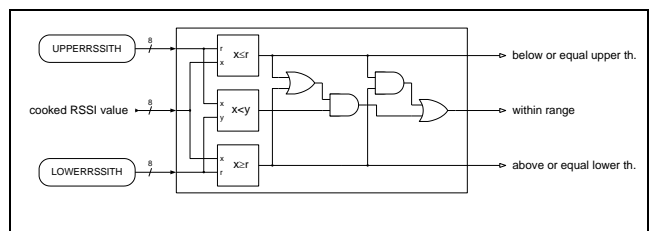
Figure 33: RSSI wake-up recognition

Input signals:

8-bit cooked RSSI value

8-bit upper limit of the desired RSSI range

8-bit lower limit of the desired RSSI range

Output signals:

Two individual signals, which indicate whether the input signal is above or below the respective threshold; these two indicators will be provided as (latched) status information.

The logic combination of the two output signals indicates that the RSSI signal is within the range defined by the two

50

Integrated UHF Transceiver

thresholds. The definition of what is actually is intended by the phrase 'within the range' depends on whether the value of the upper limit is greater or less than the lower limit. This is illustrated in the following picture.
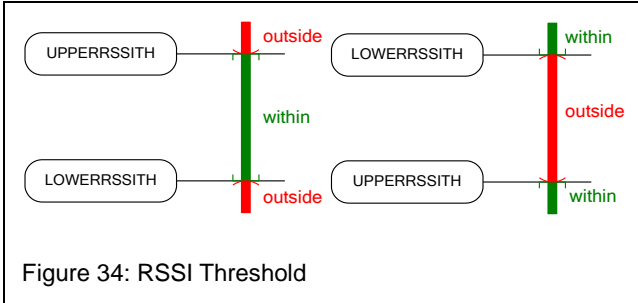
Figure 34: RSSI Threshold

If a single minimum threshold is desired, the UPPERRSSITH value has to be set to 255 (0xFF). To achieve a single maximum threshold the LOWERRSSITH register has to be set to 0.

10.2 Modulation amplitude classification

This block consists of two sub-blocks, the first of which is the amplitude measurement, which is followed by a threshold comparison and the decision logic.

Method to determine the Modulation Amplitude

The modulation amplitude classification block measures the magnitude of the transitions in the signal within one chip interval. The baseband signal is delayed by one chip, using an over sampling ratio of 4 samples per chip. A raw amplitude measurement is computed for each sample by subtracting the delayed sample and taking the absolute value of the difference. Then for each chip interval the maximum of the four adjacent raw values is determined.
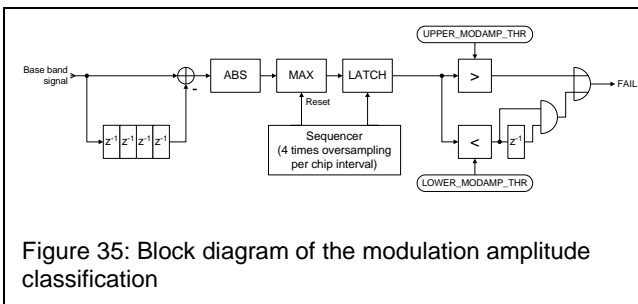
Figure 35: Block diagram of the modulation amplitude classification

If there is a transition in the chip interval, the output of this measurement is valid. If there is no transition in the interval the output from the measurement can be much lower than the nominal amplitude. This appears as a 'gap' in the sequence of measurements. If we consider a Manchester coded signal, which has at least one transition within each two-chip interval, we have to accept (and ignore) at most one gap between valid measurements. The modulation-amplitude is compared against the threshold defined with LMODAMPTH and if it is lower than the threshold for a duration greater than NUM_MODAMP_GAPS_x * (chip duration), then a 'modulation amplitude too low' error is reported in bit 0 of the SIGMONERROR register.
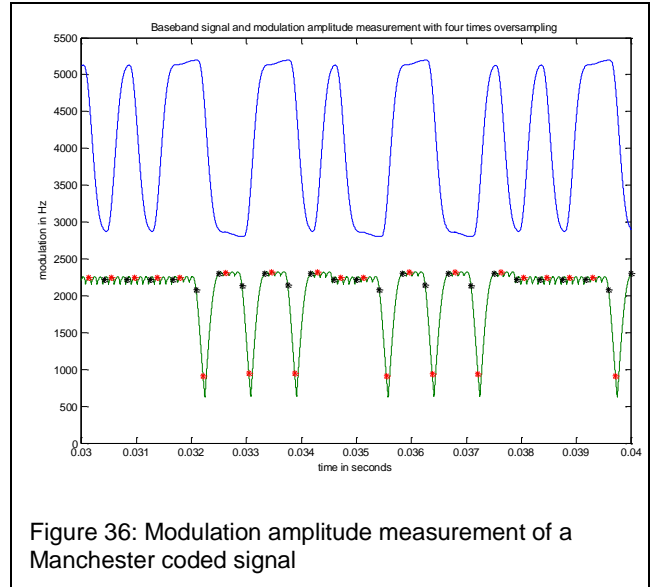
Figure 36: Modulation amplitude measurement of a Manchester coded signal

Figure 36 shows an example of the amplitude measurement when measuring a noise-free Manchester encoded baseband signal. The blue trace is the baseband signal, x(t). Please notice that this signal can have an arbitrary offset. The lower trace shows the output of the amplitude measurement. The red dots show the actual values (over-sampling rate of 4 vs. chip-clock) used for computation.

Due to the ripple in the output signal (lower trace) and the discrete sampling time, the sampled signal can be lower than the theoretical maximum value. Worst case input signals for this algorithm produce a maximum amplitude error of 8% of the maximum theoretical value.
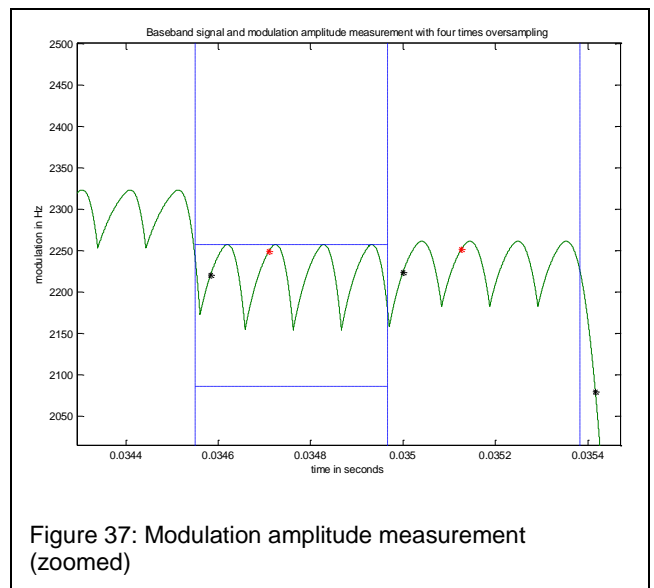
Figure 37: Modulation amplitude measurement (zoomed)

In this example the upper horizontal dashed line corresponds to the actual amplitude A_{act}. The lower horizontal dashed line corresponds to $A_{act}.-8\% = 0.92\ A_{act}$. This should be considered when calculating the lower and upper limit for the modulation amplitude detection. (the

Integrated UHF Transceiver

higher limit can be set close to the expected value, the lower limit should be at least 8% lower than the expected value)

The amplitude measurement for each chip interval is compared with two programmable thresholds. If the measured amplitude is above the upper threshold, the result is immediately classed as a FAIL. If the measured amplitude is below the lower threshold, this can be either a low amplitude condition or a 'gap'., The outcome is a FAIL if two successive amplitude measurements deliver a value which is below the lower threshold, as there should be one gap at most between valid measurements.

The lower and the upper threshold can be independently selected with the 8 bit registers LOWER_MODAMP_TH and UPPER_MODAMP_TH, respectively. The actual threshold value is defined by the associated register settings according to the following formula.

$$xxxThreshddValue = \min\left(2^{XXX\_MODAMP\_TH[7:4]} . XXX\_MODAMP\_TH[3:0], 7FFFh\right)$$

Example: FSK signal Manchester coded, 2kbits/s resp. 4kchips/s, modulation deviation: +/- 1.5kHz

The FSK signal has to be mapped to the output range of the FSK demodulator. The output signal range is from 0 to 32256. This range equals a frequency deviation of 200kHz respectively 600kHz. (dependent of the bit LARGE_FM_DEM_RANGE in the EXPERT2 register). The expected peak to peak modulation amplitude would be 1.5/200 * 32256 = 242. The UPPER_MODAMP_TH shall be set to at least the expected value: $16*2^4$ = 256. UPPER_MODAMP_TH[3:0] = 15d = 1111b UPPER_MODAMP_TH[7:4] = 4d = 0100b

The LOWER_MODAMP_TH shall be set to maximally the expected value * 0.92 = 222: $13*2^4$= 208.

LOWER _MODAMP_TH[3:0] = 13d = 1101b
LOWER _MODAMP_TH[7:4] = 4d = 0100b

The lower and the upper thresholds can be disabled. The lower threshold is disabled by setting LOWER_MODAMP_TH = 0 whereon the higher threshold is disabled by any value UPPER_MODAMP_TH >= 2^{15}.

10.3 Data Classification

The data-slicer is needed for the Timing, Code and Baud rate classification units.

10.3.1 Data Slicer

The device features a versatile collection of different data slicers with different initialisation and adaptation mechanisms, including; an edge sensitive slicer with minimum latency (used in applications where fast data-slicer settling times are crucial) and a level sensitive slicer (more robust to noise, appropriate when a longer settling time is acceptable).

Number of corrupted bits in receive mode

The number of corrupted bits during the start of receive mode is dependent on the selected slicer method and the associated settings. The edge slicer provides the fastest possible settling time, only 1 chip (1/2 bit) will be lost. The loss of bits of the level sensitive slicer depends on its initialization setting. If the initialization sequence is selected 4 chips (2 bits) or 16 chips (8 bits) can be 'lost'. It is possible to recover all bits, providing the level sensitive slicer is pre-initialized to the correct threshold.

Slicer description

The level sensitive slicer consists of two registers: the actual slicer threshold register SLICERTHR and an initialisation register SLICERINITTHR. The register SLICERINITTHR can be accessed via the SPI interface.

Integrated UHF Transceiver
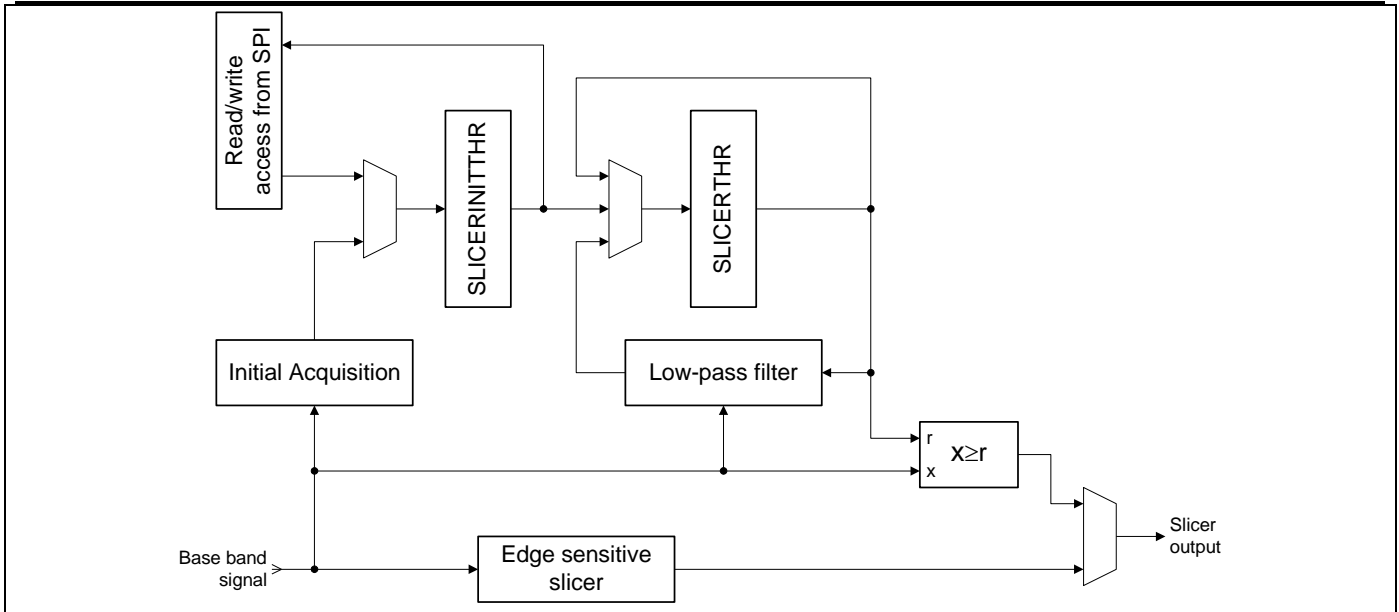
Figure 38: Slicer block diagram.

The edge sensitive slicer does not make use of these two registers. The EDGE_MODAMP_TH contains the expected peak modulation amplitude with which the edge slicer is initialized.

10.3.2 Edge Sensitive Slicer

The edge slicer operates as a differentiating slicer in combination with a fixed level slicer. The time constant is automatically adjusted in accordance with the selected

The operation mode of the slicer is selected with the slicer selection bits SLICERSEL according to Table

chip-rate of the baud-rate generator unit. This slicer is also capable of demodulating NRZ code with long constant bit sequences providing the expected peak modulation amplitude has been initialized correctly. The basic principle of the edge slicer is explained with the following diagrams.
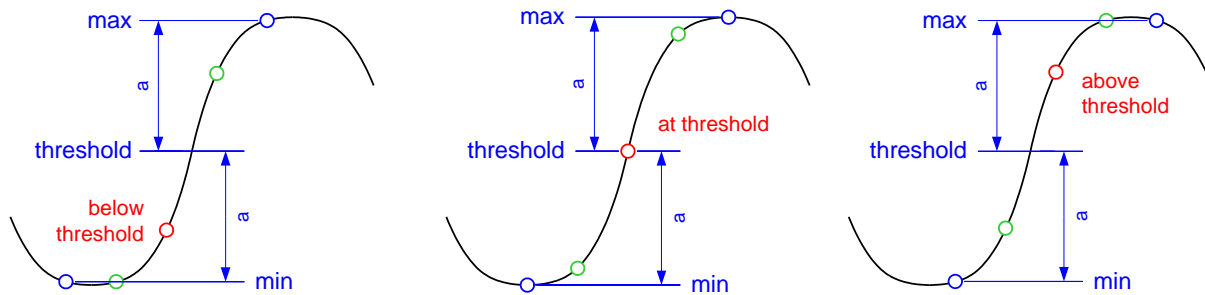
Figure 39: Working principle of the edge slicer

The edge slicer takes five adjacent samples at intervals equivalent to ¼ of the chip width. The four outermost samples (the blue and the green dots in the diagram above) are used to make up a dynamic threshold and the middle sample (red) is compared against this. The threshold value is the average of the maximum and minimum of the four outermost points.

The exact description of the algorithm for the edge slicer is

- Consider 5 consecutive samples taken at the a distance of ¼ of the chip width

- Compute the minimum and the maximum of all samples except the middle one

- Take the average of the maximum and the minimum as the slicer threshold

- Compute the maximum and the minimum of the two neighbours of the middle sample

53

Integrated UHF Transceiver

- Take the difference of the maximum and the minimum as the amplitude measurement

- Compare the measured amplitude against the peak value of the signal which is provided through the EDGE_MODAMP_TH register

- If the amplitude is above the threshold, set the slicer output according to the comparison of the signal (middle sample) with respect to the slicer threshold

- If the amplitude is below the threshold, keep the current state of the slicer output

The following list summarizes the properties of the edge slicer algorithm

- Because the input signal needs to be fed through a delay line and because of the necessary linear interpolation the slicer has a delay of about one chip interval.

- Since the slicer acts only on valid signal edges and since it ignores what is between these edges, it can handle arbitrary coded signals, including NRZ.

- The slicer output is valid after the first signal edge (and the slicer delay).

- Due to its differentiating function the edge slicer is more susceptible to noise than slicer threshold generation methods which average over the signal (Level sensitive slicer).

For the amplitude classification the slicer needs to know the expected amplitude of the baseband signal; this can be easily provided for FSK signals.

The following configuration settings have to be initialized when the edge slicer is used:

Expected peak modulation value: has to be provided through the EDGE_MODAMP_TH[7:0] register. The EDGE_MODAMP_TH has to be calculated according the following procedure:

$$ThresholdValue = 2^{EDGE\_MODAMP\_TH[7:4]} \cdot EDGE\_MODAMP\_TH[3:0]$$

Example: FSK signal Manchester coded, 2kbits/s resp. 4kchips/s, modulation deviation: +/- 1.5kHz

The FSK signal has to be mapped to the output range of the FSK demodulator. The output signal range is from 0 to 32256. This range equals a frequency deviation of 200kHz respectively 600kHz. (dependent on the bit LARGE_FM_DEM_RANGE in the EXPERT2 register). The expected peak modulation amplitude would be 1.5/200 * 32256 = 242. The EDGE_MODAMP_TH shall be set as close as possible to the expected value: $15*2^4 = 240$.
EDGE_MODAMP_TH[3:0] = 15d = 1111b
EDGE_MODAMP_TH[7:4] = 4d = 0100b

The lower and upper thresholds for the peak to peak amplitude of the baseband signal (FSK modulation) are simply the transmitted peak to peak frequency deviation plus and minus a guard band tolerance (factor of 3/4 or 5/4) mapped to the output range of the FSK demodulator. They can be calculated from following equations:

LMODAMPTH = 3000 * (32256/200000) * (3/4) = 362

UMODAMPTH = 3000 * (32256/200000) * (5/4) = 605

The UMODAMPTH register should be set to the higher value than 605 (10 * 2^6 = 640).

UMODAMPTH [3:0] = 10d = 1010b

UMODAMPTH [7:4] = 6d = 0110b

The LMODAMPTH register should be set to the lower value than 362 (11 * 2^5 = 352).

LMODAMPTH [3:0] = 11d = 1011b

LMODAMPTH [7:4] = 5d = 0101b

NOTE: the amplitude threshold shall be set to the expected **peak** amplitude value.

10.3.3 Level Sensitive Slicer

The level sensitive slicer offers various features which can be configured to improve noise immunity or reduce latency. These include:

- User definable initialisation value.

- Initial acquisition of the threshold by averaging the baseband signal over 2, 4, and 8 bits.

- Continuously variable threshold configured according to output from 1st order low pass filter.

The operation mode of the slicer is selected with the slicer selection bits SLICERSEL according to the following table.

The time constant for the low-pass filter is derived from the settings of the baud rate generator. It is assumed that a single bit consists of two chips, e.g. Manchester coding.

The various level slicer initialisation mechanisms are controlled by the SLICERINITSEL bits. If the slicer is initialized, its output becomes invalid for at least one cycle, which restarts the deglitcher and the edge detector. The output remains valid even when the slicer threshold is updated after the initial acquisition has refined its threshold value (after 4 and 8 bits).

10.3.3.1 Initial Acquisition

The initial acquisition generates a first estimate of the threshold by averaging the received baseband signal over a fixed time interval of two bits. If a constant 0 or 1 sequence or an alternating 01 sequence is received, the expected value of the error is exactly zero. If a Manchester

54

Integrated UHF Transceiver

encoded signal is being received, the maximum error can be ¼ of the whole swing, which is sufficient as an initial estimation. After having calculated this average, the slicer output changes from UNKNOWN to VALID.

The following samples from the baseband signal will be used to improve the initially found threshold. After processing an additional two bit interval (4 bits in total), a new average is computed which has less uncertainty as the initial value (by a factor sqrt(2)). This will be used as the new slicer threshold. Once an additional 4-bit interval is accumulated, having processed 8 bits in total, the final, more accurate estimate for the threshold can be calculated. This threshold value can be read via the SLICERINITTHR register. The register SLICERTHR is automatically updated every time a new initial slicer threshold is available.

It is possible that the two-bit interval period used for the initial estimate lies in a time period where there is either no RF at all, RF with only CW (no modulation) or the frame start containing Manchester code violations. In this case the slicer output may have no edges for a long time interval, which could be an indication that a wrong threshold value has been chosen. If the Timing Verification Block detects a timeout (time interval between edges > 3.5 chip width) it makes sense to reset the threshold estimation in order to get a better initial threshold value. The output of the slicer will again be UNKNOWN after the reset for the next two-bit interval. The slicer output will then become VALID again and the classification of its output edges may lead successful data reception. If the received signal is not usable the slicer may be reset several times until the selected receive operation is aborted.

If the initial acquisition is not used during the wake-up search, it might be useful to disable the auto-reset feature mentioned above. This can be accomplished by a dedicated setting in register SLICERINITSEL.

The initial acquisition operation always inhibits the use of the slicer output (status to UNKNOWN) during the calculation of the first two bits, regardless of whether the initial acquisition was triggered for the first time (by a receive event) or if it was re-triggered from a bit timeout.

The initial acquisition updates the slicer initialisation register and the slicer register after the calculation of 2, 4, and 8 bits (selectable with INIT_ACQ_BITS) providing the receive event was not interrupted by the higher level state machine. In these circumstances the initial acquisition is stopped in order to avoid unwanted data corrupting the calculation of the threshold.

The SLICERINITTHR register should only be accessed via the SPI if the initial acquisition is not active. Failure to comply with this could result in the reading of unstable values and the content of the register SLICERINITTHR could become undefined.

10.3.3.2 Deglitcher and Edge Detector

The purpose of the deglitcher is to suppress multiple signal transitions when a noisy baseband signal crosses the slicer threshold. The deglitcher works as follows: if a signal transition is detected, the deglitcher passes the transition to its output and then it locks this output for a certain time period, which can be selected with the DEGLITCHER_WINDOW_LEN bits according to the following table.

The lock timer is held in its reset state while the slicer output is invalid. This means that the deglitcher can only enter its locking state when the edge detector produces an output event.

The edge detector locates the edges in the deglitched slicer output and supplies the blocks which measure and classify time intervals between edges. The edge detector produces edges only after the slicer output has become valid. If the slicer produces a transition at the same time as its output becomes valid, it is suppressed by the edge detector. The deglitcher lock window is also suppressed by the edge detector and only becomes active when the edge detector produces an output event.

10.3.4 Timing Classification Block

The purpose of this unit is to classify the time intervals between the transitions from the slicer and to determine whether the received signal is a Manchester coded signal. Certain additional conditions can be selected.

The property of a Manchester coded signal, which will be used as the main classification criteria in this block, is that there are only two different time intervals, namely one chip width or two chip widths between two transitions.

10.3.4.1 Chip Timing Verification

In the proposed implementation the signal is oversampled with an OSR of 128, giving a time measurement resolution, which is better than 1%. The time interval between each pair of transitions is measured. If the measured time interval is < 1.5*chip width, then it is assumed that the associated nominal width is 1*chip width and so 1*chip width is subtracted from the measurement to calculate the timing error. If the measured time interval is > 1.5*chip width then it is assumed that the associated nominal width is 2*chip width and so 2*chip width is subtracted from the measurement to calculate the timing error. This measurement includes a sort of timeout such that widths greater than 3.5*chip width are always rejected. The absolute value of the timing error is calculated and compared to a limit, which can be chosen from the 16, 24, 32, or 48 counts of the oversampling clock according to the setting of bits SGLBITTMGERRTH. The time interval is accepted, if its absolute value is below the limit. This corresponds to timing errors, which are less than 12.5 %, 18.75 %, 25 % and 37.5% of a nominal chip width,

Integrated UHF Transceiver

respectively. The single chip timing verification block is a powerful means to classify signals with a given baudrate. The edges of these signals are assumed to emerge at a virtual chip grid. Therefore, the same absolute error limit is applied for short and long intervals in order to allow a specified range of edge jitter.

The chip timeout value can be changed with an expert bit. The standard value is 3.5 T_{Chip}. This value can be reduced to 2.5 T_{Chip}, if the bit REDUCED_BIT_TIMEOUT is set.
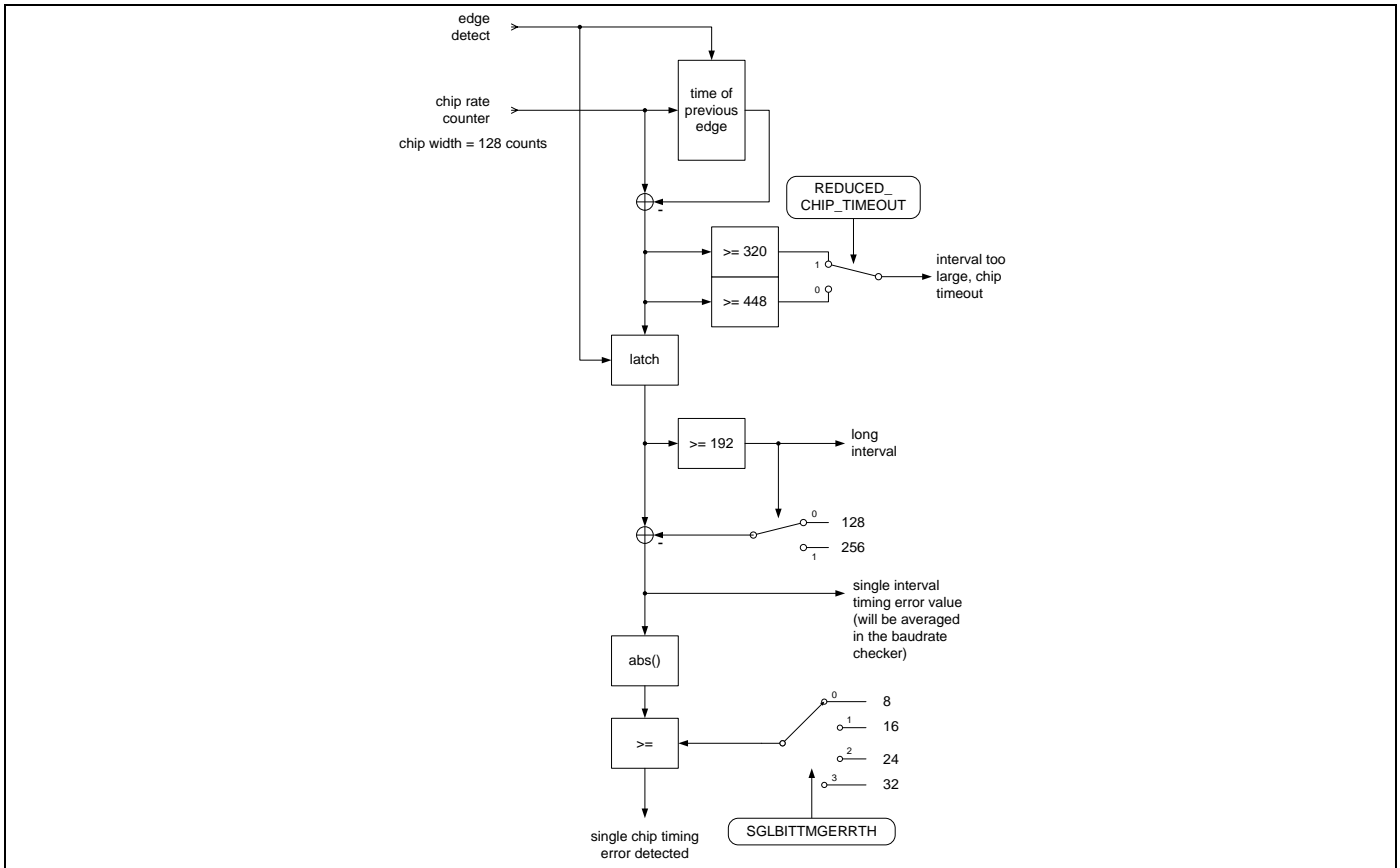
Figure 40: Block schematic of chip timing verification block

56

Integrated UHF Transceiver
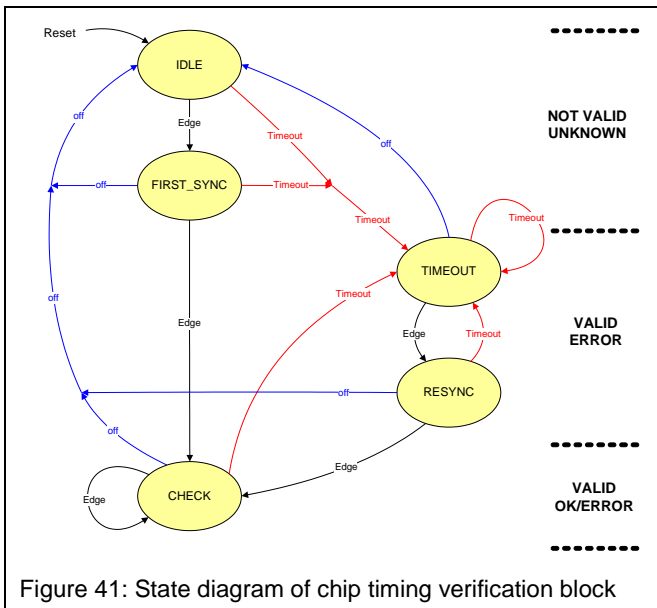
Figure 41: State diagram of chip timing verification block

After the first synchronisation (reception of two edges) the chip timing verification block becomes VALID and the chip timing CHECK begins. The last chip timing step is directly used as the ERROR criteria when in this state.

If a timeout occurs the state machine will signal an ERROR. Upon reception of two consecutive edges, the timing verification block can be re-synchronised, the state machine then again entering the CHECK state.

Please note that a single chip timing error does not change the state of the state machine unless it is a timeout.

10.3.4.2 Code Checker

Typical wakeup patterns consist either of a constant 0 sequence, a constant 1 sequence or an alternating 01 sequence. In these cases the pattern only contains a single time interval length. It is therefore possible to apply further restrictions on the accepted time intervals.

Correct chip timing is a prerequisite for the code checker. A single bit timing error will always cause a code checker error. Changing the setting of the CODINGRESTR bits, while the code checker is running, is not recommended. This can cause a false error indication. A false error indication may arise at a later stage if Manchester code checking is newly selected. The Manchester MANCHESTER START state is not necessarily executed immediately.

57

Integrated UHF Transceiver
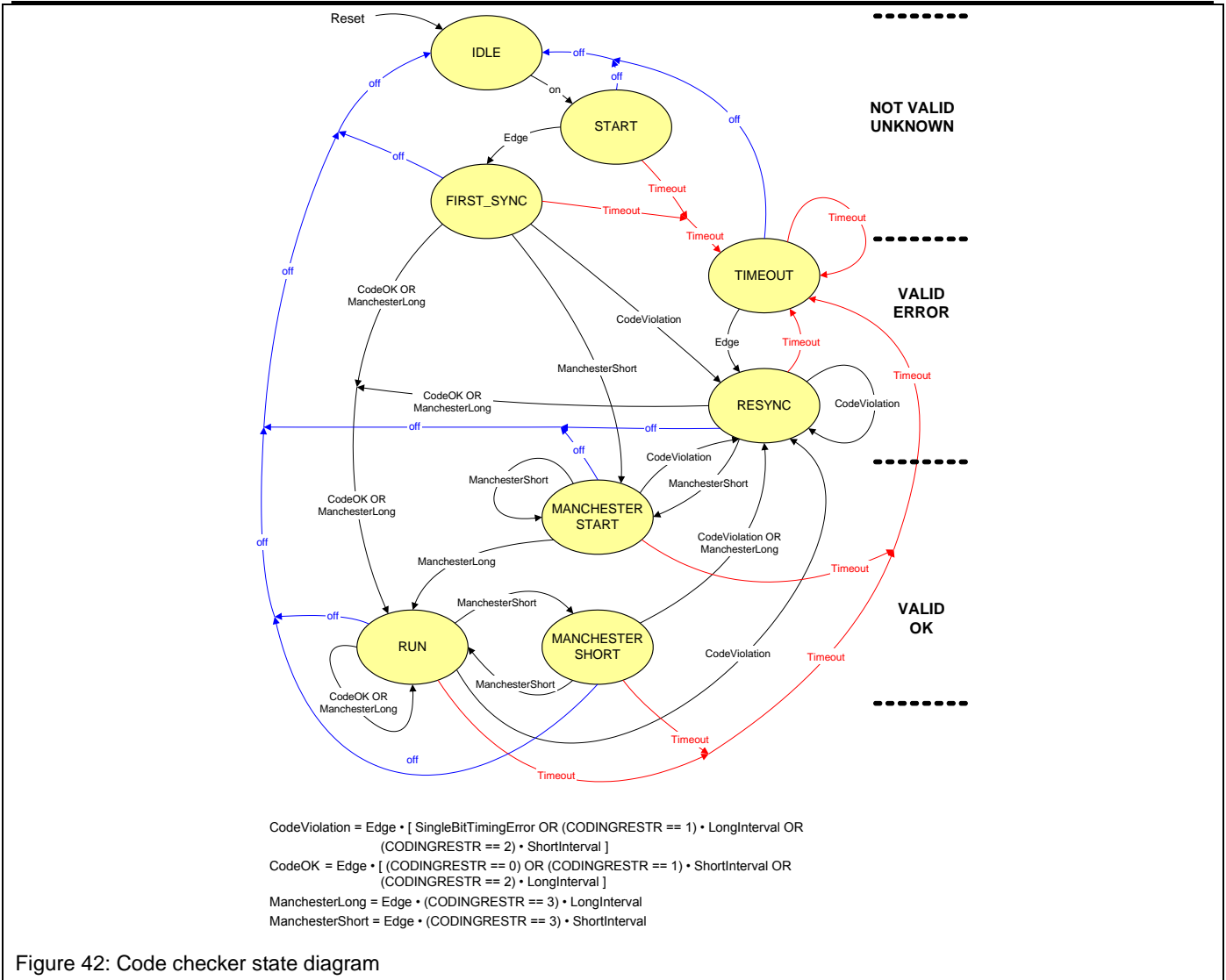
Figure 42: Code checker state diagram

The timeout is derived from the chip timing verification block, i.e. a timeout is generated, if a bit exceeds a length of 3.5*chip width.

The OK/ERROR information is directly derived from the state machine. The RESYNC state is initiated after a code violation is recognised by any of the other states, unlike the Chip Timing verification block which only enters the RESYNC state after the occurrence of a timeout.

With both CODINGRESTR bits set it is only possible to differentiate between a run of zeros or a run of ones (short time intervals) if the first long time interval is received, thus determining if the data represents a 01 or a 10 transition. Once the long time interval has been received the remaining sequence can be checked against Manchester coding rules. After a long interval has been detected, the short intervals should always come in pairs. E.g. the

following would be an illegal sequence. SSSSSLLSSLSSSSSLSSSL.

10.3.4.3 Baud Rate Checker

An averaging facility is implemented increase the accuracy of the single time interval check baud rate detection by a factor of 4. This averaging is performed on blocks of 8 bits, where the first block is started whenever the chip timing block reaches either FIRST_SYNC state or RESYNC state. Proper timing of a single bit is a prerequisite for the baud rate checker, therefore averaging is restarted if a single bit timing error occurs.

The baud rate checker has no information about the coding of the signal. Thus it is possible that a sequence of 8 bits comprises 17 instead of 16 chips, e.g. if 15 short intervals followed by one long interval are to be examined. If a

Integrated UHF Transceiver

sequence of several 8 bit blocks is assessed the accumulated timing uncertainty is never more than 1 chip.

Averaging over 16 chips would require dividing the sum of the individual timing errors by 16, thus causing an unnecessary loss of precision. Therefore the division is omitted and only the timing errors are summed during an 8 bit block. The product of the 8 bits is compared against a limit, which can be selected with SUMBITTMGERRTH according to the following table.

This block can be easily extended to allow adjusting the number of observed bits, which can be 8, 16, 24 or 32 bits according to the baud rate observation length setting BROBSLENGTH.

The output of the baud rate checker will only be VALID after the absolute value of the sum of the received 8 bits is checked against the limit. The output immediately signals an ERROR if the limit is violated. If the value of the sum is within the limit the measurement proceeds until either a limit violation is detected or the requested number of bits have been observed. In the latter case the output becomes VALID and signals OK.

The baud rate checker continues checking on an 8 bit base after the requested number of bits was successfully checked. The ERROR signal is updated at the end of every 8 bit sequence. It stays VALID and OK as long as the baud rate is within the limit. If the baud rate is out of the limit, an ERROR is signalled and the baud rate checker starts over again. The ERROR signal is retained as long as no 8 bit sequence is within the limit. If the selected observation length is greater than 8 bits, the baud rate checker enters the NOT VALID state as soon as the first correct 8 bit sequence is received and finally signals VALID and OK after successful reception of the selected observation length. This mechanism assures that the baud rate checker can only signal VALID and OK once the selected number of consecutive bits have been received with the correct baud rate.

A timeout or a single bit timing error resets the baud rate checker immediately whereon NOT VALID is signalled instantaneously and the baud rate checker starts over.

10.3.5 Timeout Timer for the Wakeup Search

The control logic includes a timeout timer for the Wakeup Search operation. When used, this timer will generate a negative wakeup detection outcome providing a positive wakeup detection is not generated prior to the expiration of the timer. When this timer is disabled, the outcome of the wakeup search operation is instantly negative upon a failure signal from any of the detection operations.
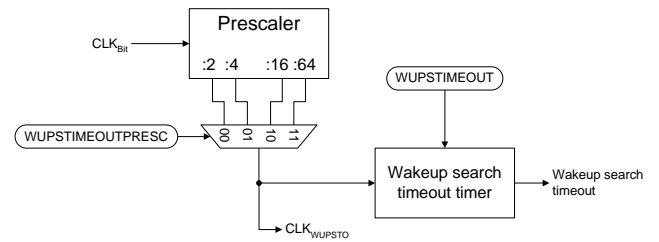
Figure 43: Schematic of wakeup search timeout timer

The wakeup search timer consists of a prescaler and a timer register. The clock is derived from the mainscaler clock and is therefore associated with the selected baud rate.

The actual timeout can be selected with the 6 bit field WUPSTIMEOUT and calculates to WUPSTIMEOUT * T_{WUPSTO} for WUPSTIMEOUT = 1…63.

The value WUPSTIMEOUT = 0 disables the timeout timer and selects an infinite timeout.

The generated timeout has an uncertainty of $-2…0\ T_{Bit}$ regardless of the setting of WUPSTIMEOUTPRESC and WUPSTIMEOUT.

Resolution and range of the timeout timer:

For the fast bit rate of 50 kbit/s the timeout can be adjusted in a range of 40 µs up to 80 ms with a resolution of 40 µs, 80 µs, 320 µs, and 1.28 ms, respectively.

For a bit rate of 1 kbit/s the timeout can be adjusted in a range of 2 ms up to 4 s with a resolution of 2 ms, 4 ms, 16 ms, and 64 ms, respectively.

10.3.6 Wakeup search logic

The following table shows a summary of the signal monitoring conditions which can be used as 'wakeup' criteria.

59

Integrated UHF Transceiver

block name	processes the signal	started by	output becomes valid after	can be restarted by
RSSI level classification	cooked RSSI		input is valid	
Modulation amplitude classification	demodulated baseband	start of wakeup search	2 chips	
Slicer	demodulated baseband	start of wakeup search, only if initial acquisition is enabled	2 bits if initial acquisition, otherwise immediately	timeout from chip timing verification, only if enabled and in mode 2
Chip Timing verification and code checker	slicer output	slicer output valid after start of wakeup search	$0 < t < 5$ chips (2 chip timeouts)	in mode 2 by the slicer, only if initial acquisition is enabled
Baud rate checker	slicer output	FIRST_SYNC or RESYNC of the Timing verification after start of wakeup search	8 bits $\leq t \leq$ configured observation length (8, 16, 24 or 32 bits)	in mode 2 by the Chip timing verification with another FIRST_SYNC or RESYNC
Wakeup search timer		start of wakeup search	FAIL after configured timeout	

Table 18: Overview of (signal monitoring) means

At the beginning of a wakeup search the following blocks are reset:

- wakeup search timer

- modulation amplitude classification

- chip timing verification and code checker

- baud rate checker

- and conditionally the slicer

The slicer is only reset if it has been configured to acquire the value from the slicer initialisation register (SLICERINITSEL not equal to 00b). If the initial acquisition is selected for the slicer, the chip timing verification, code checker block and baud rate checker are held in the reset state for the duration of the slicer initial acquisition mode.

The register SIGMON_EN_W provides enable bits, which determine signal monitors that are considered for the overall wakeup detection decision. All signal monitors operate regardless of these enable bits and, after the wakeup search has finished, their results are available in the corresponding status bits. The following sections describe how the individual results from the several signal monitors can be combined in order to achieve an overall wakeup decision.

Each of the signal monitors can have an invalid period, caused by an initialisation or resynchronisation, during which the output result is not considered. The logic depicted in Figure 44: Creation of PASS/FAIL information from one signal monitor, shows how this information is translated into the PASS/FAIL condition used by the wakeup search logic. If a signal monitor is in its invalid state, neither a PASS or FAIL condition is generated. If a signal monitor is not selected for the wakeup search, the FAIL is always zero and the PASS always one. These signals PASS and FAIL are exclusively used for the wakeup search logic and they must not be confused with the actual state of the corresponding signal monitor, i.e. signals VALID and ERROR, which can be observed at registers SIGMONSTATUS and SIGMONERROR.
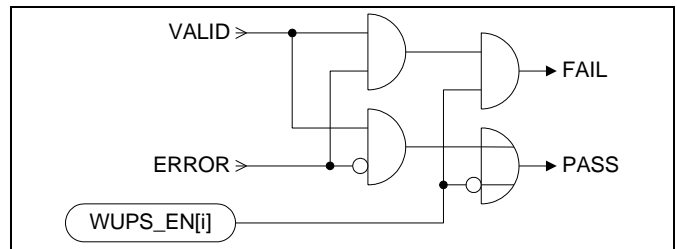
Figure 44: Creation of PASS/FAIL information from one signal monitor

Two different mechanisms are provided for the wakeup search:

- 'pessimistic wakeup search': in this document also referred to as mode 1

- 'optimistic wakeup search': also called mode 2

In the pessimistic wakeup search (mode 1) the wakeup search timer has no meaning and therefore does not influence the result. In the optimistic wakeup search (mode 2) the wakeup search timer is always active.

Integrated UHF Transceiver
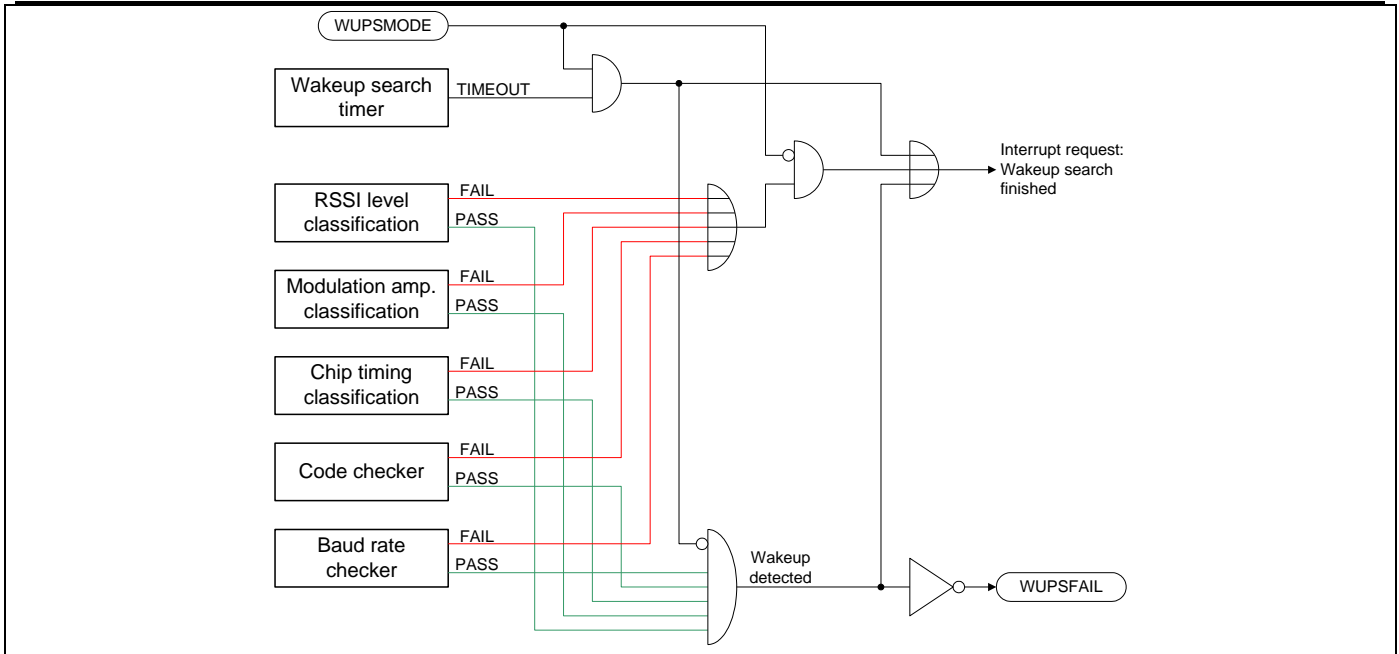
Figure 45: Block diagram for wakeup search.

At the end of the wakeup search an interrupt request is generated and the result is stored in bit WUPSFAIL. If this bit is set, it signals that the wakeup criteria were not met. Otherwise it is cleared. The content of this bit is undefined prior to first use of the wakeup search.

The polarity of the bit WUPSFAIL has been chosen in a way so that the register SIGMONSTATUS can be used as a mask for register SIGMONERROR when the host controller is interested in retrieving the cause of an unsuccessful wakeup detection. If the wakeup search was successful, hence bit WUPSFAIL is cleared, the content of register SIGMONERROR does not need to be considered as all relevant bits will be cleared.
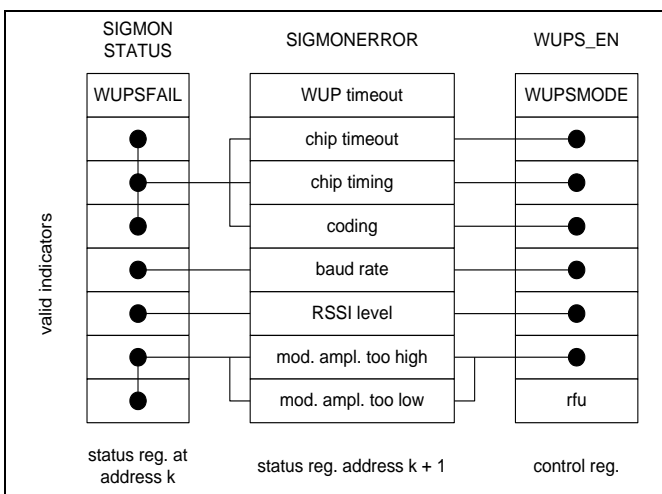
Figure 46: Wakeup search registers

10.3.6.1 Sampling the signal monitoring status

Since the information from the OL2381's signal monitoring means is made up of more than 8 bits, it is desirable to provide a mechanism, which ensures that the controller can always retrieve a consistent set of status information. Therefore the OL2381 provides three status registers, SIGMONSTATUS, SIGMONERROR and RSSILEVEL, into which the status is simultaneously transferred, whenever it is either actively requested by the controller or automatically saved by the wakeup search logic.

There are two cases in which the status is sampled:

1. after a Read command, regardless of the address that will follow, but only if the bit STATAUTOSAMPLE is set

2. always at the end of a wakeup search

The bit STATAUTOSAMPLE allows software to control the sampling of the status information with each read command (1) or whether the status should be unaffected by any read command (0). This allows reading a consistent set of status information as shown in the following two example sequences of Read and Write commands.

61

Integrated UHF Transceiver

Example 1: using Single Byte Reads

Command	Description
Write (STATAUTOSAMPLE, 1)	enable sampling the status with the next Read
Read (SIGMONSTATUS)	this samples the consistent status
Write (STATAUTOSAMPLE, 0)	disable sampling the status with the next Reads
Read (SIGMONERROR)	consistent with line 2
Read (RSSILEVEL)	consistent with line 2
Read (SIGMONSTATUS)	reads the same as line 2
Read (RSSILEVEL)	reads the same as line 5
Read (SIGMONERROR)	reads the same as line 4

The SIGMONSTATUS, SIGMONERROR and RSSILEVEL status is only sampled in line 2. Single Byte Read commands (lines 4 and 5) only transfer the previously sampled status once the STATAUTOSAMPLE bit has been set back to '0'. Lines 4 through to 8 do not change the contents of the registers, because sampling the status has already been disabled.

Example 2: using the address auto-increment of the Read command

Command	Description
Write (STATAUTOSAMPLE, 1)	enable sampling the status with the next Read
Read (SIGMONSTATUS, SIGMONERROR, RSSILEVEL)	Using the address auto-increment feature, the status is sampled at the beginning of the Read command and then, since the status registers occupy adjacent addresses, the continuous reading of these bytes transfers the consistent status to the controller.

The STATAUTOSAMPLE bit is automatically set to 0 at the end of a wakeup search. This guarantees that the important wakeup search results are retained until they have been transferred to the controller. It can also be automatically set to 1 whenever the status register (RSSILEVEL) is transferred to the controller, providing the bit AUTOSAMPLEMANUAL is in the cleared state. This grants the following scenario, following a wakeup search: the status information is automatically sampled and stored in the status registers until the last status register (RSSILEVEL) has been read. The controller can now continue polling the signal monitors without explicitly switching the status into 'live' mode, because reading the RSSILEVEL register has automatically set the STATAUTOSAMPLE bit. Please note that further consistent status polling requires the address auto-increment feature to continue being used.

If automatic entry to 'live' mode is undesired, the AUTOSAMPLEMANUAL bit can be set to keep the bit STATAUTOSAMPLE under software control. It should be noted that STATAUTOSAMPLE is always cleared after finishing a wakeup search. This is necessary to guarantee that the wakeup search results are unconditionally sampled and saved until the controller has acquired them.

10.3.6.2 Evaluating the wakeup search result

The bits in the register SIGMONSTATUS provide the VALID information for the signal monitors. If a VALID flag is zero, the corresponding bit in the register SIGMONERROR is also zero. The SIGMONERROR bit is set if an error has occurred.The failing signal monitor can be identified by reading the SIGMONERROR register. Calculating the expression SIGMONSTATUS & ~SIGMONERROR will indicate which signal monitors provided a pass result.

62

Integrated UHF Transceiver

11 Data Reception

11.1 Preamble detection

A preamble detection can be issued upon completion of a wakeup search or at any time when expecting a frame. The preamble pattern can be configured with a length between 1 and 32 chips. The preamble length is set with the PREA_LEN control bits. If PREA_LEN is set to 0 a length of 32 chips is used. The bit-error rate of the Preamble can be configured with the PREA_TOL register.

11.2 Receive Data decoding

After a wakeup search and if configured, a preamble detection the data reception follows seamlessly. After successful completion of the wakeup-search and the preamble detection the receive data is switched to the corresponding port pins (dependent on the device configuration). The data-pin is kept low during wakeup search and high during preamble detection. Data reception can be interleaved with SPI commands. Details can be found in section 9.10. The device has a Manchester code recovery feature which enables inversion of the received data. The precondition of this code recovery unit is the full reception of a Manchester data-stream with at least one polarity change within the code. The accumulated sum of data changes within a chip can be found in the MANCHESTER_COUNT field in EXTRXSTATUS register. This is a 4-bit signed number which is applicable only when receiving data through the Manchester decoder. It should not be needed when the frame start is properly synchronised with a preamble detection. If data reception is initiated with the DATA sub-command (without a preamble detection), the Manchester decoding starts at the first chip it gets, without knowing whether this is the left or the right bit half. The receive data line could deliver the data correctly or inverted. If the signal contains any bit transitions, this counter counts up if the transition occurs at the assumed bit boundary (i.e. when it is correct) and it counts down if the transition occurs in the middle of the assumed bit grid (i.e. when it is incorrect). The result is that bit 3 of this counter is zero if the data is decoded properly and it is 1 if the data is delivered inverted. The whole counter stays at zero if the received signal contains no bit transitions in which case it is not possible to tell whether the received data is a long runs of only zeros or a run of ones. If the sum is negative, the received code has to be treated as inverted, if the sum is positive, the data-reception was correct. It is possible to invert the receive data stream by setting the bit INV_RX_DATA. See also clock-recovery.

If the receiver is configured in a transparent way the data pin is directly switched to the selected data-slicer and mapped to the corresponding port-pin after the receive command is issued.

11.3 Receive Clock generation

After a wakeup search and if configured, a preamble detection and clock recovery operate in parallel. Sufficient settling time should be allowed from the beginning of data reception to the successful recovery of a stable clock. The run-in time (wakeup time and length of preamble) should be longer than the programmed settling time and no code timing violations should occur in between the different phases to ensure correct operation. After successful completion of the wakeup-search and the preamble detection the bit or chip-clock is switched to the corresponding port pin (dependent of the device configuration). During wakeup search and preamble detection the clock pin is kept at a constant high. Data reception can be interleaved by SPI commands. Details can be found in section 9.10.

If the RX_MANCHESTER bit is set, the clock rate is set to the bit-rate so that every second chip is sampled at the correct time. This enables the micro-controller to directly decode the Manchester bit-stream by sampling the received data with the negative clock edges.

If the receiver is configured in a transparent mode the clock pin is directly switched to clock recovery and mapped to the corresponding port-pin after the receive command is issued.

Integrated UHF Transceiver

12 Digital Signal Processing (Rx)

12.1.1 FM Demodulator

The FM demodulator consists of a discrete delay line and an XOR gate. This principle has been selected, because it features perfect linearity over the full input frequency range. The FM demodulator takes the limited IF I signal and optionally also the Q signal as its input and produces a square-wave-like output signal whose time varying average – the low frequency component – is directly proportional to the input frequency. The diagram below shows a detailed block diagram of the FM demodulator.
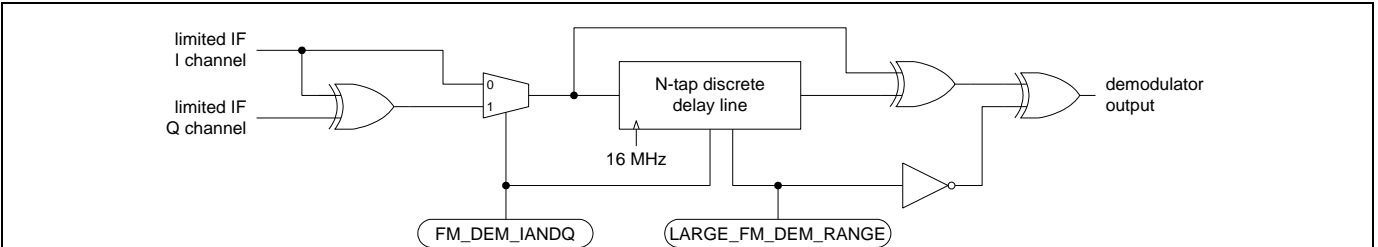
Figure 47: XOR FM demodulator

If the bit FM_DEM_IANDQ is set to 0, only the limited I channel IF input is used for demodulation. In this case the demodulator is set to a centre frequency of 300 kHz. If the bit FM_DEM_IANDQ is set to 1, the I and the Q signals, which have a phase difference of 90°, are combined with an XOR gate. In these circumstances the demodulator is set to a centre frequency of 600 kHz as the I and Q combination has the effect of doubling the frequency.

If the input frequency is within the specified range, the average value of the second XOR's output is a perfectly linear function of the input frequency.

If the bit LARGE_FM_DEM_RANGE is cleared, the input frequency range of the FM demodulator is between 200 and 400 kHz. This is the appropriate setting for frequency deviations up to ±100 kHz. If this bit is set to 1, the input frequency range is extended to between 0 and 600 kHz, allowing for process frequency deviations, which are is only limited by the analogue channel filter. The demodulator output noise will increase by the same factor (3) as the frequency range in these circumstances.

Switching to the large input frequency range is achieved by cutting the length of the delay line into one third of its original value. However, this also changes the slope of the output characteristics from positive to negative thereby inverting the demodulator output. The third XOR compensates for this inversion.

D7	D6	Centre Freq (KHz)	Input Freq. range (KHz)	Max. Freq. Dev. (KHz)	No. of Delay Elements
0	0	300	200-400	±100	40
0	1	300	0-600	±300	13
1	0	600	200-400	±100	20
1	1	600	0-600	±300	7

Table 110: FM Demodulator Configurations

Baseband filter

The baseband filter serves the following purposes:

1. suppresses the high frequency (square-wave) components from the FM demodulator, leaving only the time-varying average, or baseband component, of the demodulated signal

2. suppresses spectral portions of the quantization noise from the demodulator and the demodulated noise coming from the RF input, which do not fall into the baseband signal's bandwidth

3. helps to decimate the sampling rate to that which is suitable for further processing of the baseband signal

The baseband filter is a 3rd order IIR filter topology, which has been optimized such that it features a step response with almost no ringing (see figure 49).

RX baseband configuration

The filter has been split into a 1st order and a 2nd order section in order to minimize the internal quantization noise. The following block diagram shows that the baseband filter is distributed over two filter blocks.
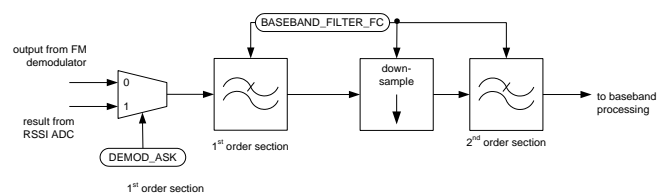
Figure 48 Baseband filter signal flow

The 1st and 2nd order sections combine to make the 3rd order baseband filter for ASK or FSK. The cut-off frequency of this filter is controlled by the BASEBAND_FILTER_FC register control bits. The 1st order section filters the RSSI information, which has been sampled with the ADC in the

64

Integrated UHF Transceiver

limiter/RSSI analogue circuitry. Its cut-off frequency can be controlled separately by the RSSI_FILTER_FC register.

It should be noted that the baseband filter and the RSSI filter are two separate filters.

The following figures 49 and 50 show the step response and the frequency response of the baseband filter, respectively. figure 49 shows that the step response has an

'undershoot' (negative overshoot) of approximately 3% and an overshoot which is almost unnoticeable. This demonstrates a characteristic close to that of an analogue Bessel filter. Figure 50 contains one frequency response curve for each of the ten implemented cut-off frequency control values (0 thru 9).

65

Integrated UHF Transceiver

Figure 49 Step response of the baseband filter

Figure 50 Frequency response of the baseband filter
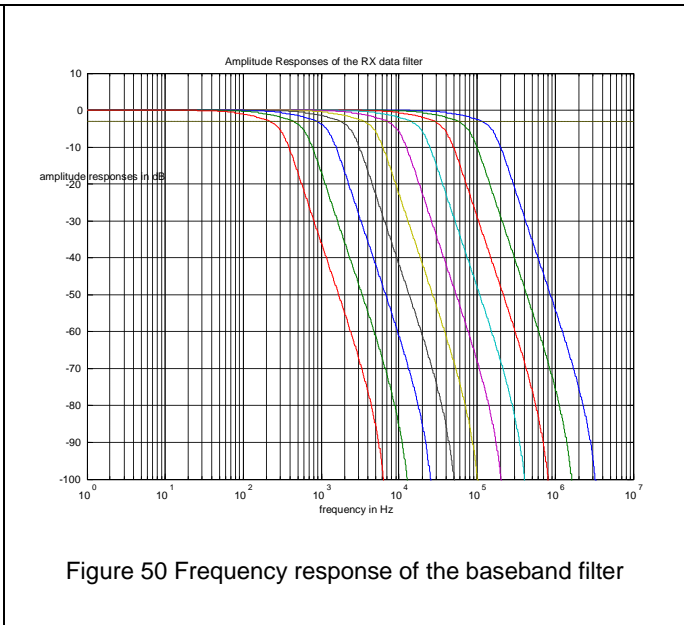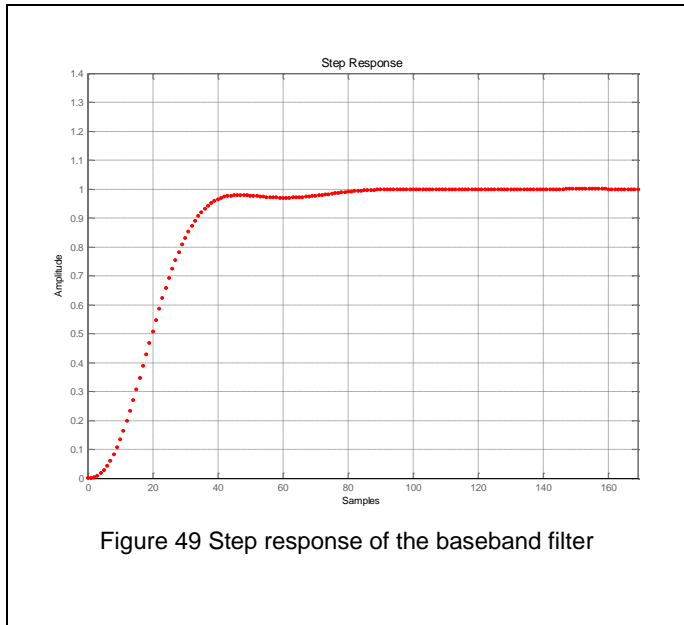
The accurate output sampling frequency of the data filter can be calculated. The frequency is divided by a factor of 2 when the cut-off frequency control setting is incremented by 1. The relevant formula is

$$f_c \approx \frac{114\,kHz}{2^{FskFilterFc}}$$

It can be seen that each increment in the cut-off frequency control setting divides the corner frequency of the filter by approximately a factor of 2.

D3	D2	D1	D0	cut-off frequency f_c	down-sampling factor	output sampling rate
0	0	0	0	115.45 kHz	2	8 MHz
0	0	0	1	57.174 kHz	4	4 MHz
0	0	1	0	28.405 kHz	8	2 MHz
0	0	1	1	14.204 kHz	16	1 MHz
0	1	0	0	7.0795 kHz	32	500 kHz
0	1	0	1	3.5400 kHz	64	250 kHz
0	1	1	0	1.7701 kHz	128	125 kHz
0	1	1	1	885.12 Hz	256	62.5 kHz
1	0	0	0	442.59 Hz	512	31.25 kHz
1	0	0	1	221.31 Hz	1024	15625 Hz
…	…	…	…	undefined	undefined	undefined

Table 19: BASEBAND_FILTER_FC definition.

66

Integrated UHF Transceiver

13 RXD Debug Interface

If the digital scan test is not active and if the channel filter multi-tone test is not active (CF_MULTITONE_EN = 0), setting the register field RXD_DBG_SEL to a nonzero value switches the ports P10/DATA/TEST4, P11/INT/TEST5 and P12/CLOCK into receiver digital debug mode. In this mode the normal function of these pins is overwritten with the function of a fast 3-wire synchronous serial transmission, where

- P12/CLOCK outputs the 16 MHz serial clock.

- P10/DATA/TEST4 outputs the serial data.
  This data changes with the rising edge of the 16 MHz clock and it is stable at the falling edge of the clock.
  Each data word consists of 16 bits.
  Words are transmitted starting with the MSBit and ending with the LSBit.

- P11/INT/TEST5 outputs a synchronization pulse for each serial 16-bit data word. This line goes high during transmission of bit 0, which is the last bit of each word. After the pulse transmission continues with the MSBit of the next 16-bit word.
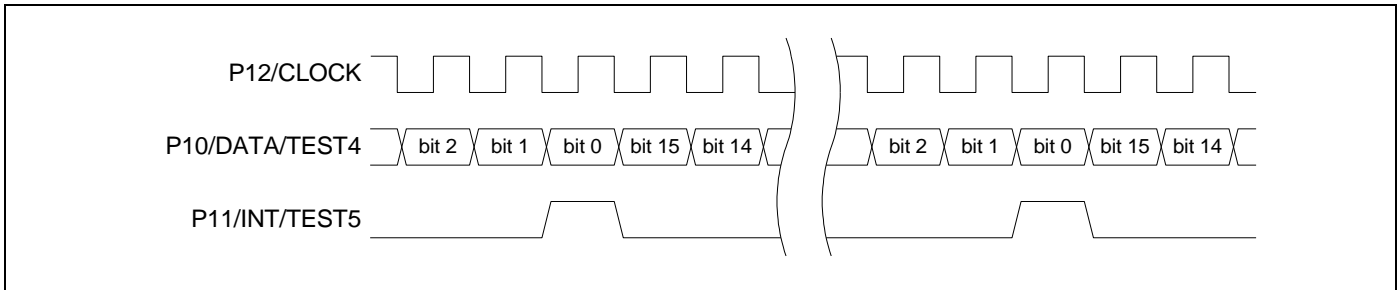
Figure 51: Data transmission on the receiver digital debug interface

67

Integrated UHF Transceiver

Register field RXD_DBG_SEL determines which 16-bit signal vector is sampled in parallel at 1 Msamples/s and output as a serial data stream as shown above. The following table lists the available debug signal vectors.

RXD_DBG_SEL	bit range	signal name	signal description
1	[15:8]	w8RssiLevelOut	Cooked RSSI result as it can be retrieved through the status register RSSI_LEVEL
1	[7]	wIFSettledIn	Indicates when the 300 kHz IF signal is declared stable
1	[6]	wRssiSettled	Indicates when the RSSI result is declared stable
1	[5:0]	r6RawRssiAdcValOut	Raw RSSI ADC readings
2	[15:4]	w12FiltdRssi	RSSI signal after the 1st order low-pass filter
2	[3]	rFrontEndGainLoOut	Indicates which of the front-end gain settings are applied. 0: RX_HI_GAIN, 1: RX_LO_GAIN
2	[2]	wRssiGtUpperTh	Indicates when the RSSI result is greater than the threshold set with UPPERRSSITH
2	[1]	wRssiLtLowerTh	Indicates when the RSSI result is less than the threshold set with LOWERRSSITH
2	[0]	wRssiOutsideLimitsOut	Indicates when the RSSI is outside the limits defined with both LOWERRSSITH and UPPERRSSITH.
3	[15:4]	w12DataFilter1Res	Baseband signal after the 1st order part of the baseband filter
3	[3]	wLimIfIIn	Digital IF input from the I channel limiter
3	[2]	wLimIfQIn	Digital IF input from the Q channel limiter
3	[1]	wRawXorFmDemod	Raw, unfiltered output from the XOR FM demodulator
3	[0]	wIFSettled	Indicates when the 300 kHz IF signal is declared stable
4	[15:1]	w15BasebandSig	filtered and interpolated baseband signal
4	[0]	wBasebandValid	Indicates when the baseband signal is declared valid
5	[15:1]	w15SlicerInitThrRegOut	Contents of the initial slicer threshold register. This is the same as it is available through the SLICERINITTHR_LO and SLICERINITTHR_HI registers.
5	[0]	wLoadInitSlicerThr	Indicates when the initial threshold register is re-loaded. For chip rates > 7812 chip/s this pulse is shorter than the sampling interval and so pulses may be missed.
6	[15:1]	w15SlicerThr	Threshold of the level slicer.
6	[0]	wLoadSlicerThr	Indicates when the threshold is re-loaded. For chip rates > 7812 chip/s this pulse is shorter than the sampling interval and so pulses may be missed.
7	[15:8]	ws8ClkRcvPllPhaseError	Signed clock recovery phase error measurement value in offset binary format.
7	[7:0]		always zero (Reserved)
8	[15]	wRxFrame	Indicates when data is being received
8	[14]	wRxData	Received data sampled with wRxClock and optionally Manchester decoded
8	[13]	wRxClock	Recovered bit clock
8	[12]	wPatternMatch	Raw pattern match indicator from the preamble detection block
8	[11]	wChipClock	Raw chip clock from the clock recovery PLL
8	[10]	wEdgeDetected	Edge detector output from the deglitcher. For chip rates > 7812 chip/s these pulses are shorter than the sampling interval and so pulses may be missed.
8	[9]	wDeglitchedLevel	Output from the deglitcher block.
8	[8]	wDeglitchedLevelValid	Indicates when the deglitcher output and the edge detector output are valid
8	[7]	wSlicerResult	Result from the selected slicer
8	[6]	wSlicerReady	Indicates when the selected slicer is ready to deliver a valid signal
8	[5]	wSlicerValid	Indicates when the selected slicer actually delivers a valid signal
8	[4]	wBasebandValid	Indicates when the baseband signal is declared valid

Integrated UHF Transceiver

8	[3]	wRxRdyOut	Indicates when the receiver hardware is ready and the baseband signal has stabilized. This is the same as the RX_RDY bit in the DEVICE_STATUS register.
8	[2]	wIfSigSettledTo2ndOrderFilt	Indicates when the IF signal is declared stable. This signal is principally the same as the next one but it has been made longer so that it can be processed with a slower clock.
8	[1]	wIfSigSettled	Indicates when the IF signal is declared stable
8	[0]	wRxAnaRdy	Indicates when the analogue receiver hardware is ready (powered up and calibrated)
9	[15]	wCmdTimeout	Indicates when a timeout occurs during a wakeup search or a preamble detection
9	[14]	wSigMonFail	Is 1 when the enabled signal monitors indicate a fail condition
9	[13]	wSigMonPass	Is 1 when the signal monitors indicate a pass condition
9	[12]	wCmdTimeoutEn	Indicates when the command timeout counter is active
9	[11]	wCTVTimeout	Indicates a chip timing verification timeout (no edges for more than (3.5 - REDUCED_CHIP_TIMEOUT) times the chip duration)
9	[10]	wSingleBitTmgError	Single chip timing error (the interval between two edges exceeds the limits defined with SGLBITTMGERRTH)
9	[9]	wCodeCheckerError	Indicates that the code checker detected an error
9	[8]	wCTVValid	Valid signal for the chip timing verification block. Indicates the validity of the chip timeout, the single chip timing error and the code checker.
9	[7]	wBaudrateCheckerError	Indicates an error from the baud rate checker.
9	[6]	wBaudrateCheckerValid	Valid signal for the baud rate checker result.
9	[5]	wRssiOutsideLimits	Indicates that the current RSSI result is outside the limits defined by UPPERRSSITH and LOWERRSSITH.
9	[4]	wRssiSettledOut	Indicates when the RSSI result has been declared stable
9	[3]	wSigAmpTooHigh	Indicates that the baseband amplitude (modulation amplitude) is greater than the limit defined with UPPER_MODAMP_TH
9	[2]	wSigAmpTooHighValid	Is the valid indicator for the wSigAmpTooHigh signal
9	[1]	wSigAmpTooLow	Indicates that the baseband amplitude (modulation amplitude) is smaller than the limit defined with LOWER_MODAMP_TH
9	[0]	wSigAmpTooLowValid	Is the valid indicator for the wSigAmpTooLowValid signal
10 through 15			always zero (Reserved)

Table 20: Available receiver debug signal vectors

Integrated UHF Transceiver

14 Special Function Register-Set Summary (Table and description)

All control registers can be accessed via the SPI interface. If a control register contains less than 8 bits, writing to a non-existent bit has no effect and reading from a non-existent bit always returns a zero. Reading from a status register returns the current status of the device. Writing to a status register is ignored by the device.

The SFR map features two register pages. Bytes 0-2Dh and 3Fh are always available, independent of the setting of the bit BANK_SEL in the BANKSEL register (3Fh). Clearing BANK_SEL enables the bytes 2Eh-3Eh of bank 0, the contents of bank 1 remain unchanged. Setting BANKSEL sets bytes 2Eh-3Eh of bank 1 to active.

Some register bits provide information about the implemented state-machines and can alter without SPI transmission, in addition to the status bits, indicated in green in the table below, other bits such as the VCO_SUBBAND can also alter.

The configuration registers remain stable during power-down. When a power on reset occurs (can be evaluated by checking the IF_POR bit in the IFLAG register) the register bits, which are marked with a pink background below, are preset to their default values.

Bits marked as RFU are reserved. These bits can be written and read normally, but do not have any other effect on the device.

ADDRESS			NAME	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Value
Decimal												
	Hexadecimal											
		Visible in Bank										
0	00h	01	FC0L	FC0L				0	0	0	0	0000 0000
1	01h	01	FC0M	FC0M								0000 0000
2	02h	01	FC0H	FC0H								1011 0001
3	03h	01	FC1L	FC1L				0	0	0	0	XXXX XXXX
4	04h	01	FC1M	FC1M								XXXX XXXX
5	05h	01	FC1H	FC1H								XXXX XXXX
6	06h	01	FC2L	FC2L				0	0	0	0	XXXX XXXX
7	07h	01	FC2M	FC2M								XXXX XXXX
8	08h	01	FC2H	FC2H								XXXX XXXX
9	09h	01	FC3L	FC3L				0	0	0	0	XXXX XXXX
10	0Ah	01	FC3M	FC3M								XXXX XXXX
11	0Bh	01	FC3H	FC3H								XXXX XXXX
12	0Ch	01	VCOCON	FORCE_-VCO_CAL	VCO_CAL_RUNNING	VCO_SUBBAND						0?XX XXXX
13	0Dh	01	LOCON	CLK2SCLK_DELAY				SKIP_VCO CAL	LOCK_DET ON	VCO_-BAND	RF_LO_DIV	0000 0001
14	0Eh	01	TIMING0	MAINSCL								0000 0000
15	0Fh	01	TIMING1	WATCHDOG_TIME		PRESC		MAINSCH				0110 0000
16	10h	01	PORTCON0	P11C				P11INV	P10C		P10INV	0010 1000
17	11h	01	PORTCON1	P13C			P13INV	P12C			P12INV	0000 1110
18	12h	01	PORTCON2	SEP_SDO	SEP_RX_-OUT	SEP_TX_-LINES	RFU	RFU	P14C		P14INV	0000 0000
19	13h	01	PWRMODE	0	0	0	POLLTIM_EN	DEV_MODE		PD	RESET	000? 0000
20	14h	01	IEN	IE_TXRX_-RDY	IE_EOF	IE_PREA	IE_WUPS	IE_-POLLTIM	IE_WATCH DOG	IE_BROWN OUT	0	0000 0000
21	15h	01	IFLAG	IF_TXRX_-RDY	IF_EOF	IF_PREA	IF_WUPS	IF_-POLLTIM	IF_WATCH DOG	IF_BROWN OUT	IF_POR	0000 0001
22	16h	01	POLLWUPTIME	POLLWUPTIME								1111 1111
23	17h	01	POLLACTION	POLL_MODE		RX_FREQ		RX_CMD	RX_GAIN		SET_RX_-FLAGS	00XX XXXX

70

Integrated UHF Transceiver

ADDRESS			NAME	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Value
Decimal												
	Hexadecimal											
		Visible in Bank										
24	18h	01	CLOCKCON	MANUAL-PTCAL	PTCALRUNNING	EXTPOLL-TIMRNG	CLKSOURCESEL			EXT_CLK_BUF_EN	XODIS	0?00 0100
25	19h	01	DEVSTATUS	0	PA_ON	PA_PWR_RDY	LO_PWR_RDY	RX_RDY	TX_RDY	LO_RDY	REFCLK_-RDY	0??? ????
26	1Ah	01	FDEV	FDEV_EXP			FDEV_MANT					XXXX XXXX
27	1Bh	01	FRMP	0	FRMP_EXP			FRMP_MANT				0XXX XXXX
28	1Ch	01	ACON0	ASK0	0	AMH0X	AMH0					10X1 1111
29	1Dh	01	ACON1	ASK1	0	0	AMH1					X00X XXXX
30	1Eh	01	ACON2	0	0	0	AML					0000 0000
31	1Fh	01	ARMP	0	ARMP_EXP		ARMP_MANT					0XX0 0000
32	20h	01	TXCON	DOUBLE_SD_RESULT	INV_TX_-DATA RFU	TXCLKSEL RFU	TXCLKOUTSEL RFU		RFU	PAM RFU		0000 0001
33	21h	01	RXGAIN	RX_HI_GAIN				RX_LOW_GAIN				1111 0000
34	22h	01	RXBW	DEMOD_ASK	CF_BW			RSSI_FILTER_FC				X000 XXXX
35	23h	01	GAINSTEP	0	RSSI_GAIN_STEP_ADJ							0XXX XXXX
36	24h	01	HIGAINLIM	HI_GAIN_LIMIT								XXXX XXXX
37	25h	01	UPPERRSSITH	UPPERRSSITH								XXXX XXXX
38	26h	01	LOWERRSSITH	LOWERRSSITH								XXXX XXXX
39	27h	01	RXBBCON	DEGLITCHER_-WINDOW_LEN		BASEBAND_SETTL_TIME		BASEBAND_FILTER_FC				XXXX XXXX
40	28h	01	UMODAMPTH	UPPER_MODAMP_TH_EXP				UPPER_MODAMP_TH_MANT				XXXX XXXX
41	29h	01	LMODAMPTH	LOWER_MODAMP_TH_EXP				LOWER_MODAMP_TH_MANT				XXXX XXXX
42	2Ah	01	EMODAMPTH	EDGE_MODAMP_TH_EXP				EDGE_MODAMP_TH_MANT				XXXX XXXX
43	2Bh	01	RXDCON0	NUM_MODAMP_GAPS_W		SLICERSEL_W		SLICERINITSEL_W		INIT_ACQ_BITS_W		XXXX XXXX
44	2Ch	01	RXDCON1	NUM_MODAMP_GAPS_P		SLICERSEL_P		SLICERINITSEL_PD		INIT_ACQ_BITS_PD		XXXX XXXX
45	2Dh	01	RXDCON2	NUM_MODAMP_GAPS_D		SLICERSEL_D		CODINGRESTR_W		CODING RESTR_P	CODING RESTR_D	XXXX XXXX
46	2Eh	0	SIGMON0	WUPS_MODE	SIGMON_EN_W						0	XXXX XXX0
47	2Fh	0	SIGMON1	EN_PREADET_TIMEOUT	SIGMON_EN_P						ACCU_SIG FAILS_P	XXXX XXXX
48	30h	0	SIGMON2	0	SIGMON_EN_D						ACCU_SIG FAILS_D	0XXX XXXX
49	31h	0	WUPSTO	WUPSTIMEOUTPRESC		WUPSTIMEOUT						XXXX XXXX
50	32h	0	SLICERINITL	SLICERINITTHR_LO								XXXX XXXX
51	33h	0	SLICERINITH	0	SLICERINITTHR_HI							0XXX XXXX
52	34h	0	TIMINGCHK	RFU	BROBSLENGTH		SUMBITTMGERRTH			SGLBITTMGERRTH		XXXX XXXX
53	35h	0	RXCON	STATAUTOSAMPLE	AUTOSAMPLEMANUAL	INV_RX_-DATA	CLOCK_RECOV_TC		RX_MANCHESTER	RX_CLOCK TRANSP	RX_DATA_TRANSP	XXXX XXXX
54	36h	0	RXFOLLOWUP	PREA_FU_TF	PREA_FU_CF	WUPS_FU_TS		WUPS_FU_TF	WUPS_FU_CS		WUPS_FU_CF	1000 1000
55	37h	0	SIGMONSTATUS	SIGMONSTATUS								???? ????
56	38h	0	SIGMONERROR	SIGMONERROR								???? ????
57	39h	0	RSSILEVEL	RSSI_LEVEL								???? ????
58	3Ah	0	PREACON	RFU	PREA_TOL		PREA_LEN					XXXX XXXX
59	3Bh	0	PREA0	PREA0								XXXX XXXX

Integrated UHF Transceiver

Decimal	Hex	Visible in Bank	NAME	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Value
60	3Ch	0	PREA1	PREA1								XXXX XXXX
61	3Dh	0	PREA2	PREA2								XXXX XXXX
62	3Eh	0	PREA3	PREA3								XXXX XXXX
46	2Eh	1	EXTRXSTATUS	RX_HI_GAIN	LIVE_STATUS	RXCMD		MANCHESTER_COUNT				???? ????
47	2Fh	1	CFRCCAL	CF_IQ_CAL_RUNNING	CF_RC_CAL_RUNING	0	0	CF_RC_CAL_RES				??00 ????
48	30h	1	CFIQCAL	START_CF_IQ_CAL	CF_IQ_CALVAL							0000 0000
49	31h	1	EXPERT0	RED_VCO_SWING	LARGE_PLL_RST_DELAY	FASTCF FILTSETTL	PLL_ICP					0000 0100
50	32h	1	EXPERT1	XOSTARTUPDELAY		ASKRST BBMID	RFU	RFU	DISFRAC	LOCK_DET_TIME		0100 1001
51	33h	1	EXPERT2	FM_DEM_IANDQ	LARGE_FM_DEM_RANGE	WIDE_AMPL_WINDOW	REDUCED BIT_TIME	TWORSSIMS BITSSLOW	FASTRSSI FILTSETTL	CAP_RSSI		0000 0010
52	34h	1	EXPERT3	0	0	0	0	RFU	ALLOWRE GSWITCH	LTDIQ PHASECAL	DONOTDIST URBPTCAL	0000 0000
53	35h	1	TEST0	CF_MULTITONE_EN	DIG_TEST_SEL			RXD_DBG_SEL				0110 0000
54	36h	1	TEST1	IQ_TEST_LV	ANA_TEST_SEL			REG_DIG_DIS	PLL_CTRL		VCO_TEST_ON	0000 0000
55	37h	1	TEST2	REG_VCO_ON	REG_PLL_ON	REG_PA_ON	FORCE_REG_VCO_RDY	FORCE_REG_PLL_RDY	FORCE_REG_PA_RDY	FORCE_LOCK_DETECTED	FORCE_XO_RDY	0000 0000
56	38h	1	TEST3	VCO_ON	PRESC_ON	PFD_ON	CLK_PLL_ON	TX_ON	RX_GAP_ON	RX_ON	PA_STEP_TEST	0000 0000
57	39h	1	TEST4	FORCE_CF_RC_CAL	SKIP_CF_RC_CAL	CF_RC_ADJUSTCAL		MAN_CF_RC_CALVAL				0000 XXXX
58	3Ah	1	TEST5	XO_IOFFS			XO_IOFFS SINK_EN	XO_IOFFS EN	XO_KICK_DIS	XO_DET_DIS	XO_BIAS_DIS	XXXX 0000
59	3Bh	1	RFU									0000 0000
60	3Ch	1	TCBEN0									0000 0000
61	3Dh	1	TCBR					IDDQ1	IDDQ0	ASYNCSCAN	SCANEN	0000 0000
62	3Eh	1	TCBEN1									0000 0000
63	3Fh	01	BANKSEL	0	0	0	0	0	0	0	BANK_SEL	0000 0000

Register bit/field is (p)reset at power-on.

Register bit/field is reset when in power-down mode.

Status bit

Not preset

Most of the test Registers are reset on power down. However FC0==FFFFFh THEN the registers are reset with power-on reset. (There are however some exceptions)

Command bit

72

Integrated UHF Transceiver

14.1 Detailed Description of the function registers

The SFR's are divided into two banks. Bank 0 or bank 1 can be selected by setting the BANK_SEL bit in the BANKSEL register (which is visible in both banks) accordingly.

14.2 Registers visible in both Bank 0 and 1

Frequency Configuration Registers

The frequency configuration registers contain the frequency control information for the PLL. Four values can be stored to providing four independent frequency settings available for Tx and Rx purposes. The frequency values are 20 bits long. These 20 bits are divided into 4 least significant bits (L) a medium significant byte (M) and a high significant byte (H).

14.2.1 Register FC0L at address 00h

Reset value = 00h.

Bit	Function	Description	Def
7	FCxL	Low 4bits of 15bit fractional part of the operating frequency value FCx.	0
6			0
5			0
4			0
3	0	0	0
2			0
1			0
0			0

Table 21: Frequency Control register FCxL

This register contains the bits 0 through 3 of the frequency configuration register FC0.

14.2.2 Register FC0M at address 01h

Reset value = 00h.

Bit	Function	Description	Def
7	FCxM	Mid 8bits of 15bit fractional part of the operating frequency value FCx.	0
6			0
5			0
4			0
3			0
2			0
1			0
0			0

Table 22: Frequency Control register FCxM

This register contains the bits 4 through 11 of the frequency configuration register FC0.

14.2.3 Register FC0H at address 02h

Reset value = B1h.

This register contains the bits 12 through 19 of the frequency configuration register FC0.

Bit	Function	Description	Def
7	FCxH	5 Integer bits of operating frequency value FCx.	0
6			0
5			0
4			0
3			0
2	FCxH	High 3bits of 15bit fractional part of the operating frequency value FCx.	1
1			1
0			0

Table 23: Frequency Control register FCxH

14.2.4 Register Space from FC1L at address 03h to FC3H at address 0Bh

All registers Reset value = XXh.

These are the frequency configuration registers FC1, FC2 and FC3.

14.2.5 Register VCOCON at address 0Ch

Bit	Function	Description	Def
7	FORCE_VCO_CAL	starts a VCO calibration unconditionally on µC request. If a 1 is written to this bit, the calibration is started.	0
6	VCO_CAL_RUNNING	indication that the VCO-calibration has been requested or is in progress. The SUB_BAND value, which can be read from this register is valid and stable only when this status bit reads zero	?
5	VCO_SUBBAND	resulting sub-band settings from the automatic VCO calibration, value can be overwritten at any time by the uC. If the value is written during an ongoing calibration, the result will become undefined. A setting of 0 corresponds to the maximum frequency, and 63h to the minimum frequency.	X
4			X
3			X
2			X
1			X
0			X

Table 24: Address 0Ch: VCOCON, VCO control register.

73

Integrated UHF Transceiver

14.2.6 Register LOCON at address 0Dh

Bit	Function	Description	Def
7	CLK2S CLK_DELAY	Delay from the 9th SCLK edge in a Transmit/Receive command until the device starts driving the SCLK line. This is only applicable if SEP_TX_LINES is cleared when sending a Tx command, or SEP_RX_OUT is cleared when sending an Rx command.	0
6			0
5			0
4			0
3	SKIP_VCO_CAL	Automatic VCO Calibration is carried out under the following circumstances: 1. When the active FCxH, VCO_BAND, RF_LO_DIV, DOUBLE_SD_RESULT, DISFRAC changes 2. When the device mode switches from to RX mode 3. When Frequency selection flags A,B change 4. When the PLL is started from idle mode. Calibration under conditions 1, 2 and 3 can be suppressed by setting this bit. Calibration is always executed on PLL start up.	0
2	LOCK_DET_ON	When set, the lock detector will continuously monitor the PLL during operation. When cleared, the lock detector will only monitor the PLL for a short time after VCO Calibration.	0
1	VCO_BAND	For the RF frequency bands below 400MHz, this bit has to be set to 1. For all other bands this should be set to 0.	0
0	RF_LO_DIV	If 0, the VCO freq. is divided by 2 to achieve TX and RX freq. above 500 MHz. If 1, the VCO freq. is divided by 4 to achieve TX and RX freq. below 500 MHz.	1

Table 25: Address 0Dh: LOCON, Local Oscillator control register.

14.2.7 Register TIMING0 at address 0Eh

MAINSCL: Main Scaler Lo Byte of the baud-rate generator, Please see TIMING1 register for an explanation.

14.2.8 Register TIMING1 at address 0Fh

Bit	Function	Description	Def
7	WATCHDOG_TIME	programmable watchdog time-out: $Watchdog\ timeout = \dfrac{2^{15+WATCHDOG\_TIME}}{CLK_{REF}}$	0
6			1
5	PRESC	Prescaler setting of the baud-rate generator. Calculation of the baudrate: $baud\ rate = \dfrac{CLK_{REF}}{2^{PRESC}} \cdot \dfrac{2^{11}+MAINSC}{2^{12}} \cdot \dfrac{1}{128}$ $with\ CLK_{REF}=16\,MHz$ where PRESC is an exponent in the range from 0 through 7 and 2^{11} + MAINSC is the mantissa in the range 2048 through 4095. The resulting baud rate clock can jitter by one prescaler clock cycle CLK_{PSC}.	1
4			0
3			0
2	MAINSCH	3 high bits of the Main Scaler of the baud-rate generator,	0
1			0
0			0

Table 26: Address 0Fh: TIMING1,

14.2.9 Registers PORTCON0, address 10h to PORTCON2 address 12h

General port control information, applicable for all ports:

P1xCx	P1xINV	Function
0…00	X	Port disabled (HIGH Z)
0…01	0	Output zero
0…01	1	Output one
else	0	Alternative port function (not inverted)
else	1	Alternative port function (inverted)

Table 27:General Port Control Information,

14.2.10 Register PORTCON0 at address 10h

Port control of P10 and P11

Bit	Function	Description	Def
7	P11C	Configures P11/INT	0
6			0
5			1
4			0
3	P11INV	Inverts the polarity of the pin if set	1
2	P10C	Configures P10/DATA	0
1			0
0	P10INV	Inverts the polarity of the pin if set	0

Table 28: Address 10h: PORTCON0

D2	D1	Function
0	0	tristate
0	1	constant zero
1	0	Output of PRNG
1	1	reserved

Table 29: Port control with P10C

74

Integrated UHF Transceiver

D7	D6	D5	D4	Function
0	0	0	0	tristate
0	0	0	1	always zero
0	0	1	0	Interrupt request
0	0	1	1	Clock output from clock generation according to settings CLKSOURCESEL
0	1	0	0	CF_IQ_CAL_RUNNING
0	1	0	1	LO_RDY flag
0	1	1	0	RX_RDY flag
0	1	1	1	TX_RDY flag
1	0	0	0	PA_ON flag
1	0	0	1	PA on request
1	0	1	0	Reserved signal, always 0.
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	Test signals controlled by bits DIG_TEST_SEL
1	1	1	1	

Table 30: Port control with P11C

D6	D5	D4	Function
0	0	0	Digital regulator enable
0	0	1	VCO regulator enable
0	1	0	PLL regulator enable
0	1	1	PA regulator enable
1	0	0	XO enable
1	0	1	
1	1	0	
1	1	1	XO startup signal kick A

Table 31: P11C Function (with D5-7=1, D4=0) defined by DIG_TEST_SEL bits D4-6

D6	D5	D4	Function
0	0	0	Signal I from limiter
0	0	1	Channel filter RC calibration enable
0	1	0	Polling timer enable
0	1	1	LSBit of RSSI DAC value
1	0	0	PLL lock detector enable
1	0	1	
1	1	0	reserved
1	1	1	

Table 32: P11C Function (with D5-7=1, D4=1) defined by DIG_TEST_SEL bits D4-6

14.2.11 Register PORTCON1 at address 11h

Bit	Function	Description	Def
7			0
6	P13C	Configures P13/SDO	0
5			0
4	P13INV	Inverts the polarity of the pin if set	0
3			0
2	P12C	Configures P12/CLOCK	1
1			1
0	P12INV	Inverts the polarity of the pin if set	0

Table 33: Address 11h: PORTCON1

D3	D2	D1	Function
0	0	0	tristate
0	0	1	always zero
0	1	0	TX clock output, if bit SEP_TX_LINES = 1 and the transmitter is activated or RX clock output, if bit SEP_RX_OUT = 1 and the receiver is activated.
0	1	1	Clock output from clock generation according to settings CLKSOURCESEL
1	0	0	PLL feedback clock
1	0	1	Polling timer clock (uncalibrated)
1	1	0	Test signals controlled by bits DIG_TEST_SEL
1	1	1	

Table 34: Port control with P12C

D6	D5	D4	Function
0	0	0	Digital regulator brown-out detection
0	0	1	VCO regulator brown-out detection
0	1	0	PLL regulator brown-out detection
0	1	1	PA regulator brown-out detection
1	0	0	XO_RDY
1	0	1	XO startup signal kick A
1	1	0	XO startup signal kick C
1	1	1	

Table 35: P12C Function (with D2-3=1, D1=0) defined by DIG_TEST_SEL bits D4-6

D6	D5	D4	Function
0	0	0	Signal Q from limiter
0	0	1	CF_RC_CAL_RUNNING flag
0	1	0	Uncalibrated polling timer clock
0	1	1	Comparator output of RSSI ADC
1	0	0	PLL lock detector signal (raw)
1	0	1	PLL lock detector signal (digitally filtered)
1	1	0	Continuous 1MHz clock
1	1	1	Constant zero (reserved)

Table 36: P12C Function (with D2-3=1, D1=1) defined by DIG_TEST_SEL bits D4-6

75

Integrated UHF Transceiver

D7	D6	D5	Function
0	0	0	tristate
0	0	1	always zero
0	1	0	modulation signal of the transmitter, including Manchester encoding if applicable. This is a bistate signal, ramp control of the modulator is handled separately.
0	1	1	RX_RDY or TX_RDY
1	0	0	REFCLK_RDY
1	0	1	LO_RDY
1	1	0	RX_RDY
1	1	1	TX_RDY

Table 37: Port control with P13C

14.2.12 Register PORTCON2 at address 12h

Bit	Function	Description	Def
7	SEP_SDO	If set, P13 is tristate or SPI data output. **This then has priority over the normal function of P13.**	0
6	SEP_RX_OUT	If this bit is set and a receive command is active then P10 is 'always' (independent of the P10C settings) used as RX data and P12 is conditionally used as the RX clock output, depending on the P12C configuration.	0
5	SEP_TX_LINES	If this bit is set and a transmit command is active then P10 is 'always' (independent of the P10C settings) used as TX data input and P12 is conditionally used as the TX clock output, depending on the P12C configuration.	0
4	RFU	RESERVED	0
3	RFU	RESERVED	0
2	P14C	Configures P14/PIND	0
1			0
0	P14INV	Inverts the polarity of the pin if set	0

Table 38: Address 12h: PORTCON2

The SEP_xxx bits override all other port settings of P13. Functions configured with P10C are also overridden if SEP_TX_LINES = 1 and the transmitter is activated or if SEP_RX_OUT = 1 and the receiver is activated.

SEP_TX_LINES	Transmitter data input	Transmitter clock output
0	SDIO	SCLK
1	P10/DATA	P12/CLOCK (optional, only if P12C = 010b)

SEP_RX_OUT	Receiver data output	Receiver clock output
0	SDIO or SDO, (depending on SEP_SDO)	SCLK
1	P10/DATA	P12/CLOCK (optional, only if P12C = 010b)

D2	D1	Function
0	0	tristate
0	1	constant zero
1	0	0 in RX_MODE, 1 in TX_MODE, else tristate
1	1	0 in RX_MODE, 1 in TX_MODE, else 0

Table 39: Port control with P14C

14.2.13 Register PWRMODE at address 13h

Bit	Function	Description	Def
7			0
6	0	0	0
5			0
4	POLLTIM_EN	Enable bit for Polling Timer. Initialization occurs on every (power-on) reset. The POLLTIM_EN bit is set to the inverse of the RSTDIS pin. The initial condition of the Polling Timer is therefore controlled by this pin. When set the polling is initially disabled.	?
3	DEV_MODE	Control Bits for Device Mode	0
2			0
1	PD	Power Down Bit	1
0	RESET	Reset Bit	0

Table 40: Address 13h: PWRMODE

General power-mode register

POLLTIM_EN: polling timer enable bit,

D4	Function
0	The polling timer is turned off and it does not draw any current.
1	The polling timer is turned on.

Table 41: Polling Timer Control

RSTDIS	Status of the polling timer after a master reset
0	POLLTIM_EN = 1; the polling timer is activated with the settings POLLWUPTIME = 255 and EXTPOLLTIMRNG = 0.
1	POLLTIM_EN = 0; the polling timer is not activated.

Table 42: Status of the polling timer after a master reset.

Integrated UHF Transceiver

D3	D2	Function
0	0	The crystal oscillator or the external clock buffer is enabled and after the stabilization of the crystal oscillator (if selected) the device is supplied with the reference clock.
0	1	The PLL controlled local oscillator (LO) is enabled. The powering up procedure of the LO includes the VCO sub-band calibration (unconditionally) and a PLL lock-in detection.
1	0	Prepare and enable Receive operation. The LO is enabled and after the PLL has acquired lock, the RX is switched on and enabled.
1	1	Prepare and enable Transmit operation. The LO is enabled and after the PLL has acquired a lock, the TX path and the PA Regulator are switched on and enabled. Although the PA is effectively now switched on, the power control is held at zero, this results in an RF leakage through the PA of approx. -30 dBm RF output.

Table 43: DEV_MODE: these two control bits indicate the actual active device mode.

RESET bit:

Setting this bit brings the device into the power-on state, the same state reached after powering up the device. If this bit is set with a Write command, all other bits, which are simultaneously written to the PWRMODE register, are ignored as the register is forced to the power-on state.

PD (power down) bit:

Setting this bit brings the device into standby mode where it consumes very little power. All analogue receive and transmit circuitry and the XTAL oscillator are turned off. All dynamic digital activity is stopped, except the SPI and the polling timer (if enabled). This bit can also be set automatically when:

- power-on reset or setting the RESET bit

- watchdog timer time out

- on request of the receive state machine.

It should be noted that it is never possible to read this bit as a 1 as the SPI Read command causes the OL2381 to leave power-down mode.

14.2.14 Register IEN at address 14h

Interrupt enable register: the following interrupt sources can be enabled or disabled:

Bit	Function	Description	Def
7	IE_TXRX_RDY	Triggered if either Rx mode or Tx mode is successfully reached after automatic start-up sequences have been issued. **N.B. issuing another Transmit or Receive command does not trigger this interrupt when the device is already in transmit or receive mode, respectively. Only reaching the ready state generates an interrupt.**	0
6	IE_EOF	The EOF is generated in data reception mode if one of the enabled signal monitors detects an unsatisfactory receive signal condition. This is the case when data reception mode is reached either automatically after a successful preamble detection or upon receipt of a DATA Receive command,	0
5	IE_PREA	This is triggered on every completion of a preamble detection, regardless of whether it was successful or not.	0
4	IE_WUPS	This is triggered on every completion of a wakeup search, regardless of whether it was successful or not.	0
3	IE_POLLTIM	Triggered when a polling timer event takes place.	0
2	IE_WATCHDOG	Triggered when a watchdog overflow takes place.	0
1	IE_BROWNOUT	Triggered on brown-out detection of the voltage regulators (under-voltage detection)	0
0	0	0	0

Table 44: Address 14h: IEN

14.2.15 Register IFLAG at address 15h

Interrupt flag register. These bits indicate if an interrupt source has been triggered since last reading this register. This register is always cleared after being read.

Bit	Function	Description	Def
7	IF_TXRX_RDY	set after completion of automatic start-up sequences (Rx or Tx)	0
6	IF_EOF	Please see above.	0
5	IF_PREA	successful preamble detection (non-maskable)	0
4	IF_WUPS	successful wake-up search (non-maskable)	0
3	IF_POLLTIM	polling timer event (non-maskable)	0
2	IF_WATCHDOG	watchdog overflow	0
1	IF_BROWNOUT	under-voltage detection	0
0	IF_POR	first battery power on reset (battery insertion detection). N.B: setting the RESET bit also sets the IF_POR flag.	1

Table 45: Address 15h: IFLAG

Integrated UHF Transceiver

14.2.16 Register POLLWUPTIME at address 16h

Timer setting for polling timer setting:

Bit	Function	Description	Def
7			1
6			1
5		Control register for polling timer The	1
4	POLLW	wakeup time calculates to:	1
3	UPTIME		1
2		T_{WUP} = (POLLWUPTIME + 1) ·	1
1		$T_{WUPTICK}$	1
0			1

Table 46: Sub Address 16h: POLLWUPTIME

The wakeup time of the polling timer can be set with the 8-bit control register POLLWUPTIME. The wakeup time is calculated as follows:

$$T_{WUP} = (POLLWUPTIME + 1) \cdot T_{WUPTICK}$$

where TWUPTICK is either 1 ms or 16 ms, depending on the bit EXTPOLLTIMRNG (extended polling timer range).

14.2.17 Register POLLACTION at address 17h

The POLLACTION register defines which action the device carries out after a polling timer event

Bit	Function	Description	Def
7	POLL_	Defines the operating mode the device	0
6	MODE	is to enter after a polling timer event.	0
5	RX_FR	The RX_FREQ bits have the same	X
4	EQ	meaning as the Receive flags RA and RB (frequency selection).	X
3	RX_CM D	The RX_CMD bit has the same meaning as the Receive flag RC. It allows choosing between a WUPS (0) and a PRDA command (1).	X
2	RX_GAI	The two RX_GAIN bits have the same	X
1	N	meaning as the Receive flags RE and RF (gain step/switch selection bits).	X
0	SET_R X_FLAG S	SET_RX_FLAGS: defines whether the current contents of the RX flag register is used for the automatically initiated Receive command (if 0) or whether the Receive flags RA, RB, RC, RE and RF flags are overwritten with the contents of the RX_FREQ, RX_CMD and RX_GAIN settings of this register, respectively, before the command is actually launched (if 1). If the flags are overwritten, the Receive flag RD is set to 1 in order to make the sub-command either a WUPS or a PRDA command.	X

Table 47: Address 17h: POLLACTION

D7	D6	Function
0	0	After signalling the polling timer interrupt, which is unmaskable, the device remains in power-down mode.
0	1	After signalling the polling timer interrupt, which is unmaskable, the device leaves the power-down mode, which turns the crystal oscillator or the external clock buffer on.
1	0	The device is fully powered up to receive mode. If the polling timer interrupt is enabled, an interrupt occurs either with the polling timer event. Otherwise an interrupt is signalled when the receiver is ready.
1	1	The device is fully powered up to receive mode and after the receiver has settled, a Receive command is automatically initiated as configured with the remaining bits of this register. It is guaranteed that at least one interrupt will occur in the command sequence.

Table 48: POLL_MODE definition

14.2.18 Register CLOCKCON at address 18h

Bit	Function	Description	Def
7	MANUA LPTCAL	manual start of polling timer calibration. Reading of bit MANUALPTCAL will always yield zero. The manual calibration is only executed if the polling timer and the crystal oscillator are running. Otherwise the request is ignored.	0
6	PTCAL RUNNI NG	Set when polling timer calibration is running.	?
5	EXTPO LLTIMR NG	extended timer range for polling timer $T_{WUPTICK}$ = (1 + 15*EXTPOLLTIMRNG) ms	0
4	CLKSO	clock-selection for selected port-pin	0
3	URCES		0
2	EL		1
1	EXT_CL K_BUF_ EN	The external clock buffer enable bit is used to turn on the clock buffer for the external clock. The effect of this bit	0
0	XODIS	depends also on bit XO_DIS	0

Table 49: Address 18h: CLOCKCON

EXTPOLLTIMRNG	Resolution of wakeup counter $T_{WUPTICK}$	Range of selectable wakeup times T_{WUP}
0	1 ms	1…256 ms
1	16 ms	16…4096 ms

Table 50: EXTPOLLTIMRNG definition

Integrated UHF Transceiver

D4	D3	D2	Port Pin
0	0	0	Reference Clock (16MHz)
0	0	1	Reference Clock / 2 (8MHz)
0	1	0	Reference Clock / 4 (4MHz)
0	1	1	Reference Clock / 8 (2MHz)
1	0	0	4* Chip clock
1	0	1	2 * Chip clock
1	1	0	Chip clock
1	1	1	Bit clock

Table 51: CLKSOURCESEL definition

D1	D0	Function
0	0	Crystal oscillator enabled. The digital reference clock is disabled during oscillator start-up.
0	1	Crystal oscillator and external clock buffer disabled.
1	0	Crystal oscillator enabled. The digital reference clock is enabled all the time also during oscillator start-up.
1	1	Crystal oscillator disabled and external clock buffer enabled. The digital reference clock is enabled all the time.

Table 52: EXT_CLK_BUF_EN / XODIS definition

14.2.19 Register DEVSTATUS address 19h

Bit	Function	Description	Def
7	0	0	0
6	PA_ON	When set this indicates that either the PA is turned on by a TX command. This remains set until the ramping-down is completed (if engaged) after the request has been made to terminate the transmission. 0 indicates that the PA is not transmitting (although it might be supplied with power and thus emitting some RF (-30 dBm) due to leakage.	0
5	PA_PWR_RDY	When set indicates that the PA regulator is supplying power to the PA.	0
4	LO_PWR_RDY	When set indicates that the VCO regulator and the PLL regulator are delivering power to the respective parts of the local oscillator.	0
3	RX_RDY	automated receive mode preparation sequence ready, device ready for Rx	?
2	TX_RDY	automated transmit mode preparation sequence ready, device ready for Tx	?
1	LO_RDY	VCO running, PLL settled and locked.	?
0	REFCLK_RDY	XTAL oscillator stable or external clock available (stability of the external clock is not checked by the device).	?

Table 53: Address 19h: DEVSTATUS

14.2.20 Register FDEV address 1Ah

Bit	Function	Description	Def
7	FDEV_EXP	3-bit exponent of the FSK frequency deviation.	X
6			X
5			X
4	FDEV_MANT	5-bit mantissa of the FSK frequency deviation. 0 = no modulation.	X
3			X
2			X
1			X
0			X

Table 54: Address 1Ah: FDEV

This register sets the FSK frequency deviation of the transmitter. Please refer to 8.5.1 for the calculation of the actually applied frequency deviation

14.2.21 Register FRMP address 1Bh

Bit	Function	Description	Def
7	0	0	0
6	FRMP_EXP	3-bit exponent of the soft FSK ramp duration setting.	X
5			X
4			X
3	FRMP_MANT	4-bit mantissa of the soft FSK ramp duration setting. 0 = no ramp (squarewave shaped modulation).	X
2			X
1			X
0			X

Table 55: Address 1Bh: FRMP

This register contains parameters to adjust the FSK ramping (GFSK like modulation), please refer to section 8.5.2.

FRMP_EXP	min(0,4-FRMP_EXP)	min(0,FRMP_EXP-4)	difference = 4-FRMP_EXP)
0	4	0	4
1	3	0	3
2	2	0	2
3	1	0	1
4	0	0	0
5	0	1	-1
6	0	2	-2
7	0	3	-3

Table 56: Effect of the FRMP_EXP setting

79

Integrated UHF Transceiver

14.2.22 Register ACON0 address 1Ch

Bit	Function	Description	Def
7	ASK0	If this bit is set to 1 and if ACON0 is the active configuration set, then ASK modulation is used instead of FSK modulation.	1
6	0		0
5	AMH0X	If the test bit PA_STEP_TEST (TEST3.0) is set, this is the MSBit of the linear 6-bit power control word.	X
4	AMH0	When this power control set is selected for transmission (Transmit command flag F = 0), this becomes the output power control in FSK mode or the power setting when the modulation signal is 0 in ASK mode.	1
3			1
2			1
1			1
0			1

Table 57: Address 1Ch: ACON0

14.2.23 Register ACON1 address 1Dh

Bit	Function	Description	Def
7	ASK1	If this bit is set to 1 and if ACON1 is the active configuration set, then ASK modulation is used instead of FSK modulation.	X
6	0	0	0
5	0	0	0
4	AMH1	When this power control set is selected for transmission (Transmit command flag F = 1), this becomes the output power control in FSK mode or the power setting when the modulation signal is 0 in ASK mode.	X
3			X
2			X
1			X
0			X

Table 58: Address 1Dh: ACON1

14.2.24 Register ACON2 address 1Eh

Bit	Function	Description	Def
7	0	0	0
6	0	0	0
5	0	0	0
4	AML	If ASK modulation is selected, this controls the output power when the modulation signal is 1.	0
3			0
2			0
1			0
0			0

Table 59: Address 1Eh: ACON2

14.2.25 Register ARMP address 1Fh

Bit	Function	Description	Def
7	0	0	0
6	ARMP_EXP	2-bit exponent of the amplitude ramp duration setting ARMP.	0
5			0
4	ARMP_MANT	5-bit mantissa of the amplitude ramp duration setting ARMP.	0
3			0
2			0
1			0
0			0

Table 60: Address 1Fh: ARMP

This register contains parameters to adjust ASK ramping

(soft power on sequence). Please see section 8.4 for further details. These settings are also applied in FSK mode for ramping the carrier up and down at the start and the end of the transmission frame.

14.2.26 Register TXCON at address 20h

Transmitter control register. This register contains several control-bits to select different power-modes and control the PLL and clock-references.

Bit	Function	Description	Def
7	DOUBLE_SD_RESULT	Used to configure the Sigma delta frac-N modulator. For a detailed description please refer to section 7.2.	0
6	INV_TX_DATA	If this bit is cleared, then a data zero produces centre frequency plus frequency deviation in FSK mode and it produces the power value set with AMHx in ASK mode; a data one produces centre frequency minus frequency deviation in FSK mode and it produces the power value set with AML. Setting the INV_TX_DATA bit inverts this assignment. This is valid for NRZ mode and for the first bit half in Manchester mode; during the second half the signal is inverted with respect to the first half.	0
5	TXCLKSEL	select clock source for data-transmission synchronization. When this bit is set the bit clock is used as the transmit clock (CLK$_{TX}$ = CLK$_{BIT}$). If this bit is cleared the chip clock is used as the transmit clock (CLK$_{TX}$ = CLK$_{CHIP}$). If automatic Manchester generation is required the bit clock must be selected.	0
4	TXCLKOUTSEL	Selects the clock output at port pin SCLK or P12/CLOCK.	0
3			0
2	RFU	RESERVED	0
1	PAM	Power mode selection for PA. The PA supply voltage can be selected between 3 different levels, enabling different output power ranges to be selected	0
0			1

Table 61: Address 20h: TXCON

80

Integrated UHF Transceiver

RF_LO_DIV	DOUBLE_SD_RESULT	Offset Value	Frequency resolution	RX frequency offset
0	0	614	488.3 Hz	299.805 kHz
0	1	307	976.6 Hz	299.805 kHz
1	0	1228	244.1 Hz	299.805 kHz
1	1	614	488.3 Hz	299.805 kHz

Table 62: RX frequency offset

D4	D3	Selected clock at SCLK or P12/CLOCK during transmit command
0	0	CLK_{TX}
0	1	twice the frequency of CLK_{TX}
1	0	four times the frequency of CLK_{TX}
1	1	no clock selected

Table 63 Clock output selection for the transmit command, TXCLKOUTSEL

D1	D0	PA Supply	Output power Range
0	0	1.5V	-17 to 10dBm
0	1	1.75V	-13 to 11dBm
1	0	1.95V	-11 to 12dBm
1	1	reserved	

Table 64: PAM definition

The values in the above table were obtained with a fixed matching network, with an output load of 150 Ohm at 900 MHz.

In a specific cases where really low power values (below -10 dBm) are required, the optimum matching network should be adapted.

Power steps of 1 dB (max) are valid only when the output power is above 0 dBm.

14.2.27 Register RXGAIN at address 21h

Gain configuration of the receiver for Hi gain and LO gain mode. If automatic gain switching is activated, the receiver configuration will be automatically changed from HI to LO gain when a certain signal level is exceeded.

Bit	Function	Group	Description	Def
7	RX_HI_GAIN	LNA 1	This register allows the user to program the desired gain for high gain mode. This register includes both RF front-end gain as well as channel filter gain settings	1
6		LNA 0		1
5		CF 1		1
4		CF0		1
3	RX_LO_GAIN	LNA 1	This register allows the user to program the desired gain for low gain mode. This register includes both RF front-end gain as well as channel filter gain settings.	0
2		LNA 0		0
1		CF 1		0
0		CF 0		0

Table 65: Address 21h: RXGAIN

14.2.28 Register RXBW at address 22h

CF Filter bandwidth and RSSI filter settings

Bit	Function	Description	Def
7	DEMOD_ASK	switches input of the digital baseband filter and baseband signal processing chain to the output of the ASK demodulator	X
6	CF_BW	channel filter bandwidth selection bits.	0
5			0
4			0
3	RSSI_FILTER_FC	RSSI corner Frequency selection bits.	X
2			X
1			X
0			X

Table 66: Address 22h: RXBW

D6	D5	D4	Bandwidth
0	0	0	300kHz
0	0	1	200kHz
0	1	0	150kHz
0	1	1	100kHz
1	0	0	75kHz
1	0	1	50kHz

Table 67: Channel Filter Bandwidth Setting

14.2.29 Register GAINSTEP at address 23h

Bit	Function	Description	Def
7	0	0	0
6	RSSI_GAIN_STEP_ADJ	The receiver automatically adds this value to the (filtered and properly scaled) reading of the RSSI whenever it is in low gain mode in order to compensate for the difference (high gain minus low gain). This then seamlessly extends the dynamic range of the RSSI by switching the gain of the receiver chain.	X
5			X
4			X
3			X
2			X
1			X
0			X

Table 68: Address 23h: GAINSTEP

Integrated UHF Transceiver

14.2.30 Register HIGAINLIM at address 24h

Bit	Function	Description	Def
7			0
6			0
5			0
4	HI_GAIN_LIMIT	HI_GAIN_LIMIT control word.	0
3			X
2			X
1			X
0			X

Table 69: Sub Address 24h: HIGAINLIM

This register contains the 8-bit gain switching threshold value. If the RSSI reading exceeds this value during a wakeup search the Rx gain can be switched from RX_HI_GAIN to RX_LO_GAIN automatically, providing it has been programmed to do so (flags E,F = 01b).

14.2.31 Register UPPERRSSITH at address 25h

This register contains the 8-bit upper RSSI threshold level. This value is compared against the cooked RSSI value in the RSSI level classification unit.

14.2.32 Register LOWERRSSITH at address 26h

This register contains the 8-bit lower RSSI threshold. This value is compared against the cooked RSSI value in the RSSI level classification unit.

14.2.33 Register RXBBCON at address 27h

This register controls the Rx baseband configuration bits.

Bit	Function	Description	Def
7	DEGLITCHER_WINDOW_LEN	The purpose of these bits is to control the deglitcher's hold-off time.in order to suppress multiple signal transitions when a noisy baseband signal crosses the slicer threshold.	X
6			X
5	BASEBAND_SETTL_TIME	This 2-bit field adjusts the baseband settling delay. This delay is the time between the IF signal being declared valid and the baseband signal being declared valid. The delay is 2*(1+BASEBAND_SETTL_TIME)*chip duration. The proper adjustment of this delay is especially crucial when operating a wakeup search in pessimistic mode, as the measurement and classification of the signal and should not be started until the whole receiver chain (including the channel and baseband filters) have been settled. The dominant settling time is usually that of the baseband filter and must therefore be taken into account.	X
4			X
3	BASEBAND_FILTER_FC	baseband digital filter cut-off frequency.	X
2			X
1			X
0			X

Table 70: Address 27h: RXBBCON

D7	D6	Deglitcher lock duration
0	0	0
0	1	2/16 of the chip width.
1	0	3/16 of the chip width.
1	1	4/16 of the chip width.

Table 71: DEGLITCHER_WINDOW_LEN definition.

82

Integrated UHF Transceiver

14.2.34 Register UMODAMPTH at address 28h

Bit	Function	Description	Def
7	UPPER		X
6	_MODA	$UPPER\_MODAMP\_TH\_EXP = \max\left(0, \left\lfloor \log_2\left(\frac{UMODAMPTH}{7.75}\right)\right\rfloor\right)$	X
5	MP_TH		X
4	_EXP		X
3	UPPER		X
2	_MODA	$UPPER\_MODAMP\_TH\_MANT = \left\lfloor 0.5 + \frac{UMODAMPTH}{2^{UPPER\_MODAMP\_TH\_EXP}}\right\rfloor$	X
1	MP_TH		X
0	_MANT		X

Table 72: Address 28h: UMODAMPTH

This register contains the 8 bits that make up the Upper Modulation Amplitude measurement threshold level. (Modulation amplitude classification unit). In FSK mode one increment corresponds to approx. 6.2 Hz when LARGE_FM_DEM_RANGE is 0 and approx. 18.6 Hz when LARGE_FM_DEM_RANGE is 1. In ASK mode one increment corresponds to approx. 1.5 dB / 512 = 0.00293 dB.

In FSK mode:

$$UMODAMPTH = F_{DEV} \cdot \frac{1 + \frac{T}{100}}{200KHz*(1 + 2.LARGE\_FM\_DEM\_RANGE)} \cdot 32256$$

Where:
$F_{DEV} = $ Nominal Peak - to - Peak Frequency Deviation (Hz)
$T = $ Tolerance in %

In ASK mode:

$$UMODAMPTH = ASK_{MOD} \cdot \frac{1 + \frac{T}{100}}{1.5} \cdot 512$$

Where:
$ASK_{MOD} = $ ASK modulation amplitude ratio in dB
$T = $ Tolerance in %

N.B. The specified amplitude is peak to peak.

14.2.35 Register LMODAMPTH at address 29h

This register contains the 8 bits that make up the Lower Modulation Amplitude measurement threshold level. (Modulation amplitude classification unit). This register configures the threshold level in a similar way as described for the UPPERMODAMPTH.

In FSK mode:

$$UMODAMPTH = F_{DEV} \cdot \frac{1 - \frac{T}{100}}{200KHz*(1 + 2.LARGE\_FM\_DEM\_RANGE)} \cdot 32256$$

Where:
$F_{DEV} = $ Nominal Peak - to - Peak Frequency Deviation (Hz)
$T = $ Tolerance in %

In ASK mode:

$$UMODAMPTH = ASK_{MOD} \cdot \frac{1 - \frac{T}{100}}{1.5} \cdot 512$$

Where:
$ASK_{MOD} = $ ASK modulation amplitude ratio in dB
$T = $ Tolerance in %

N.B. The specified amplitude is peak to peak.

14.2.36 Register EMODAMPTH at address 2Ah

Bit	Function	Description	Def
7			0
6			0
5	EDGE_		0
4	MODAM	Expected peak modulation value	0
3	P_TH		0
2			0
1			0
0			0

Table 73: Sub Address 2Ah: EMODAMPTH

This register contains the 8 bit that make up the expected peak modulation value used as the amplitude reference value for the edge slicer. This register configures the threshold level in the same way as described for the UMODAMPTH.

In FSK mode:

$$UMODAMPTH = \frac{F_{DEV}}{200KHz*(1 + 2.LARGE\_FM\_DEM\_RANGE)} \cdot 32256$$

Where:
$F_{DEV} = $ Nominal Peak Frequency Deviation (Hz)

In ASK mode:

$$UMODAMPTH = \frac{ASK_{MOD}}{3} \cdot 512$$

Where:
$ASK_{MOD} = $ ASK modulation amplitude ratio in dB

N.B: The specified amplitude is Peak.

14.2.37 Register RXDCON0 at address 2Bh

Register	Nomenclature
RXDCON0	Wake-Up Search Settings
RXDCON1	Preamble-Detection Settings
RXDCON2	Data Reception Settings

Table 74: RXDCON Registers

Integrated UHF Transceiver

Bit	Function	Description	Def
7	NUM_M ODAMP _GAPS _W	This is the maximum expected duration (expressed as a number of chip widths) between any two transitions minus 1. E.g. If the following data stream '0000' were Manchester encoded, the data stream at chip level would appear as '01010101', a transition occurring every single chip width, therefore the value here would be 0.	X
6			X
5	SLICER SEL_W	data-slicer selection for wakeup search phase	X
4			X
3	SLICER INIT_SE L_W	initial initialization mode selection for selected slicer type for wake-up search phase	X
2			X
1	INIT_AC Q_BITS _W	2, 4 or 8 bit averaging on initial acquisition during wakeup search. The initial acquisition updates the slicer initialisation register and the slicer threshold every time after the calculation of 2, 4, and 8 bits.	X
0			X

Table 75: Address 2Bh: RXDCON0

D5	D4	Function
0	0	The edge sensitive slicer is selected.
0	1	The level sensitive slicer is selected. The low-pass filter is not activated, which means that the current slicer threshold, SLICERTHR, is held constant. The initialisation of the slicer threshold is accomplished according to the setting of the SLICERINITSEL_W.
1	0	The level sensitive slicer is selected and the low-pass filter with a time constant of 2 bits (4 chips) is activated continuously. The initialisation of the slicer threshold is accomplished according to the setting of bits SLICERINITSEL_W.
1	1	The level sensitive slicer is selected and the low-pass filter with a time constant of 8 bits (16 chips) is activated continuously. The initialisation of the slicer threshold is accomplished according to the setting of bits SLICERINITSEL_W.

Table 76: SLICERSEL_W Definition

D3	D2	Function
0	0	The slicer threshold is never initialised.
0	1	The slicer threshold is initialised with the content of register SLICERINITTHR at the beginning of a receive event.
1	0	The initial acquisition is accomplished at the beginning of a receive event. The slicer threshold is updated every time a new result is available from the initial acquisition.
1	1	Same as setting 10 but, moreover, the initial acquisition is automatically restarted when a chip duration timeout occurs.

Table 77: SLICERINITSEL definition

D1	D0	No. of Bits over which the slicer threshold is calculated
0	0	0
0	1	2
1	0	4
1	1	8

Table 78: INIT_ACQ_BITS_x

14.2.38 Register RXDCON1 at address 2Ch

Dynamic receive mode configuration register, see also RXDCON0 for detailed explanation of control-bits.

Bit	Function	Description	Def
7	NUM_M ODAMP _GAPS _P	number of expected modulation gaps during preamble detection	X
6			X
5	SLICER SEL_P	data-slicer selection for preamble detection phase.	X
4			X
3	SLICER INIT_SE L_PD	initial initialization mode selection for selected slicer type for preamble detection and data reception.	X
2			X
1	INIT_AC Q_BITS _PD	2, 4 or 8 bit averaging on initial acquisition during preamble detection and data reception. The initial acquisition updates the slicer initialisation register and the slicer threshold every time after the calculation of 2, 4, and 8 bits.	X
0			X

Table 79: Address 2Ch: RXDCON1

14.2.39 Register RXDCON2 at address 2Dh

Dynamic receive mode configuration register, see also RXDCON0 for detailed explanation of control-bits.

84

Integrated UHF Transceiver

Bit	Function	Description	Def
7	NUM_MODAMP_GAPS_D	number of expected modulation gaps during data reception.	X
6			X
5	SLICERSEL_D	data-slicer selection for data reception phase	X
4			X
3	CODINGRESTR_W	wake up search, coding verification unit. Selection of the permitted signal encoding.	X
2			X
1	CODINGRESTR_P	coding restriction selection for preamble detection. When this bit is 0, no restriction, both time intervals (1*chip and 2* chip width) are accepted in an arbitrary order. When this bet is set both time intervals are accepted and the sequence is checked for Manchester coding.	X
0	CODINGRESTR_D	coding restriction selection for data reception. When this bit is 0, no restriction, both time intervals (1*chip and 2* chip width) are accepted in an arbitrary order. When this bit is set both time intervals are accepted and the sequence is checked for Manchester coding.	X

Table 80: Address 2Dh: RXDCON2

D3	D2	Function
0	0	No restriction, both time intervals (1*chip and 2* chip width) are accepted in an arbitrary order.
0	1	Only the short time interval (1*chip width) is accepted.
1	0	Only the long time interval (2*chip width) is accepted.
1	1	Both time intervals are accepted and the sequence is checked for Manchester coding.

Table 81: CODINGRESTR_W Definition.

14.3 Registers visible in BANK0 only

14.3.1 Register SIGMON0 at address 2Eh

Register	Nomenclature
SIGMON0	Wake-Up Search Settings
SIGMON1	Preamble-Detection Settings
SIGMON2	Data Reception Settings

Table 82: Signal Monitoring Registers

Signal monitoring configuration register.

Bit	Function	Description	Def
7	WUPS_MODE	Wakeup Search Mode Selection Bit	X
6			X
5			X
4	SIGMON_EN_W	Selection of signal monitor (signal signature recognition unit) to be activated during wakeup search.	X
3			X
2			X
1			X
0	0	0	0

Table 83: Address 2E: SIGMON0

D7	Function
0	Pessimistic wakeup search (also called mode 1): The wakeup search is finished when either one of the enabled signal monitors signals a FAIL or all enabled signal monitors signal PASS. In the first case the result of the wakeup search is FAIL; in the latter case it is PASS.
1	Optimistic wakeup search (also called mode 2): The wakeup search is finished when either all enabled signal monitors signal a PASS or the wakeup search timer expires. In the first case the result of the wakeup search is PASS; in the latter case it is FAIL.

Table 84: WUPSMODE definition.

Bit	Function	Description (If set)	Def
6	SIGMON_EN_W	enable chip timeout	X
5		enable chip timing check	X
4		enable coding check	X
3		enable baudrate check	X
2		enable RSSI level check	X
1		enable modulation amplitude detection	X

Table 85: SIGMON_EN_W definition

14.3.2 Register SIGMON1 at address 2Fh

Signal monitoring configuration register

Bit	Function	Description	Def
7	EN_PREADET_TIMEOUT	If this bit is set the wakeup search timeout (WUPSTO) is also applied to the preamble detection.	X
6	SIGMON_EN_P	Selection of signal monitor (signal signature recognition unit) to be active during preamble detection, see SIGMON_EN_W definition table.	X
5			X
4			X
3			X
2			X
1			X
0	ACCU_SIG_FAILS_P	Setting this bit causes the error indicators to be accumulated over the duration of the preamble detection. The accumulator is reset at the beginning of the preamble detection and when the µC samples the status.	X

Table 86: Address 2Fh: SIGMON1

85

Integrated UHF Transceiver

14.3.3 Register SIGMON2 at address 30h

Bit	Function	Description	Def
7	0	0	0
6		Selection of signal monitor (signal signature recognition unit) to be active during data reception, see SIGMON_EN_W definition table. If any of the enabled signal monitors detects an abnormal condition this is indicated by the IF_EOF (End of Frame Flag).	X
5			X
4	SIGMON_EN_D		X
3			X
2			X
1			X
0	ACCU_SIG_FAILS_D	Setting this bit causes the error indicators to be accumulated over the duration of the data reception. The accumulator is reset at the beginning of the data reception and when the µC samples the status.	X

Table 87: Address 30h: SIGMON2

14.3.4 Register WUPSTO at address 31h

Wake up search timeout configuration register.

Bit	Function	Description	Def
7	WUPSTIMEOUTPRESC	prescaler for wakeup search timeout counter	X
6			X
5	WUPSTIMEOUT	sets timeout to WUPSTIMEOUT * T_{WUPSTO} for WUPSTIMEOUT = 1…63. The value WUPSTIMEOUT = 0 disables the timeout timer and selects an infinite timeout	X
4			X
3			X
2			X
1			X
0			X

Table 88: Address 31h: WUPSTO

D7	D6	Clock selection for wakeup search timeout timer T_{WUPSTO}
0	0	2 T_{Bit}
0	1	4 T_{Bit}
1	0	16 T_{Bit}
1	1	64 T_{Bit}

Table 89: WUPSTIMEOUTPRESC Definition

14.3.5 Register SLICERINITL at address 32h

These are the 8 least significant bits of the SLICER of the dataslicer threshold acquired during initial. This register can be read to measure e.g. the TX to RX frequency offset or to save a proper threshold value to be reused later. The register can be written e.g. to restore a previously saved threshold value. Please note that the SLICERINIT register is different from the actual threshold value.

14.3.6 Register SLICERINITH at address 33h

These are the 7 most significant bits of the SLICER of the dataslicer threshold acquired during initial..

14.3.7 Register TIMINGCHK at address 34h

Configuration register for timing-check units.

Bit	Function	Description	Def
7	RFU	RESERVED	X
6	BROBSLENGTH	baud rate observation length setting, number of observed bits configurable to 8, 16, 24 or 32 bits	X
5			X
4	SUMBITTMGERRTH	baudrate checker threshold-value for the sum of 8 bits timing.	X
3			X
2			X
1	SGLBITTMGERRTH	single chip timing check threshold value. The time interval is accepted, if its absolute value is below the limit. This corresponds to timing errors, which are less than 12.5 %, 18.75 %, 25 % and 37.5% of a nominal chip width, respectively.	X
0			X

Table 90: Address 34h: TIMINGCHK

D6	D5	Number of nominal bits to be considered for the baud rate checker
0	0	8
0	1	16
1	0	24
1	1	32

Table 91: BROBSLENGTH definition

D4	D3	D2	Total timing error threshold in $T_{Chip}/128$ per 8 bits	Relative limit in % with respect to 8 nominal bits
0	0	0	16	0.78
0	0	1	24	1.17
0	1	0	32	1.56
0	1	1	48	2.34
1	0	0	64	3.13
1	0	1	96	4.69
1	1	0	128	6.25
1	1	1	192	9.38

Table 92: SUMBITTMGERRTH definition

D1	D0	Single chip timing error threshold in $T_{Chip}/128$ per interval
0	0	16
0	1	24
1	0	32
1	1	48

Table 93: SGLBITTMGERRTH definition

14.3.8 Register RXCON at address 35h

Receive mode configuration register.

Integrated UHF Transceiver

Bit	Function	Description	Def
7	STATAU TOSAM PLE	allows the software to control whether the status should be sampled when certain Read commands are issued. Automatically set to 0 after a wakeup-search and a preamble detection in order to save the result of this command.	X
6	AUTOS AMPLE MANUA L	Setting this bit prevents the STATAUTOSAMPLE bit from being set on completion of an RSSILEVEL read.	X
5	INV_RX _DATA	This bit simply inverts the slicer output. If this bit is in the cleared state, in FSK mode the lower frequency is received as a 1 and the higher frequency is received as a 0, whereas in ASK mode the lower RF amplitude is received as a 0 and the higher RF amplitude is received as a 1. When synchronizing the Manchester decoder with a preamble it samples the slicer output in the middle of the first half of a bit.	X
4	CLOCK_ RECOV _TC	set time constant of clock recovery settling time.	X
3			X
2	RX_MA NCHES TER	If set data is Manchester decoded. Manchester decoding is done by skipping every other chip clock pulse. Which of the two possible pulse trains will be omitted is set upon recognizing the programmed preamble during a preamble detection. If data reception is initiated without a prior preamble detection, there is an equal chance that either the right or the wrong clock pulse train is suppressed. In the first case the received data would be decoded properly; in the latter case the received data would be inverted. The MANCHESTER_COUNT in the EXTRXSTATUS register helps determining whether data was received correctly or inverted.	X
1	RX_CLO CK_TRA NSP	If set, the clock output is always the chip clock as produced by the clock recovery PLL. If cleared, the clock output is always the bit clock, which is equal to the chip clock in NRZ mode, during data reception. During the wakeup search and preamble detection the clock is held at 1. The µC should sample the receive data line with the 1-to-0 transition of the bit clock.	X
0	RX_DAT A_TRAN SP	If set, the data output is taken from the deglitched slicer result. If cleared the deglitched slicer result is re-sampled with the rising edge of the bit clock. Therefore the µC should take the data with the 1-to-0 transition of the bit clock. During the wakeup search the data line is kept at a constant 0, whereas during preamble detection it is held at 1.	X

Table 94: Address 35h: RXCON

D4	D3	Max settling time [chips]	Max bit edge phase error (degs)
0	0	3 (not recommended)	8
0	1	7	15
1	0	15	30
1	1	31	60

Table 95: CLOCK_RECOV_TC settings

14.3.9 Register RXFOLLOWUP at address 36h

Follow up receive mode configuration register.

Bit	Function	Description	Def
7	PREA_ FU_TF	power-down (1) or stop (0) after an unsuccessful preamble detection when initiated by the polling timer event. Generate an unmaskable preamble detected interrupt if stop is selected.	1
6	PREA_ FU_CF	power-down (1) or stop (0) after an unsuccessful preamble detection, when initiated by a Receive PRDA command or by a WUPS command which completed successfully and was succeeded by a preamble detection.	0
5	WUPS_ FU_TS	enter stop (0x), DATA (11) or PRDA (10) mode after a successful wakeup search, when initiated from a polling timer event. Generate an unmaskable WUPS interrupt if stop is selected. Also generate an interrupt if DATA is selected, as µC must be informed that data is available for collection.	0
4			0
3	WUPS_ FU_TF	power-down (1) or stop (0) after an unsuccessful wakeup search when initiated by the polling timer event. Generate an unmaskable WUPS interrupt if stop is selected.	1
2	WUPS_ FU_CS	enter stop (0x), DATA (11) or PRDA (10) mode after a successful wakeup search, when initiated from a Receive WUPS command.	0
1			0
0	WUPS_ FU_CF	power-down (1) or stop (0) after an unsuccessful wakeup search, when initiated from a Receive WUPS command.	0

Table 96: Address 36h: RXFOLLOWUP

14.3.10 Register SIGMONSTATUS at address 37h

Status register for signal monitoring. Please refer to section 10.3.6 for further details.

87

Integrated UHF Transceiver

Bit	Function	Description	Def
7	SIGMONSTATUS	If this bit is set, the previous wakeup search or preamble detection has failed. If this bit is zero, the command completed successfully. The other status registers can be read to ascertain more information if required.	?
6		Chip timeout	?
5		Chip timing	?
4		Coding	?
3		Baudrate	?
2		RSSI level	?
1		Modulation amplitude too high	?
0		Modulation amplitude too low	?

Table 97: Address 37h: SIGMONSTATUS

14.3.11 Register SIGMONERROR at address 38h

Status register for signal monitoring

Bit	Function	Description	Def
7	SIGMONERROR	WUP timeout	?
6		Chip timeout	?
5		Chip timing	?
4		Coding	?
3		Baud rate	?
2		RSSI level	?
1		Modulation amplitude too high	?
0		Modulation amplitude too low	?

Table 98: Address 38h: SIGMONERROR

SIGMONSTATUS	SIGMONERROR	Function
0	0	The signal monitor has not yet reached a decision.
0	1	not possible
1	0	The signal monitor did not detect an error.
1	1	The signal monitor detected an error.

Table 99: General meaning of the register bits located in SIGMONSTATUS and SIGMONERROR:

14.3.12 Register RSSILEVEL at address 39h

Bit	Function	Description	Def
7	RSSI_LEVEL	Result of RSSI conversion	0
6			0
5			0
4			0
3			X
2			X
1			X
0			X

Table 100: Sub Address 39h: RSSILEVEL

Status register for signal monitoring. Measured RSSI level at the completion of a wakeup search or preamble detection or at the moment the µC recently triggered sampling the received signal status.

14.3.13 Register PREACON at address 3Ah

Preamble detection configuration register

Bit	Function	Description	Def
7	RFU	RESERVED	0
6	PREA_TOL	definition of allowed chip-errors during preamble detection	X
5			X
4	PREA_LEN	definition of pattern length of the preamble to be detected. This is defined in chips, 1 to 31 is the length in chips; 0 is 32 chips.	X
3			X
2			X
1			X
0			X

Table 101: Address 3Ah, PREACON

D6	D5	Value
0	0	0
0	1	1
1	0	2
1	1	3

Table 102: PREA_TOL definition

14.3.14 Register PREA0 at address 3Bh

Preamble pattern chips [7:0]. Assuming the preamble is sent MSB first. These 8 chips represent the 8 least significant chips of the preamble pattern, bit 0.

14.3.15 Register PREA1 at address 3Ch

Preamble pattern chips [15:8]

14.3.16 Register PREA2 at address 3Dh

Preamble pattern chips [23:16]

14.3.17 Register PREA3 at address 3Eh

Preamble pattern chips [31:24]

Integrated UHF Transceiver

14.4 Registers visible in BANK1 only

14.4.1 Register EXTRXSTATUS at address 2Eh

Bit	Function	Description	Def
7	RX_HIGH_GAIN	This bit is 1 when high gain is selected and it is 0 when low gain is selected (either automatically or by command).	?
6	LIVE_STATUS	This bit is 0 if the consistent set of status information has been automatically sampled on completion of a wakeup search or preamble detection. It is 1 if the status has been sampled by a read operation from one of the 4 receiver status registers.	?
5	RX_CMD	This is the code of the receive sub-command during which or on completion of which the status has been sampled. 00=IDLE, 01=WUPS, 10=PREA and 11=DATA.	?
4			?
3	MANCHESTER_COUNT	Accumulated sum of received data-changes within a single chip period. Please refer to section 11.2.	?
2			?
1			?
0			?

Table 103: Address 2Eh, Bank 1, EXTRXSTATUS

14.4.2 Register CFRCCAL at address 2Fh

Channel filter RC calibration register

Bit	Function	Description	Def
7	CF_IQ_CAL_RUNNING	status bit indicating a running IQ calibration.	?
6	CF_CAL_RUNNING	status bit indicating a running RC calibration.	?
5	0	0	0
4	0	0	0
3	CF_RC_CAL_RES	Result bits of RC auto calibration	?
2			?
1			?
0			?

Table 104: Address 2Fh, Bank 1, CFRCCAL

14.4.3 Register CFIQCAL at address 30h

I/Q calibration register

Bit	Function	Description	Def
7	START_CF_IQ_CAL	setting this bits starts the I/Q calibration sequence.	0
6	CF_IQ_CALVAL	Configuration for the best I/Q calibration. Is the result of a triggered calibration sequence (used in production test). This configuration value shall be initialized and stored by the external microcontroller for every individual device in order to achieve best image rejection performance.	?
5			0
4			0
3			0
2			0
1			0
0			0

Table 105: Address 30h, Bank 1, CFIQCAL

14.5 Expert registers

Purpose of the expert registers is to enable the use of built in functions for very special application cases. Generally it is not recommended to change these settings.

14.5.1 Register EXPERT0 at address 31h

Bit	Function	Description	Def
7	RED_VCO_SWING	Automatically set at lower band, if set VCO output swing is reduced, LO power consumption is reduced. If cleared, VCO is running at highest drive level	0
6	LARGE_PLL_RST_DELAY	If set, the reset pulse width in the phase detector of the PLL is slightly increased (from 2.1 ns to 3.1 ns).	0
5	FASTCFFILTSETTL	If this bit is at zero sufficient delay is provided until the channel filter is declared settled after a transient at the input. This is especially important if a WUPS is carried out in pessimistic mode. Setting this bit reduces the delay which allows for faster operation. The slight reduction of settling accuracy should be acceptable for all other Receive commands.	0
4	PLL_ICP	manual programming of PLL charge pump current, The following formula can be used to compute the final CP-current as a function of the register setting: Icp = PLL_ICP * 15 µA	0
3			0
2			1
1			0
0			0

Table 106: Address 31h, Bank 1, EXPERT0

Integrated UHF Transceiver

14.5.2 Register EXPERT1 at address 32h

Bit	Function	Description	Def
7	XOSTARTUPDELAY	set / influence delay after XO_READY detection; This is required for influencing automated startup sequences.	0
6			1
5	ASKRSTBBMID	This bit applies only when receiving ASK. If this bit is left at 0, the baseband filter is reset to 0 (which corresponds to minus infinite dBm plus noise level) after an input transient. If this bit is set, the baseband filter is reset to the midpoint (which corresponds to RSSI midrange in dBm).	0
4	RFU	RESERVED	0
3			1
2	DISFRAC	disable frac-n mode of the PLL	0
1	LOCK_DET_TIME	set additional delay after 'physical' PLL lock detection; available delays are: 00 = 16 µs, 01 = 32 µs, 10 = 48 µs, 11 = 64 µs. Required for influencing automated startup sequences.	0
0			1

Table 107: Address 32h, Bank 1, EXPERT1

D7	D6	Function – Delay Time
0	0	256 µs
0	1	512 µs (default (power-on reset) value)
1	0	768 µs
1	1	1024 µs

Table 108: XOSTARTUPDELAY

14.5.3 Register EXPERT2 at address 33h

Bit	Function	Description	Def
7	FM_DEM_IANDQ	if set I and Q limiter outputs are used for FSK demodulation	0
6	LARGE_FM_DEM_RANGE	0 selects 200 kHz range (200 kHz to 400 kHz). 1 selects 600 kHz range (0 to 600 kHz – the 0 is a theoretical value which is limited to the lower corner frequency of the AC coupling in the channel filter).	0
5	WIDE_AMPL_WINDOW	Selects the window (number of samples) to be used for the amplitude criterion of the edge detection. 0 selects 2 samples at -1 and +1 about the centre. 1 selects 4 samples at -2, -1, +1 and +2 about the centre.	0
4	REDUCED_CHIP_TIMEOUT	This bit selects the timeout value for the chip timing verification block. 0 selects 3.5 chips; 1 selects 2.5 chips	0
3	TWORSSIMSBITSSLOW	This bit determines how much time is spent for the acquisition of the two MSBits in the RSSI ADC. 0 selects 3 clocks for bit 5 and 1 clock for bit 4. 1 selects 2 clocks for bit 5 and 2 clocks for bit 4.	0
2	FASTRSSIFILTSETTL	The bit controls the settling time for the RSSI filter. 0 selects 4 time constants (settling to within 2% of the last step). 1 selects 2 time constants (settling to within 14% of the last step).	0
1	CAPRSSI	These control bits allow trimming of the RSSI analog data low pass filtering. These bits change the capacitor values of this filter affecting the low-pass cut-off frequency.	1
0			0

Table 109: Address 33h, Bank 1, EXPERT2

D7	D6	Centre Freq (KHz)	Input Freq. range (KHz)	Max. Freq. Dev. (KHz)	No. of Delay Elements
0	0	300	200-400	±100	40
0	1	300	0-600	±300	13
1	0	600	200-400	±100	20
1	1	600	0-600	±300	7

Table 110: FM Demodulator Configurations

D1	D0	Typ C (pF)	Time constant (R typ = 300k)
0	0	0	0 (parasitics only)
0	1	2	0.6 µs
1	0	5	1.5 µs
1	1	12	4.8 µs

Table 111: CAPRSSI Definition

90

Integrated UHF Transceiver

14.5.4 Register EXPERT3 at address 34h

Bit	Function	Description	Def
7	0	0	0
6	0	0	0
5	0	0	0
4	0	0	0
3	TESTBUFFERCAL	Turns the calibration path on when 1. This is required during calibration of the test buffer.	0
2	ALLOWREGSWITCH	Controls the behaviour of the REG_xxx_ON test bits. If cleared, the REG_xxx_ON bits are OR'd to the normal control lines, allowing the unconditional turn on of selected regulators. If set, the REG_xxx_ON bits replace the normal control lines, which allows full control (on and off) of the regulators.	0
1	LTDIQPHASECAL	If this bit is 0, all possible matching combinations in the receiver chain are tried in order to achieve the best image rejection. If this bit is 1, certain phase trimming values are forbidden in order to eventually achieve a better overall performance over temperature.	0
0	DONOTDISTURBPTCAL	If this bit is cleared a polling timer calibration can run in parallel with the startup of the PLL. If this bit is set, the PLL startup, when requested, is delayed until the polling timer calibration has finished.	0

Table 112: Address 34h, Bank 1, EXPERT3

14.6 TEST registers:

The content of the test registers is initialized to 0 after power-up. Test registers should never be used in standard applications. Protection of change ????

14.6.1 Register TEST0 at address 35h

Bit	Function	Description	Def
7	CF_MULTITONE_EN	Channel Filter Multi-Tone Testing.	0
6	DIG_TEST_SEL	Selection of digital test signals, should be used in conjunction with the P11C and P12C settings, see section 14.2.9.	0
5			0
4			0
3	RXD_DBG_SEL	selection of digital test signals.	0
2			0
1			0
0			0

Table 113: Address 35h, Bank 1, TEST0

14.6.2 Register TEST1 at address 36h

Bit	Function	Description	Def
7	IQ_TEST_LV	has to be set if test buffer for IF output signals is used at supply voltages below 2.0V	0
6	ANA_TEST_SEL	selection of analog test signals	0
5			0
4			0
3	REG_DIG_DIS	voltage regulator disable for digital part.	0
2	PLL_CTRL	pll control test and configuration bits	0
1			0
0	VCO_TEST_ON	vco test enable bit	0

Table 114: Address 36h, Bank 1, TEST1

14.6.3 Register TEST2 at address 37h

Bit	Function	Description		Def
7	REG_VCO_ON	switch on voltage regulator for VCO		0
6	REG_PLL_ON	switch on voltage regulator for PLL		0
5	REG_PA_ON	switch on voltage regulator for PA		0
4	FORCE_REG_VCO_RDY	These bits override internal status information and enable automatic sequences to run even in case the corresponding status information signals a failing block.	override VCO ready signal	0
3	FORCE_REG_PLL_RDY		override PLL ready signal	0
2	FORCE_REG_PA_RDY		override PA ready signal	0
1	FORCE_LOCK_DETECT		override PLL lock detect signal	0
0	FORCE_XO_RDY		override XO ready signal	0

Table 115: Address 37h, Bank 1, TEST2

91

Integrated UHF Transceiver

14.6.4 Register TEST3 at address 38h

Bit	Function	Description	Def
7	VCO_ON	enable VCO	0
6	PRESC_ON	enable prescaler	0
5	PFD_ON	enable PLL phase detector	0
4	CLK_PLL_ON	enable PLL clock	0
3	TX_ON	enable PA, Tx part	0
2	RX_GAP_ON	enable bandgap reference, needed for rx mode	0
1	RX_ON	enable receiver	0
0	PA_STEP_TEST	enable PA test mode, to bypass internal step decoding block.	0

Table 116: Address 38h, Bank 1, TEST3

14.6.5 Register TEST4 at address 39h

Bit	Function	Description	Def
7	FORCE_CF_RC_CAL	issue RC autocalibration on request	0
6	SKIP_CF_RC_CAL	don't do RC autocalibration automatically	0
5	CF_RC_ADJUSTCAL	Tunes reference time constant for value of RC calibration function.	0
4			0
3	MAN_CF_RC_CALVAL	manual entry of RC calibration value	X
2			X
1			X
0			X

Table 117: Address 39h, Bank 1, TEST4

CF_RC_ADJUST CAL <1>	CF_RC_ADJUST CAL <0>	R variation (%)
0	0	0
0	1	+12.5
1	0	-6.2
1	1	-4.1

Table 118: Auto Calibration Reference Setting

14.6.6 Register TEST5 at address 3Ah

Bit	Function	Description	Def
7	XO_IOFFS	set programmable offset current for oscillator control loop	0
6			0
5			0
4	XO_IOFFSET_SINK_EN	This bit is only active, if XO_IOFFSET_EN = 1. When it is set, the offset current shall be sinked in the bias source, otherwise it is sourced.	0
3	XO_IOFFSET_EN	The crystal oscillator offset current enable bit controls a test signal to control the bias current. This bit shall be cleared during normal crystal oscillator operation.	0
2	XO_KICK_DIS	The crystal oscillator start-up kick disable bit controls a test signal to disable the start-up kick after power-on. This bit shall be cleared during normal crystal oscillator operation.	0
1	XO_DET_DIS	The crystal oscillator detector disable bit controls a test signal to disable the detector. This bit shall be cleared during normal crystal oscillator operation.	0
0	XO_BIAS_DIS	disable XO bias circuit	0

Table 119: Address 3Ah, Bank 1, TEST5

Integrated UHF Transceiver

15 Appendix

Integrated UHF Transceiver

16 Application Circuit
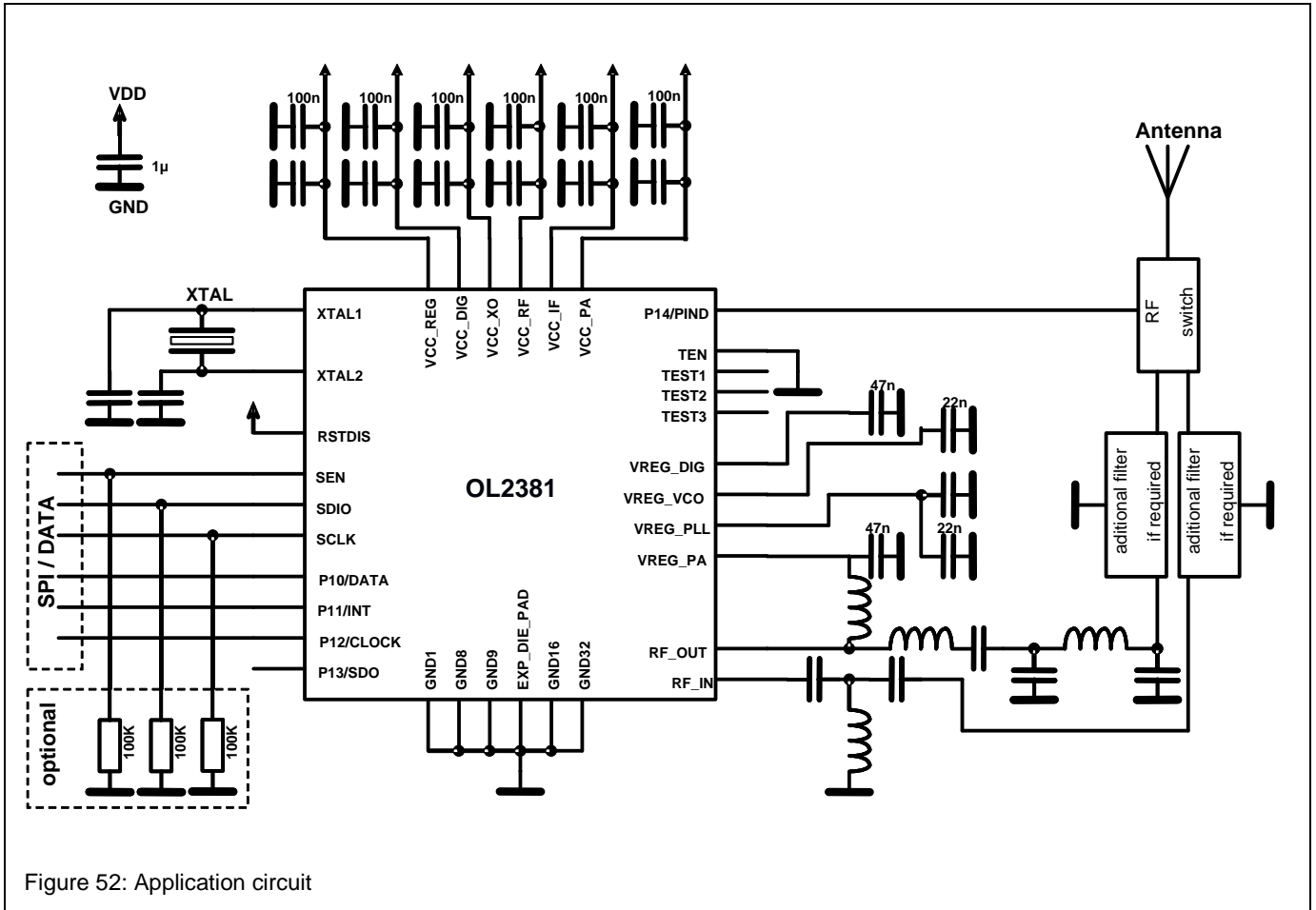
Figure 52: Application circuit

The values for the matching circuit components have to be fixed after test board layout.

All Gnd connections should be separately connected.

94

Integrated UHF Transceiver

17 Limiting Values

All values are in accordance with Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
T_{sto}	Storage Temperature Range	-55		+125	°C	
T_j	Junction Temperature			+95	°C	
$V_{max(1)}$	Voltage at any VCC or I/O Pin to Gnd	-0.3		3.6	V	
$V_{max(2)}$	Voltage at all other Pins to Gnd	-0.3		2.8	V	
$V_{max\ RF\_OUT}$	Voltage at RF_OUT pin to Gnd	-0.3		4.2	V	RF Peak Voltage
I_{IOs}	Max DC current for I/O pins			4	mA	
P_{max}	Maximum input level Rx			12.9	dBm	
$I_{latch-up}$	Latch-up current, Note 1	100			mA	Only applies to pins which are connected to active devices in the application. According to the standard, only relevant for VCC pins and digital I/O's.
$V_{ESD\ HBM1}$	Human Body Model ESD voltage immunity, (VREG_PA and RF_OUT) Note 1	1.5			kVp	
$V_{ESD\ HBM2}$	Human Body Model ESD voltage immunity, (All other pins)	2			kVp	
$V_{ESD\ MM1}$	Machine Model ESD voltage immunity, (VREG_PA and RF_OUT) Note 1	100			Vp	
$V_{ESD\ MM2}$	Machine Model ESD voltage immunity, (All other pins)	200			Vp	
$P_{wr}\ D_{iss}$	Power dissipation			120	mW	

GENERAL NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the Operating Conditions and Electrical Characteristics section of this specification is not implied.

2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.

95

Integrated UHF Transceiver

18 Electrical Characteristics

18.1 Operating Conditions

Capacitors of 22 nF // 270pF connected between VREG_PLL and GND_PLL, VREG_VCO and GND_VCO .
Capacitor of 47 nF // 270pF connected between VREG_PA and GND_PA and VREG_DIG and GND_DIG
Unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Vcc	Supply voltage	2.1	2.7	3.6	V	
T $_{amb}$	Operating temperature	-25	25	85	°C	

96

Integrated UHF Transceiver

18.2 DC Characteristics

T_{AMB} = -25 to +85°C, VCC_xxx = 2.7V, GND_xxx = 0V,
Capacitors of 22 nF // 270pF connected between VREG_PLL and GND_PLL, VREG_VCO and GND_VCO .
Capacitor of 47 nF // 270pF connected between VREG_PA and GND_PA and VREG_DIG and GND_DIG
Quartz Crystal NDK NX5032SA with CL=12pF
Unless otherwise specified.

The Edge Slicer was used for all relevant measurements.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Current Consumption						
Icc_{PWD}	Power-down mode		0.5	1.6	µA	+25°C
			5		µA	85°C
Icc_{IDLE}	Crystal oscillator on, digital active		900	1200	µA	PLL and PA off
$Icc_{LO\ 434/868\ MHz}$	LO supply current in the 315/434/868 MHz band		5	7	mA	PA off
$Icc_{RX\ 434/868\ MHz}$	Receiver supply current in the 315/434/868 MHz band	15.5	16.5	18	mA	25degC
$Icc_{RX\ 434/868\ MHz}$	Receiver supply current in the 315/434/868 MHz band	13.5	16.5	21.5	mA	-25 to +85degC
$Icc_{TX\ 434/868\ MHz}$	Transmitter supply current in the 315/434/868 MHz band		22	25	mA	10 dBm output power PA Matching Dependent
			14	17	mA	6 dBm output power PA Matching Dependent
Digital I/Os						
V_{IH}	High Level input voltage	0.8*Vcc		Vcc	V	Vcc=2.1 to 3.6V
V_{IL}	Low Level input voltage	0		0.4	V	Vcc=2.1 to 3.6V
I_{IH}	High Level input current	-1		1	µA	
I_{IL}	Low Level input current	-1		1	µA	
$V_{OH(1)}$	High Level output voltage	0.7*Vcc		Vcc	V	SPI Pins (SCLK, SDIO and SDO) Vcc=2.1 to 3.6V
$V_{OL(1)}$	Low Level output voltage	0		0.3*Vcc	V	SPI Pins (SCLK, SDIO and SDO) Vcc=2.1 to 3.6V
$V_{OH(2)}$	High Level output voltage	0.8*Vcc		Vcc	V	Vcc=2.1 to 3.6V
$V_{OL(2)}$	Low Level output voltage	0		0.2*Vcc	V	Vcc=2.1 to 3.6V
I_{OH}	High Level output current	-1			mA	
I_{OL}	Low Level output current	1			mA	
$F_{I/Os}$	IOs operating frequency			4	MHz	With 10pF output load

Note: Different biasing configurations are available in the receiver to trim performances (mainly sensitivity and linearity) vs. power consumption.

Integrated UHF Transceiver

18.3 AC Characteristics

T_{AMB} = -25 to +85°C, VCC_xxx = 2.7V, GND_xxx = 0V,

Capacitors of 22 nF // 270pF connected between VREG_PLL and GND_PLL, VREG_VCO and GND_VCO .
Capacitor of 47 nF // 270pF connected between VREG_PA and GND_PA and VREG_DIG and GND_DIG.
Quartz Crystal NDK NX5032SA with CL=12pF
Unless otherwise specified.

The Edge Slicer was used for all relevant measurements.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Operating RF Frequency						
$f_{RF\ 315}$	Frequency band 315 MHz	300	315	320	MHz	
$f_{Step\ 315}$	Frequency step at 315 MHz		150		Hz	
$f_{RF\ 434}$	Frequency band 434 MHz	415	434	450	MHz	
$f_{Step\ 434}$	Frequency step at 434 MHz		200		Hz	
$f_{RF\ 868}$	Frequency band 868 MHz	865	868	870	MHz	
$f_{Step\ 868}$	Frequency step at 868 MHz		400		Hz	
$f_{RF\ 915}$	Frequency band 915 MHz	902	915	928	MHz	
$f_{Step\ 915}$	Frequency step at 915 MHz		415		Hz	
Modulation						
DR	Data rate	0.4		112	kchip/s	Manchester (or NRZ) encoding
DR_{step}	Data rate step		0.1		kchip/s	
$f_{dev\ FSK}$	Frequency deviation FSK			249	kHz	Minimum Frequency deviation is the resolution of the LO (dependent on application settings) Crystal/Band dependant
$f_{dev\ step}$	Frequency deviation step	3		6	%	Detailed information see: 8.5.1 Frequency modulation
$M_{depth\ ASK}$	Modulation depth ASK	25	40		dB	Constant PAM, difference between (ACON0=0-31)
Reference Crystal Oscillator						
f_{XO}	Crystal reference input frequency	15.95	16	16.05	MHz	
t_{onXOl}	Crystal oscillator start-up time			1	ms	Start-up time including XOSTARUPDELAY=256us
$C_{load\ XO}$	Crystal driver capacitance		1		pF	
R_{Margin}	Oscillator start-up margin	700			Ω	-10°C to 65°C, Min 2.1V Quartz Crystal NDK NX5032SA with CL=12pF
$V_{XO(HIGH)}$	External clock input signal level		1.8		V	Signal applied to XTAL2 pin.. Only for test purposes, this should not be used in the application.

Integrated UHF Transceiver

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
V $_{XO(LOW)}$	External clock input signal level		0		V	Signal applied to XTAL2 pin.. Only for test purposes, this should not be used in the application.

Phase Locked Loop						
PLL $_{BW}$	PLL loop bandwidth, -3dB closed loop at 868MHz.		150		kHz	On-chip loop filter: ICP Value = 2
t $_{CAL\_VCO}$	VCO auto-calibration time		110		µs	Note 1
t $_{PLL ready}$	Time from PLL start-up to PLL locked		120	200	µs	Note 1
Power amplifier						
Po $_{Txmax}$	TX PA output power max	10	11		dBm	At TX output, nominal power mode **Please Note: Using a SAW filter in the Transmit path with this device may produce undesired operation.**
Po $_{Txmin}$	TX PA output power min			-15	dBm	At TX output, in Low Power mode
Po $_{Txvar}$	TX PA output power variance		+/-1		dB	Output power device variation at constant power-setting over temperature and supply voltage
Po $_{Tx step}$	TX PA output power number of steps		30			
Co $_{TX}$	TX PA output capacitance		0.7		pF	
t $_{startTX}$	VREG PA start up time		3	10	µs	
t $_{TX ready}$	Time from PLL start to TX ready		200	300	µs	
E $_{spur}$	Spurious Emission Device operating in TX Modulation is off (conducted measurements, standard matching circuit (LC, class E))			-54	dBm	47-230M or 470-862MHz Note 2
				-36	dBm	Others below 1GHz Note 2
				-30	dBm	Above 1GHz Note 2
PN$_{LB/HB (50kHz)}$				-92 / -86	dBc/Hz	Offset 50kHz. ICP Setting = 2
PN$_{LB/HB}$ (100kHz)	Phase Noise at TX output in the 434MHz / 868 MHz			-92 / -86	dBc/Hz	Offset 100kHz ICP Setting = 2
PN$_{LB/HB (1MHz)}$				-113/ -107	dBc/Hz	Offset 1MHz ICP Setting = 2
PN$_{LB/HB (2MHz)}$				-121/ -115	dBc/Hz	Offset 2MHz ICP Setting = 2

Integrated UHF Transceiver

					-131/ -125	dBc/Hz	Offset 5 MHz ICP Setting = 2
$PN_{LB/HB (5MHz)}$							
$PN_{LB/HB (10MHz)}$					-134/ -130	dBc/Hz	Offset 10 MHz ICP Setting = 2

Receiver section							
$Zin_{(RX\ 868MHz)}$	RX input impedance at 868MHz		66-j94			Ω	Input resistance in series with reactance in High Gain Mode. These values are indicative, input impedance should be determined on an application basis, please see the application note.
$Zin_{(RX\ 434MHz)}$	RX input impedance at 434MHz		125-j139			Ω	
$Zin_{(RX\ 315MHz)}$	RX input impedance at 315MHz		157-j138			Ω	
f_{BW}	Channel filter bandwidth	50		300		kHz	
$f_{Step\ Number}$	Channel filter number of step		6				50, 75, 100, 150, 200, 300 kHz
$t_{RX\ ready}$	Time from PLL startup to RX ready		250	350		µs	Note 1
NF_{RX}	RX cascaded Noise Figure		7			dB	Frontend Gain max
$S_{LB/HBFSK\ 2.4}$	Sensitivity at input for BER $\leq 10^{-3}$ Manchester enc. data rate = 2.4kbps Deviation = 2.4kHz Channel filter BW = 50kHz	-109	-112			dBm	Eb/No of 9.8dB Frontend Gain max
$S_{LB/HBFSK\ 4.8}$	Sensitivity at input for BER $\leq 10^{-3}$ Manchester enc. data rate = 4.8kbps Deviation = 4.8kHz Channel filter BW = 50kHz	-108	-110			dBm	Eb/No of 9.8dB Frontend Gain max
$S_{LB/HB\ FSK\ 9.6}$	Sensitivity at input for BER $\leq 10^{-3}$ Manchester enc. data rate = 9.6kbps Deviation = 15kHz Channel filter BW = 75kHz	-106	-109			dBm	Eb/No of 9.8dB Frontend Gain max
$S_{LB/HB\ FSK\ 20}$	Sensitivity at input for BER $\leq 10^{-3}$ Manchester enc. data rate = 20kbps Deviation = 20kHz Channel filter BW = 100kHz	-103	-105			dBm	Eb/No of 9.8dB Frontend Gain max
$S_{LB/HB\ ASK\ 2.4}$	Sensitivity at input for BER $\leq 10^{-3}$ Manchester enc. data rate = 2.4kbps Channel filter BW = 50kHz		-118			dBm	Carrier Output Power Eb/No of 9.8dB Frontend Gain max ASK-Modulation with 50% Duty-Cycle-Square Wave. OOK

Integrated UHF Transceiver

$S_{LB/HB\ ASK\ 4.8}$	Sensitivity at input for BER $\leq 10^{-3}$ Manchester enc. data rate = 4.8kbps Channel filter BW = 50kHz		-117		dBm	Carrier Output Power Eb/No of 9.8dB Frontend Gain max ASK-Modulation with 50% Duty-Cycle-Square Wave OOK
$R_{C/I(N)}$	Co channel rejection		-11		dB	When using Edge Slicer
$R_{LB/HB\ C/I(N\pm1)}$	Adjacent channel rejection for channel spacing = channel bandwidth	10			dB	Wanted 3dB above the sensitivity level, CW jammer, BER $\leq 10^{-2}$
$R_{LB/HB\ C/I(N\pm2,3,...)}$	Rejection with $\geq$ 2 channels separation	30			dB	Wanted 3dB above the sensitivity level, CW jammer, BER $\leq 10^{-2}$
IFS	Image frequency suppression		30		dB	
$IFScal_{LOW-BAND1}$	Image frequency suppression with calibration, 315 and 434MHz , Note 3	50			dB	For 315 and 434 Band with trimming @ RT and nominal voltage FSK Modulation Manchester enc. data rate = 2.4kbps Channel filter BW = 50kHz
$IFScal_{LOW-BAND1}$	Image frequency suppression with calibration, 315 and 434MHz	45			dB	For 315 and 434 Band with trimming @ RT and nominal voltage FSK Modulation Manchester enc. data rate = 20kbps Channel filter BW = 300kHz
$IFScal_{HIGH-BAND2}$	Image frequency suppression with calibration, 868MHz, Note 3	45			dB	For 868MHz Band with trimming @ RT and nominal voltage FSK Modulation Manchester enc. data rate = 2.4kbps Channel filter BW = 50kHz
$IFScal_{HIGH-BAND2}$	Image frequency suppression with calibration, 868MHz	40			dB	For 868MHz Band with trimming @ RT and nominal voltage FSK Modulation Manchester enc. data rate = 20kbps Channel filter BW = 300kHz
ICR	Image channel rejection, Note 3		22		dB	Wanted 3dB above the sensitivity level, CW jammer at image frequency, BER $\leq 10^{-2}$
$ICR_{cal-LOW-BAND1}$	Image channel rejection with calibration, 315 and 434MHz, Note 3	40			dB	Calibration with ext RF signal. Wanted 3dB above the sensitivity level, CW jammer at image frequency, BER $\leq 10^{-2}$ FSK Modulation Manchester enc. data rate = 2.4kbps Channel filter BW = 50kHz

Integrated UHF Transceiver

$ICR_{cal\text{-}LOW\text{-}BAND1}$	Image channel rejection with calibration, 315 and 434MHz, Note 3	30			dB	Calibration with ext RF signal. Wanted 3dB above the sensitivity level, CW jammer at image frequency, BER $\leq 10^{-2}$ FSK Modulation Manchester enc. data rate = 20kbps Channel filter BW = 300kHz
$ICR_{cal\text{-}HIGH\text{-}BAND2}$	Image channel rejection with calibration, 868MHz, Note 3	30			dB	Calibration with ext RF signal. Wanted 3dB above the sensitivity level, CW jammer at image frequency, BER $\leq 10^{-2}$ FSK Modulation Manchester enc. data rate = 2.4kbps Channel filter BW = 50kHz
$ICR_{cal\text{-}HIGH\text{-}BAND2}$	Image channel rejection with calibration, 868MHz, Note 3	25			dB	Calibration with ext RF signal. Wanted 3dB above the sensitivity level, CW jammer at image frequency, BER $\leq 10^{-2}$ FSK Modulation Manchester enc. data rate = 20kbps Channel filter BW = 300kHz
$Blocking_{LB/HB\ 1MHz}$	Rejection of out of band blocking signal @ ± 1MHz from edge band	40			dB	
$Blocking_{LB/HB\ 2MHz}$	Rejection of out of band blocking signal @ ± 2MHz from edge band	50			dB	
$Blocking_{LB/HB\ 5MHz}$	Rejection of out of band blocking signal @ ± 5MHz from edge band	60			dB	
$Blocking_{LB/HB\ 10MHz}$	Rejection of out of band blocking signal @ ±10MHz from edge band	60			dB	
$ICP1_{close}$	1dB compression point. 10kHz offset from RF		-36		dBm	To the output of the mixer with maximum front end Gain.
IIP3	Input IP3 (+5/10 MHz)		-23		dBm	To the output of the mixer with maximum front end Gain.
$LO_{leakage}$	LO leakage power at receiver input			-47	dBm	LO > 1GHz
$RX_{Spurious}$	Spurious emission in RX mode 9kHz-1GHz 1-4GHz			-57 -47	dBm dBm	
RSSI						
$RSSI_{range}$	RSSI dynamic range		80		dB	

Integrated UHF Transceiver

| RSSI $_{abs\_acc}$	RSSI absolute accuracy, Note 3		+/- 12		dB	Input power variation (in range of -90dBm) to achieve nominal digital code of 89 LSB for any device under any condition
RSSI $_{variation}$	RSSI variation, Note 3		+/- 3		dB	Input power variation (in range of -90dBm) for one device over supply and temperature
RSSI $_{gain}$	RSSI Gain	0.4		0.9	dB/LSB	
RSSI $_{min}$	RSSI minimum level		-110	-100	dBm	Linked to reference sensitivity

Notes

1. Guaranteed by Design.
2. Tested at 315Mhz, 434MHz and 868MHz
   a. 315MHz: Output power limit 5dBm
   b. 434MHz: Output power limit 5dBm
   c. 868MHz: Output power limit 5dBm
3. Values derived from characterization result

Integrated UHF Transceiver

19 Package Outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads;
32 terminals; body 5 x 5 x 0.85 mm

SOT617-3
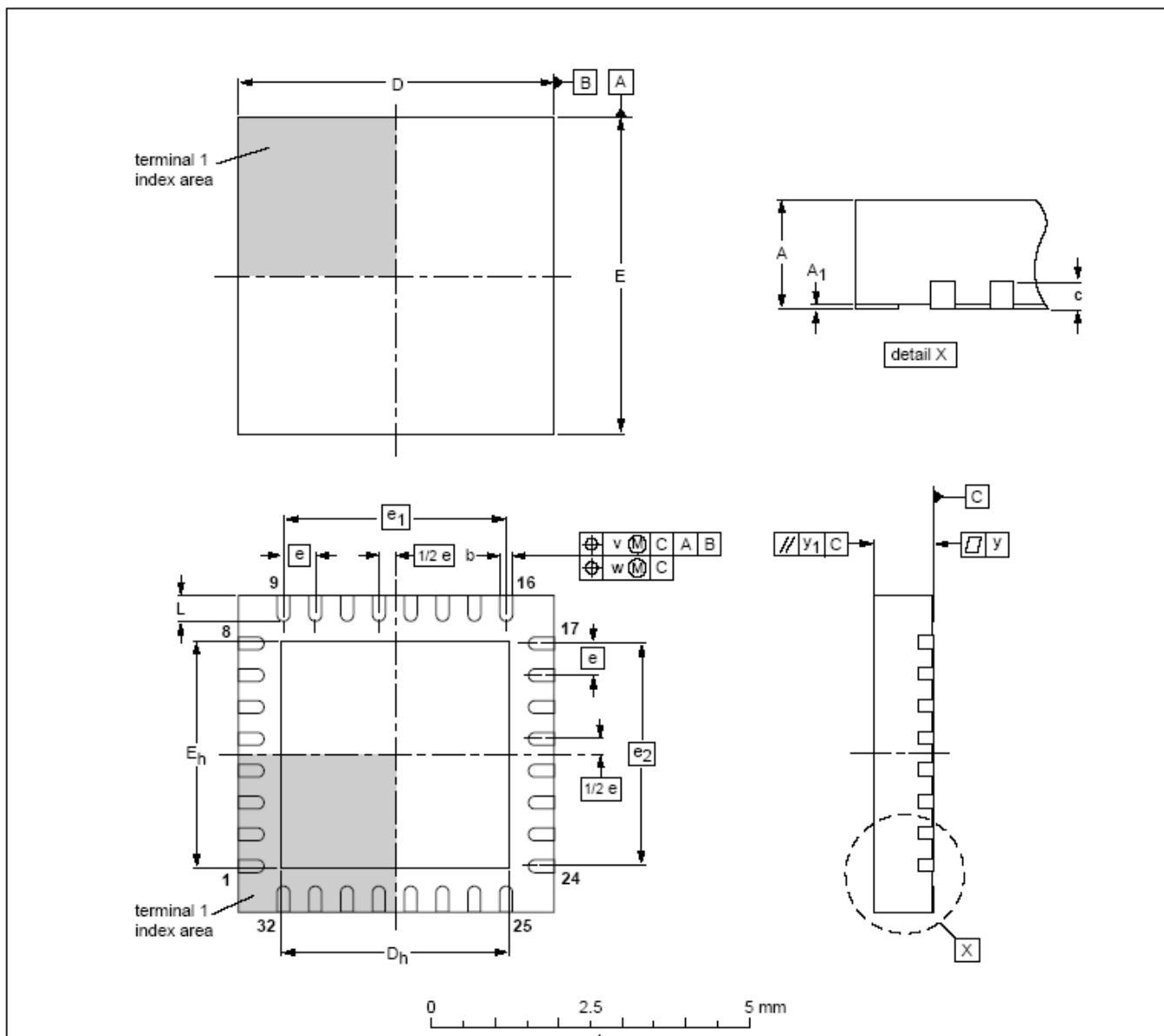
DIMENSIONS (mm are the original dimensions)

UNIT	A[1] max.	A₁	b	c	D[1]	Dₕ	E[1]	Eₕ	e	e₁	e₂	L	v	w	y	y₁
mm	1	0.05 0.00	0.30 0.18	0.2	5.1 4.9	3.75 3.45	5.1 4.9	3.75 3.45	0.5	3.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT617-3	- - -	MO-220	- - -			02-04-18 02-10-22

Integrated UHF Transceiver

20 Definitions

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Draft Specification	This data sheet contains final Draft Specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics section of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

21 Life Support Applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. NXP customers using or selling these products for use in such applications do so on their own risk and agree to fully indemnify NXP for any damages resulting from such improper use or sale.

Integrated UHF Transceiver

22 Abbreviations

SFR	Special Function
SPI	Serial Peripheral Interface
PLL	Phase Locked Loop
ASK	Amplitude Shift Keying
FSK	Frequency Shift Keying
ISM	Industrial, Scientific & Medical
VCO	Voltage Controlled Oscillator
LO	Local Oscillator
PA	Power Amplifier
LNA	Low Noise Amplifier
IF	Intermediate Frequency
RSSI	Received Signal Strength Indicator
POR	Power-on-Reset
PRNG	Psuedo-Random Number Generator

Integrated UHF Transceiver

23 Device History

Type	Name / Reference	Description
	2381	

Integrated UHF Transceiver

24 Related Documents

Type	Name / Reference	Description

25 Development Tools

Reference	Name	Description

26 Revision History

Revision	Date	Description
1.00	Dec '09	Initial Draft for S gate.
1.1	June '10	Product Release Datasheet Textual Corrections & General Formatting Updated Application Circuit Update of Temperature / Voltage Conditions
1.2	Oct '10	Structural & Description Updates
1.3	Oct '10	Section Updates 3.2 General Architecture description, kbits/s changed to kchips/s. 21 Life Support Applications, wording updated.

Contact information

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