Freescale Semiconductor, Inc.
Board Errata

Document Number: FRDMK64F_ERRATA
Rev. 2.0, 06/2014

FRDM-K64F Board Errata

by: Freescale Semiconductor, Inc.

1 Errata Title: I²C signals are swapped on I/O headers

Description: Pin 18 (I2C0_SCL) and pin 20 (I2C0_SDA) of J2 I/O Header, and pin 10 (I2C_SCL) and pin 12 (I2C0_SDA) of J4 I/O Header are swapped. Figure 1 and Figure 2 show the incorrect signals.

Table 1. Incorrect signals

FRDM-K64F	Signal	Arduino Uno R3	Signal
J2-18	I²C0_SCL	D14	I²C_SDA
J2-20	I²C0_SDA	D15	I²C_SCL
J4-10	I²C0_SCL	A4	I²C_SDA
J4-12	I²C0_SDA	A5	I²C_SCL

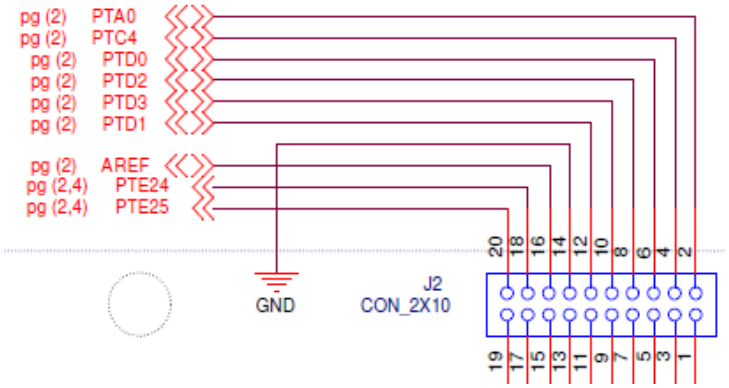

Figure 1. Swapped I²C signals Pin18 and on J2

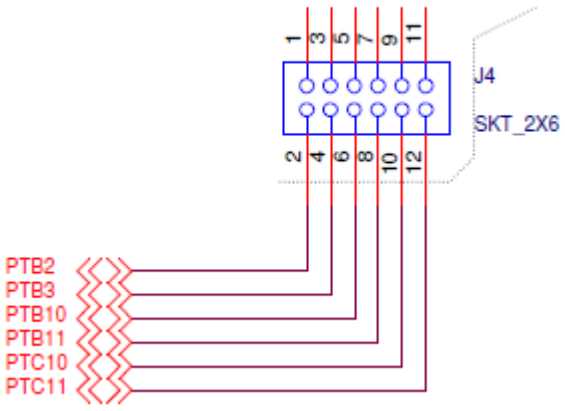

Figure 2. Swapped I²C signals Pin10 and Pin12 on J4

The correct position should be:

Table 2. Correct signals

FRDM-K64F	Signal	Arduino Uno R3	Signal
J2-18	I²C0_SDA	D14	I²C_SDA
J2-20	I²C0_SCL	D15	I²C_SCL
J4-10	I²C0_SDA	A4	I²C_SDA
J4-12	I²C0_SCL	A5	I²C_SCL

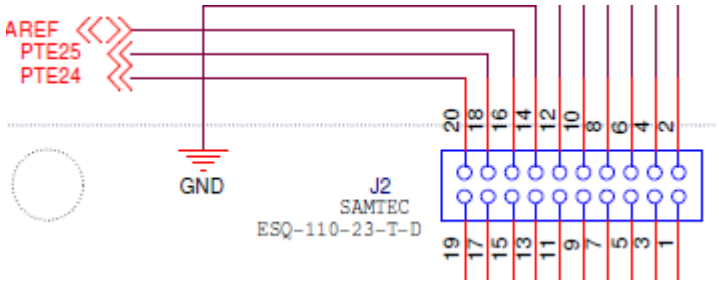

Figure 3. Correct order of I²C signals on J2

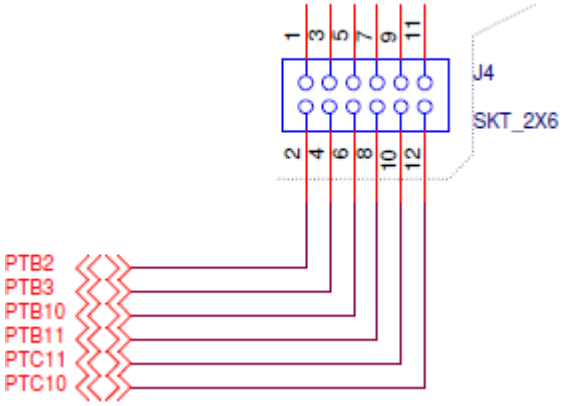

Figure 4. Correct order of I²C signals on J4

Workaround:

1. Use jumper wires to connect between Arduino compatible shield signals to the FRDM board I/O header signals. Swap the jumper wires only on the I²C signals.
2. When pin 10 of J4 (PTC10) and pin 12 of J4 (PTC11) are not used on the shield, route pin 10 of J4 to pin 20 of J2 and pin 12 of J4 to pin 18 of J2. Configure PTE24 and PTE26 (pin 18 and pin 20 of J2) as GPIO, and use PTC10 and PTC11 (pin 10 and pin 12 of J4) as I²C signals.

Fix Plan: Fixed in FRDM-K64F board (700 Assembly Rev B, Schematic Rev D1).

2 Errata Title: PTA0 is routed to Pin2 of J2

Description: Some Arduino shields are using Pin2 of J2 (connected to PTA0) as general purpose signal. The feature associated with Pin2 of J2 cannot be used while debugging.

Workaround: Use Jumper wires to connect between Arduino compatible shield and the FRDM board. The Pin2 of J2 on Ardunio shield is connected to J9 of J4 I/O Header.

Fix Plan: A fix has been planned for future FRDM-K64F boards**.**

3 Errata Title: Unable to establish link status when two FRDM-K64F boards are connected.

Description: When two FRDM-K64F boards are connected together with an Ethernet cable, the Ethernet PHY can't establish the link status, and will drop to a default state of 10Mbit and half duplex mode. This is caused by incorrect termination on the TD+ and RD+ signals, which reduces the link signal detection. This issue does not affect other connections such as PC host to FRDM-K64F, TWR-SER1/2 to FRDM-K64F, or network switch to FRDM-K64F when the cable length is less than 25 feet. This issue affects both Rev C and Rev D1 boards.

Workaround: Remove the four resistors R44, R48, R51, and R59 that connect to TD+, TD-, RD+ and RD- signals.

Fix Plan: A fix has been planned for future version of FRDM-K64F board (after 700 Assembly Rev B, Schematic Rev D1).

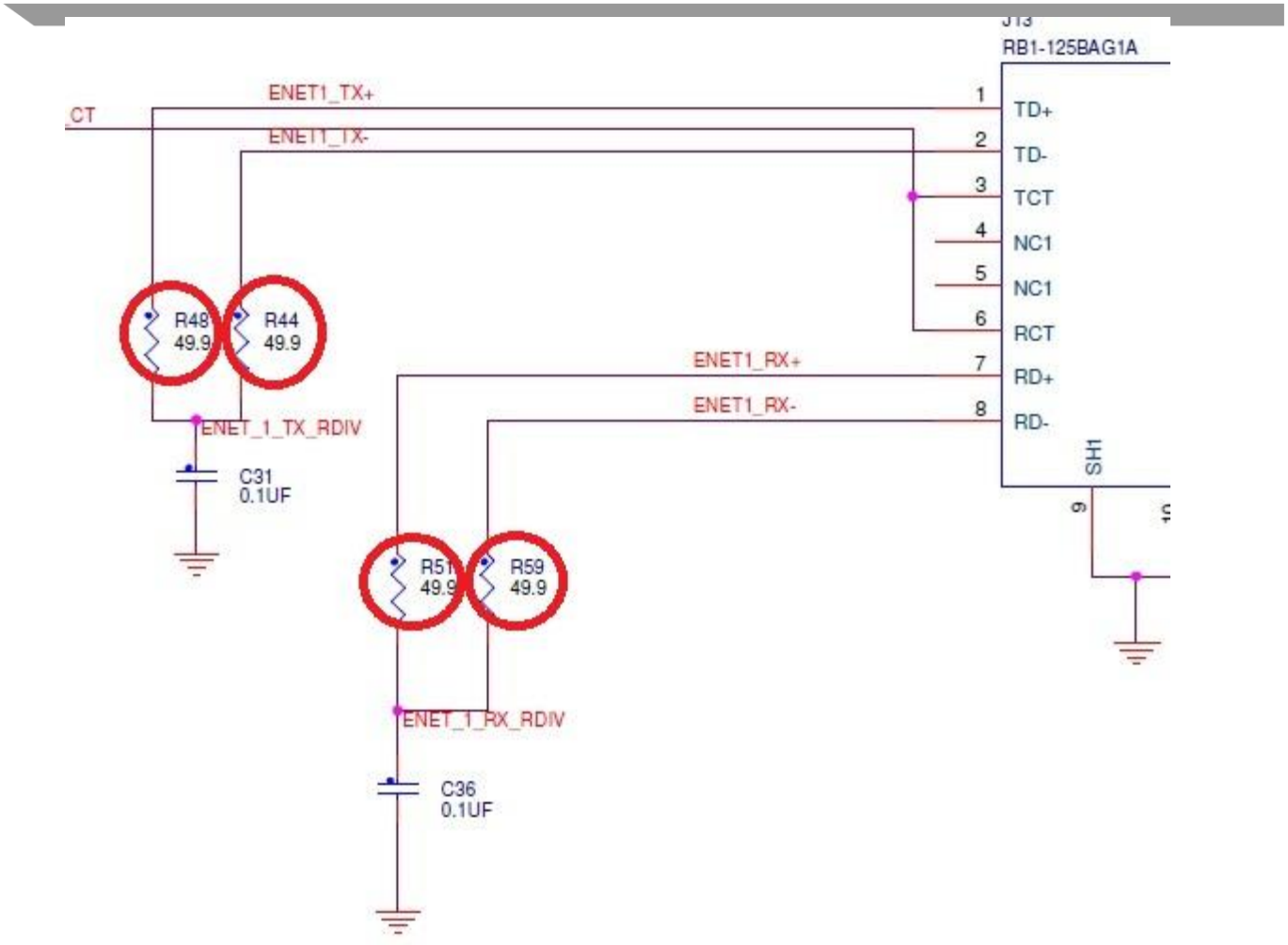

Figure 5. Correct order of I²C signals on J2

Revision history

Table 3 describes the boards to which the errata in this document apply.

Table 3. Revision of the Boards

Board Assembly Rev.	Board Schematic Rev.	Board PN
A	Rev C	FRDM-K64F
B	Rev D1	FRDM-K64F

Table 4. Document Revision History

Revision number	Date	Substantial changes

1.0	03/2014	Initial release
1.1	04/2014	Additional workaround to Errata 1
2.0	06/2014	Added errata “Unable to establish link status when two FRDM-K64F boards are connected” type

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