



TDF8597

I²C-bus controlled dual channel 43 W/2 Ω, single channel 85 W/1 Ω class-D power amplifier with full diagnostics

Rev. 1 — 17 November 2011

Preliminary short data sheet

1. General description

The TDF8597 is a dual Bridge-Tied Load (BTL) car audio amplifier comprising an NDMOST-NDMOST output stage based on SOI BCDMOS technology. The TDF8597 fully supports start/stop systems as it can operate at a battery voltage as low as 6 V. The TDF8597 can be controlled with or without I²C. I²C allows control of load detection results and fault conditions to be read. The TDF8597 is a high efficiency class-D amplifier with low dissipation. Due to the low dissipation, the device can be used with a smaller heat sink than standard class AB amplifiers. Six different I²C addresses can be selected with external resistors connected to the ADS and MOD pins. If pin ADS is a short-circuit to ground, the TDF8597 operates in non-I²C mode, and no I²C communication is possible. Use pins EN and ON to switch to operating and mute modes.

2. Features and benefits

- High-efficiency
- Low quiescent current
- Operating voltage from 6 V to 24 V
- Start/Stop ready: continues to operate without audible disturbance during engine start at a battery voltage as low as 6 V
- 4 Ω or 2 Ω capable stereo BTL channels or 1 Ω capable mono BTL channel
- Differential inputs
- Fast-mode I²C-bus
- I²C-bus mode with 6 I²C-bus addresses or non-I²C-bus mode operation
- Clip detect selectable at 0.2 % or 10 % THD
- Independent short-circuit protection for each channel
- Advanced short-circuit protection for load, GND and supply
- Thermal foldback and thermal protection
- DC-offset protection
- Selectable AD or BD modulation
- Advanced clocking:
 - ◆ Switchable oscillator clock source: internal for Master mode or external for Slave mode
 - ◆ Spread spectrum mode
 - ◆ Phase staggering
 - ◆ Frequency hopping
- No 'pop noise' caused by DC output offset voltage
- I²C-bus mode:



- ◆ Load diagnostics
 - Speaker load, open load and shorted load
 - Amplifier output to ground and to supply shorts
 - Tweeter detection
- ◆ Thermal pre-warning diagnostic level setting
- ◆ Identification of activated protection or warnings
- ◆ Selectable diagnostic information available on DIAG and CLIP pins
- Qualified in accordance with AEC-Q100

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General; V_P = 14.4 V						
V _P	supply voltage		6	14.4	24	V
I _P	supply current	off state; V _{EN} < 0.8 V	-	2	10	μA
I _q	quiescent current	no load, snubbers and output filter connected	-	90	120	mA
Stereo mode; V_P = 14.4 V						
P _o	output power	R _L = 4 Ω; THD = 10 %	24	26	-	W
		R _L = 2 Ω; THD = 10 %	39	43	-	W
Stereo mode; V_P = 24 V						
P _o	output power	R _L = 4 Ω; THD = 10 %	-	70	-	W
		R _L = 2 Ω; THD = 10 %	-	100	-	W
Parallel mode; V_P = 14.4 V						
P _o	output power	R _L = 1 Ω; THD = 10 %	-	85	-	W
Parallel mode; V_P = 24 V						
P _o	output power	R _L = 2 Ω; THD = 10 %	-	138	-	W
		R _L = 1 Ω; THD = 1 %	135	150	-	W

4. Ordering information

Table 2. Ordering information

Type number	Package		Version
	Name	Description	
TDF8597TH	HSOP36	HSOP36: plastic, heatsink small outline package; 36 leads; low stand-off height	SOT851-2

5. Block diagram

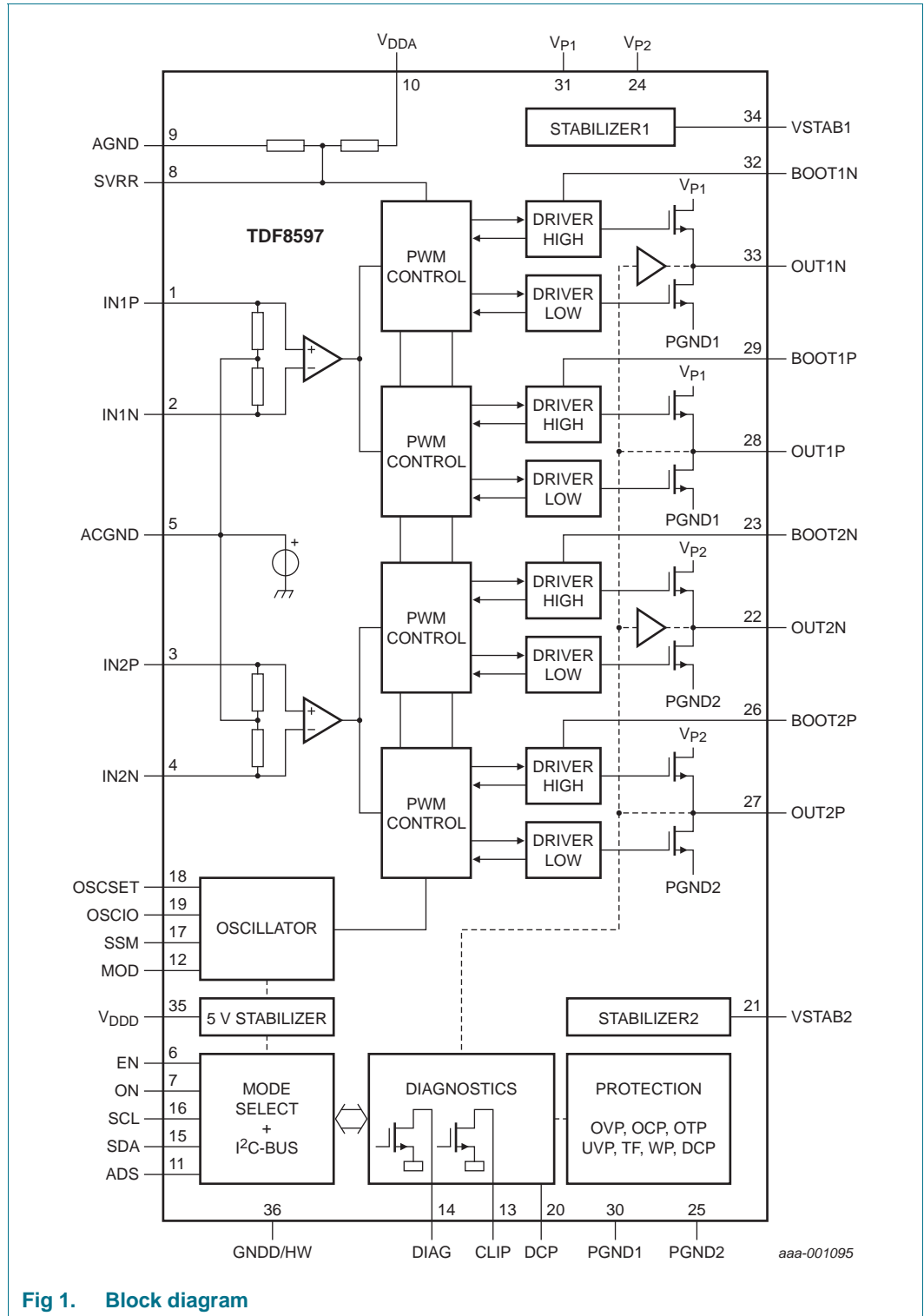


Fig 1. Block diagram

6. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _P	supply voltage	Operating mode	-	29	V
		off state	[1] -1	+50	V
		load dump; duration 50 ms; t _r > 2.5 ms	-	50	V
I _{ORM}	repetitive peak output current	maximum output current limiting	[2] 8	-	A
I _{OM}	peak output current	non-repetitive:			
		Stereo mode	-	18	A
		Parallel mode	-	12	A
I _{sink(max)}	maximum sink current	pins DIAG and CLIP	0	5	mA
V _i	input voltage	referred to GNDD:			
		pins SCL and SDA	0	5.5	V
		pins DIAG and CLIP	0	10	V
		pin OSCIO	0	5.5	V
		referred to AGND:			
		pins EN and ON	0	5.5	V
		pins ADS, MOD and SSM	0	5.5	V
		pins IN1P, IN1N, IN2P, and IN2N	0	10	V
V _{i(dif)}	differential input voltage	RMS; pins IN1P, IN1N, IN2P, and IN2N	0	3	V
R _{ESR}	equivalent series resistance	as seen between pins V _P and PGNDn	-	350	mΩ
T _j	junction temperature		-	150	°C
T _{stg}	storage temperature		-55	+150	°C
T _{amb}	ambient temperature		-40	+85	°C
V _{ESD}	electrostatic discharge voltage	HBM	[3]		
		C = 100 pF; R _s = 1.5 kΩ	-	2000	V
		CDM	[4]		
		non-corner pins (except pin 10, V _{DDA})	-	500	V
		pin 10, V _{DDA}	-	300	V
	corner pins	-	750	V	
V _(prot)	protection voltage	AC and DC short-circuit voltage of output pins across load and to supply and ground	[5] 0	V _P	V

[1] Floating condition assumed for outputs.

[2] Current limiting concept.

[3] Human Body Model (HBM).

[4] Charged-Device Model (CDM).

[5] The output pins are defined as the output pins of the filter connected between the TDF8597 output pins and the load.

7. Revision history

Table 4. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDF8597_SDS v.1	20111117	Preliminary short data sheet	-	-

8. Legal information

8.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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