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Kind regards,

Team Nexperia

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4007UB
gates
Dual complementary pair and inverter

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

Dual complementary pair and inverter

HEF4007UB gates

DESCRIPTION

The HEF4007UB is a dual complementary pair and an inverter with access to each device. It has three n-channel and three p-channel enhancement mode MOS transistors.

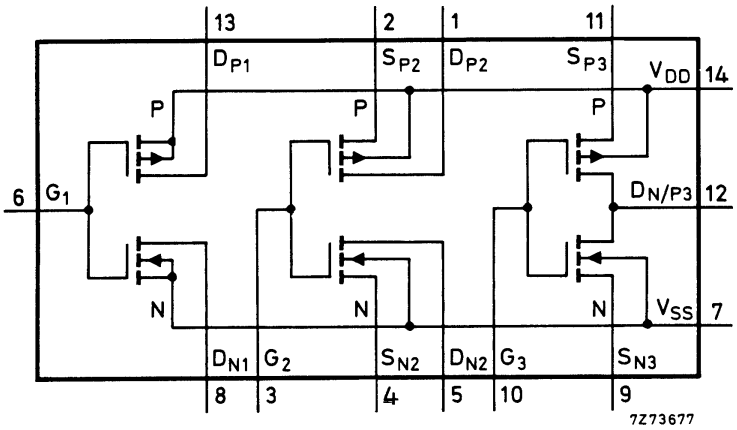


Fig.1 Schematic diagram.

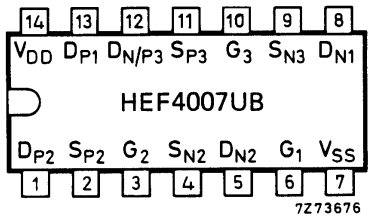


Fig.2 Pinning diagram.

HEF4007UBP(N): 14-lead DIL; plastic (SOT27-1)

HEF4007UBD(F): 14-lead DIL; ceramic (cerdip) (SOT73)

HEF4007UBT(D): 14-lead SO; plastic (SOT108-1)

( ): Package Designator North America

PINNING

S_{P2}, S_{P3}	source connections to 2nd and 3rd p-channel transistors
D_{P1}, D_{P2}	drain connections from the 1st and 2nd p-channel transistors
D_{N1}, D_{N2}	drain connections from the 1st and 2nd n-channel transistors
S_{N2}, S_{N3}	source connections to the 2nd and 3rd n-channel transistors
$D_{N/P3}$	common connection to the 3rd p-channel and n-channel transistor drains
G_1 to G_3	gate connections to n-channel and p-channel of the three transistor pairs

FAMILY DATA, I_{DD} LIMITS category GATES

See Family Specifications for V_{IH}/V_{IL} unbuffered stages

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays						
$G_n \rightarrow D_N$; D_P	5		40	80	ns	13 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	20	40	ns	9 ns + (0,23 ns/pF) C_L
	15		15	30	ns	7 ns + (0,16 ns/pF) C_L
	5		40	75	ns	13 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	20	40	ns	9 ns + (0,23 ns/pF) C_L
	15		15	30	ns	7 ns + (0,16 ns/pF) C_L
Output transition times	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power	5	$4500\ f_i + \sum (f_o C_L) \times V_{DD}^2$	where
dissipation per	10	$20\ 000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
package (P)	15	$50\ 000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
			C_L = load capacitance (pF)
			$\sum(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

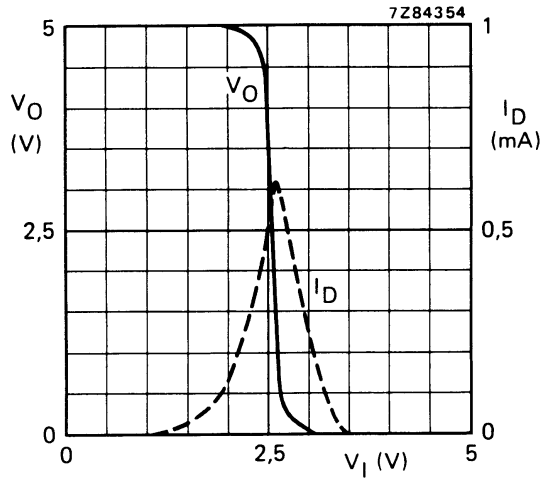


Fig.3 Typical drain current I_D and output voltage V_O as functions of input voltage; V_{DD} = 5 V; T_{amb} = 25 °C.

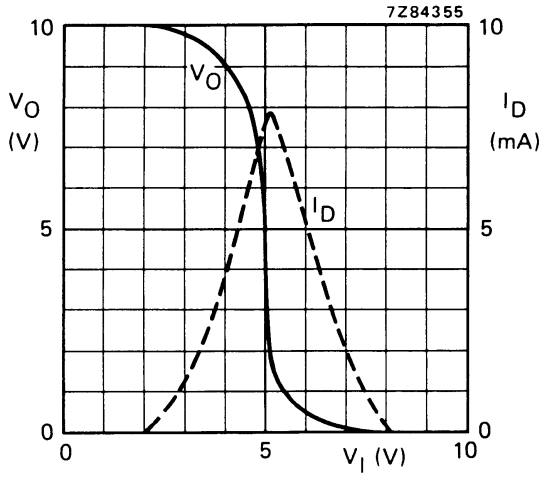


Fig.4 Typical drain current I_D and output voltage V_O as functions of input voltage; V_{DD} = 10 V; T_{amb} = 25 °C.

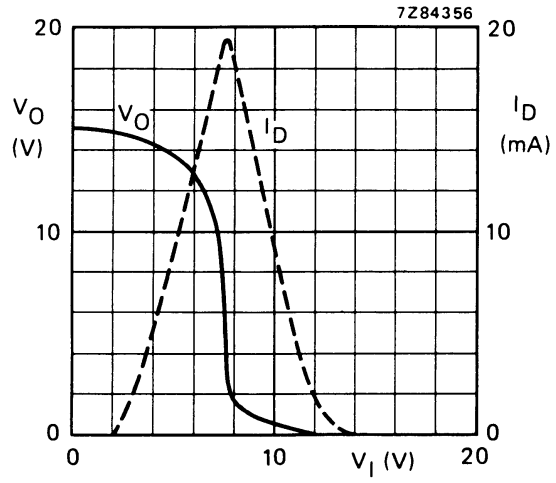


Fig.5 Typical drain current I_D and output voltage V_O as functions of input voltage; V_{DD} = 15 V; T_{amb} = 25 °C.

APPLICATION INFORMATION

Some examples of applications for the HEF4007UB are:

- High input impedance amplifiers
- Linear amplifiers
- (Crystal) oscillators
- High-current sink and source drivers
- High impedance buffers.

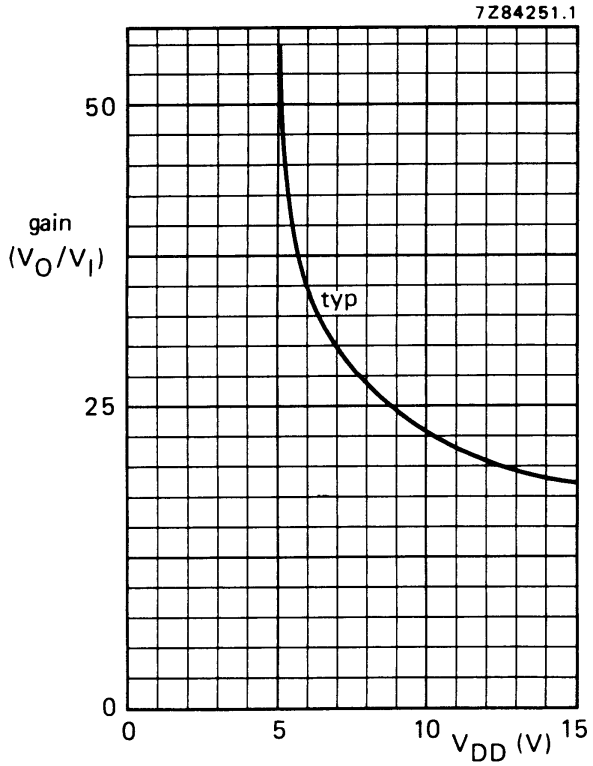


Fig.6 Voltage gain (V_o/V_i) as a function of supply voltage.

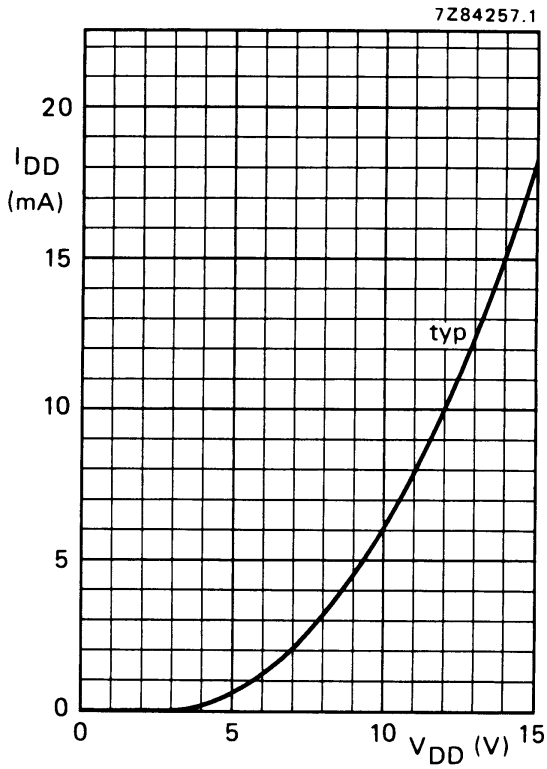
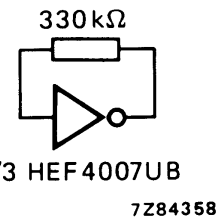


Fig.7 Supply current as a function of supply voltage.



This is also an example of an analogue amplifier using one HEF4007UB gate.

Fig.8 Test set-up for measuring graphs of Figs 6 and 7.

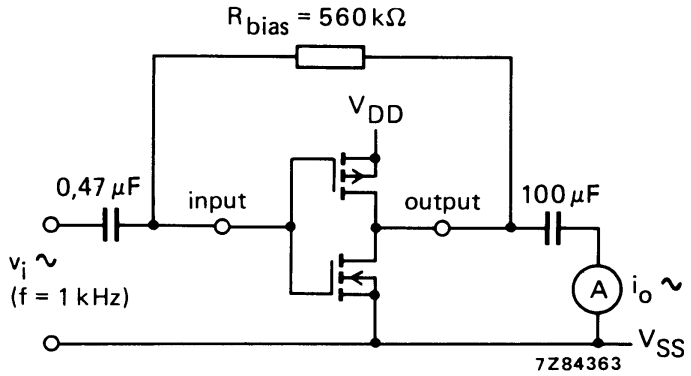
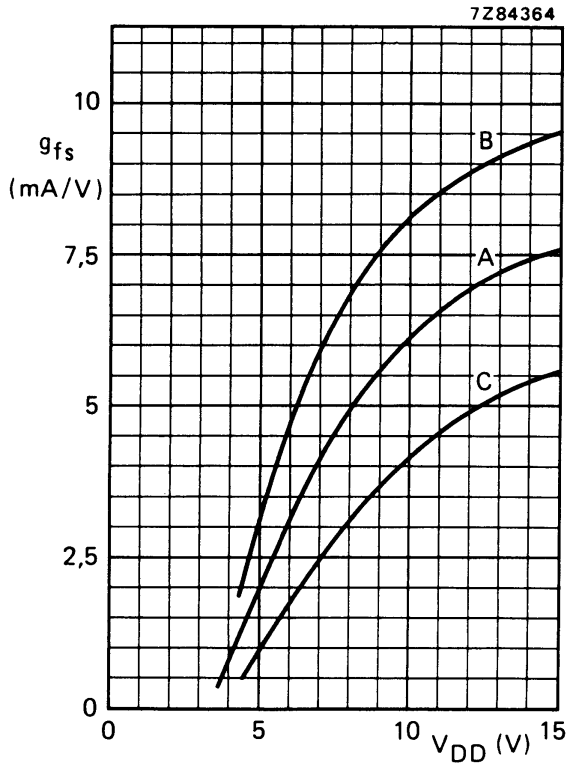


Fig.9 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Fig.10).



A: average,
B: average + 2 s,
C: average – 2 s, in where 's' is the observed standard deviation.

Fig.10 Typical forward transconductance g_{fs} as a function of the supply voltage at T_{amb} = 25 °C.

Figures 11 to 14 show some applications in which the HEF4007UB is used.

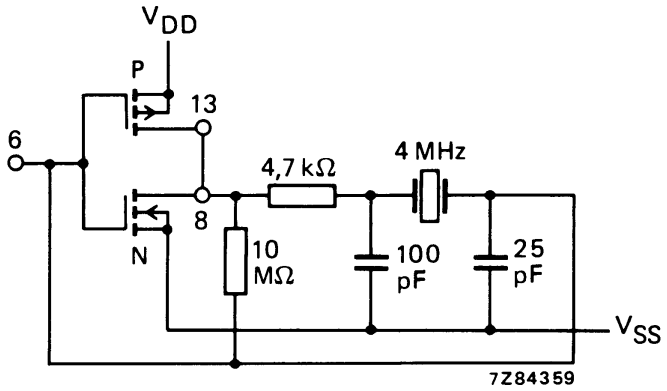


Fig.11 4 MHz crystal oscillator.

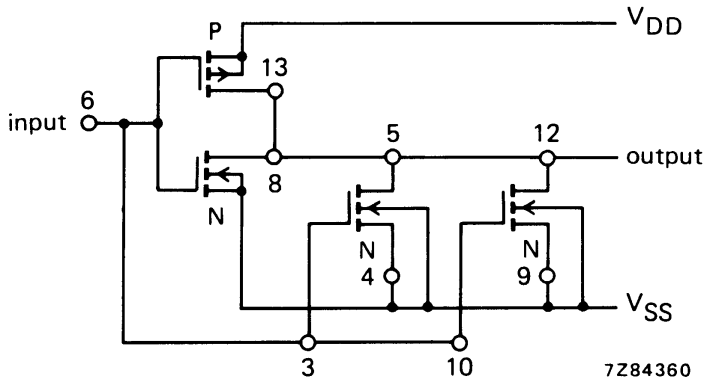


Fig.12 High current sink driver.

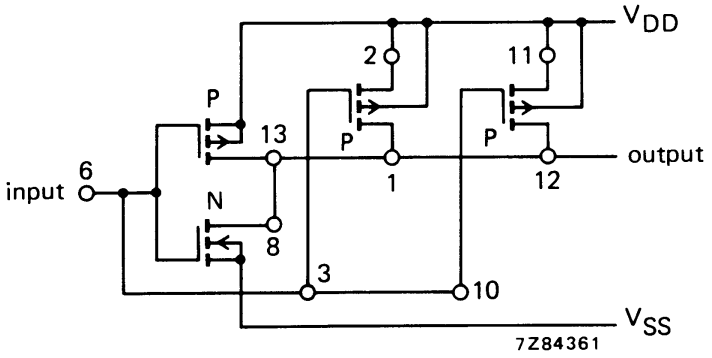


Fig.13 High current source driver.

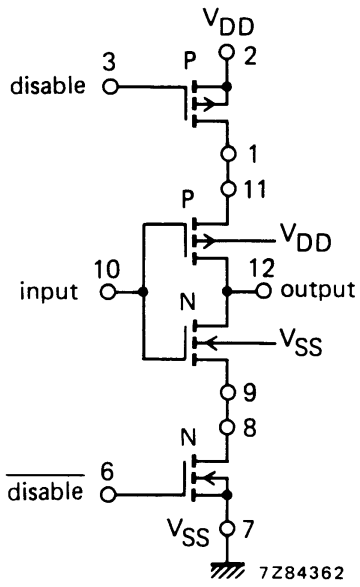


Fig.14 High impedance buffer.

FUNCTION TABLE for Fig.14.

INPUT	DISABLE	OUTPUT
H	L	L
L	L	H
X	H	open

Notes

1. H = HIGH state (the more positive voltage)
   L = LOW state (the less positive voltage)
   X = state is immaterial

NOTE

Rules for maintaining electrical isolation between transistors and monolithic substrate:

- Pin number 14 must be maintained at the most positive (or equally positive) potential with respect to any other pin of the HEF4007UB.
- Pin number 7 must be maintained at the most negative (or equally negative) potential with respect to any other pin of the HEF4007UB.

Violation of these rules will result in improper transistor operation and/or possible permanent damage to the HEF4007UB.