TEA1623P; TEA1623PH

STARplug switched mode power supply controller IC

Rev. 3 — 30 August 2010 Product data sheet

1. General description

The TEA1623 is a Switched Mode Power Supply (SMPS) controller IC that operates directly from rectified universal mains. It is implemented in the high voltage EZ-HV SOI process, combined with a low voltage BiCMOS process.

The device includes a high voltage power switch and a circuit for start-up directly from the rectified mains voltage. A dedicated circuit for valley switching is built in, which makes a very efficient slim-line electronic power-plug concept possible.

In its most basic version of application, the TEA1623 acts as a voltage source. Here, no additional secondary electronics are required. A combined voltage and current source can be realized with minimum costs for external components. Implementation of the TEA1623 renders an efficient and low cost power supply system.

2. Features and benefits

- Designed for general purpose power supplies
- Integrated power switch: 6.5 Ω and 650 V
- Operates from universal AC mains supplies: 80 V to 276 V
- Adjustable frequency for flexible design
- RC oscillator for stable output regulation
- Valley switching for minimum switch-on loss
- Frequency reduction at low power output for low standby power: < 100 mW
- Adjustable OverCurrent Protection (OCP)
- UnderVoltage Protection (UVP)
- Temperature protection
- Short-winding protection
- Safe restart mode for system fault conditions
- Simple application with both primary and secondary (opto) feedback
- Available in 8-pin and 16-pin DIP packages.

3. Applications

- Adapters
- Set-Top Box (STB)
- DVD
- VCD
- CD(R)
- PC Silverbox standby SMPS

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC(max)}$	maximum supply voltage		-	-	40	V
$V_{DRAIN(max)}$	maximum DMOS power transistor drain voltage	T_j > 0 °C	-	-	650	V
I_{DRAIN}	supply current drawn from pin DRAIN	no auxiliary supply	-	0.5	-	mA
R_{DSon}	drain-source on-state resistance	I_{SOURCE} = −0.5 A				
		T_j = 25 °C	-	6.5	7.5	Ω
		T_j = 100 °C	-	9.0	10.0	Ω
f_{osc}	oscillator frequency range		10	-	200	kHz

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TEA1623P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
TEA1623PH	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1

6. Block diagram

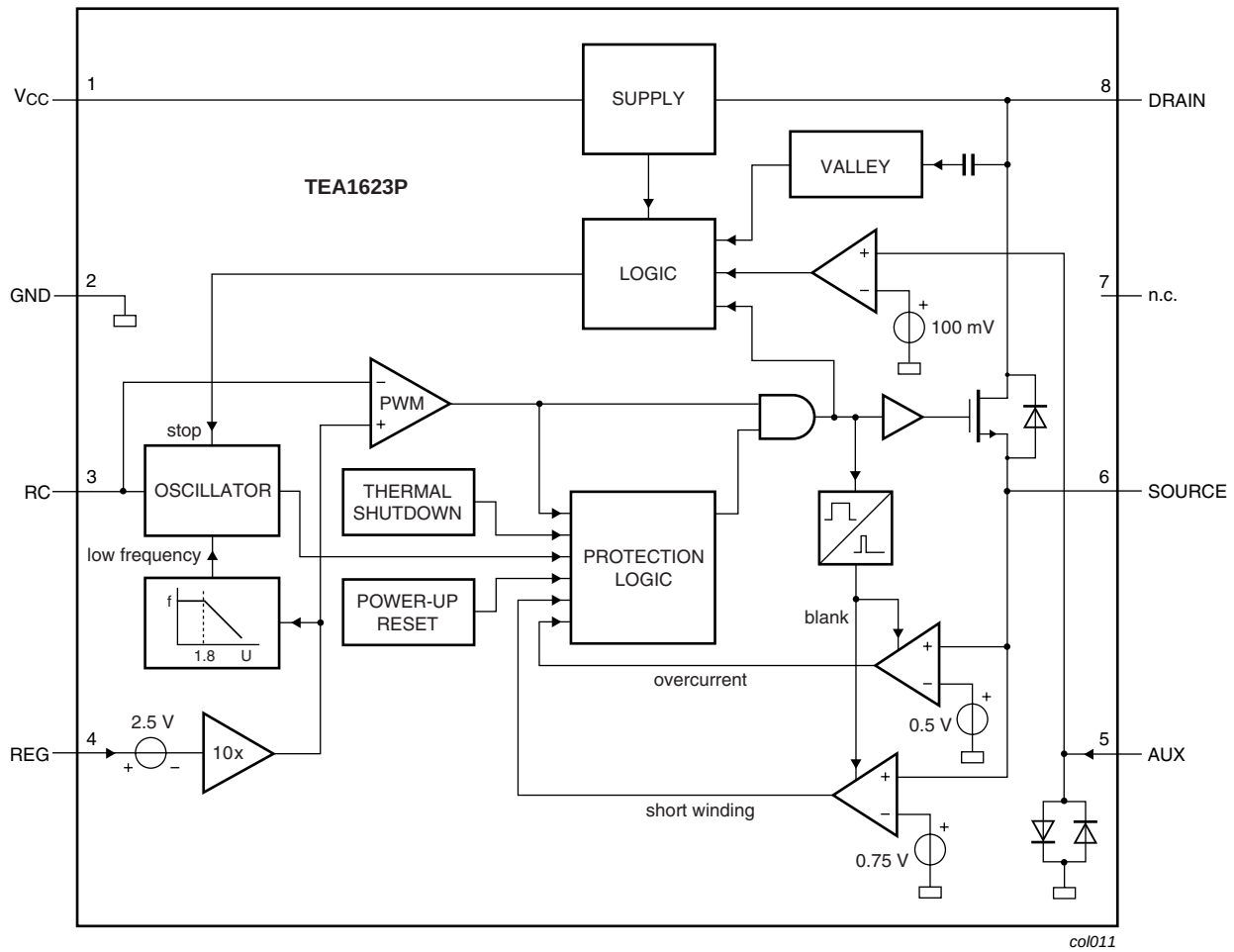


Fig 1. Block diagram of TEA1623P

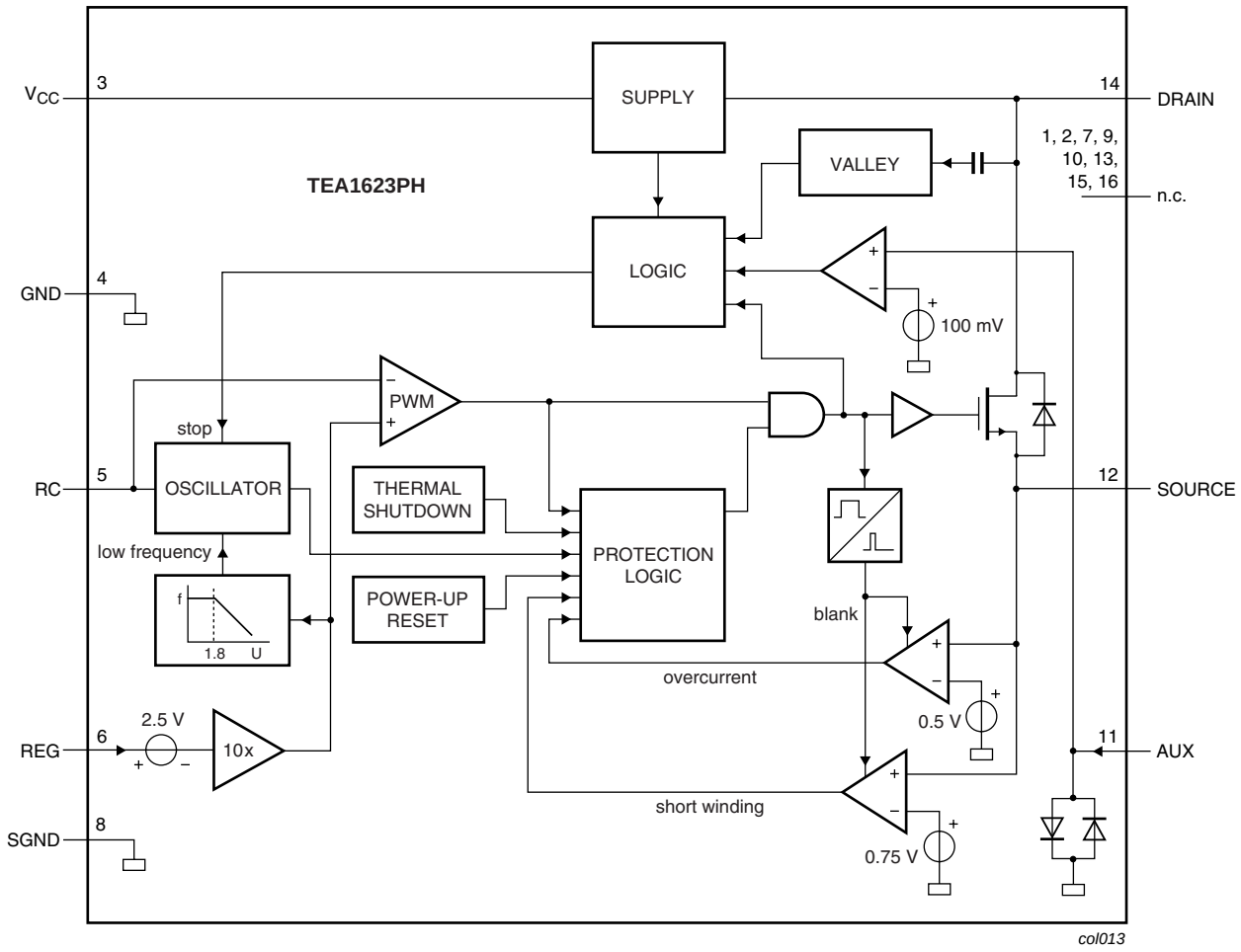


Fig 2. Block diagram of TEA1623PH

7. Pinning information

7.1 Pinning

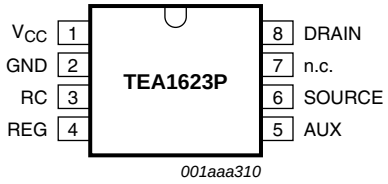


Fig 3. Pin configuration for SOT97-1 (DIP8)

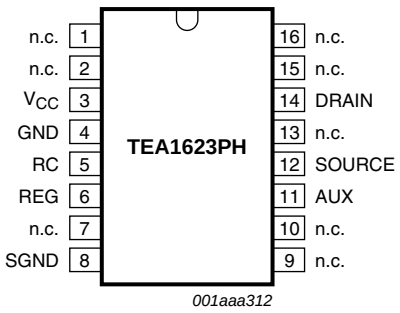


Fig 4. Pin configuration for SOT38-1 (DIP16)

7.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	TEA1623P	TEA1623PH	
V_{CC}	1	3	supply voltage
GND	2	4	ground
RC	3	5	frequency setting
REG	4	6	regulation point
SGND	-	8	signal ground; preferably connected to pin GND
AUX	5	11	input for voltage from auxiliary winding for timing (demagnetization)
SOURCE	6	12	source of internal MOS switch
n.c.	7	1, 2, 7, 9, 10, 13, 15, 16	not connected
DRAIN	8	14	drain of internal MOS switch; input for start-up current and valley sensing

8. Functional description

The TEA1623 is the heart of a compact flyback converter, with the IC placed at the primary side. The auxiliary winding of the transformer can be used for indirect feedback to control the isolated output. This additional winding also powers the IC. A more accurate control of the output voltage and/or current can be implemented with an additional secondary sensing circuit and optocoupler feedback.

The TEA1623 uses voltage mode control. The frequency is determined by the maximum transformer demagnetizing time or the frequency of the oscillator. In the first case, the converter operates in the Self Oscillating Power Supply (SOPS) mode. In the latter case, it operates at a constant frequency, which can be adjusted with external components R_{RC} and C_{RC}. This mode is called Pulse Width Modulation (PWM). Furthermore, a primary stroke is started only in a valley of the secondary ringing. This valley switching principle minimizes capacitive switch-on losses.

8.1 Start-up and UnderVoltage LockOut (UVLO)

Initially, the IC is self supplying from the rectified mains voltage. The IC starts switching as soon as the voltage on pin V_{CC} passes the $V_{CC(start)}$ level. The supply is taken over by the auxiliary winding of the transformer as soon as V_{CC} is high enough and the supply from the line is stopped for high efficiency operation.

As soon as the voltage on pin V_{CC} drops below the $V_{CC(stop)}$ level, the IC stops switching and restarts from the rectified mains voltage.

8.2 Oscillator

The frequency of the oscillator is set by the external resistor and capacitor on pin RC. The external capacitor is charged rapidly to the $V_{RC(max)}$ level and, starting from a new primary stroke, it discharges to the $V_{RC(min)}$ level. Because the discharge is exponential, the

relative sensitivity of the duty factor to the regulation voltage at low duty factor is almost equal to the sensitivity at high duty factors. This results in a more constant gain over the duty factor range compared to PWM systems with a linear sawtooth oscillator. Stable operation at low duty factors is easily realized. For high efficiency, the frequency is reduced as soon as the duty factor drops below a certain value. This is accomplished by increasing the oscillator charge time.

To ensure that the capacitor can be charged within the charge time, the value of the oscillator capacitor should be limited to approximately 1 nF.

8.3 Duty factor control

The duty factor is controlled by the internal regulation voltage and the oscillator signal on pin RC. The internal regulation voltage is equal to the external regulation voltage (−2.5 V) multiplied by the gain of the error amplifier (typical 20 dB or 10×).

The minimum duty factor of the switched mode power supply is 0 %. The maximum duty factor is set to 75 % (typical value at 100 kHz oscillation frequency).

8.4 Valley switching

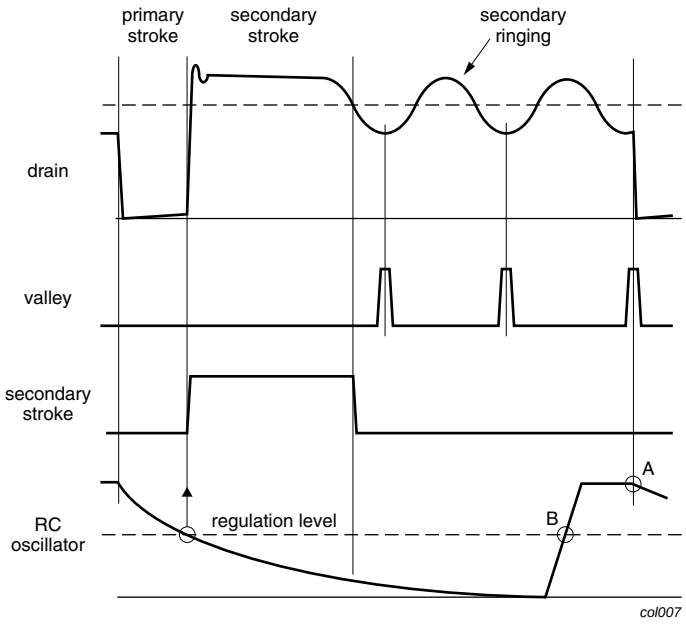
A new cycle is started at the primary stroke when the switch is switched on (see Figure 5). After a certain time (determined by the RC oscillator voltage and the internal regulation level), the switch is turned off and the secondary stroke starts. The internal regulation level is determined by the voltage on pin REG. After the secondary stroke, the drain voltage shows an oscillation with a frequency of approximately $\frac{1}{2\pi \times \sqrt{L_p C_p}}$, where:

L_p is the primary self inductance on the drain node.

C_p is the parasitic capacitance on the drain node.

As soon as the oscillator voltage is high again and the secondary stroke has ended, the circuit waits for a low drain voltage before starting a new primary stroke.

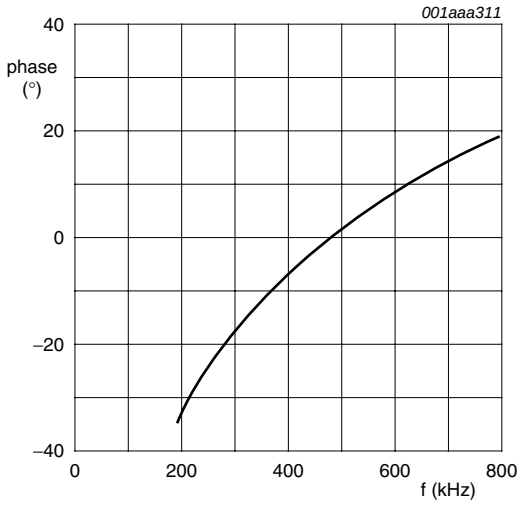
The primary stroke starts some time before the actual valley at low ringing frequencies, and some time after the actual valley at high ringing frequencies. Figure 6 shows a typical curve for a reflected voltage $N \times V_o$ of 80 V. This voltage is the output voltage V_o (see Figure 7) transferred to the primary side of the transformer with the factor N (determined by the turns ratio of the transformer). Figure 6 shows that the system switches exactly at minimum drain voltage for ringing frequencies of 480 kHz, thus reducing the switch-on losses to a minimum. At 200 kHz, the next primary stroke is started at 33 ° before the valley. The switch-on losses are still reduced significantly.



A: Start of new cycle with valley switching.

B: Start of new cycle in a classical PWM system.

Fig 5. Signals for valley switching



Reflected voltage at $N \times V_o = 80$ V.

Fig 6. Typical phase of drain ringing at switch-on

8.5 Demagnetization

The system operates in discontinuous conduction mode all the time. As long as the secondary stroke has not ended, the oscillator will not start a new primary stroke. During the suppression time t_{suppr}, demagnetization recognition is suppressed. This suppression may be necessary in applications where the transformer has a large leakage inductance and at low output voltages.

8.6 Protection

8.6.1 Overcurrent protection

The cycle-by-cycle peak drain current limit circuit uses the external source resistor R_I (see Figure 7) to measure the current. The circuit is activated after the leading edge blanking time t_{leb}. The protection circuit limits the source voltage to $V_{source(max)}$, and thus limits the primary peak current.

8.6.2 Short-winding protection

The short-winding protection circuit is also activated after the leading edge blanking time. If the source voltage exceeds the short-winding protection voltage V_{swp}, the TEA1623 stops switching. Only a power-on reset will restart normal operation. The short-winding protection also protects in case of a secondary diode short circuit.

8.6.3 OverTemperature Protection (OTP)

An accurate temperature protection is provided in the TEA1623. When the junction temperature exceeds the thermal shut-down temperature, the IC stops switching. During thermal protection, the IC current is lowered to the start-up current. The IC continues normal operation as soon as the overtemperature situation has disappeared.

8.6.4 OverVoltage Protection (OVP)

Overvoltage protection can be achieved in the application by pulling pin REG above its normal operation level, or by keeping the level of pin AUX above V_{demag}. The current primary stroke is terminated immediately and no new primary stroke is started until the voltage on pin REG drops to its normal operation level. Pin REG has an internal clamp. The current feed into pin REG must be limited.

8.7 Characteristics of the complete power-plug

8.7.1 Input

The input voltage range comprises the universal AC mains from 80 V to 276 V.

8.7.2 Accuracy

The accuracy of the complete converter, functioning as a voltage source with primary sensing, is approximately 8 % (mainly dependent on the transformer coupling). The accuracy with secondary sensing is defined by the accuracy of the external components. For safety requirements in case of optocoupler feedback loss, the primary sensing remains active when an overvoltage circuit is connected.

8.7.3 Efficiency

An efficiency of 75 % at maximum output power can be achieved for a complete converter designed for universal mains.

8.7.4 Ripple

A minimum ripple is obtained in a system designed for a maximum duty factor of 50 % under normal operating conditions and a minimized dead time. The magnitude of the ripple in the output voltage is determined by the frequency and duty factor of the converter, the output current level, and the value and ESR of the output capacitor.

9. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Voltage						
V_{CC}	supply voltage	continuous	[1]	–0.4	+40	V
V_{RC}	oscillator input voltage		[1]	–0.4	+3	V
V_{SOURCE}	DMOS power transistor source voltage			–0.4	+5	V
V_{DRAIN}	DMOS power transistor drain voltage	T_j > 0 °C		–0.4	+650	V
Current						
I_{REG}	regulation input current		[2]	-	6	mA
I_{AUX}	auxiliary winding input current		[2]	–10	+5	mA
I_{RC}	oscillator capacitor charge current			–3	-	mA
I_{SOURCE}	source current			–2	+2	A
I_{DRAIN}	drain current			–2	+2	A
General						
P_{tot}	total power dissipation					
		TEA1623P; T_{amb} < 45 °C		-	1.0	W
		TEA1623PH; T_{amb} < 50 °C		-	1.7	W
T_{stg}	storage temperature			–55	+150	°C
T_j	junction temperature			–20	+145	°C
V_{ESD}	electrostatic discharge voltage	human body model	[3]			
		pin DRAIN		–1500	+1500	V
		all other pins		–2000	+2000	V
		machine model	[4]			
		all pins		–200	+200	V

[1] Pins V_{CC} and RC are not allowed to be current driven.

[2] Pins REG and AUX are not allowed to be voltage driven.

[3] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[4] Machine model: equivalent to discharging a 200 pF capacitor through a 0.75 μH coil and a 10 Ω series resistor.

10. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]		-
		TEA1623P		100	K/W
		TEA1623PH		55	K/W

[1] Thermal resistance $R_{th(j-a)}$ can be lower when pin GND is connected to sufficient copper area on the printed-circuit board. See the *TEA152x* application note for details.

11. Characteristics

Table 6. Characteristics

T_{amb} = 25 °C; no overtemperature; all voltages are measured with respect to ground; currents are positive when flowing into the IC, unless otherwise specified.

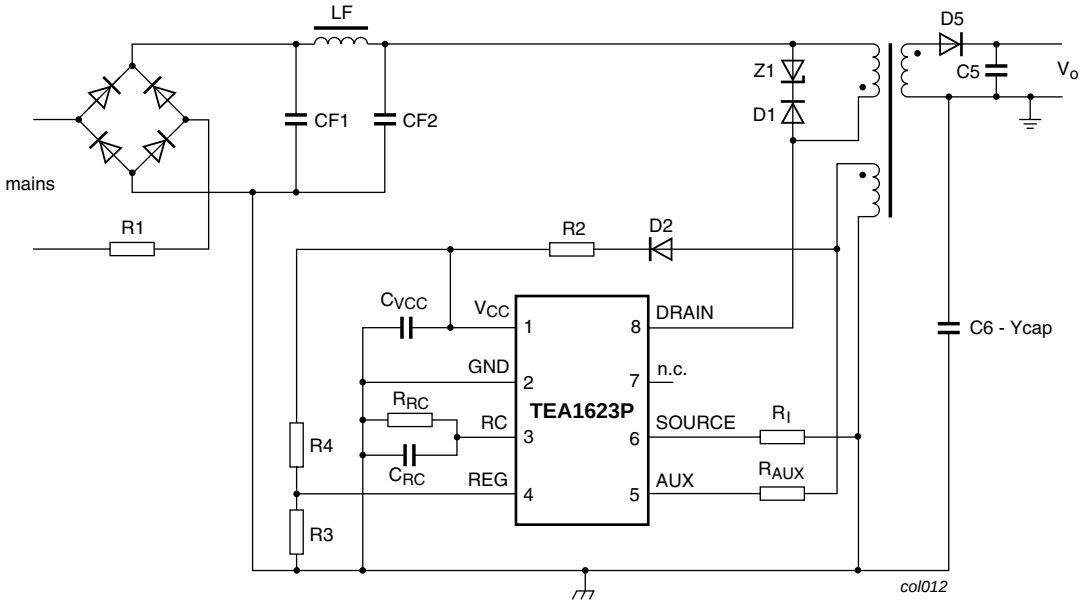
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
Supply on pin V_{CC}						
$V_{CC(start)}$	start voltage		9	9.5	10	V
$V_{CC(stop)}$	stop voltage	undervoltage lockout	7.0	7.5	8.0	V
$I_{CC(operate)}$	operating supply current	normal operation	-	1.3	1.9	mA
$I_{CC(startup)}$	start-up supply current	start-up	-	180	400	µA
$I_{CC(ch)}$	charging current	V_{DRAIN} > 60 V				
		V_{CC} = 0 V	–650	–520	–390	µA
		V_{CC} = 8.5 V	–375	–275	–175	µA
Supply on pin DRAIN						
I_{DRAIN}	supply current drawn from pin DRAIN	no auxiliary supply	-	0.5	-	mA
		with auxiliary supply; V_{DRAIN} > 60 V	-	30	125	µA
PWM mode						
δ_{min}	minimum duty factor		-	0	-	%
δ_{max}	maximum duty factor	f_{osc} = 100 kHz	-	75	-	%
Self-oscillating power supply mode						
V_{demag}	demagnetization recognition voltage level		50	100	150	mV
t_{suppr}	time of suppression of transformer ringing at start of secondary stroke		1.0	1.5	2.0	µs
Oscillator: pin RC						
$V_{RC(min)}$	minimum voltage of RC oscillator setting		60	75	90	mV
$V_{RC(max)}$	maximum voltage of RC oscillator setting		2.4	2.5	2.6	V
$t_{RC(ch)}$	RC charging time		-	1	-	µs
f_{osc}	oscillator frequency range		10	-	200	kHz
Duty factor regulator: pin REG						
V_{REG}	input voltage on pin REG		2.4	2.5	2.6	V
$G_{V(erroramp)}$	voltage gain of error amplifier		-	20	-	dB
$V_{REG(clamp)}$	clamping voltage on pin REG	I_{REG} = 6 mA	-	-	7.5	V
Valley switching recognition						
dV/dt_{valley}	valley recognition		–102	-	+102	V/µs
f_{valley}	ringing frequency for valley switching	$N \times V_o$ = 100 V	200	550	800	kHz
$t_{d(valley-on)}$	delay from valley recognition to switch-on		-	150	-	ns
Output stage (FET)						
$I_{L(drain)}$	drain leakage current	V_{DRAIN} = 650 V	-	-	125	µA

Table 6. Characteristics *...continued*

T_{amb} = 25 °C; no overtemperature; all voltages are measured with respect to ground; currents are positive when flowing into the IC, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{BR(drain)}$	drain breakdown voltage	T_j > 0 °C	650	-	-	V
R_{DSon}	drain-source on-state resistance	I_{SOURCE} = −0.5 A				
		T_j = 25 °C	-	6.5	7.5	Ω
		T_j = 100 °C	-	9.0	10.0	Ω
$t_{drain(f)}$	drain fall time	$V_{DRAIN(switch\_on)}$ = 300 V; no external capacitor at pin DRAIN	-	75	-	ns
Temperature protection						
$T_{prot(max)}$	maximum threshold temperature		150	160	170	°C
$T_{prot(hys)}$	threshold temperature hysteresis		-	2	-	°C
Overcurrent and short winding protection: pin SOURCE						
$V_{source(max)}$	overcurrent protection voltage	dV/dt = 0.1 V/µs	0.47	0.50	0.53	V
V_{swp}	short-winding protection voltage	dV/dt = 0.5 V/µs	0.7	0.75	0.8	V
$t_{d(propagation)}$	delay from detecting $V_{source(max)}$ to switch-off	dV/dt = 0.5 V/µs	-	160	185	ns
t_{leb}	leading edge blanking time	overcurrent and short-winding protection	250	350	450	ns

12. Application information

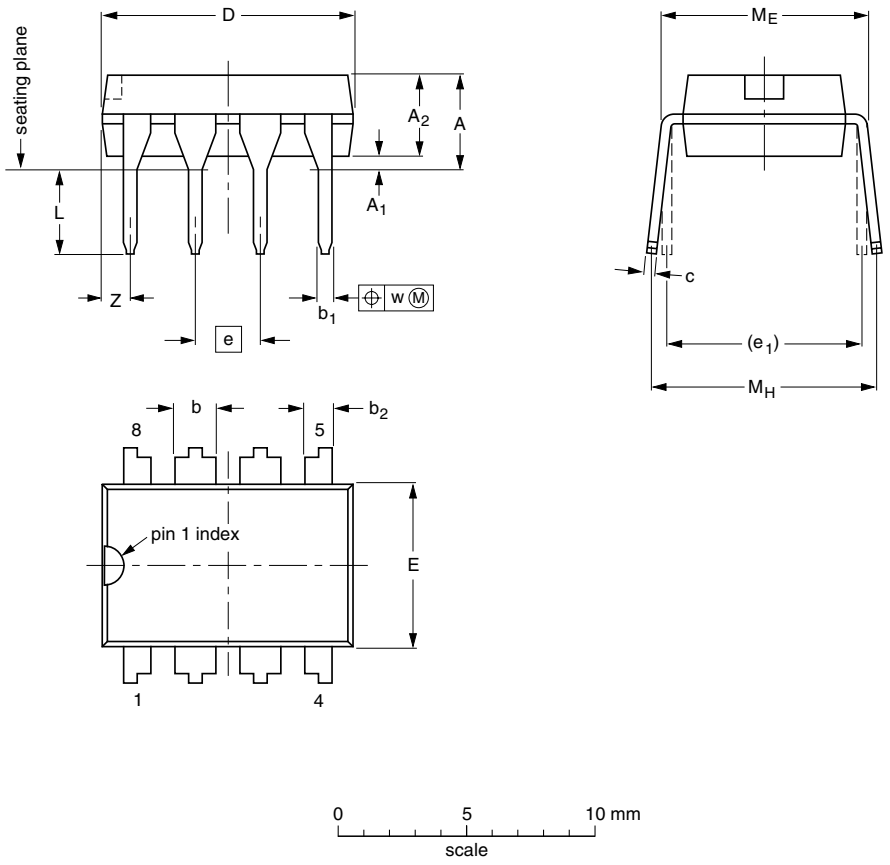


Further application information can be found in the *TEA152x* application note.

Fig 7. Application with primary sensing for TEA1623P

13. Package outline

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.02	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

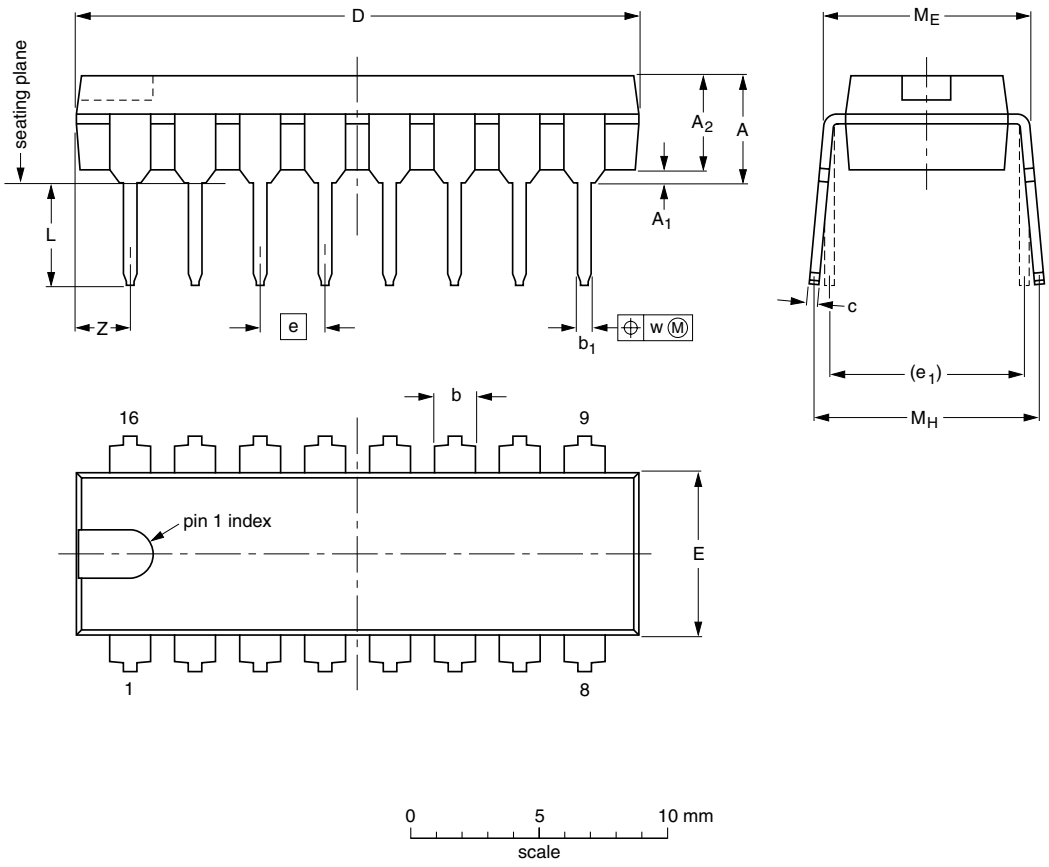
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT97-1	050G01	MO-001	SC-504-8			~~99-12-27~~ 03-02-13

Fig 8. Package outline SOT97-1 (DIP8)

DIP16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.02	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.1	0.3	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-1	050G09	MO-001	SC-503-16			~~99-12-27~~ 03-02-13

Fig 9. Package outline SOT38-1 (DIP16)

14. Soldering of through-hole mount packages

14.1 Introduction to soldering through-hole mount packages

This text gives a very brief insight into wave, dip and manual soldering.

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

14.2 Soldering by dipping or by solder wave

Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing. Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

14.3 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 °C and 400 °C, contact may be up to 5 seconds.

14.4 Package related soldering information

Table 7. Suitability of through-hole mount IC packages for dipping and wave soldering

Package	Soldering method	
	Dipping	Wave
CPGA, HCPGA	-	suitable
DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable	suitable[1]
PMFP[2]	-	not suitable

[1] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

[2] For PMFP packages hot bar soldering or manual soldering is suitable.

15. Abbreviations

Table 8. Abbreviations

Acronym	Description
BiCMOS	Bipolar CMOS
CMOS	Complementary Metal-Oxide Semiconductor
DMOS	Diffusion Metal-Oxide Semiconductor
ESR	Equivalent Series Resistance
OCP	OverCurrent Protection
OTP	OverTemperature Protection
OVP	OverVoltage Protection
PWM	Pulse Width Modulation
SMPS	Switched Mode Power Supply
SOI	Silicon On Insulator
SOPS	Self Oscillating Power Supply
STB	Set-Top Box
UVLO	UnderVoltage LockOut
UVP	UnderVoltage Protection
VCD	Video Compact Disc

16. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA1623P_TEA1623PH v.3	20100830	Product data sheet	-	TEA1623P_TEA1623PH_2
Modifications:	• Table 1 “Quick reference data” updated. • Table 4 “Limiting values” updated.			
TEA1623P_TEA1623PH_2	20091104	Product data sheet	-	TEA1623P_TEA1623PH_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Pin configuration drawing A and B split into Figure 3 “Pin configuration for SOT97-1 (DIP8)” and Figure 4 “Pin configuration for SOT38-1 (DIP16)”. • Section 15 “Abbreviations” added.			
TEA1623P_TEA1623PH_1	20040317	Product data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

17.2 Definitions

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19. Tables

Table 1. Quick reference data 2
Table 2. Ordering information 2
Table 3. Pin description 5
Table 4. Limiting values 9
Table 5. Thermal characteristics 9
Table 6. Characteristics 10
Table 7. Suitability of through-hole mount IC packages for dipping and wave soldering 14
Table 8. Abbreviations 15
Table 9. Revision history 15

continued >>

20. Figures

Fig 1. Block diagram of TEA1623P 3
Fig 2. Block diagram of TEA1623PH 4
Fig 3. Pin configuration for SOT97-1 (DIP8) 4
Fig 4. Pin configuration for SOT38-1 (DIP16) 4
Fig 5. Signals for valley switching 7
Fig 6. Typical phase of drain ringing at switch-on 7
Fig 7. Application with primary sensing for TEA1623P . 11
Fig 8. Package outline SOT97-1 (DIP8) 12
Fig 9. Package outline SOT38-1 (DIP16) 13

continued >>

21. Contents

1 General description 1
2 Features and benefits 1
3 Applications 1
4 Quick reference data 2
5 Ordering information 2
6 Block diagram 3
7 Pinning information 4
7.1 Pinning 4
7.2 Pin description 5
8 Functional description 5
8.1 Start-up and UnderVoltage LockOut (UVLO) . . 5
8.2 Oscillator 5
8.3 Duty factor control 6
8.4 Valley switching 6
8.5 Demagnetization 7
8.6 Protection 8
8.6.1 Overcurrent protection 8
8.6.2 Short-winding protection 8
8.6.3 OverTemperature Protection (OTP) 8
8.6.4 OverVoltage Protection (OVP) 8
8.7 Characteristics of the complete power-plug . . . 8
8.7.1 Input 8
8.7.2 Accuracy 8
8.7.3 Efficiency 8
8.7.4 Ripple 8
9 Limiting values 9
10 Thermal characteristics 9
11 Characteristics 10
12 Application information 11
13 Package outline 12
14 Soldering of through-hole mount packages . 14
14.1 Introduction to soldering through-hole mount packages 14
14.2 Soldering by dipping or by solder wave 14
14.3 Manual soldering 14
14.4 Package related soldering information 14
15 Abbreviations 15
16 Revision history 15
17 Legal information 16
17.1 Data sheet status 16
17.2 Definitions 16
17.3 Disclaimers 16
17.4 Trademarks 17
18 Contact information 17
19 Tables 18
20 Figures 19
21 Contents 20

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